CHIP TEMPERATURES

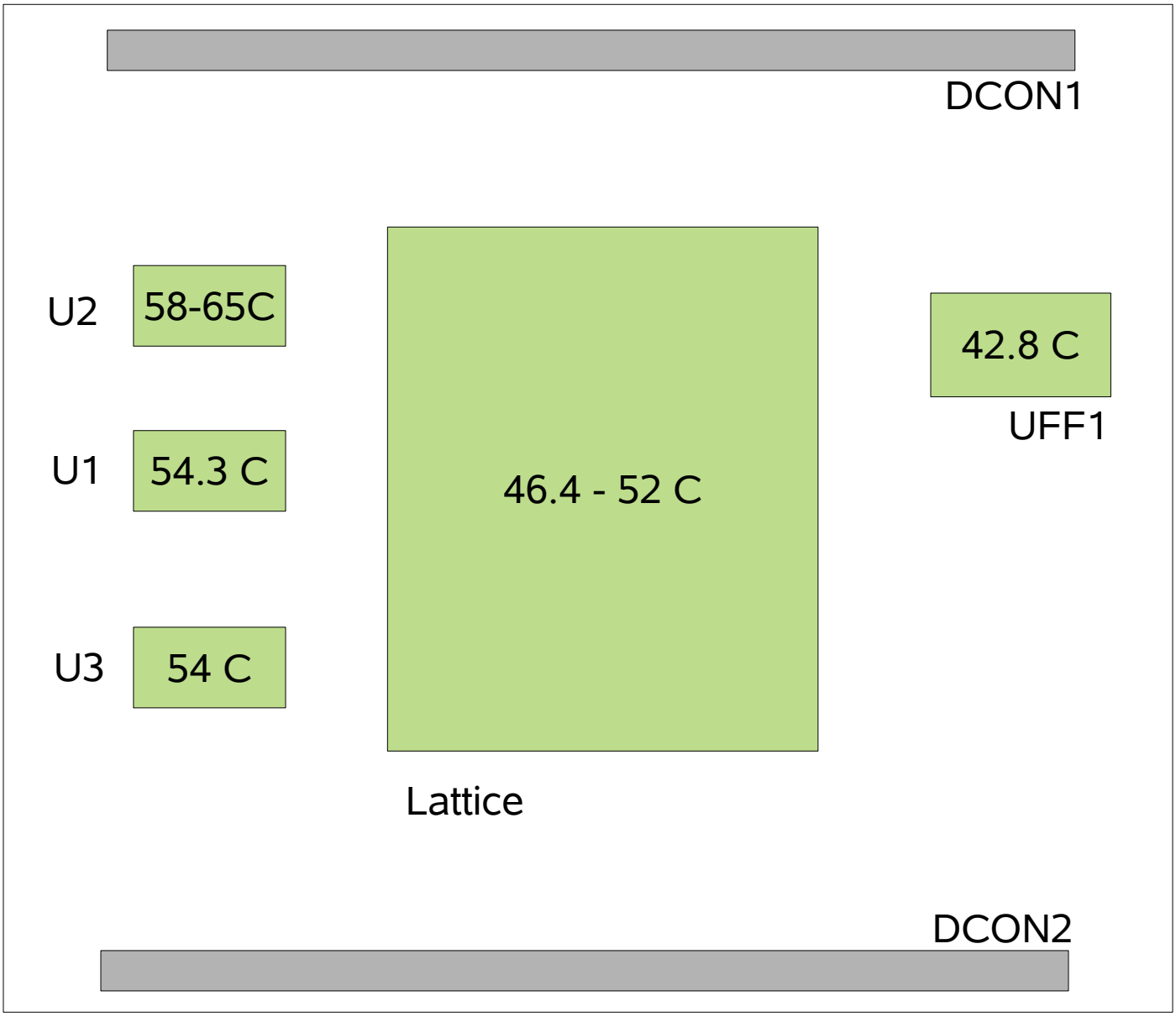
Test conditions: program in the FPGA which generates a clock signal (50 MHz). We use this clock signal as input for the level adapters.
The VHDL code has 2 PLL entities, 2 RAMs and 1 PCS entity.

We measured the following currents:

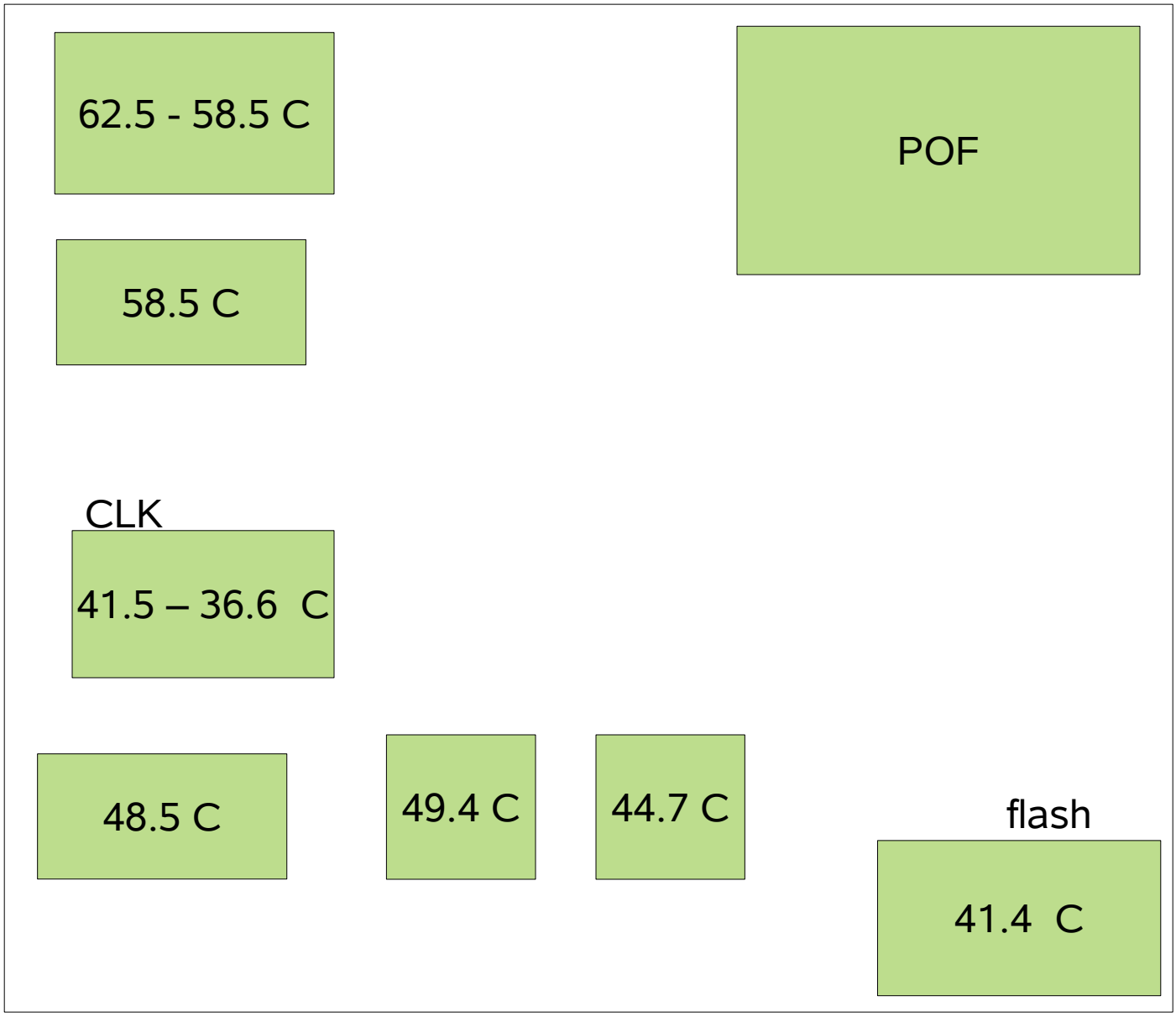
1 - Current (+5V) -> 521 mA if all pins of the level adapter U2 are used (all pins have as input the clock signal at 50 Mhz), while U1 and U3 are not used.

2 - Current (2.5V)-> 159 mA if only one pin of U2 is used. U3 and U1 are not used.
In this case all Chips on the boards are colder respect the case 1, by – 6C for all.

CHIP TEMPERATURES



CHIP TEMPERATURES



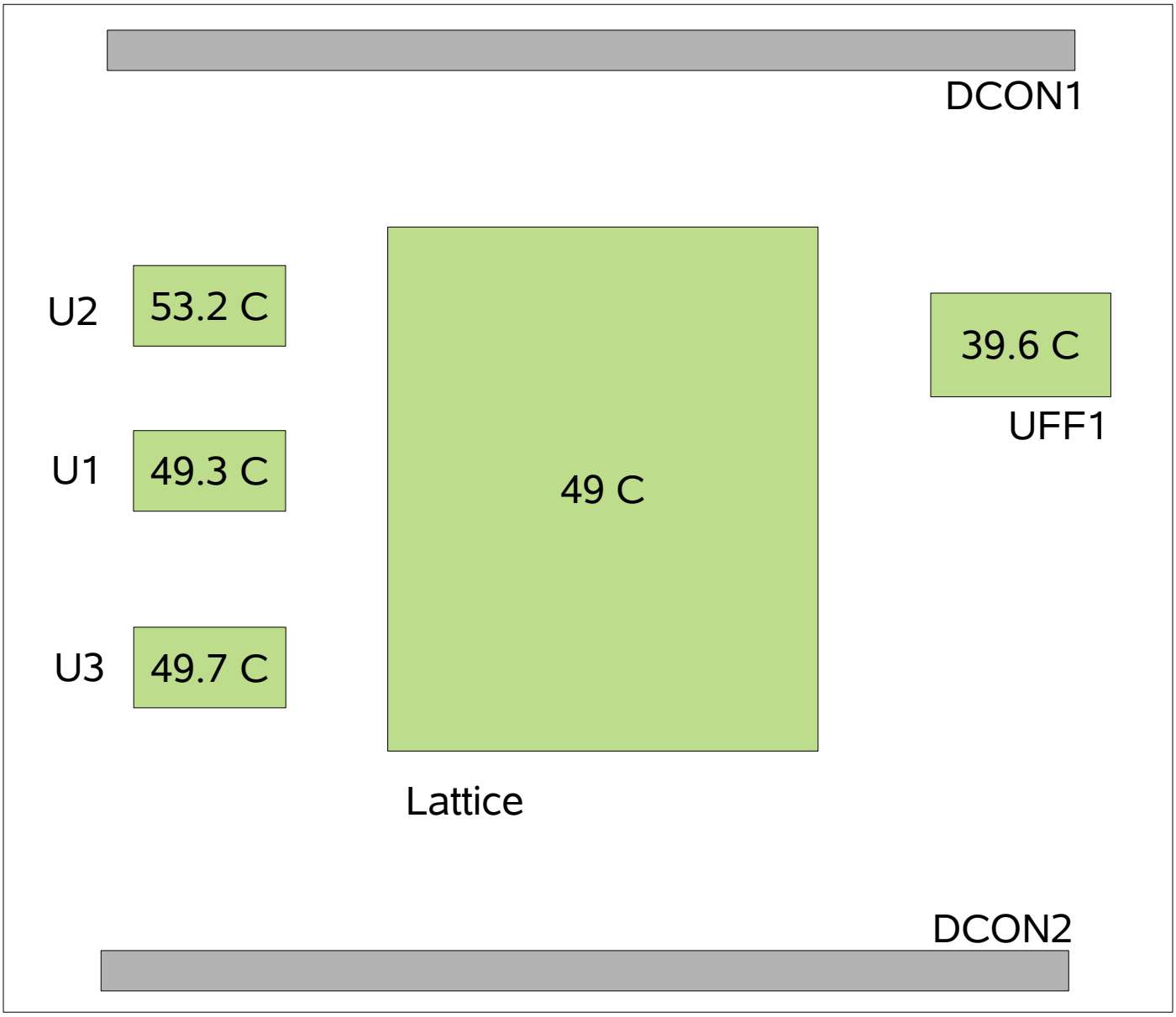
CHIP TEMPERATURES

Test conditions: program in the FPGA which generates a clock signal (**25 MHz**). We use this clock signal as input for the level adapters.
The VHDL code has 2 PLL entities, 2 RAMs and 1 PCS entity.

We measured the following currents:

- Current (+5V) -> 459 mA if all pins of the level adapter U2 are used (all pins have as input the clock signal at 25 Mhz), while U1 and U3 are not used.

CHIP TEMPERATURES (25MHz)



CHIP TEMPERATURES(25MHz)