Ideas for MDC readout

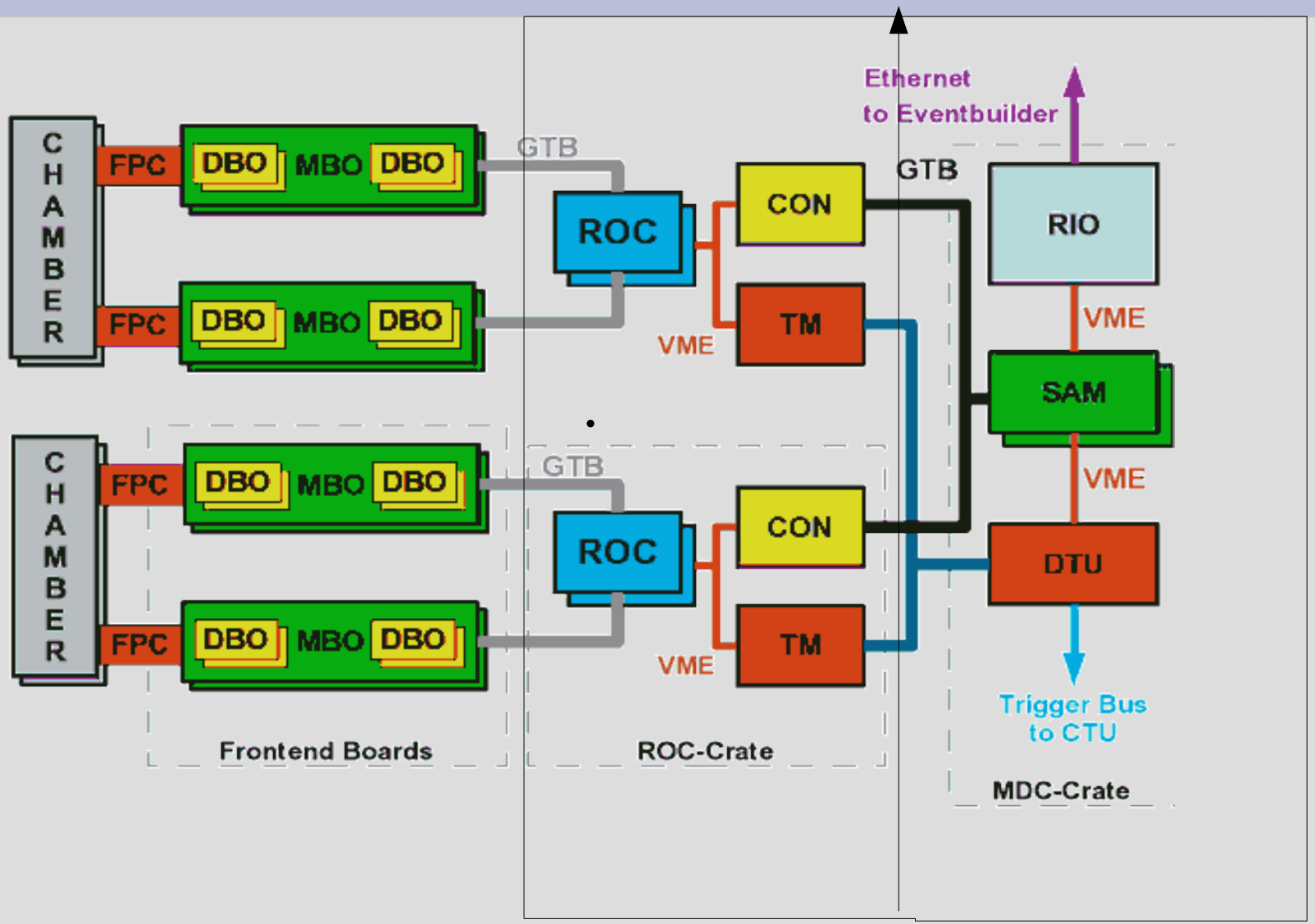
Which is the task?
Integrating MDC readout (motherboard) to the TRBv2 board.
Solution:
We build an addon board on TRBv2 that:

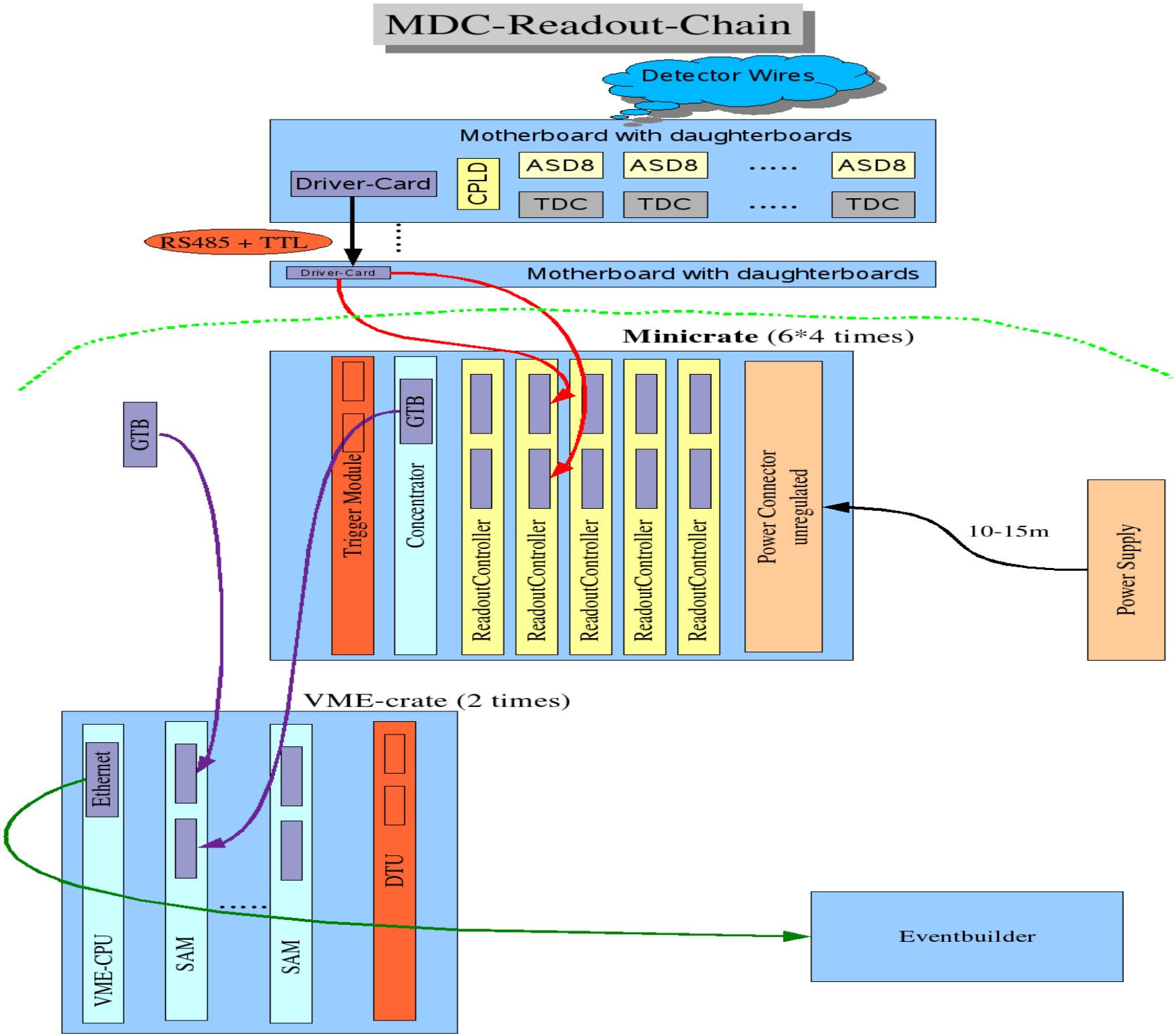
-> reads motherboard's TDC information in parallel

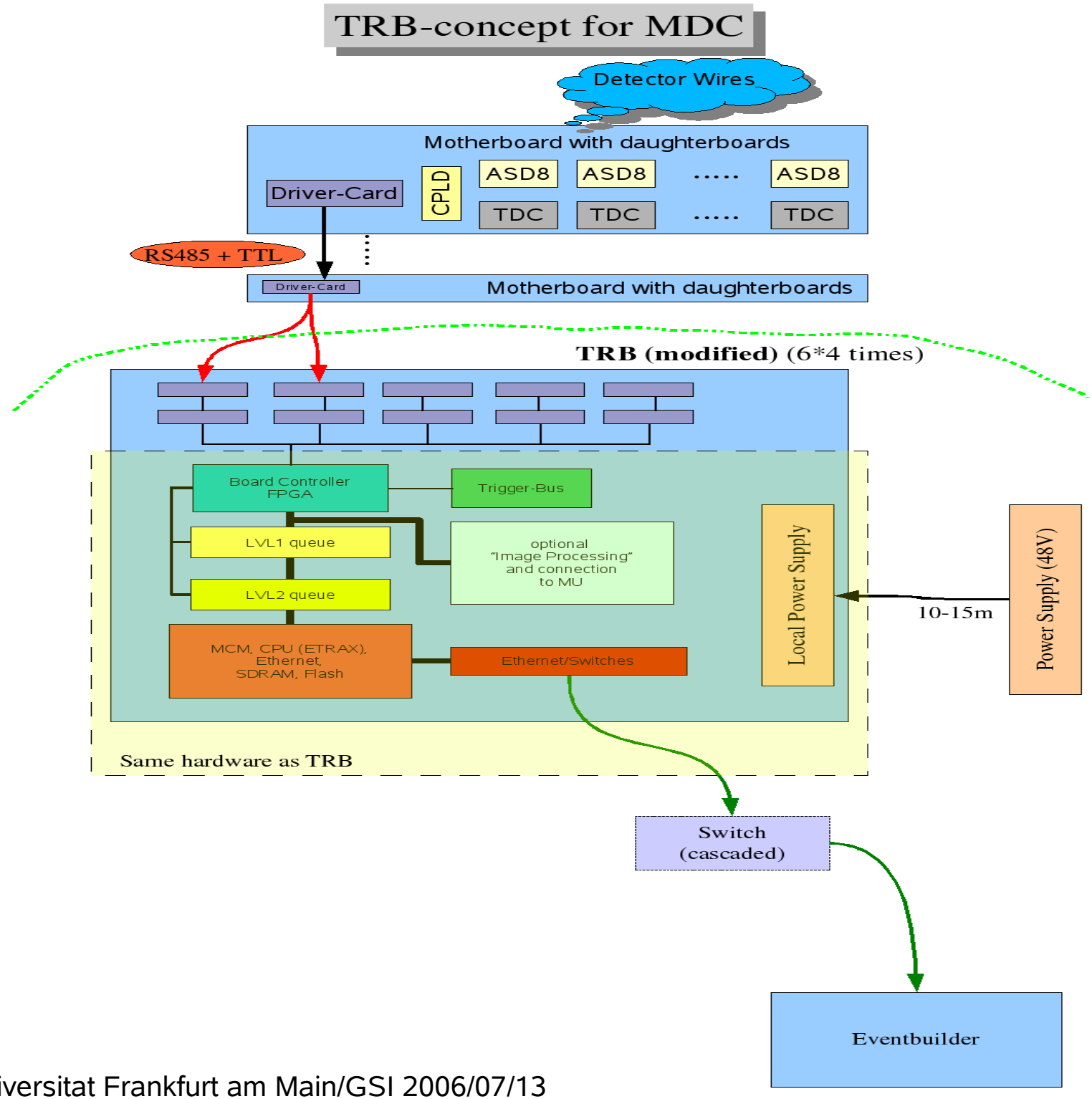
-> increase LVL1-rate capability

-> the processed data is transferred to TRBv2

MDC readout nowadays




MDC-Readout-Chain
Detector Wires
Motherboard with daughterboards
Driver-Card
CPLD
ASD8
ASD8
.....
ASD8
TDC
TDC
.....
TDC
RS485 + TTL
Driver-Card
Motherboard with daughterboards
Minicrate (6*4 times)
GTB
Trigger Module
GTB
Concentrator
ReadoutController
ReadoutController
ReadoutController
ReadoutController
ReadoutController
Power Connector unregulated
10-15m
Power Supply
VME-crate (2 times)
Ethernet
VME-CPU
SAM
SAM
DTU
Eventbuilder


TRB-concept for MDC
Detector Wires
Motherboard with daughterboards
Driver-Card
CPLD
ASD8
ASD8
.....
ASD8
TDC
TDC
.....
TDC
RS485 + TTL
Driver-Card
Motherboard with daughterboards
TRB (modified) (6*4 times)
Board Controller FPGA
Trigger-Bus
LVL1 queue
optional "Image Processing" and connection to MU
LVL2 queue
MCM, CPU (ETRAX), Ethernet, SDRAM, Flash
Ethernet/Switches
Local Power Supply
10-15m
Power Supply (48V)
Same hardware as TRB
Switch (cascaded)
Eventbuilder

How the new board looks like..

-> 400 input wires

-> 10 input RS485 connectors

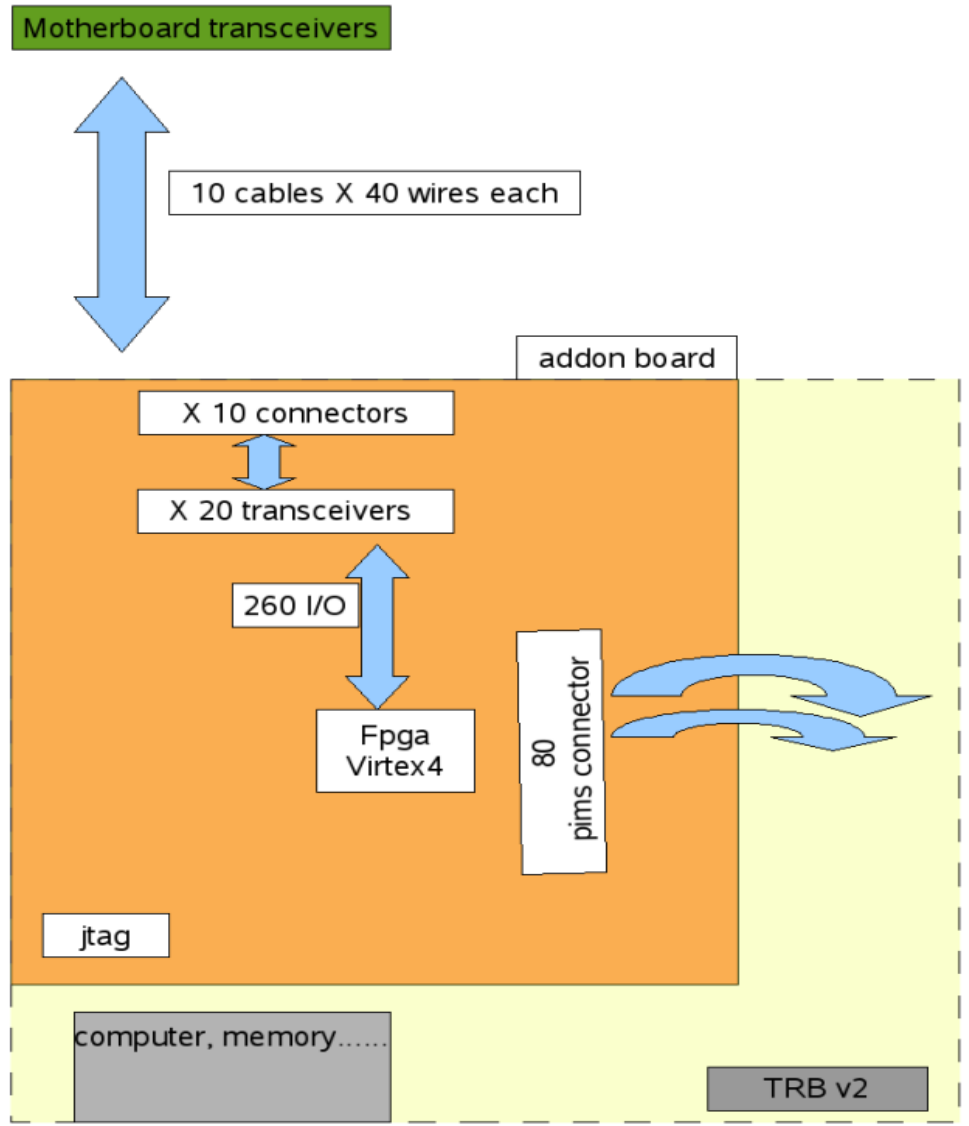
-> 20 transceivers (max 1W each)

-> FPGA (XC4VFX40):
- --> needed 260 I/O (to read transceivers)
- --> differential clk input supported?
- --> tot. power needed up to 10 W

-> 5 pin jtag on board for fast programming

-> 2 QTE-040-01-L-D-A-K-Y (40 pins each)
9 Ghz, 2 A (per pin)
- --> 24 pins for power (fpga core and I/O) DC/DC on board
- --> 5 pins for jtag chain
- --> 40 pins communication my_fpga and trb_fpga (20 LVDS channel)

-> total 69 pins + 11 general purpose

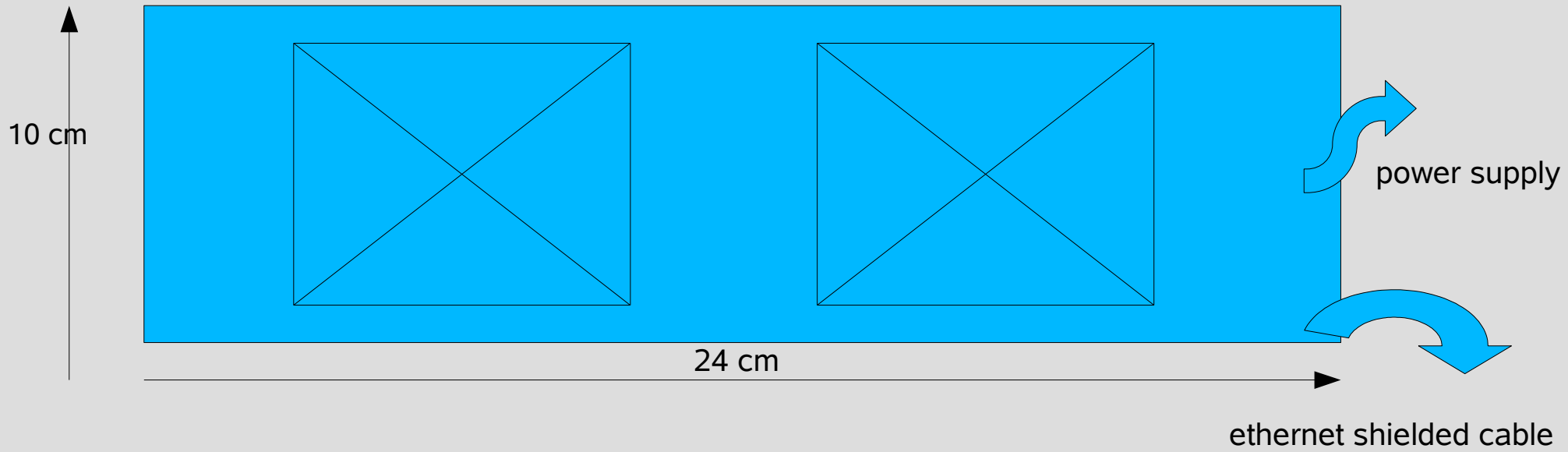


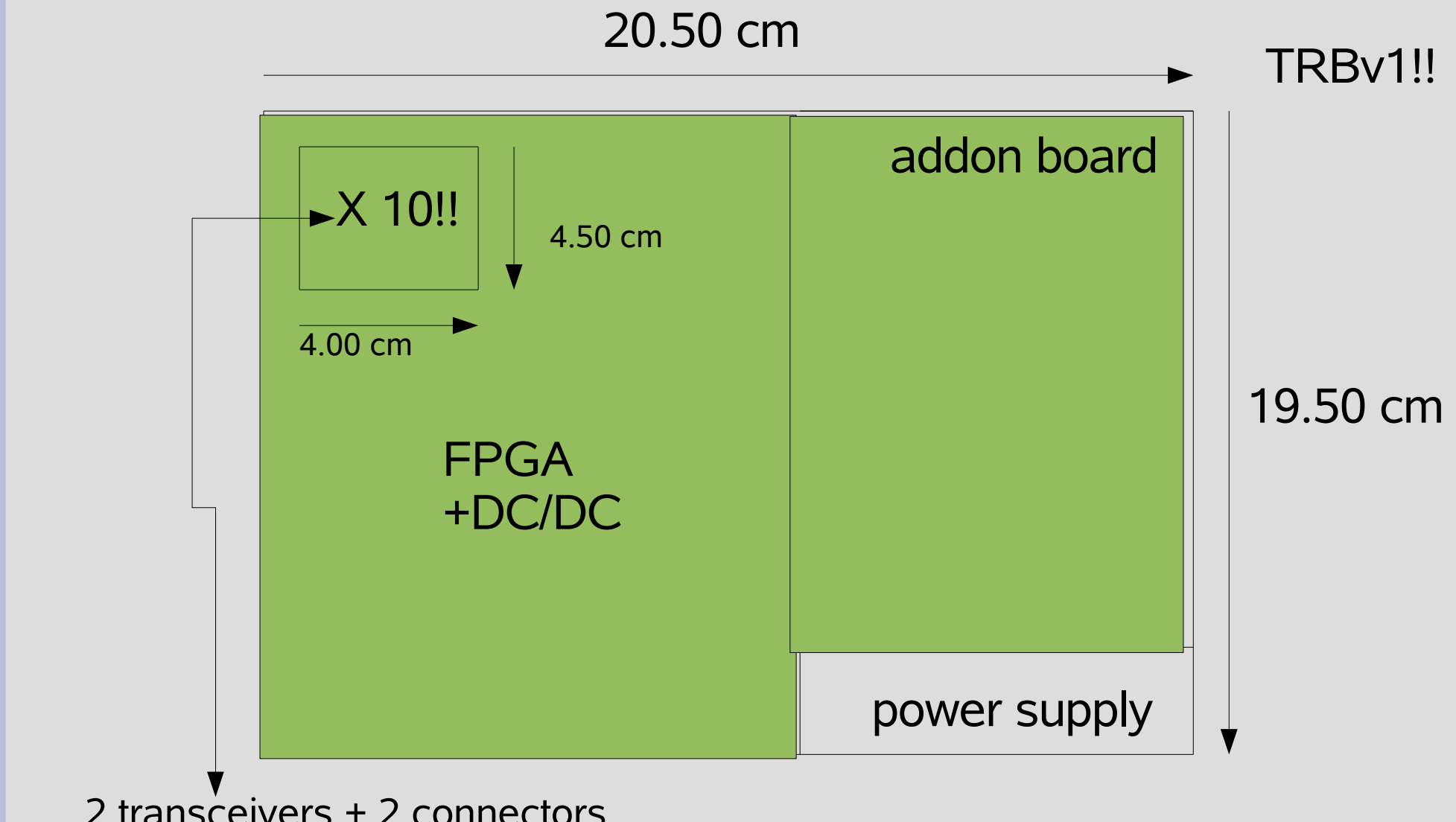
My tasks...

- Do we have enough space to connect all these wires on a small board?
- transmission protocol:
    - Hand-made bus using several lines
      ->NewTriggerBus (Ingo!!)
    - single data rate trasmitter (500MHz 16 bit word)?
      (xilinx aplication noteXAPP704)
- power supply
- case + fan

example: 1 Case + 2 fans

- aluminum case: inside the TRB and addon board.
- on one side 2 fans (1 A each 8 cm X 8 cm X 2.5 cm)




20.50 cm
TRBv1!!
addon board
X 10!!
4.50 cm
4.00 cm
FPGA
+DC/DC
19.50 cm
power supply
2 transceivers + 2 connectors