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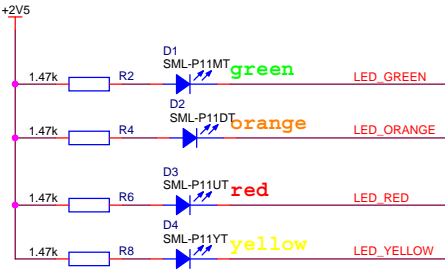
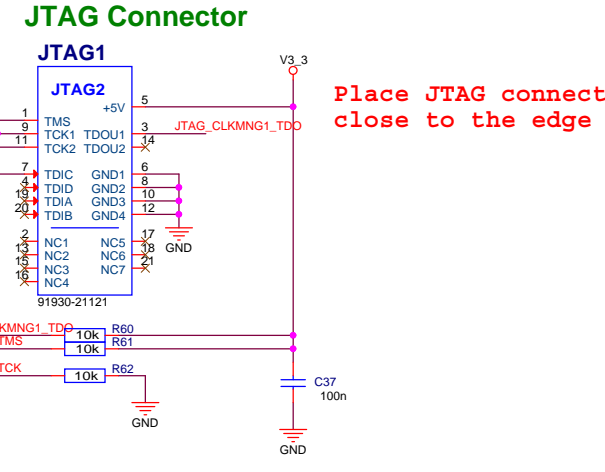
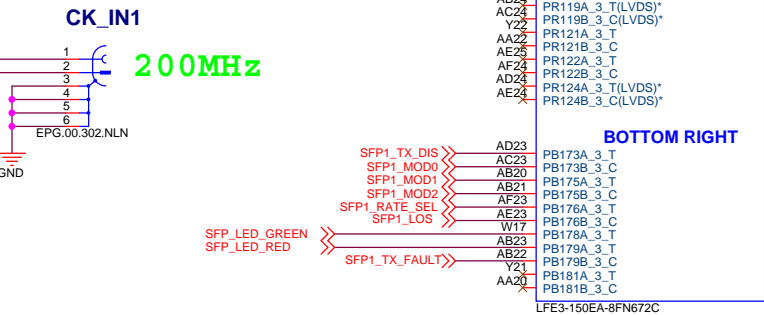
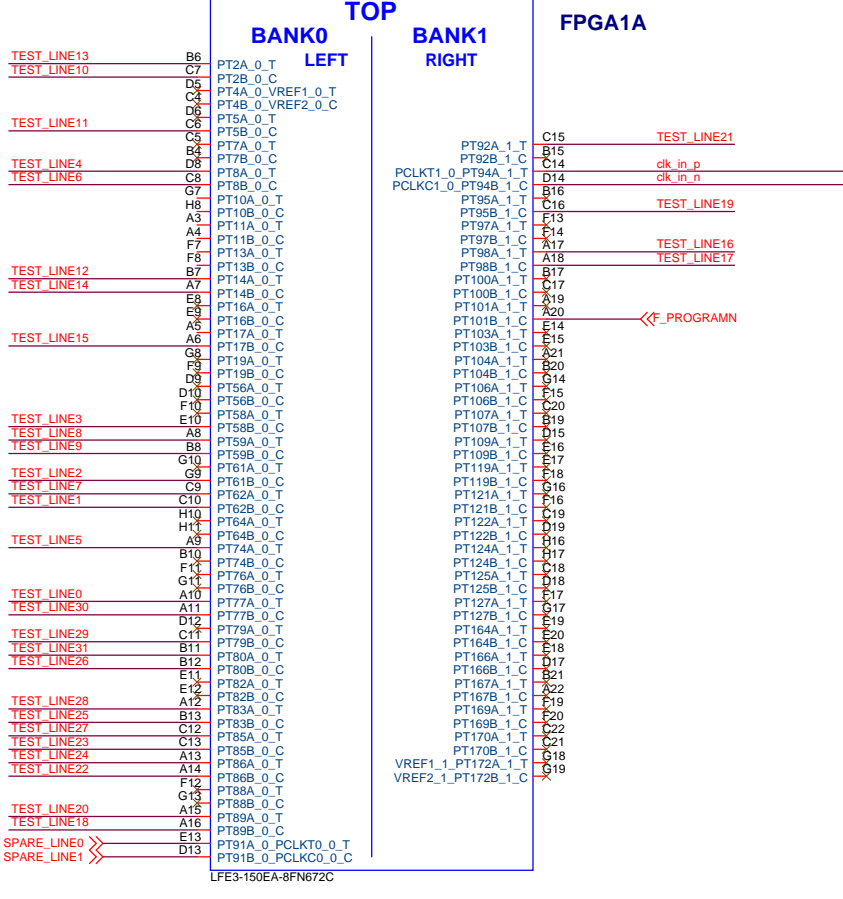
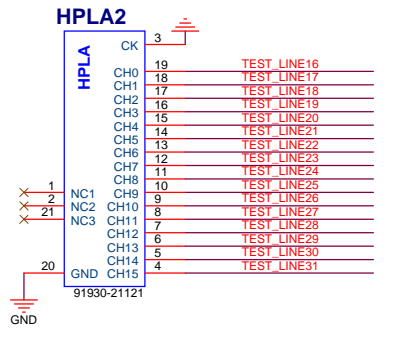
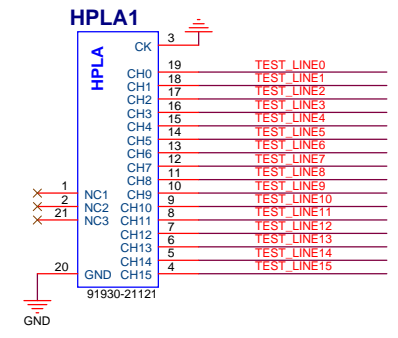
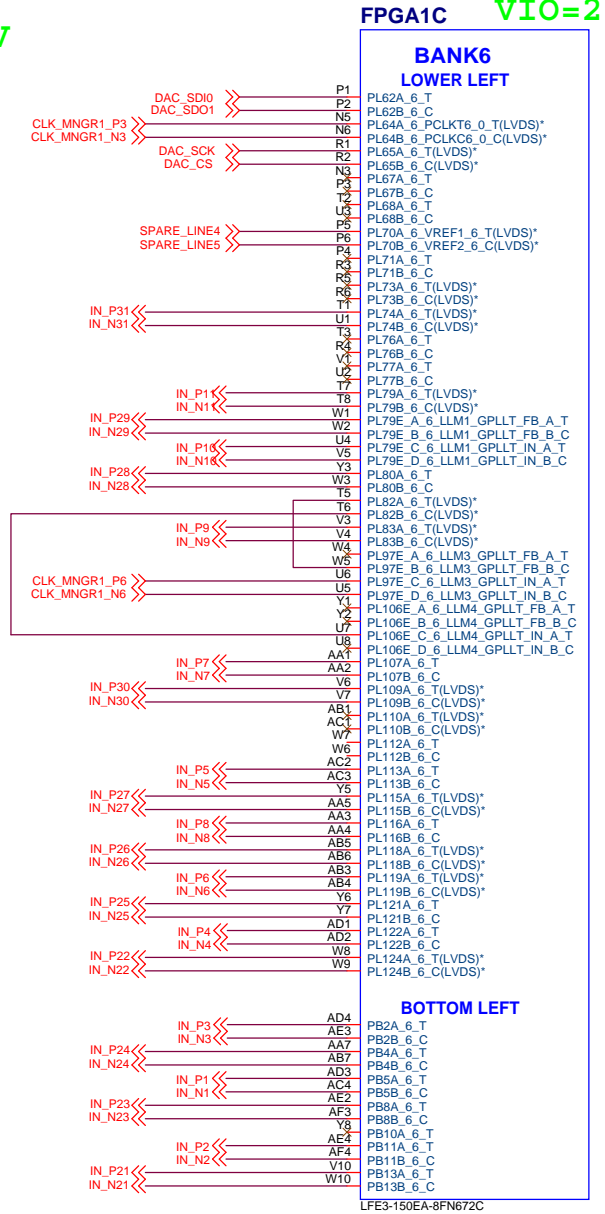
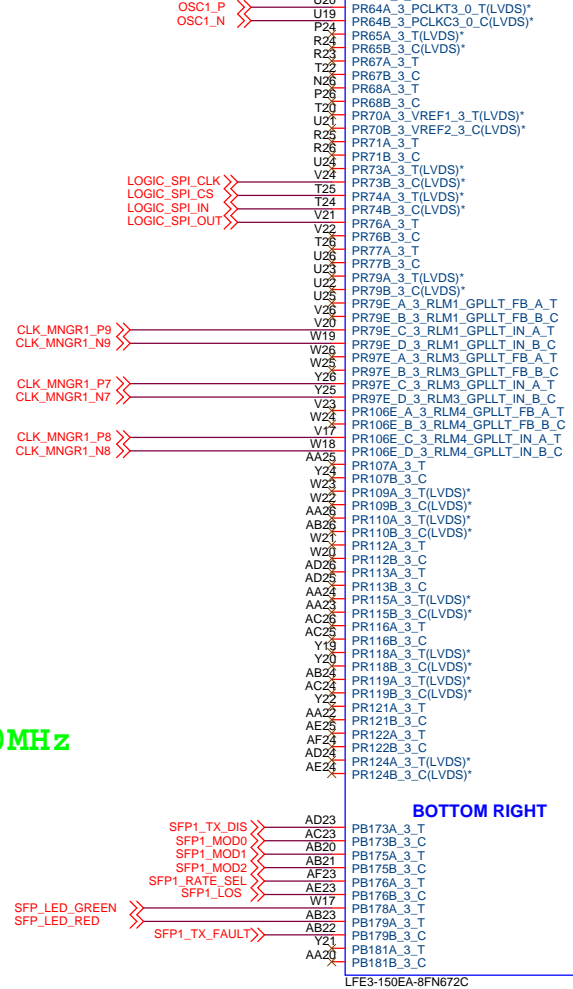
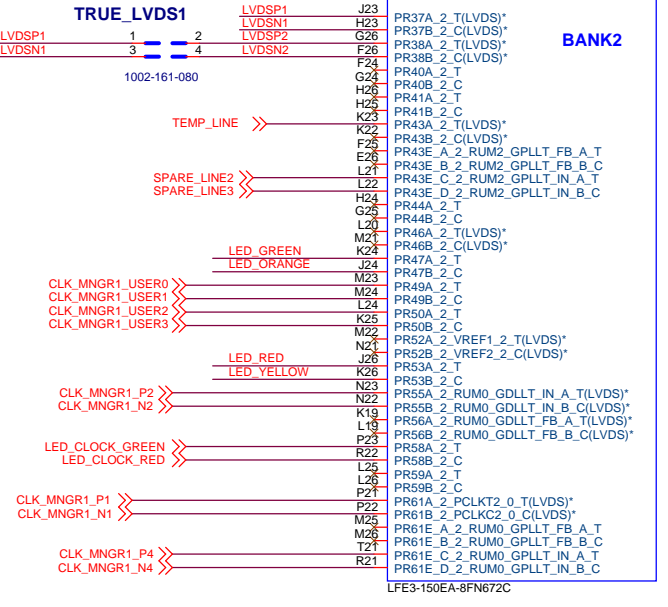
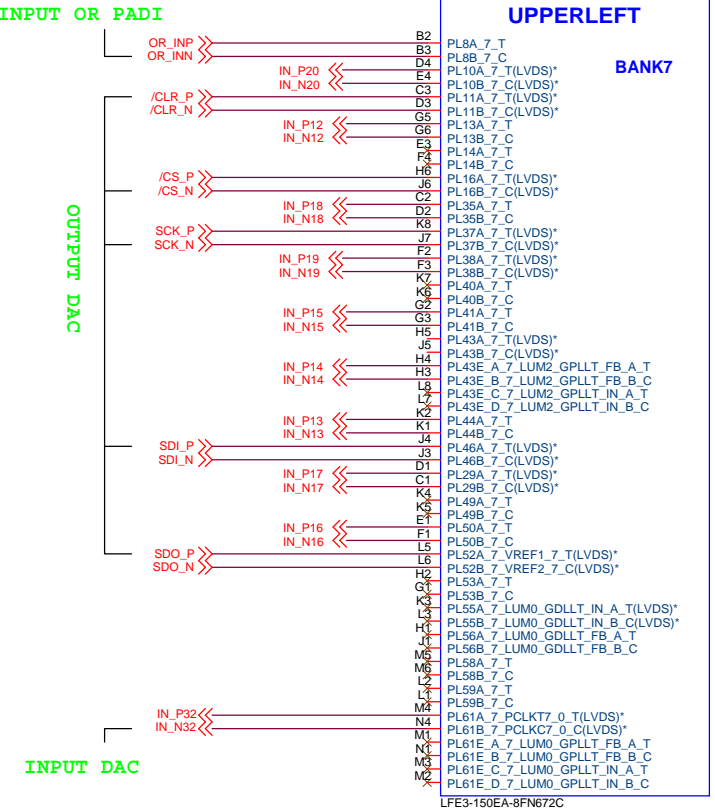
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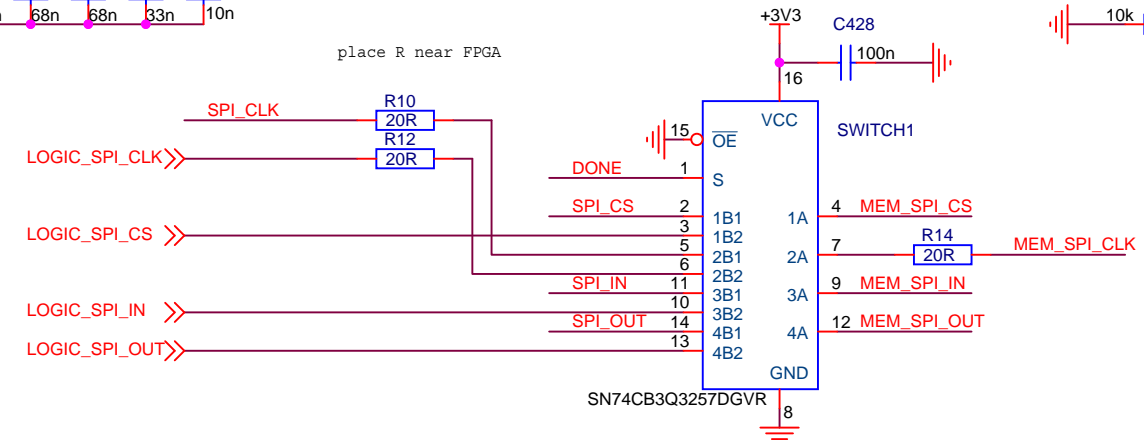
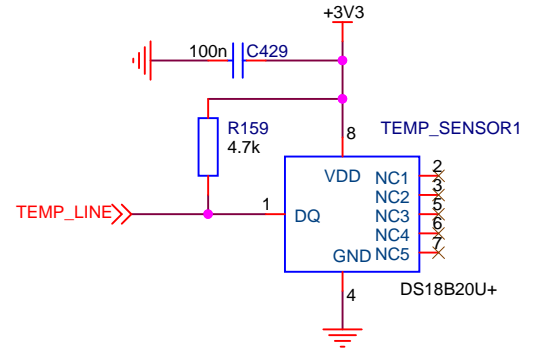
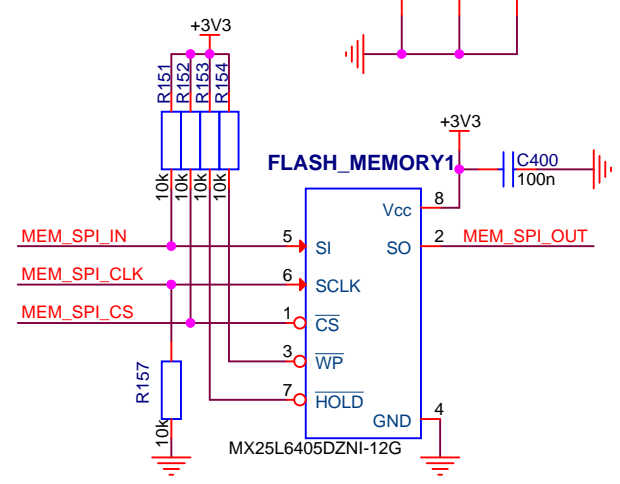
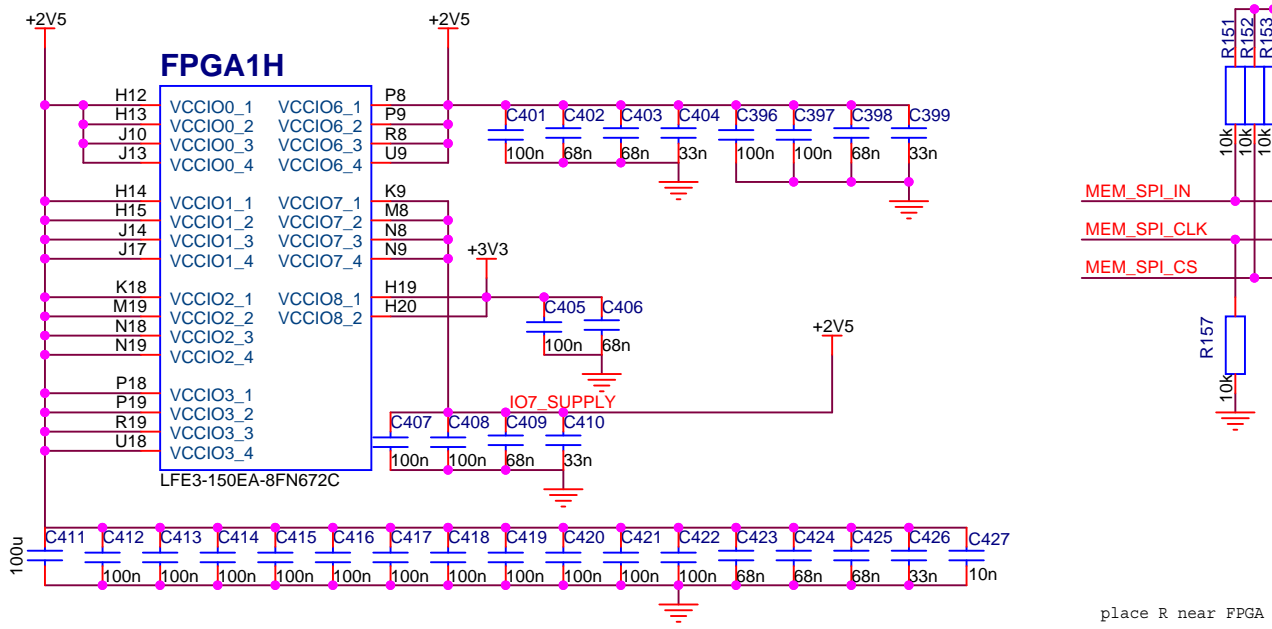
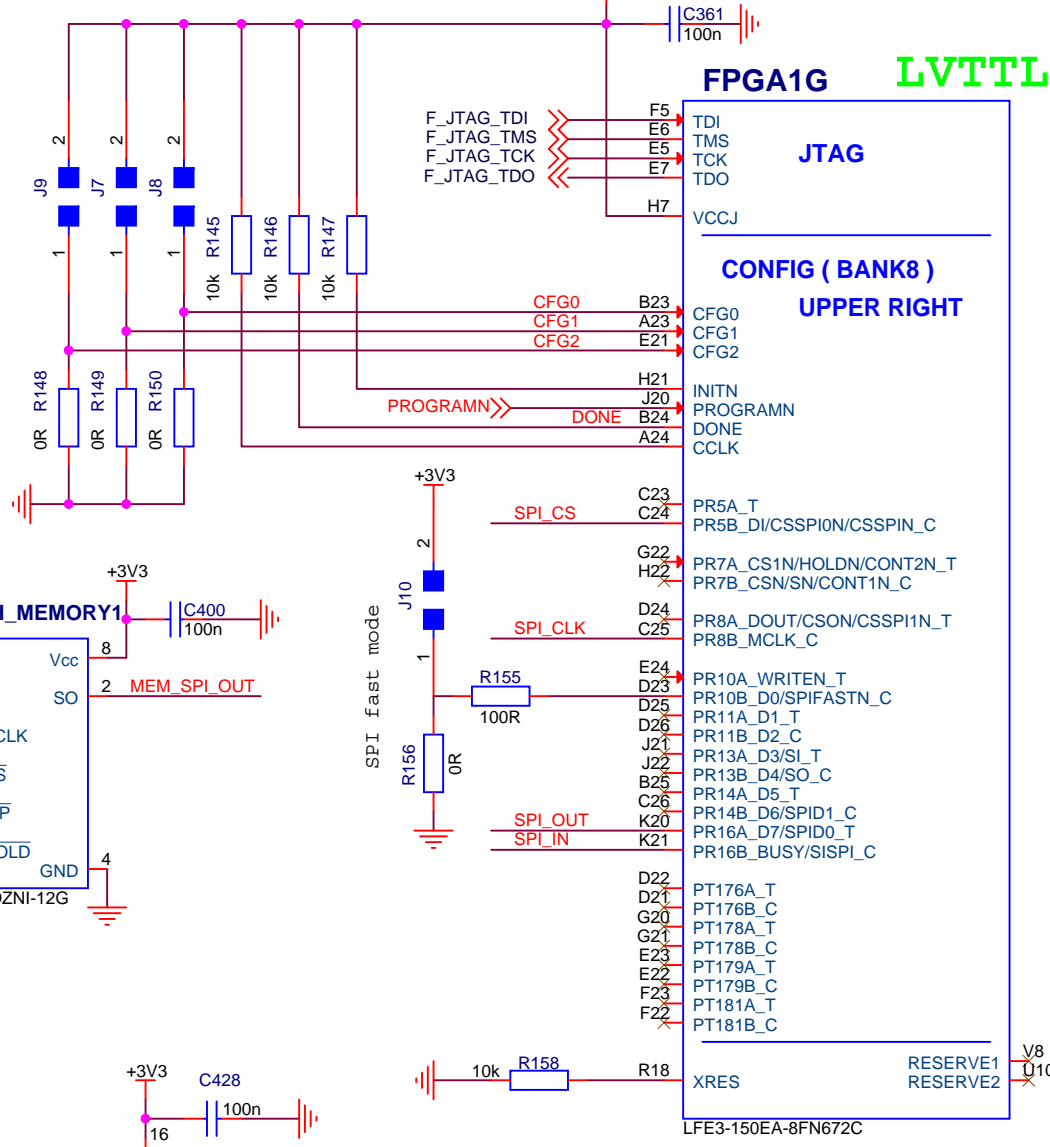
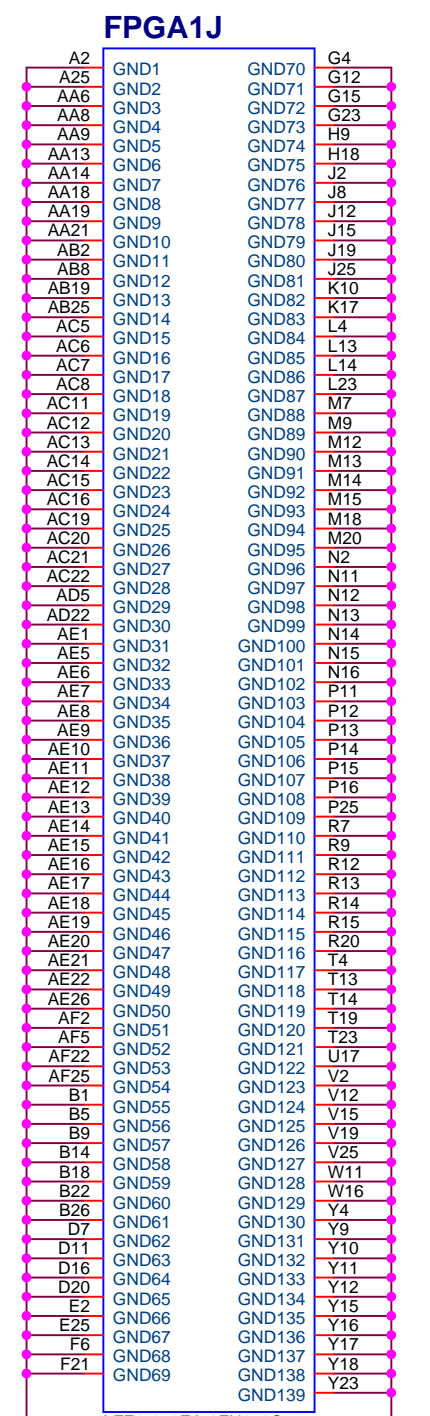
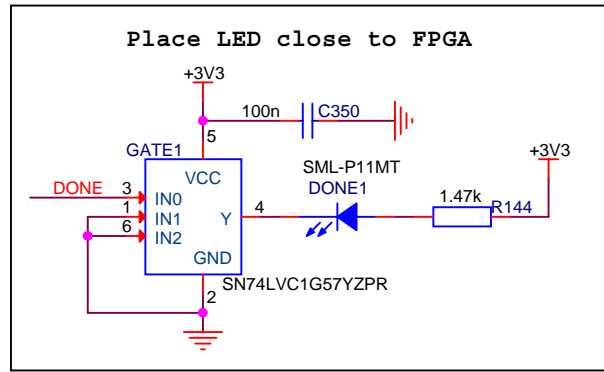
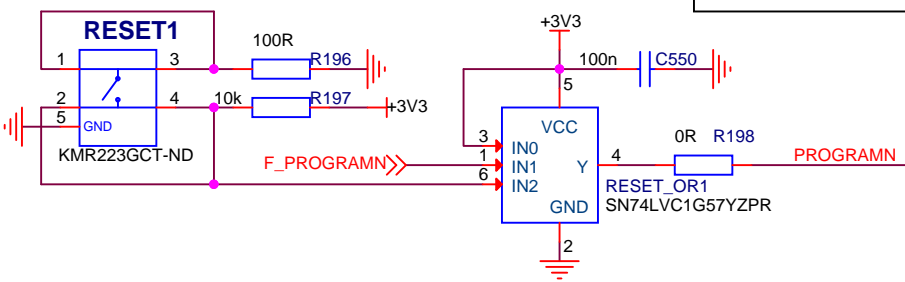
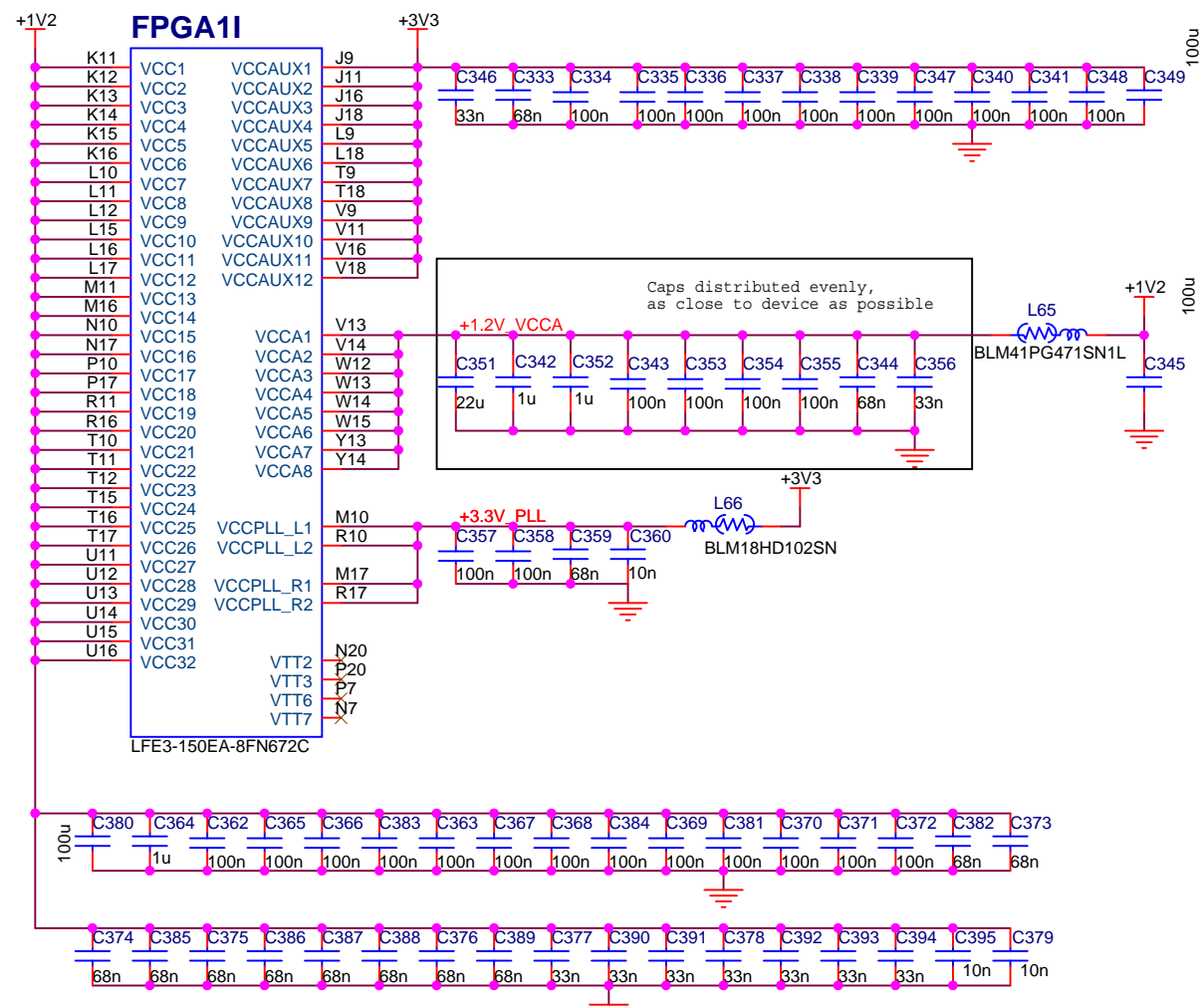
200MHz

JTAG Connector

Place JTAG connector close to the edge

no adjacent pins should be in use for changing signals





GSI

03_FPGA-Power

Gesellschaft für Schwerionenforschung mbH
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GERMANY
www.gsi.de

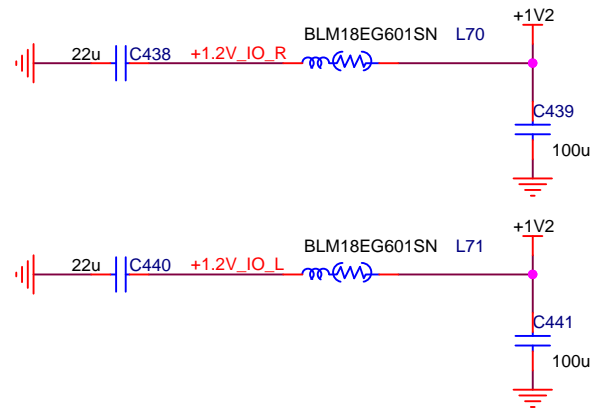
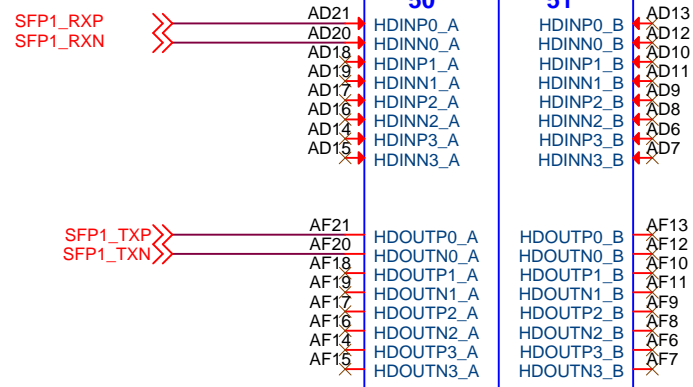
Design: K:\GSI\JOB\COME AND KISS\CBM-TOF-FEE\CBM-TOF-FEE\1CBM-TOF-FEE-03_FPGA-Power
Modified: Thursday, March 21, 2013
Designer: M. Traxler

Size: A3
Page: 3 / 6
Layouter: S.Voltz

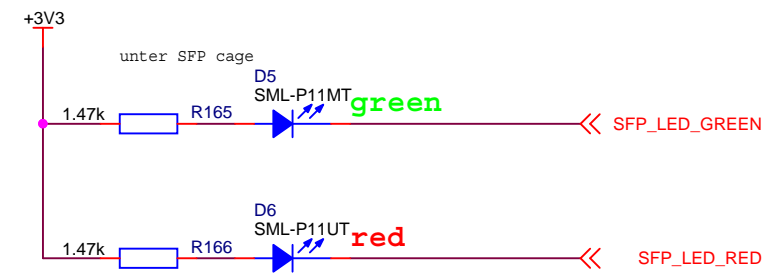
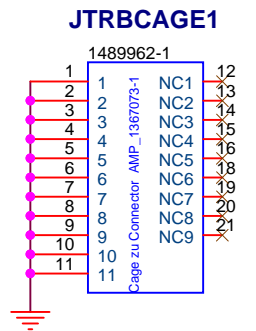
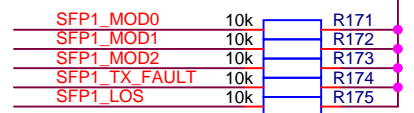
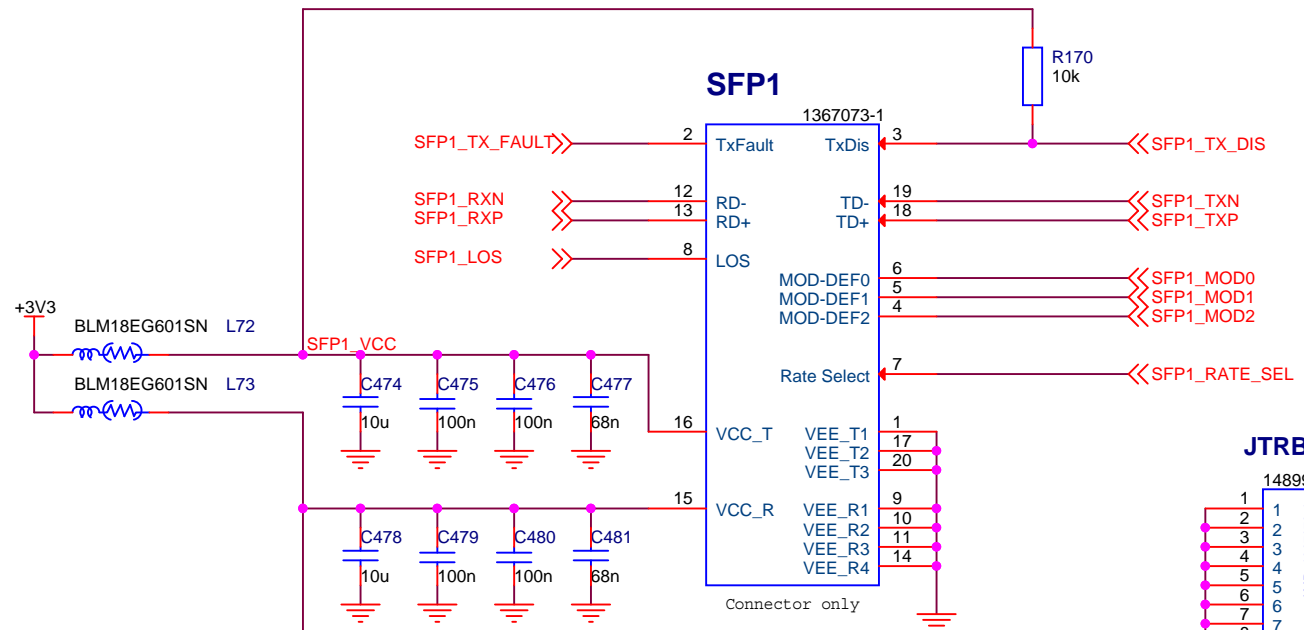
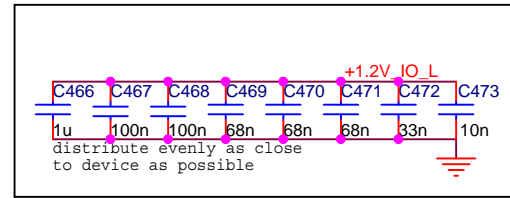
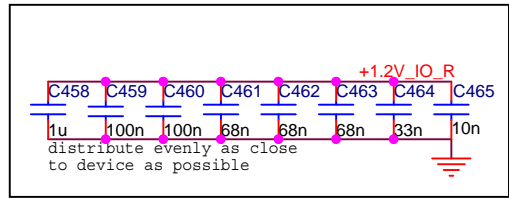
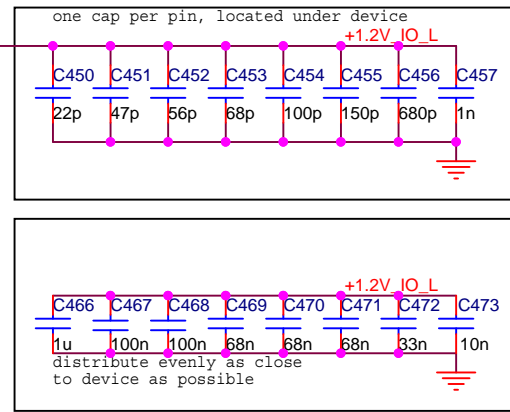
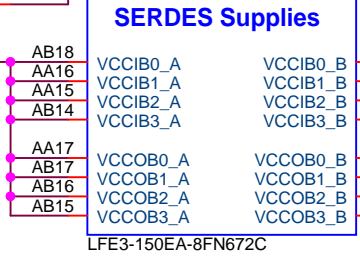
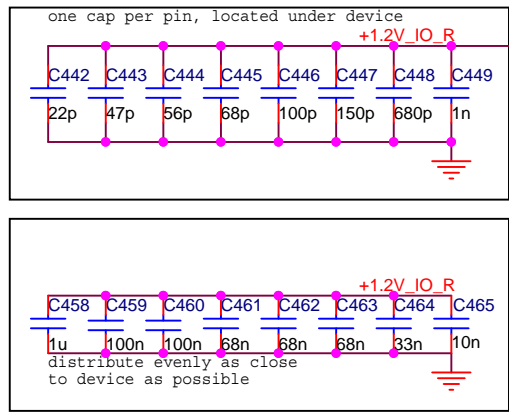
FPGA1F

SERDES
BOTTOM

RIGHT 50 LEFT 51



100Ohms here?
offen bitte



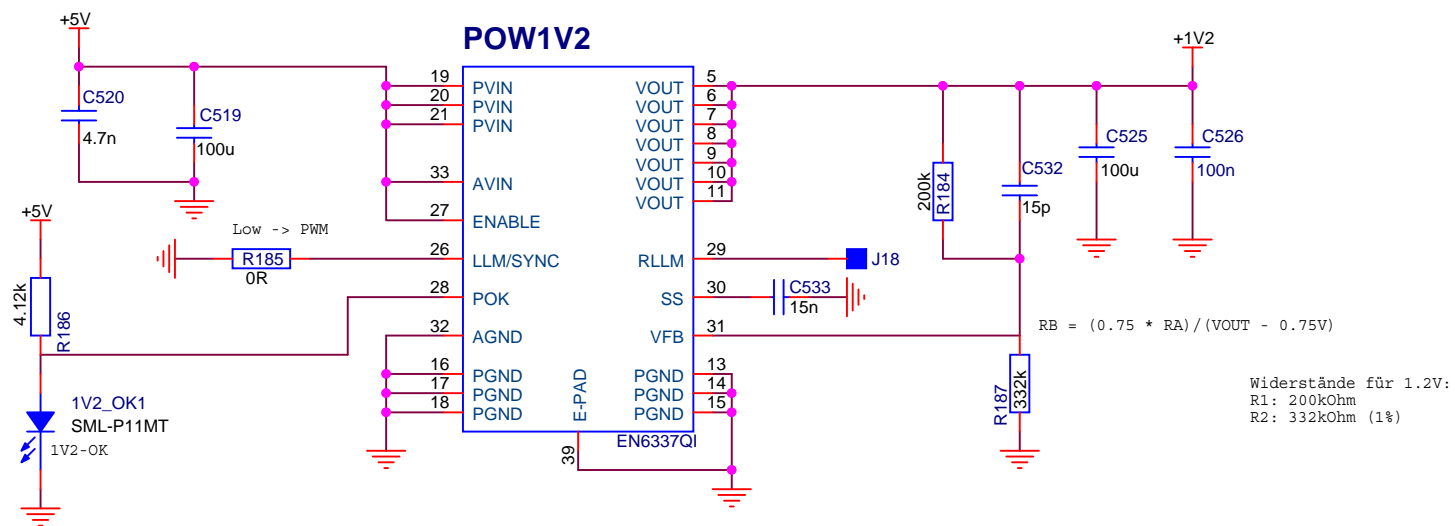
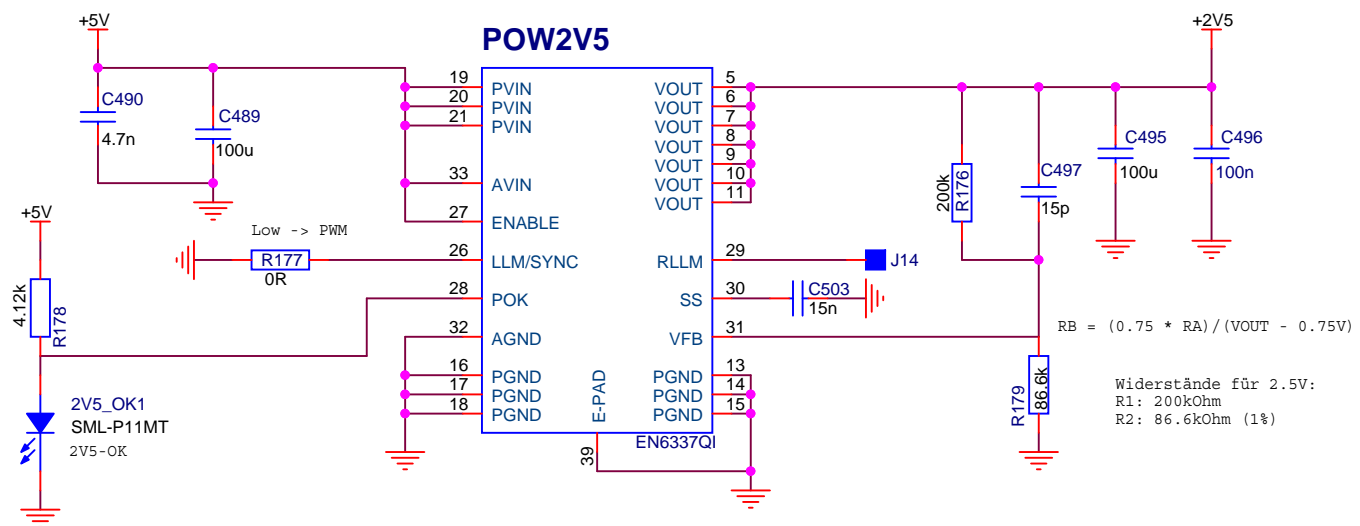
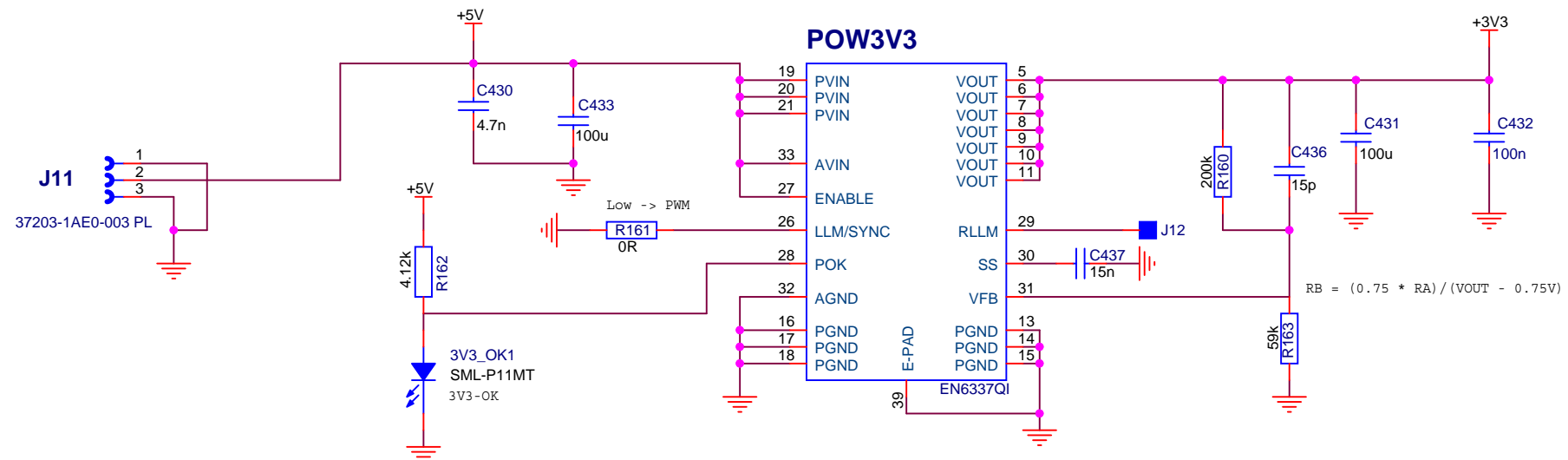
MODDEF0 is grounded by module when inserted

GSI
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GERMANY
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04_SERDES + SFP

Design: K:\GSI\JOB\COME AND KISS\CBM-TOF-FEE\CBM-TOF-FEE\1CBM-TOF-FEE-04_SERDES + SFP
Modified: Thursday, March 21, 2013
Designer: M. Traxler

Size: A3
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05_Power

Design: K:\GSI\JOB\COME_AND_KISS\CBM-TOF-FEE\CBM-TOF-FEE\1CBM-TOF-FEE-05_Power
 Modified: Thursday, March 21, 2013
 Designer: M. Traxler

Size: A3
 Page: 5 / 6
 Layouter: S.Voltz

