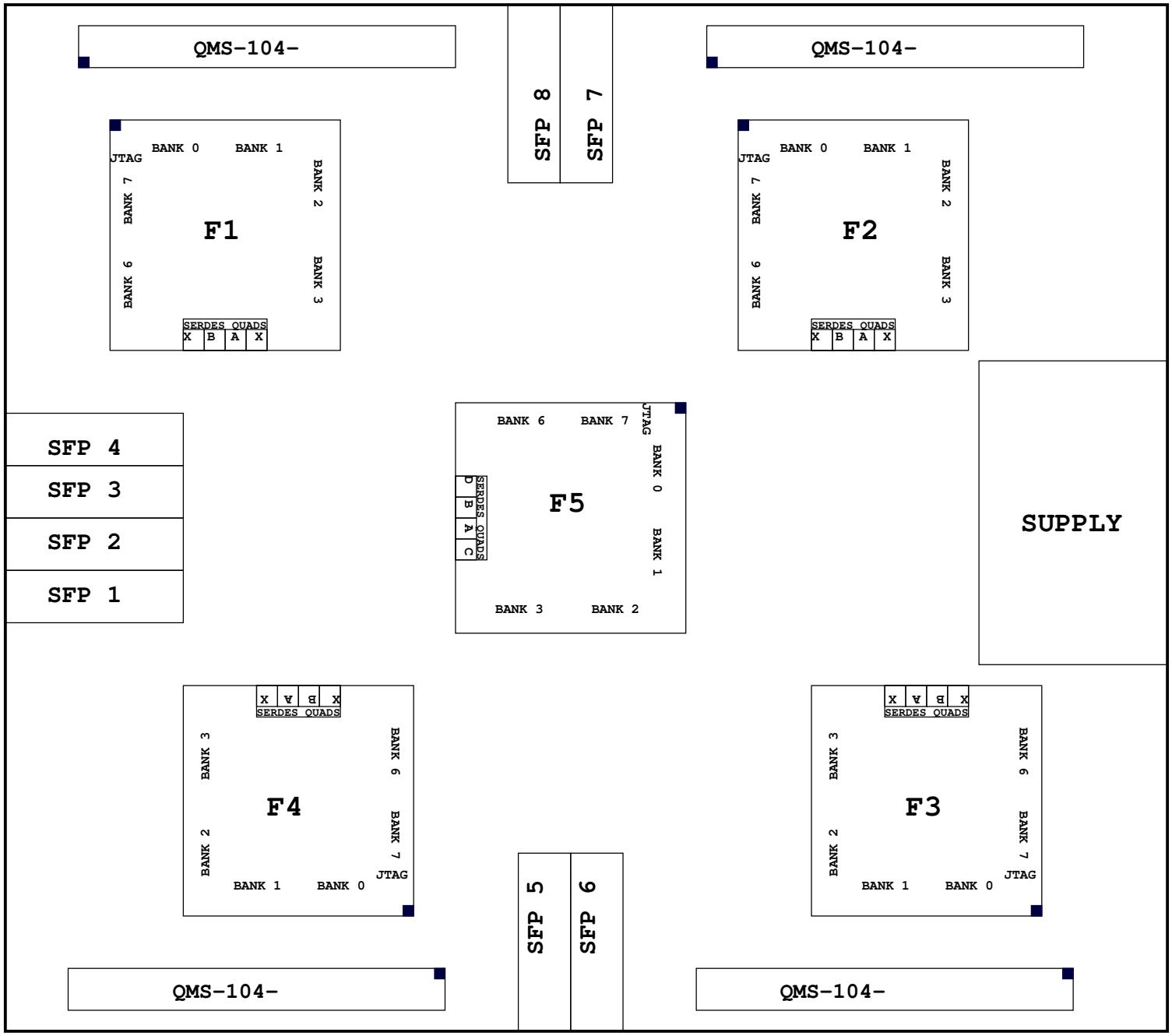

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00_LAYOUT

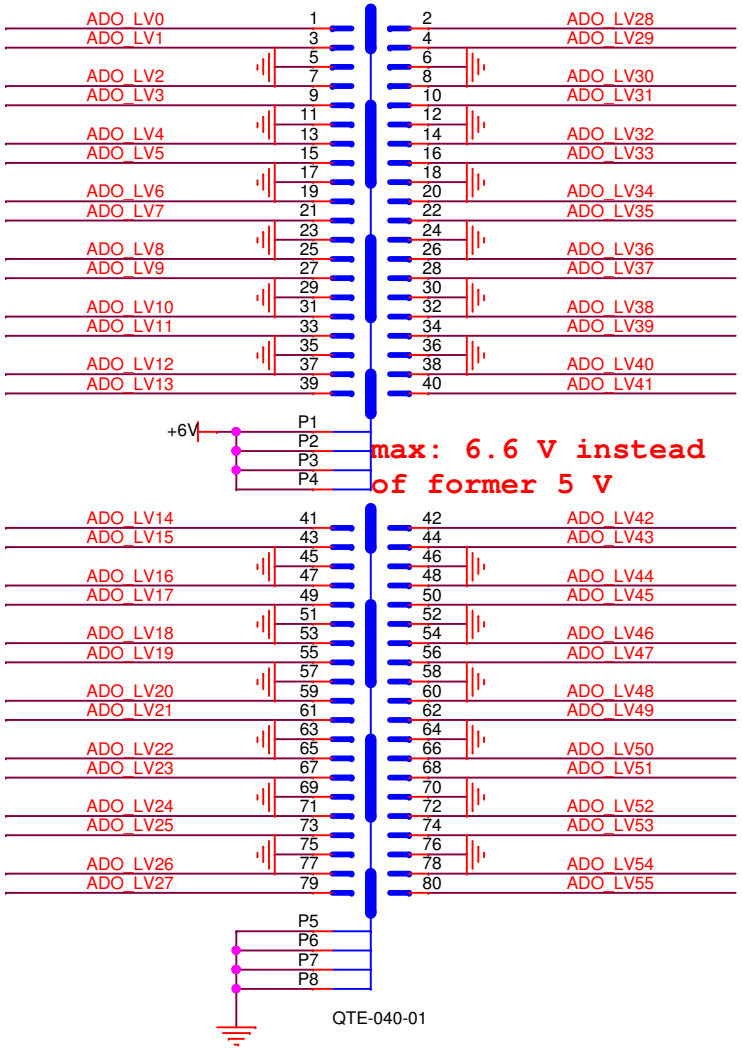
Design: K:\GSI\JOB\HADES\TRBV3\TRBV3.DSN
Modified: Wednesday, July 06, 2011 | Size: A3 | Page: 1 / 22
Designer: <Designer> | Layouter: <Layouter>

ADO_LV[61..0]

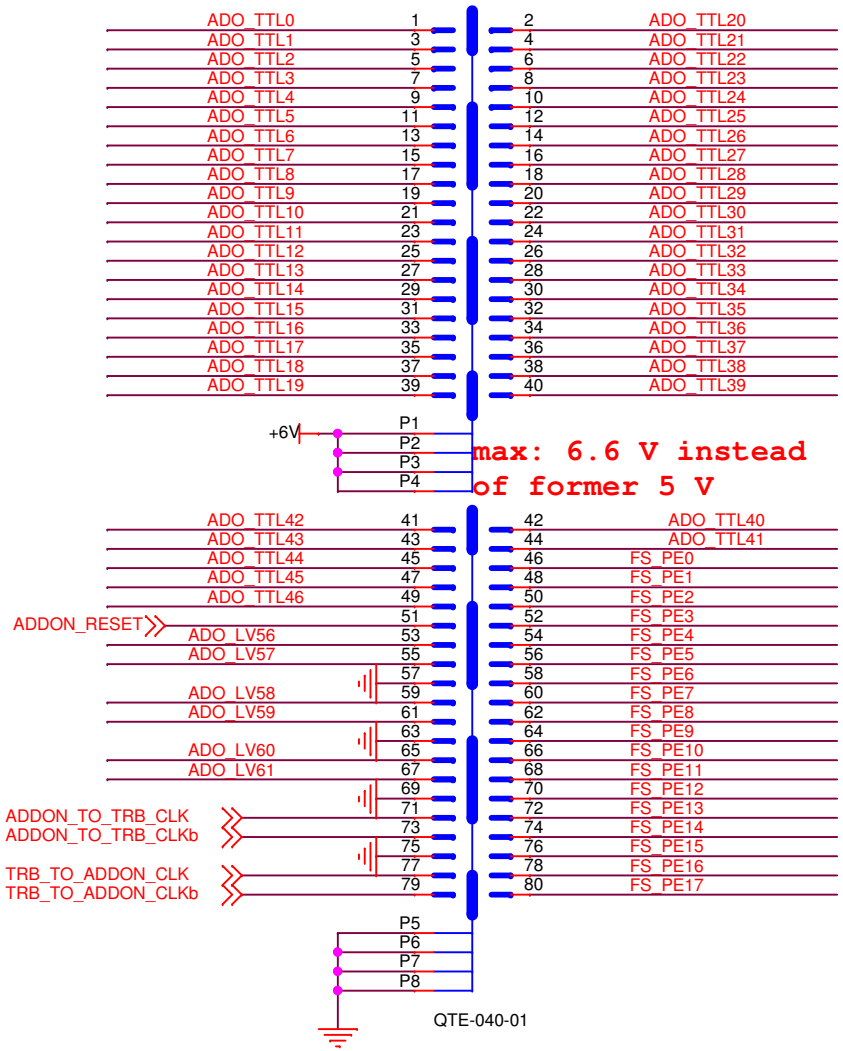
ADO_TTL[46..0]

FS_PE[17..0]

JADDON1



JADDON2



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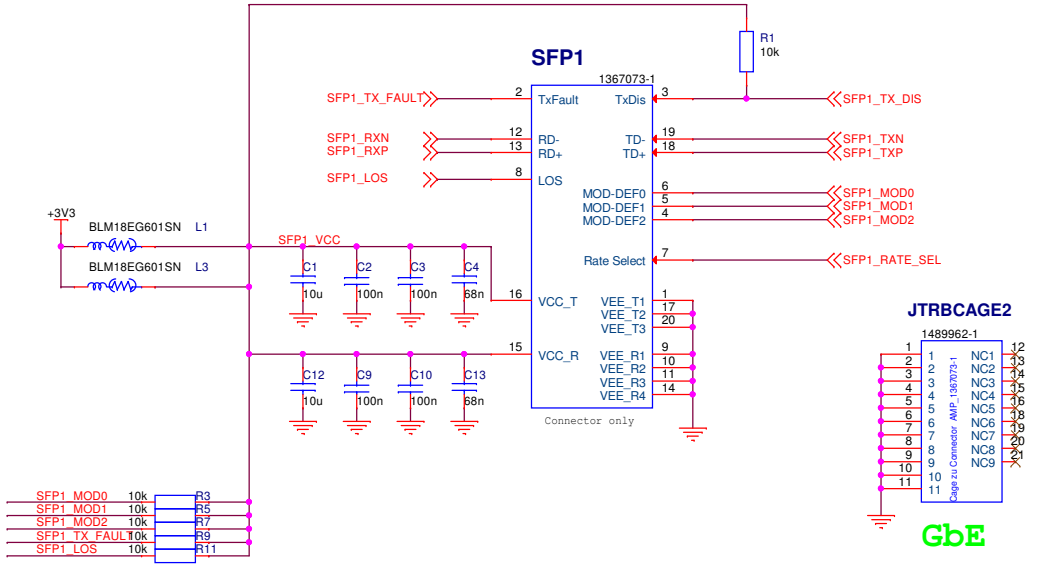
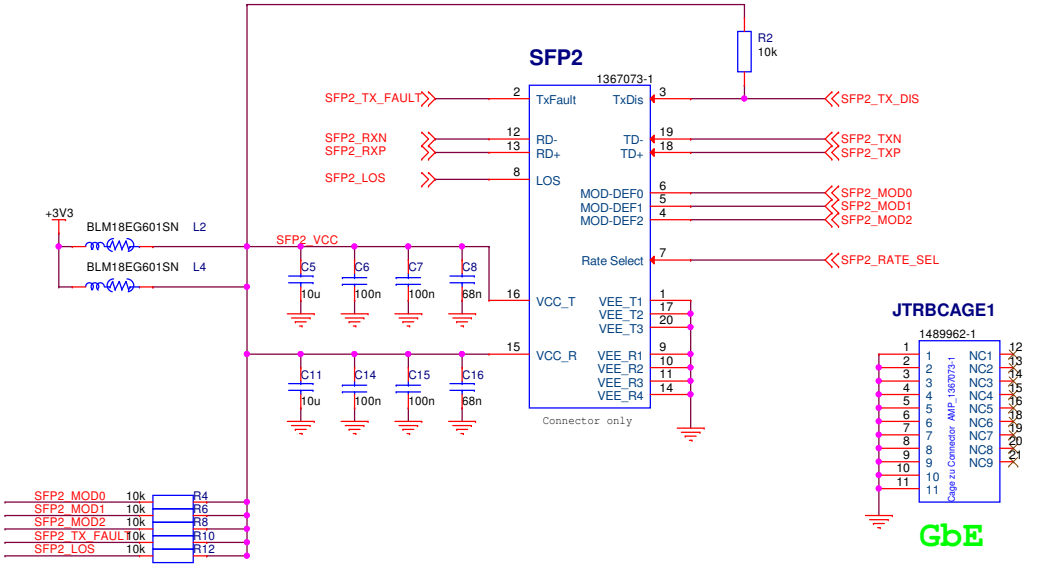
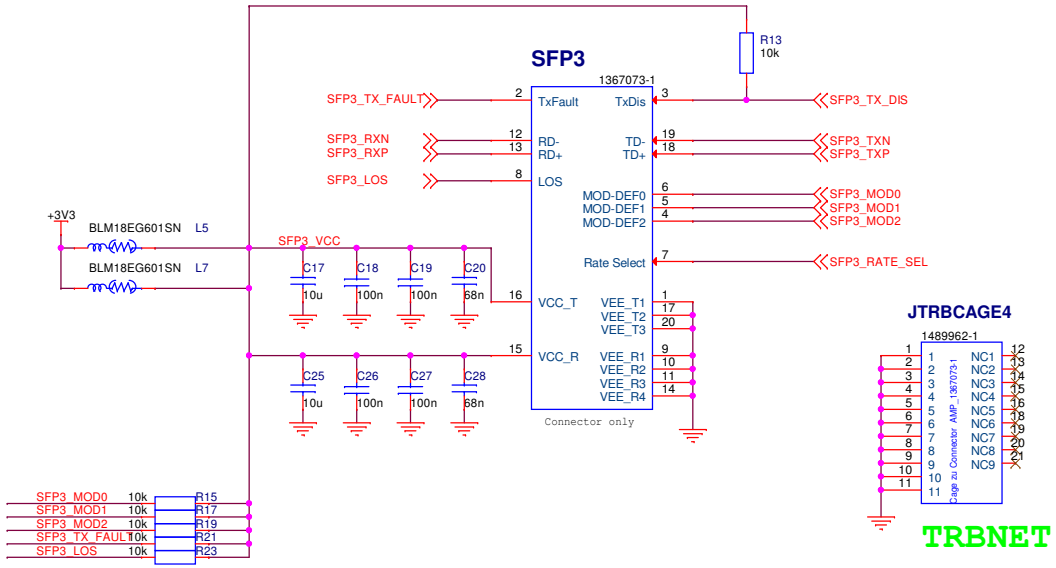
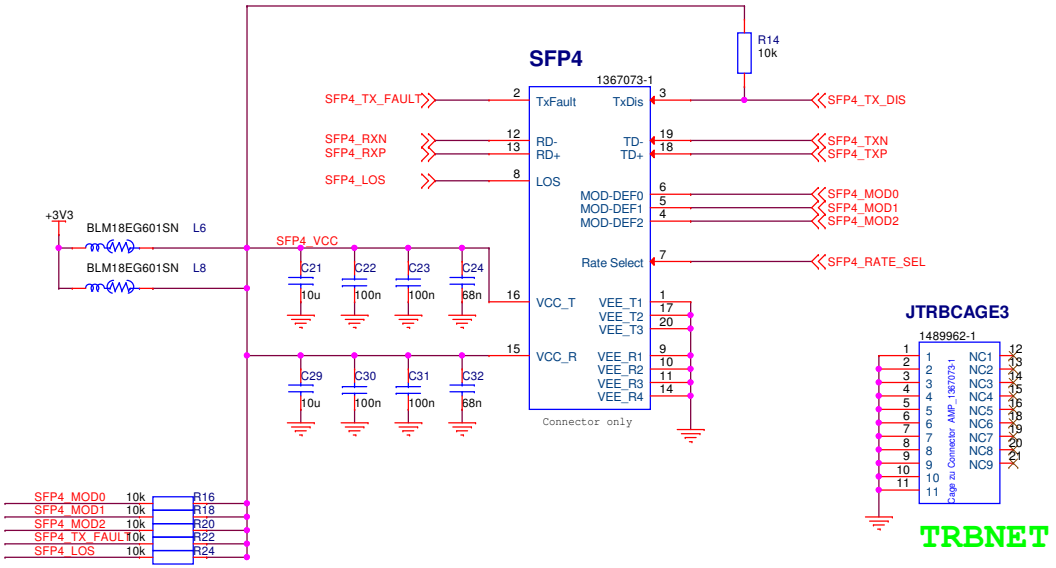
01_ADDON_CONNECTORS

Design: K:\GSIJOB\HADES\TRBV3\TRBV3.DSN		
Modified: Wednesday, July 06, 2011	Size: A4	Page: 2 / 22
Designer: <Designer>	Layouter: <Layouter>	









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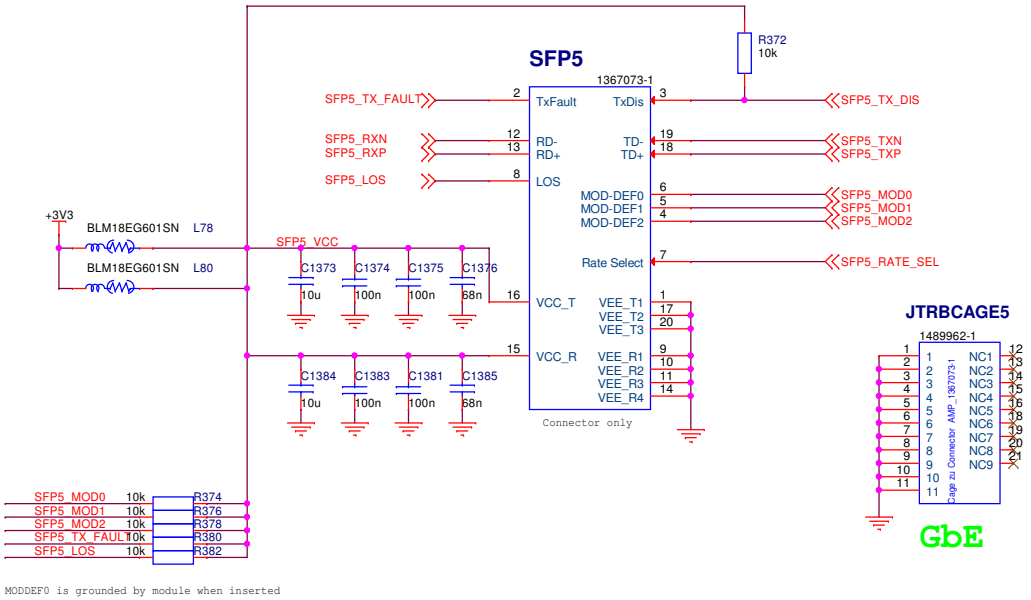
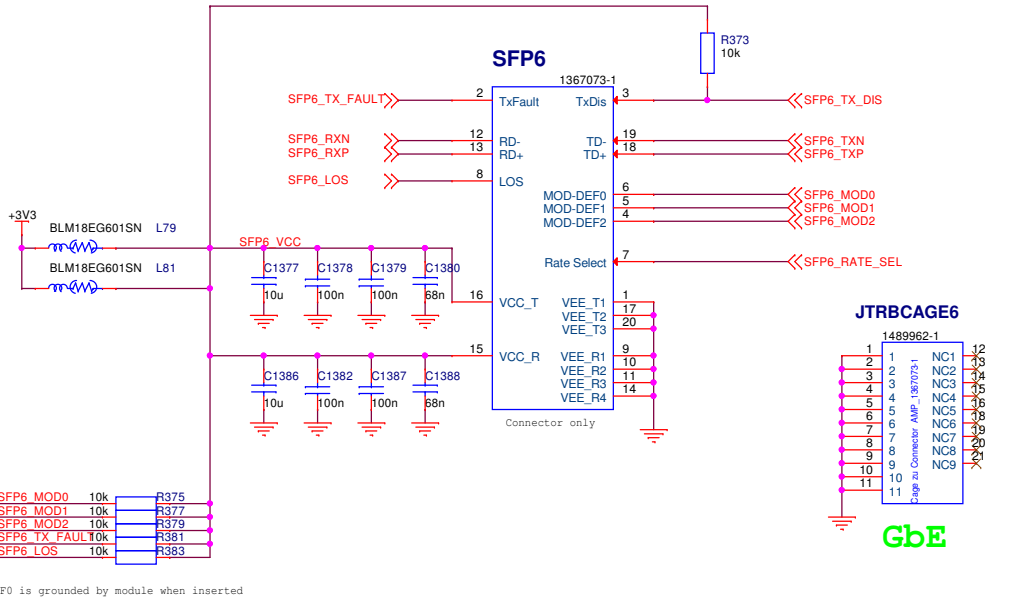
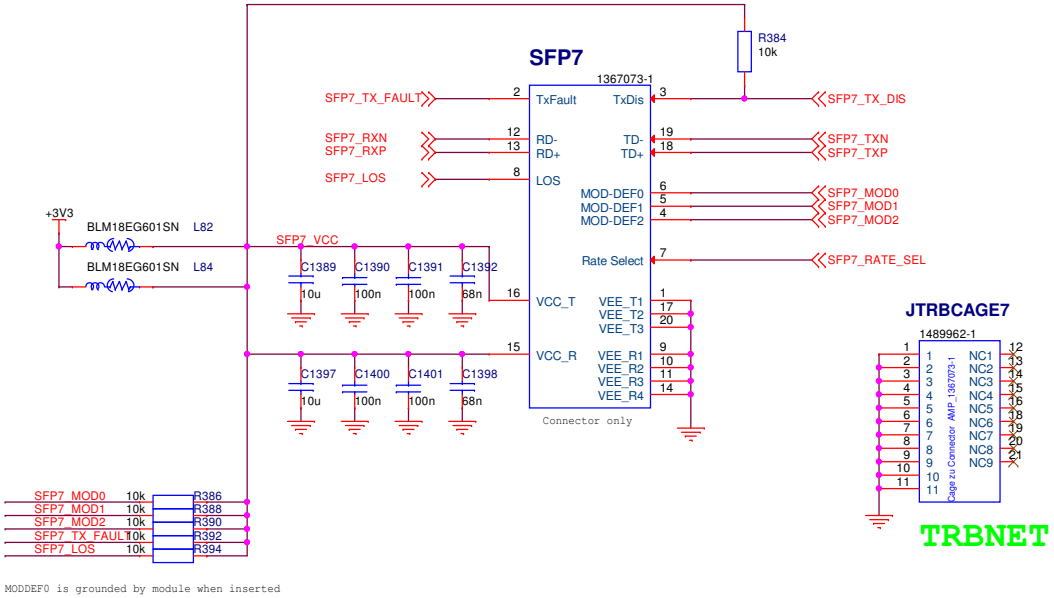
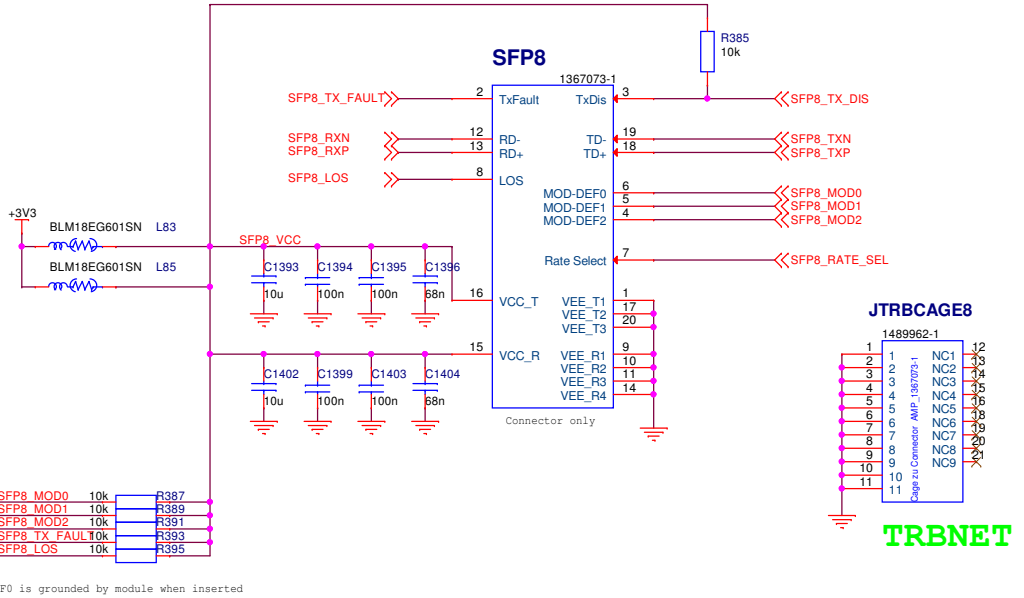
02_SFP

Design: K:\GSI\JOB\HADES\TRBV3\TRBV3.DSN
Modified: Wednesday, July 06, 2011 | Size: A3 | Page: 3 / 22
Designer: <Designer> | Layouter: <Layouter>









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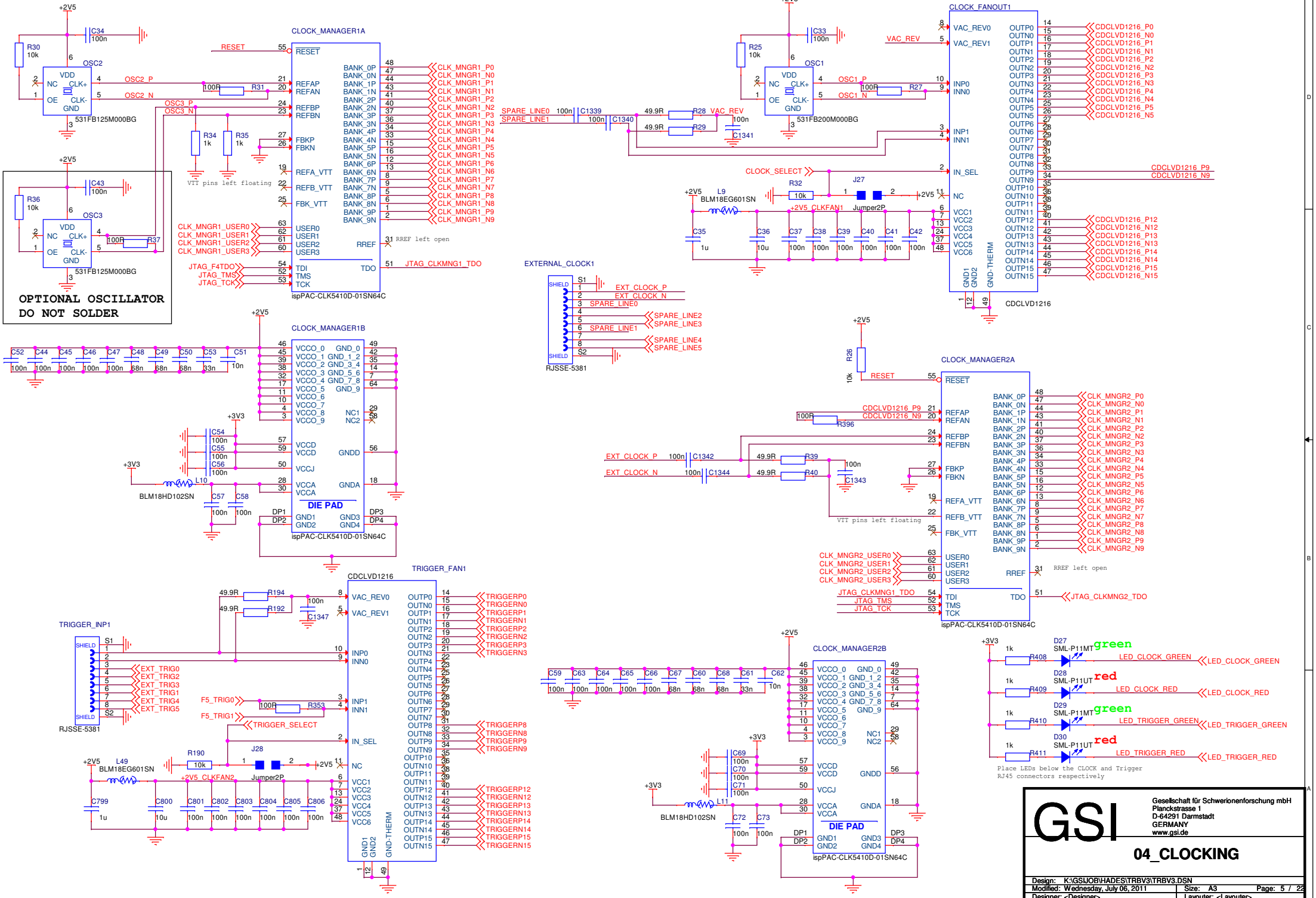
03_SFP5-8

Design: K:\GSI\JOB\HADES\TRBV3\TRBV3.DSN		
Modified: Wednesday, July 06, 2011	Size: A3	Page: 4 / 22
Designer: <Designer>	Layouter: <Layouter>	


OPTIONAL OSCILLATOR
DO NOT SOLDER
531FB125M000BG
CLOCK_MANAGER1A
ispPAC-CLK5410D-01SN64C
VTT pins left floating
RREF left open
JTAG_CLKMNG1_TDO
531FB200M000BG
CLOCK_FANOUT1
CDCLVD1216
EXTERNAL_CLOCK1
RJSSE-5381
CLOCK_MANAGER1B
DIE PAD
CLOCK_MANAGER2A
JTAG_CLKMNG2_TDO
TRIGGER_INP1
TRIGGER_FAN1
CLOCK_MANAGER2B
LED_CLOCK_GREEN
LED_CLOCK_RED
LED_TRIGGER_GREEN
LED_TRIGGER_RED
Place LEDs below the CLOCK and Trigger
RJ45 connectors respectively
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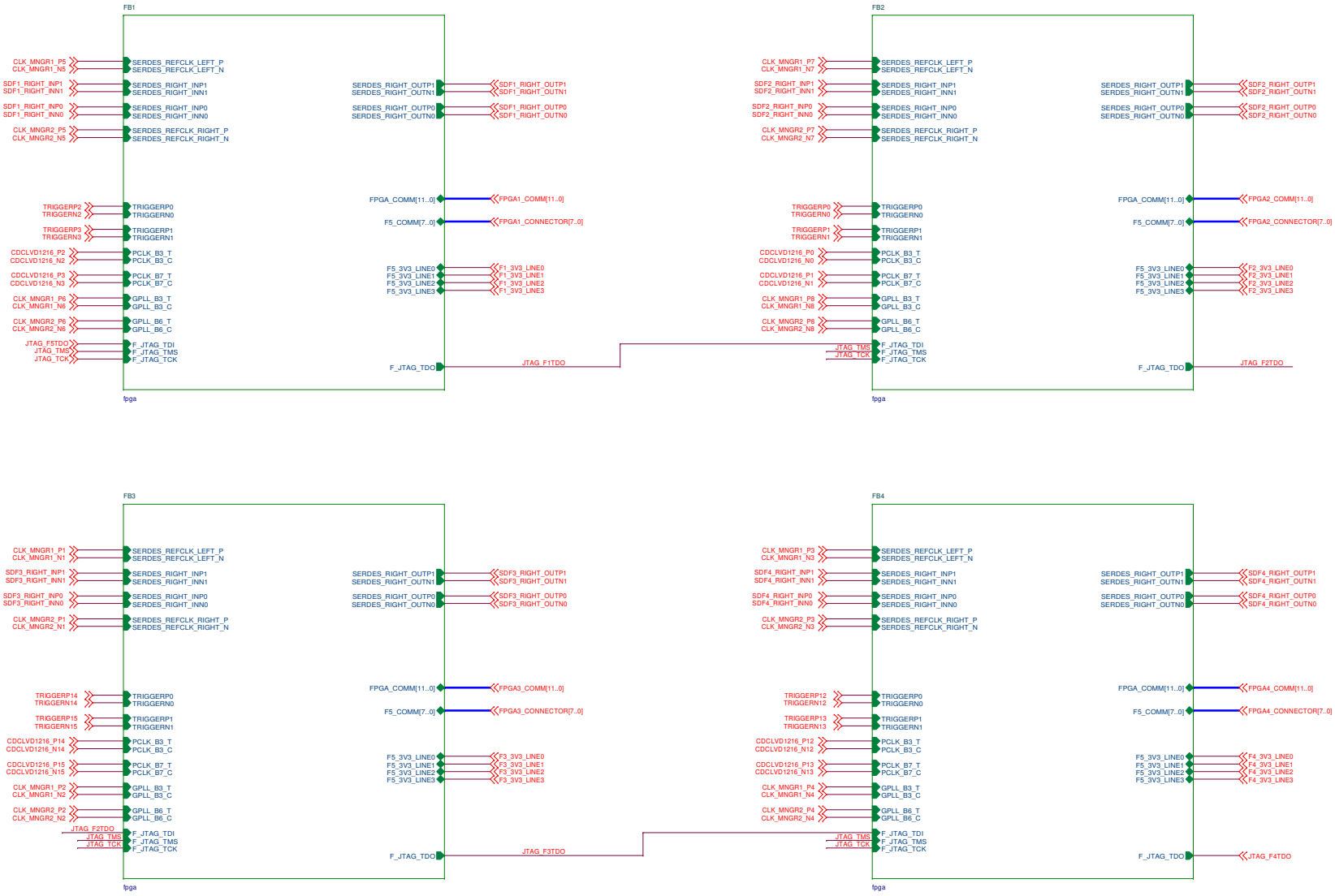
04_CLOCKING
Design: K:\GSI\JOB\HADES\TRBV3\TRBV3.DSN
Modified: Wednesday, July 06, 2011
Size: A3
Page: 5 / 22
Designer: <Designer>
Layouter: <Layouter>



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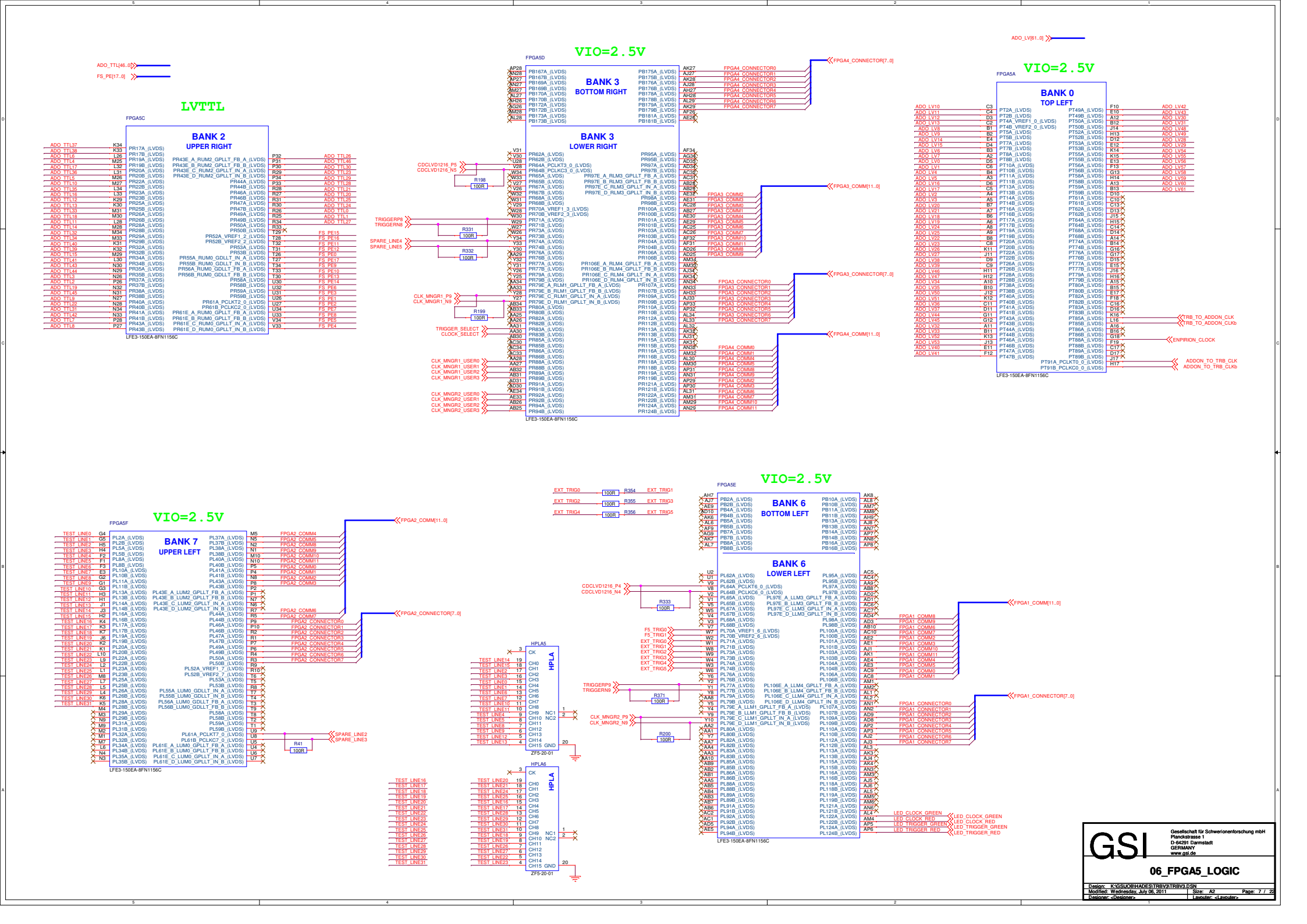
05_FPGA1-4

Design: K:\GSI\OB\HADES\TRBV3\TRBV3.DSN
Modified: Wednesday, July 06, 2011 | Size: A2 | Page: 6 / 22
Designer: <Designer> | Layouter: <Layouter>


LVTTL
VIO=2.5V
FPGA5C
BANK 2
UPPER RIGHT
FPGA5D
BANK 3
BOTTOM RIGHT
BANK 3
LOWER RIGHT
FPGA5A
BANK 0
TOP LEFT
FPGA5F
BANK 7
UPPER LEFT
FPGA5E
BANK 6
BOTTOM LEFT
BANK 6
LOWER LEFT
HPLA5
HPLA6
HPLA
ZF5-20-01
LFE3-150EA-8FN1156C
ADO_TTL[46..0]
FS_PE[17..0]
ADO_LV[61..0]
FPGA4_CONNECTOR[7..0]
FPGA3_COMM[11..0]
FPGA3_CONNECTOR[7..0]
FPGA4_COMM[11..0]
FPGA2_COMM[11..0]
FPGA2_CONNECTOR[7..0]
FPGA1_COMM[11..0]
FPGA1_CONNECTOR[7..0]
CDCLVD1216_P5
CDCLVD1216_N5
TRIGGERP8
TRIGGERN8
SPARE_LINE4
SPARE_LINE5
CLK_MNGR1_P9
CLK_MNGR1_N9
TRIGGER_SELECT
CLOCK_SELECT
CLK_MNGR1_USER0
CLK_MNGR1_USER1
CLK_MNGR1_USER2
CLK_MNGR1_USER3
CLK_MNGR2_USER0
CLK_MNGR2_USER1
CLK_MNGR2_USER2
CLK_MNGR2_USER3
EXT_TRIG0
EXT_TRIG1
EXT_TRIG2
EXT_TRIG3
EXT_TRIG4
EXT_TRIG5
CDCLVD1216_P4
CDCLVD1216_N4
TRIGGERP9
TRIGGERN9
CLK_MNGR2_P9
CLK_MNGR2_N9
TRB_TO_ADDON_CLK
TRB_TO_ADDON_CLKb
ENPIRION_CLOCK
ADDON_TO_TRB_CLK
ADDON_TO_TRB_CLKb
LED_CLOCK_GREEN
LED_CLOCK_RED
LED_TRIGGER_GREEN
LED_TRIGGER_RED
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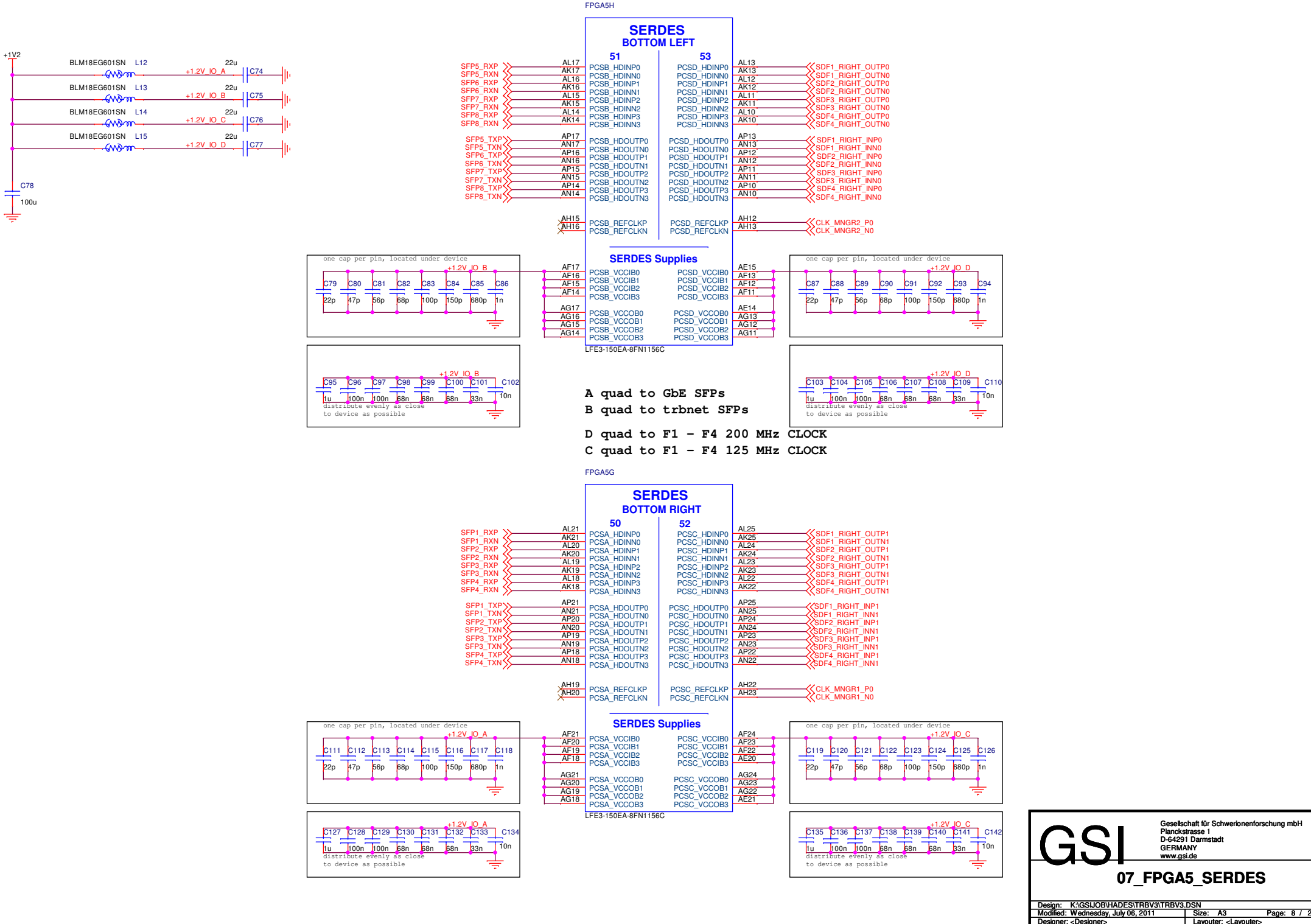
06_FPGA5_LOGIC
Design: K:\GSI\OB\HADES\TRBV3\TRBV3.DSN
Modified: Wednesday, July 06, 2011
Size: A2
Page: 7 / 22
Designer: <Designer>
Layouter: <Layouter>


+1V2
BLM18EG601SN L12
22u
+1.2V_IO_A
C74
BLM18EG601SN L13
22u
+1.2V_IO_B
C75
BLM18EG601SN L14
22u
+1.2V_IO_C
C76
BLM18EG601SN L15
22u
+1.2V_IO_D
C77
C78
100u
FPGA5H
SERDES
BOTTOM LEFT
51
53
SFP5_RXP
SFP5_RXN
SFP6_RXP
SFP6_RXN
SFP7_RXP
SFP7_RXN
SFP8_RXP
SFP8_RXN
PCSB_HDINP0
PCSB_HDINN0
PCSB_HDINP1
PCSB_HDINN1
PCSB_HDINP2
PCSB_HDINN2
PCSB_HDINP3
PCSB_HDINN3
PCSD_HDINP0
PCSD_HDINN0
PCSD_HDINP1
PCSD_HDINN1
PCSD_HDINP2
PCSD_HDINN2
PCSD_HDINP3
PCSD_HDINN3
SDF1_RIGHT_OUTP0
SDF1_RIGHT_OUTN0
SDF2_RIGHT_OUTP0
SDF2_RIGHT_OUTN0
SDF3_RIGHT_OUTP0
SDF3_RIGHT_OUTN0
SDF4_RIGHT_OUTP0
SDF4_RIGHT_OUTN0
SFP5_TXP
SFP5_TXN
SFP6_TXP
SFP6_TXN
SFP7_TXP
SFP7_TXN
SFP8_TXP
SFP8_TXN
PCSB_HDOUTP0
PCSB_HDOUTN0
PCSB_HDOUTP1
PCSB_HDOUTN1
PCSB_HDOUTP2
PCSB_HDOUTN2
PCSB_HDOUTP3
PCSB_HDOUTN3
PCSD_HDOUTP0
PCSD_HDOUTN0
PCSD_HDOUTP1
PCSD_HDOUTN1
PCSD_HDOUTP2
PCSD_HDOUTN2
PCSD_HDOUTP3
PCSD_HDOUTN3
SDF1_RIGHT_INP0
SDF1_RIGHT_INN0
SDF2_RIGHT_INP0
SDF2_RIGHT_INN0
SDF3_RIGHT_INP0
SDF3_RIGHT_INN0
SDF4_RIGHT_INP0
SDF4_RIGHT_INN0
PCSB_REFCLKP
PCSB_REFCLKN
PCSD_REFCLKP
PCSD_REFCLKN
CLK_MNGR2_P0
CLK_MNGR2_N0
SERDES Supplies
PCSB_VCCIB0
PCSB_VCCIB1
PCSB_VCCIB2
PCSB_VCCIB3
PCSB_VCCOB0
PCSB_VCCOB1
PCSB_VCCOB2
PCSB_VCCOB3
PCSD_VCCIB0
PCSD_VCCIB1
PCSD_VCCIB2
PCSD_VCCIB3
PCSD_VCCOB0
PCSD_VCCOB1
PCSD_VCCOB2
PCSD_VCCOB3
LFE3-150EA-8FN1156C
one cap per pin, located under device
+1.2V_IO_B
C79 C80 C81 C82 C83 C84 C85 C86
22p 47p 56p 68p 100p 150p 680p 1n
one cap per pin, located under device
+1.2V_IO_D
C87 C88 C89 C90 C91 C92 C93 C94
22p 47p 56p 68p 100p 150p 680p 1n
+1.2V_IO_B
C95 C96 C97 C98 C99 C100 C101 C102
1u 100n 100n 68n 68n 68n 33n 10n
distribute evenly as close
to device as possible
+1.2V_IO_D
C103 C104 C105 C106 C107 C108 C109 C110
1u 100n 100n 68n 68n 68n 33n 10n
distribute evenly as close
to device as possible
A quad to GbE SFPs
B quad to trbnet SFPs
D quad to F1 - F4 200 MHz CLOCK
C quad to F1 - F4 125 MHz CLOCK
FPGA5G
SERDES
BOTTOM RIGHT
50
52
SFP1_RXP
SFP1_RXN
SFP2_RXP
SFP2_RXN
SFP3_RXP
SFP3_RXN
SFP4_RXP
SFP4_RXN
PCSA_HDINP0
PCSA_HDINN0
PCSA_HDINP1
PCSA_HDINN1
PCSA_HDINP2
PCSA_HDINN2
PCSA_HDINP3
PCSA_HDINN3
PCSC_HDINP0
PCSC_HDINN0
PCSC_HDINP1
PCSC_HDINN1
PCSC_HDINP2
PCSC_HDINN2
PCSC_HDINP3
PCSC_HDINN3
SDF1_RIGHT_OUTP1
SDF1_RIGHT_OUTN1
SDF2_RIGHT_OUTP1
SDF2_RIGHT_OUTN1
SDF3_RIGHT_OUTP1
SDF3_RIGHT_OUTN1
SDF4_RIGHT_OUTP1
SDF4_RIGHT_OUTN1
SFP1_TXP
SFP1_TXN
SFP2_TXP
SFP2_TXN
SFP3_TXP
SFP3_TXN
SFP4_TXP
SFP4_TXN
PCSA_HDOUTP0
PCSA_HDOUTN0
PCSA_HDOUTP1
PCSA_HDOUTN1
PCSA_HDOUTP2
PCSA_HDOUTN2
PCSA_HDOUTP3
PCSA_HDOUTN3
PCSC_HDOUTP0
PCSC_HDOUTN0
PCSC_HDOUTP1
PCSC_HDOUTN1
PCSC_HDOUTP2
PCSC_HDOUTN2
PCSC_HDOUTP3
PCSC_HDOUTN3
SDF1_RIGHT_INP1
SDF1_RIGHT_INN1
SDF2_RIGHT_INP1
SDF2_RIGHT_INN1
SDF3_RIGHT_INP1
SDF3_RIGHT_INN1
SDF4_RIGHT_INP1
SDF4_RIGHT_INN1
PCSA_REFCLKP
PCSA_REFCLKN
PCSC_REFCLKP
PCSC_REFCLKN
CLK_MNGR1_P0
CLK_MNGR1_N0
SERDES Supplies
PCSA_VCCIB0
PCSA_VCCIB1
PCSA_VCCIB2
PCSA_VCCIB3
PCSA_VCCOB0
PCSA_VCCOB1
PCSA_VCCOB2
PCSA_VCCOB3
PCSC_VCCIB0
PCSC_VCCIB1
PCSC_VCCIB2
PCSC_VCCIB3
PCSC_VCCOB0
PCSC_VCCOB1
PCSC_VCCOB2
PCSC_VCCOB3
LFE3-150EA-8FN1156C
one cap per pin, located under device
+1.2V_IO_A
C111 C112 C113 C114 C115 C116 C117 C118
22p 47p 56p 68p 100p 150p 680p 1n
one cap per pin, located under device
+1.2V_IO_C
C119 C120 C121 C122 C123 C124 C125 C126
22p 47p 56p 68p 100p 150p 680p 1n
+1.2V_IO_A
C127 C128 C129 C130 C131 C132 C133 C134
1u 100n 100n 68n 68n 68n 33n 10n
distribute evenly as close
to device as possible
+1.2V_IO_C
C135 C136 C137 C138 C139 C140 C141 C142
1u 100n 100n 68n 68n 68n 33n 10n
distribute evenly as close
to device as possible
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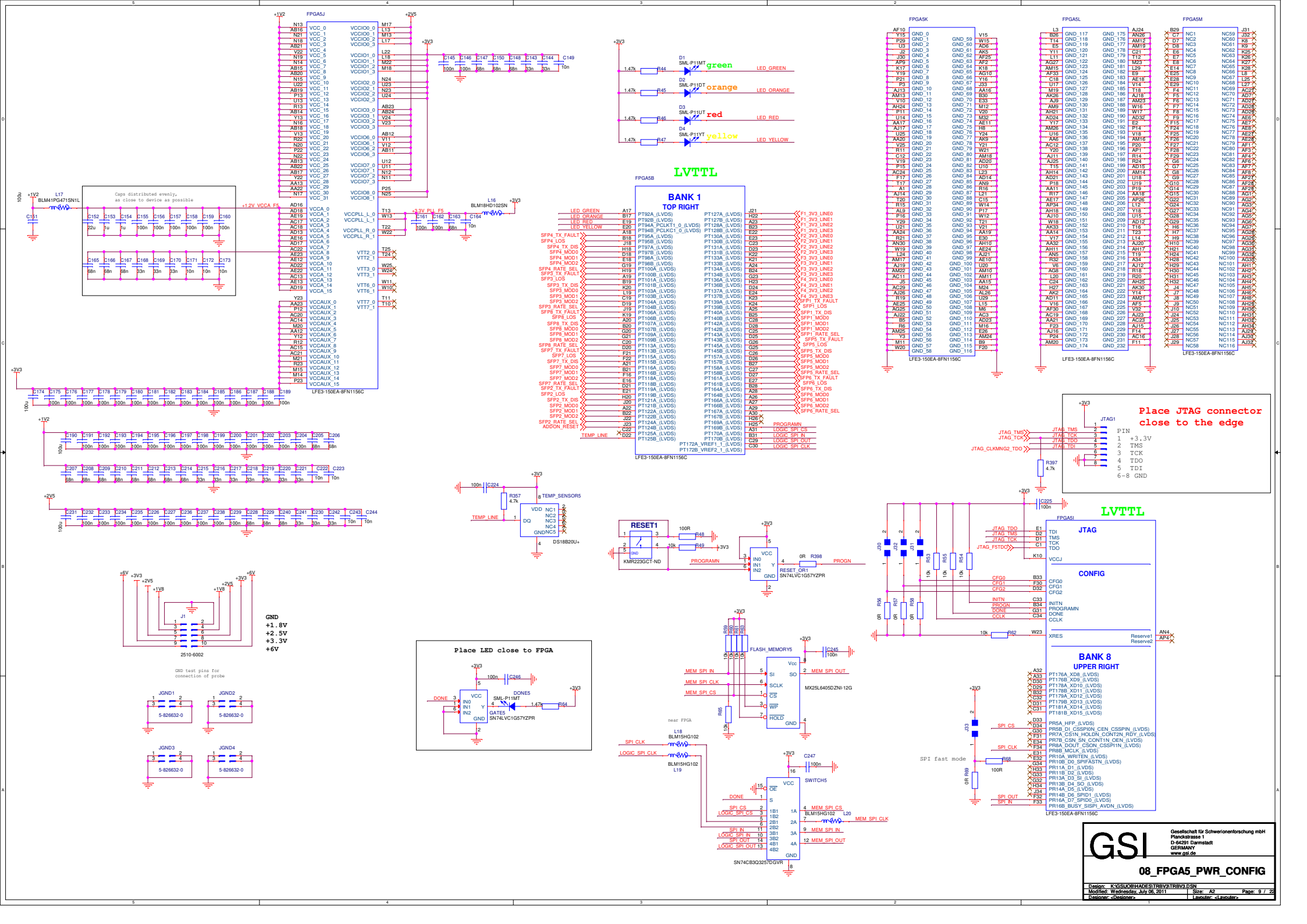
07_FPGA5_SERDES
Design: K:\GSI\JOB\HADES\TRBV3\TRBV3.DSN
Modified: Wednesday, July 06, 2011
Size: A3
Page: 8 / 22
Designer: <Designer>
Layouter: <Layouter>


FPGA5J
FPGA5K
FPGA5L
FPGA5M
FPGA5B
FPGA5I
LFE3-150EA-8FN1156C
LVTTL
BANK 1
TOP RIGHT
BANK 8
UPPER RIGHT
JTAG
CONFIG
Caps distributed evenly,
as close to device as possible
+1.2V VCCA FS
Place JTAG connector
close to the edge
JTAG1
PIN
1 +3.3V
2 TMS
3 TCK
4 TDO
5 TDI
6-8 GND
Place LED close to FPGA
RESET1
KMR223GCT-ND
SN74LVC1G57YZPR
DS18B20U+
TEMP_SENSOR5
FLASH_MEMORY5
MX25L6405DZNI-12G
SWITCH5
SN74CB3Q3257DGVR
JGND1
JGND2
JGND3
JGND4
5-826632-0
2510-6002
GND test pins for
connection of probe
GND
+1.8V
+2.5V
+3.3V
+6V
SPI fast mode
LED_GREEN
LED_ORANGE
LED_RED
LED_YELLOW
PROGRAMN
PROGN
TEMP_LINE
SPI CLK
LOGIC_SPI_CLK
MEM_SPI_IN
MEM_SPI_OUT
MEM_SPI_CS
MEM_SPI_CLK
JTAG_TMS
JTAG_TCK
JTAG_TDO
JTAG_TDI
JTAG_F5TDO
JTAG_CLKMNG2_TDO
CFG0
CFG1
CFG2
INITN
PROGRAMN
DONE
CCLK
XRES
Reserve1
Reserve2
SPI CS
SPI CLK
SPI OUT
SPI IN
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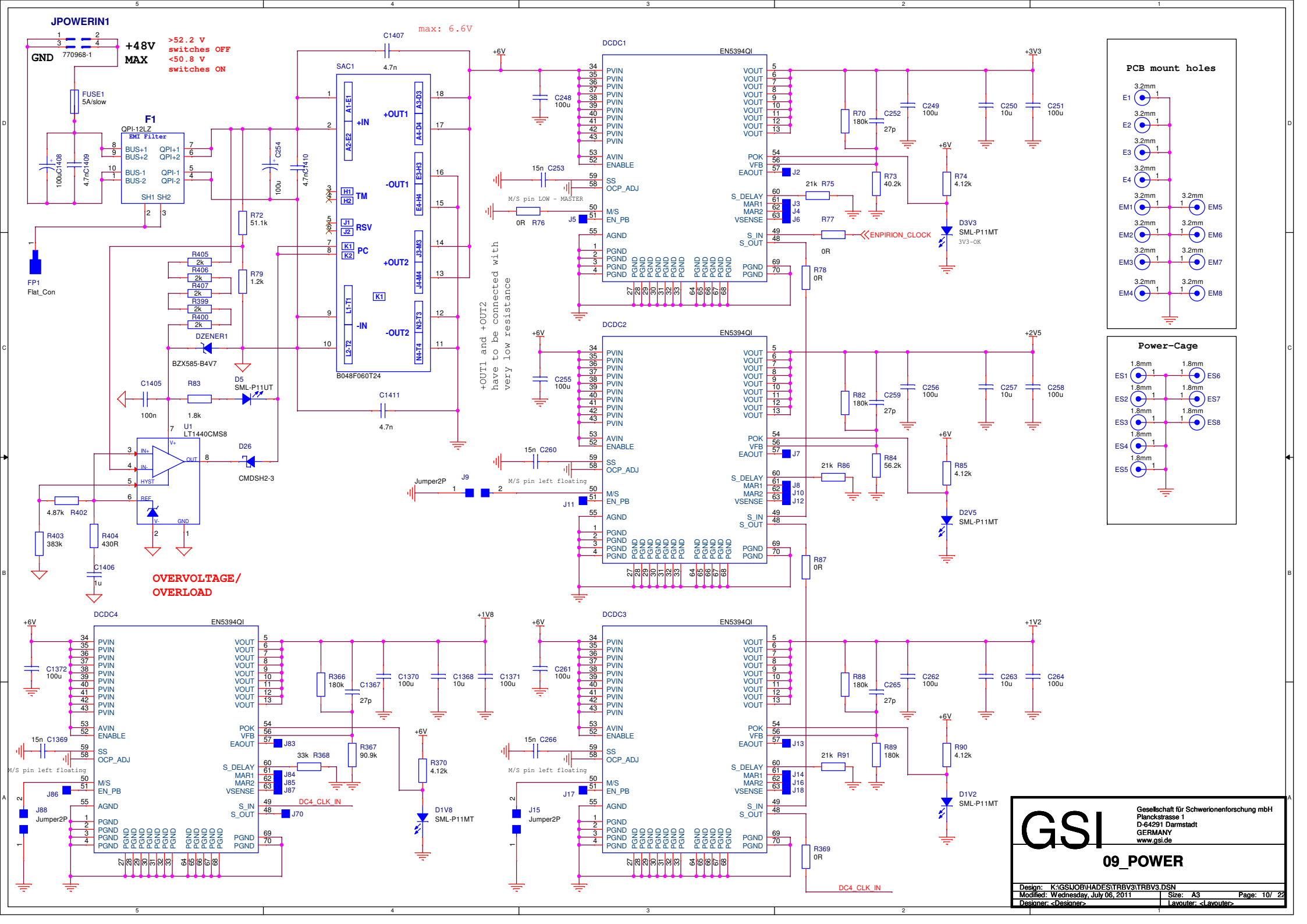
08_FPGA5_PWR_CONFIG
Design: K:\GSI\OB\HADES\TRBV3\TRBV3.DSN
Modified: Wednesday, July 06, 2011
Size: A2
Page: 9 / 22
Designer: <Designer>
Layouter: <Layouter>


JPOWERIN1
GND
770968-1
+48V
MAX
>52.2 V
switches OFF
<50.8 V
switches ON
FUSE1
5A/slow
F1
QPI-12LZ
EMI Filter
SH1 SH2
FP1
Flat_Con
max: 6.6V
C1407
4.7n
SAC1
+IN
-IN
+OUT1
-OUT1
+OUT2
-OUT2
TM
RSV
PC
B048F060T24
R72
51.1k
R79
1.2k
R405
R406
R407
R399
R400
2k
DZENER1
BZX585-B4V7
C1405
100n
R83
1.8k
D5
SML-P11UT
U1
LT1440CMS8
D26
CMDSH2-3
4.87k R402
R403
383k
R404
430R
C1406
1u
C1411
4.7n
OVERVOLTAGE/
OVERLOAD
+OUT1 and +OUT2
have to be connected with
very low resistance
DCDC1
DCDC2
DCDC3
DCDC4
EN5394QI
+6V
C248
100u
15n C253
M/S pin LOW - MASTER
0R R76
J5
21k R75
R77
0R
ENPIRION_CLOCK
R70
180k
C252
27p
C249
100u
C250
10u
C251
100u
+3V3
R73
40.2k
R74
4.12k
D3V3
SML-P11MT
3V3-OK
R78
0R
C255
100u
15n C260
M/S pin left floating
Jumper2P
J9
J11
R82
180k
C259
27p
C256
100u
C257
10u
C258
100u
+2V5
R84
56.2k
R85
4.12k
D2V5
SML-P11MT
R87
0R
C261
100u
15n C266
M/S pin left floating
J17
J15
Jumper2P
R88
180k
C265
27p
C262
100u
C263
10u
C264
100u
+1V2
R89
180k
R90
4.12k
D1V2
SML-P11MT
R369
0R
C1372
100u
15n C1369
M/S pin left floating
J86
J88
Jumper2P
R366
180k
C1367
27p
C1370
100u
C1368
10u
C1371
100u
+1V8
R367
90.9k
33k R368
R370
4.12k
D1V8
SML-P11MT
DC4_CLK_IN
J70
PCB mount holes
Power-Cage
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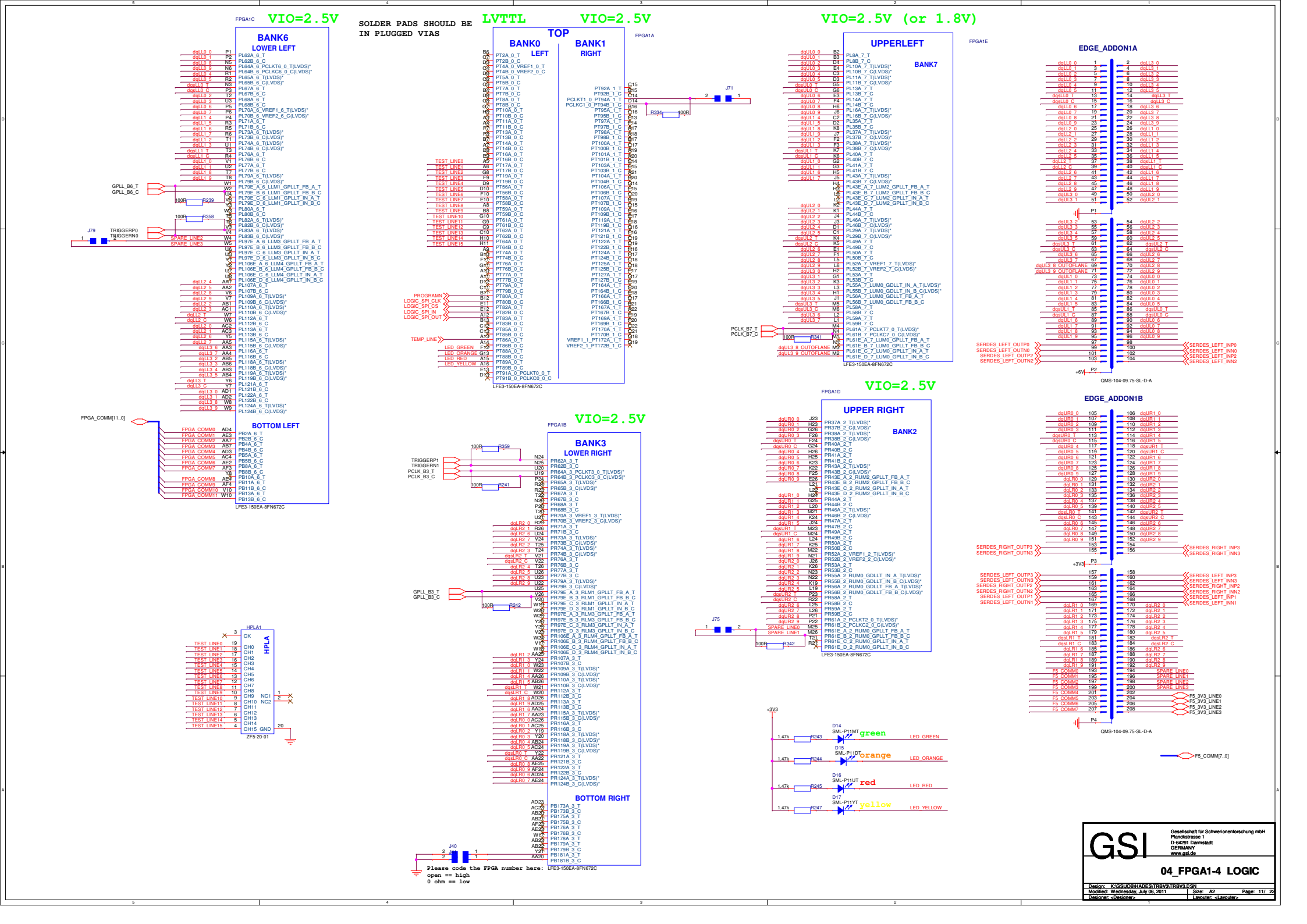
09_POWER
Design: K:\GSI\JOB\HADES\TRBV3\TRBV3.DSN
Modified: Wednesday, July 06, 2011
Size: A3
Page: 10/ 22
Designer: <Designer>
Layouter: <Layouter>


FPGA1C
VIO=2.5V
BANK6
LOWER LEFT
BOTTOM LEFT
LFE3-150EA-8FN672C
SOLDER PADS SHOULD BE
IN PLUGGED VIAS
LVTTL
VIO=2.5V
TOP
BANK0
LEFT
BANK1
RIGHT
FPGA1A
LFE3-150EA-8FN672C
VIO=2.5V (or 1.8V)
UPPERLEFT
BANK7
FPGA1E
LFE3-150EA-8FN672C
EDGE_ADDON1A
QMS-104-09.75-SL-D-A
VIO=2.5V
FPGA1D
UPPER RIGHT
BANK2
LFE3-150EA-8FN672C
EDGE_ADDON1B
QMS-104-09.75-SL-D-A
VIO=2.5V
FPGA1B
BANK3
LOWER RIGHT
BOTTOM RIGHT
LFE3-150EA-8FN672C
HPLA1
HPLA
ZF5-20-01
Please code the FPGA number here:
open == high
0 ohm == low
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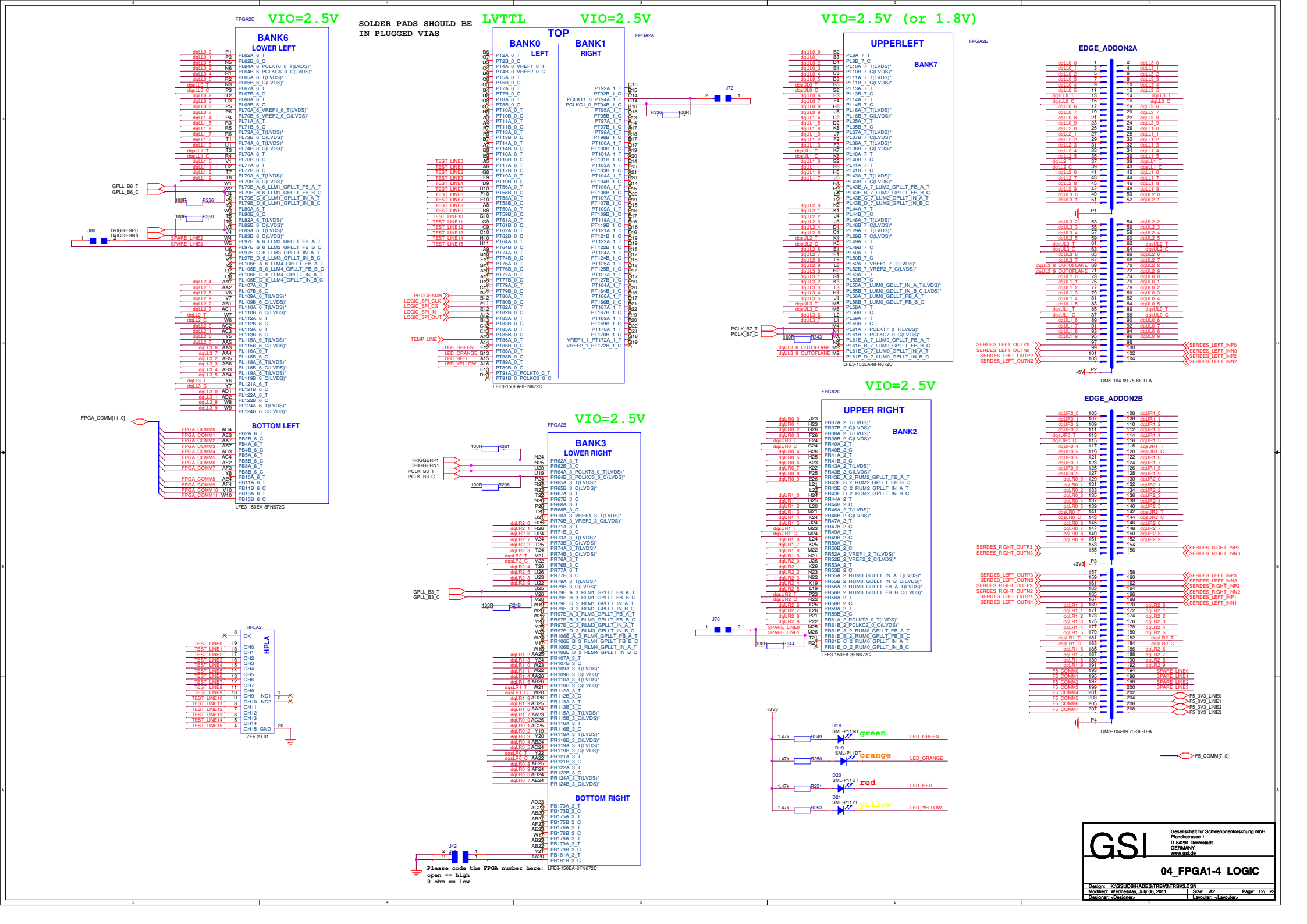
04_FPGA1-4 LOGIC
Design: K:\GSI\JOB\HADES\TRBV3\TRBV3.DSN
Modified: Wednesday, July 06, 2011
Size: A2
Page: 11/ 22
Designer: <Designer>
Layouter: <Layouter>


FPGA2C
VIO=2.5V
BANK6
LOWER LEFT
BOTTOM LEFT
LFE3-150EA-8FN672C
SOLDER PADS SHOULD BE
IN PLUGGED VIAS
LVTTL
VIO=2.5V
TOP
BANK0
LEFT
BANK1
RIGHT
FPGA2A
LFE3-150EA-8FN672C
VIO=2.5V (or 1.8V)
UPPERLEFT
BANK7
FPGA2E
LFE3-150EA-8FN672C
EDGE_ADDON2A
QMS-104-09.75-SL-D-A
VIO=2.5V
FPGA2D
UPPER RIGHT
BANK2
LFE3-150EA-8FN672C
EDGE_ADDON2B
QMS-104-09.75-SL-D-A
VIO=2.5V
FPGA2B
BANK3
LOWER RIGHT
BOTTOM RIGHT
LFE3-150EA-8FN672C
HPLA2
HPLA
ZF5-20-01
Please code the FPGA number here:
open == high
0 ohm == low
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04_FPGA1-4 LOGIC
Design: K:\GSI\JOB\HADES\TRBV3\TRBV3.DSN
Modified: Wednesday, July 06, 2011
Size: A2
Page: 12/ 22
Designer: <Designer>
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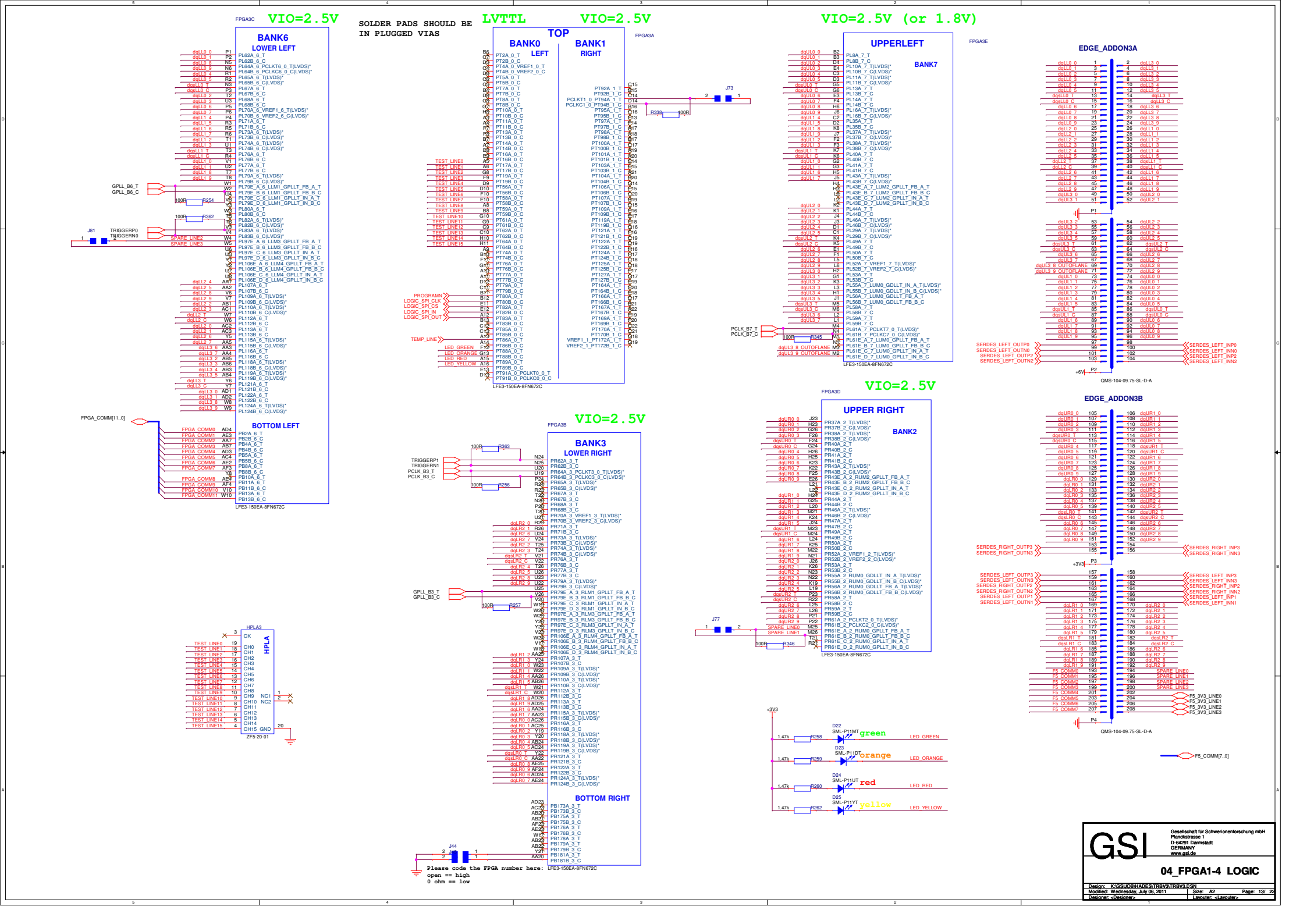
FPGA3C
VIO=2.5V
BANK6
LOWER LEFT
BOTTOM LEFT
LFE3-150EA-8FN672C
SOLDER PADS SHOULD BE
IN PLUGGED VIAS
LVTTL
VIO=2.5V
TOP
BANK0
LEFT
BANK1
RIGHT
FPGA3A
LFE3-150EA-8FN672C
VIO=2.5V (or 1.8V)
UPPERLEFT
BANK7
FPGA3E
LFE3-150EA-8FN672C
EDGE_ADDON3A
QMS-104-09.75-SL-D-A
VIO=2.5V
FPGA3D
UPPER RIGHT
BANK2
LFE3-150EA-8FN672C
EDGE_ADDON3B
QMS-104-09.75-SL-D-A
VIO=2.5V
FPGA3B
BANK3
LOWER RIGHT
BOTTOM RIGHT
LFE3-150EA-8FN672C
HPLA3
HPLA
ZF5-20-01
Please code the FPGA number here:
open == high
0 ohm == low
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04_FPGA1-4 LOGIC
Design: K:\GSI\JOB\HADES\TRBV3\TRBV3.DSN
Modified: Wednesday, July 06, 2011
Size: A2
Page: 13/ 22
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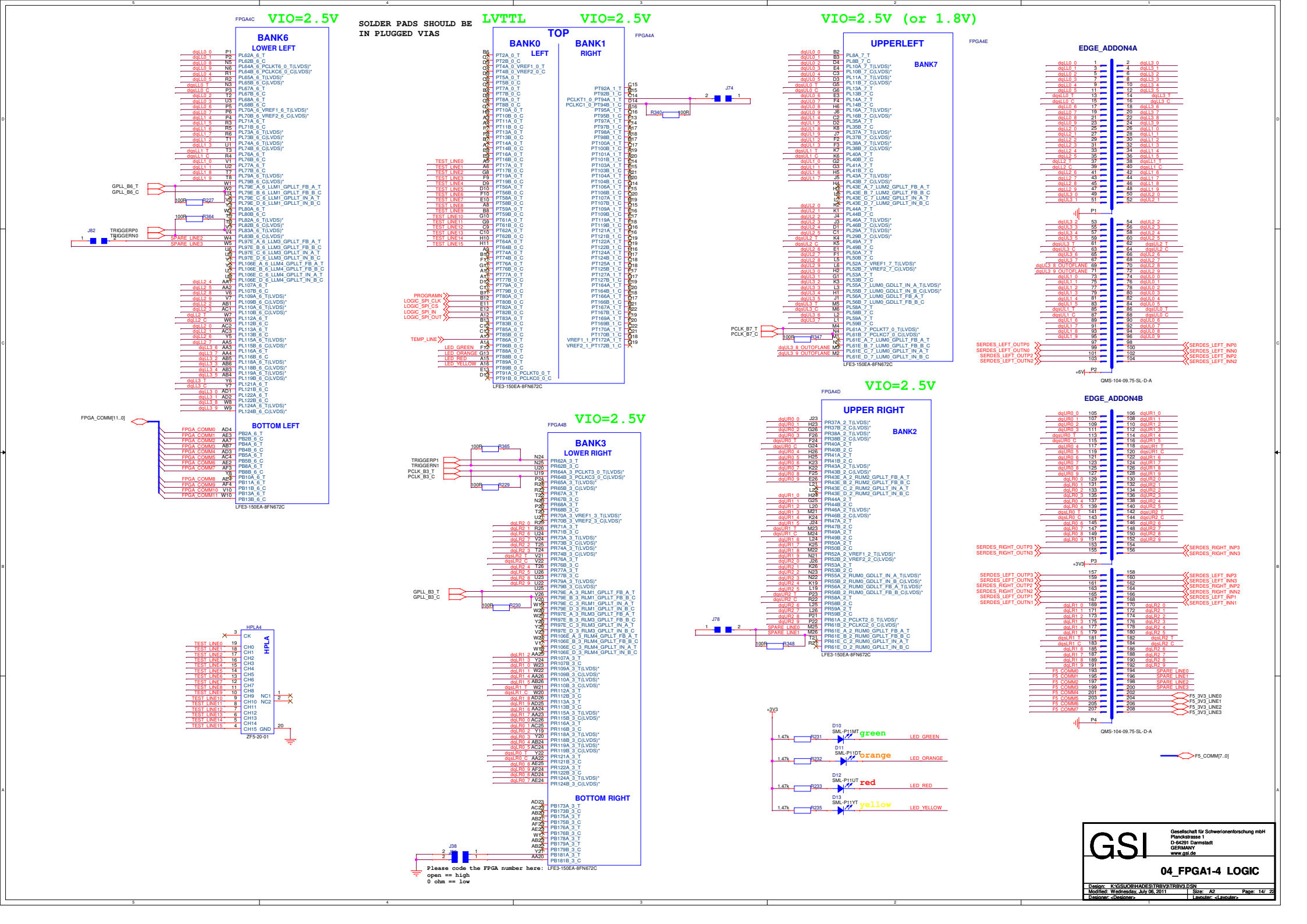
FPGA4C
VIO=2.5V
BANK6
LOWER LEFT
BOTTOM LEFT
LFE3-150EA-8FN672C
SOLDER PADS SHOULD BE
IN PLUGGED VIAS
LVTTL
VIO=2.5V
TOP
BANK0
LEFT
BANK1
RIGHT
FPGA4A
LFE3-150EA-8FN672C
VIO=2.5V (or 1.8V)
UPPERLEFT
BANK7
FPGA4E
LFE3-150EA-8FN672C
EDGE_ADDON4A
QMS-104-09.75-SL-D-A
VIO=2.5V
FPGA4D
UPPER RIGHT
BANK2
LFE3-150EA-8FN672C
EDGE_ADDON4B
QMS-104-09.75-SL-D-A
VIO=2.5V
FPGA4B
BANK3
LOWER RIGHT
BOTTOM RIGHT
LFE3-150EA-8FN672C
HPLA4
HPLA
ZF5-20-01
Please code the FPGA number here:
open == high
0 ohm == low
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04_FPGA1-4 LOGIC
Design: K:\GSI\JOB\HADES\TRBV3\TRBV3.DSN
Modified: Wednesday, July 06, 2011
Size: A2
Page: 14/ 22
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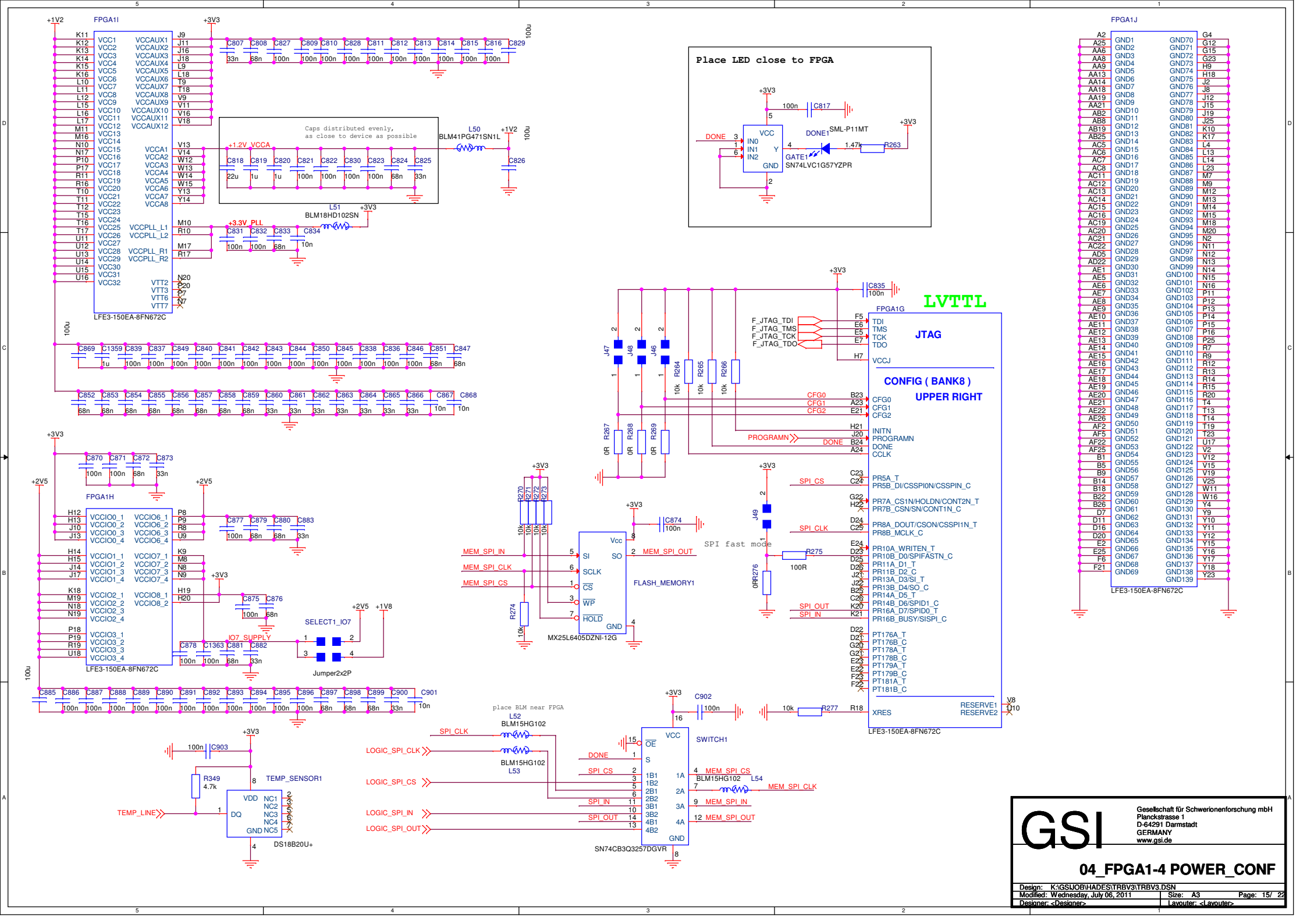
FPGA1I
LFE3-150EA-8FN672C
Caps distributed evenly, as close to device as possible
+1.2V_VCCA
+3.3V_PLL
L50 BLM41PG471SN1L
L51 BLM18HD102SN
Place LED close to FPGA
SML-P11MT
SN74LVC1G57YZPR
FPGA1J
LFE3-150EA-8FN672C
FPGA1G
LVTTL
JTAG
CONFIG (BANK8)
UPPER RIGHT
F_JTAG_TDI
F_JTAG_TMS
F_JTAG_TCK
F_JTAG_TDO
CFG0
CFG1
CFG2
PROGRAMN
DONE
CCLK
INITN
SPI_CS
SPI_CLK
SPI_OUT
SPI_IN
PR5A_T
PR5B_DI/CSSPI0N/CSSPIN_C
PR7A_CS1N/HOLDN/CONT2N_T
PR7B_CSN/SN/CONT1N_C
PR8A_DOUT/CSON/CSSPI1N_T
PR8B_MCLK_C
PR10A_WRITEN_T
PR10B_D0/SPIFASTN_C
PR11A_D1_T
PR11B_D2_C
PR13A_D3/SI_T
PR13B_D4/SO_C
PR14A_D5_T
PR14B_D6/SPID1_C
PR16A_D7/SPID0_T
PR16B_BUSY/SISPI_C
PT176A_T
PT176B_C
PT178A_T
PT178B_C
PT179A_T
PT179B_C
PT181A_T
PT181B_C
RESERVE1
RESERVE2
XRES
SPI fast mode
FPGA1H
IO7_SUPPLY
SELECT1_IO7
Jumper2x2P
MX25L6405DZNI-12G
FLASH_MEMORY1
MEM_SPI_IN
MEM_SPI_CLK
MEM_SPI_CS
MEM_SPI_OUT
TEMP_SENSOR1
TEMP_LINE
DS18B20U+
place BLM near FPGA
L52 BLM15HG102
L53 BLM15HG102
L54 BLM15HG102
LOGIC_SPI_CLK
LOGIC_SPI_CS
LOGIC_SPI_IN
LOGIC_SPI_OUT
SWITCH1
SN74CB3Q3257DGVR
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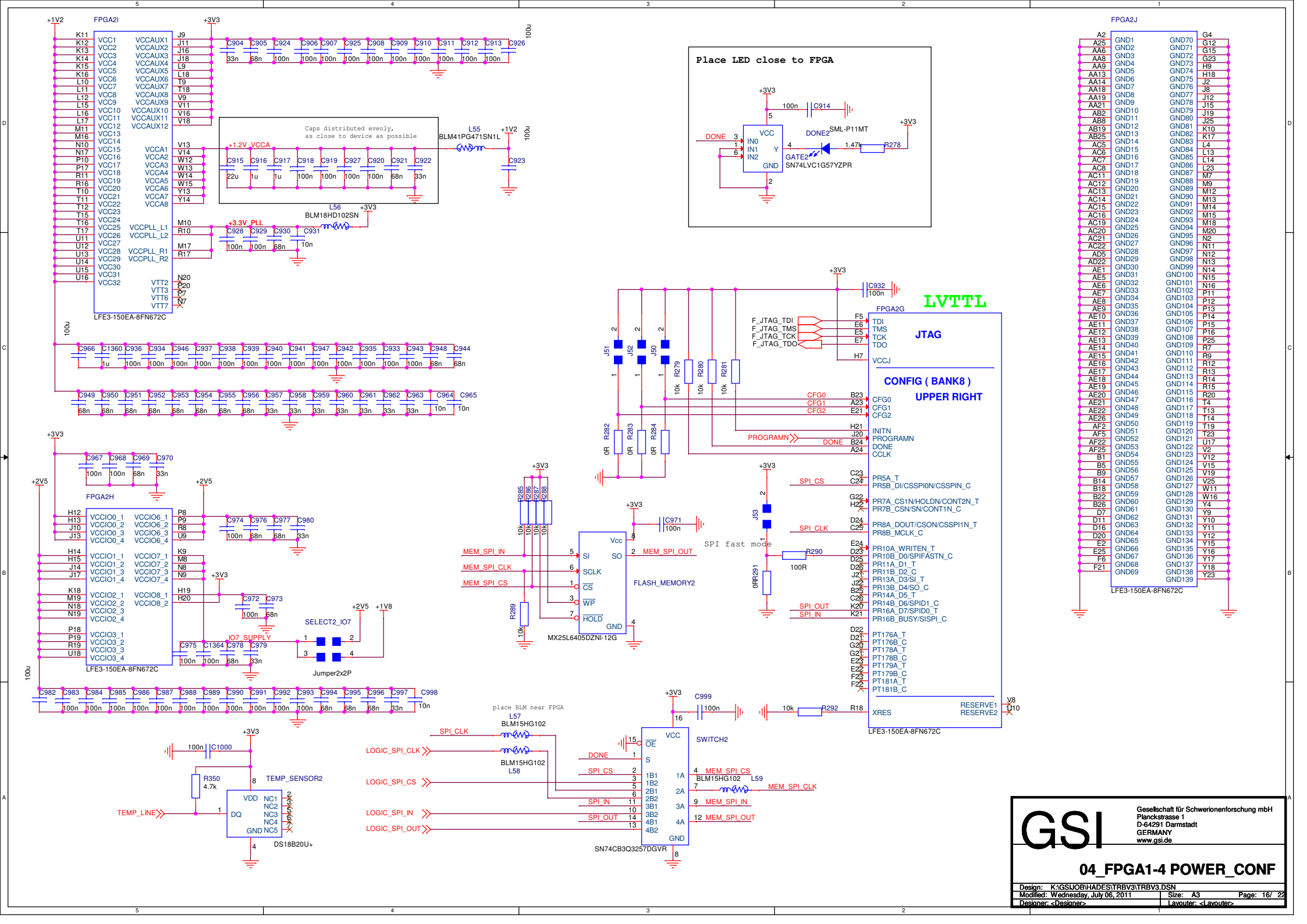
04_FPGA1-4 POWER_CONF
Design: K:\GSI\JOB\HADES\TRBV3\TRBV3.DSN
Modified: Wednesday, July 06, 2011
Size: A3
Page: 15/ 22
Designer: <Designer>
Layouter: <Layouter>


FPGA2I
LFE3-150EA-8FN672C
Caps distributed evenly, as close to device as possible
+1.2V_VCCA
+3.3V_PLL
L55 BLM41PG471SN1L
L56 BLM18HD102SN
Place LED close to FPGA
SML-P11MT
SN74LVC1G57YZPR
FPGA2J
FPGA2G
LVTTL
JTAG
CONFIG (BANK8)
UPPER RIGHT
F_JTAG_TDI
F_JTAG_TMS
F_JTAG_TCK
F_JTAG_TDO
CFG0
CFG1
CFG2
PROGRAMN
DONE
CCLK
INITN
SPI_CS
SPI_CLK
SPI_OUT
SPI_IN
SPI fast mode
FPGA2H
IO7_SUPPLY
SELECT2_IO7
Jumper2x2P
MEM_SPI_IN
MEM_SPI_CLK
MEM_SPI_CS
MEM_SPI_OUT
FLASH_MEMORY2
MX25L6405DZNI-12G
TEMP_SENSOR2
TEMP_LINE
DS18B20U+
LOGIC_SPI_CLK
LOGIC_SPI_CS
LOGIC_SPI_IN
LOGIC_SPI_OUT
SWITCH2
SN74CB3Q3257DGVR
place BLM near FPGA
XRES
RESERVE1
RESERVE2
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04_FPGA1-4 POWER_CONF
Design: K:\GSI\JOB\HADES\TRBV3\TRBV3.DSN
Modified: Wednesday, July 06, 2011
Size: A3
Page: 16/ 22
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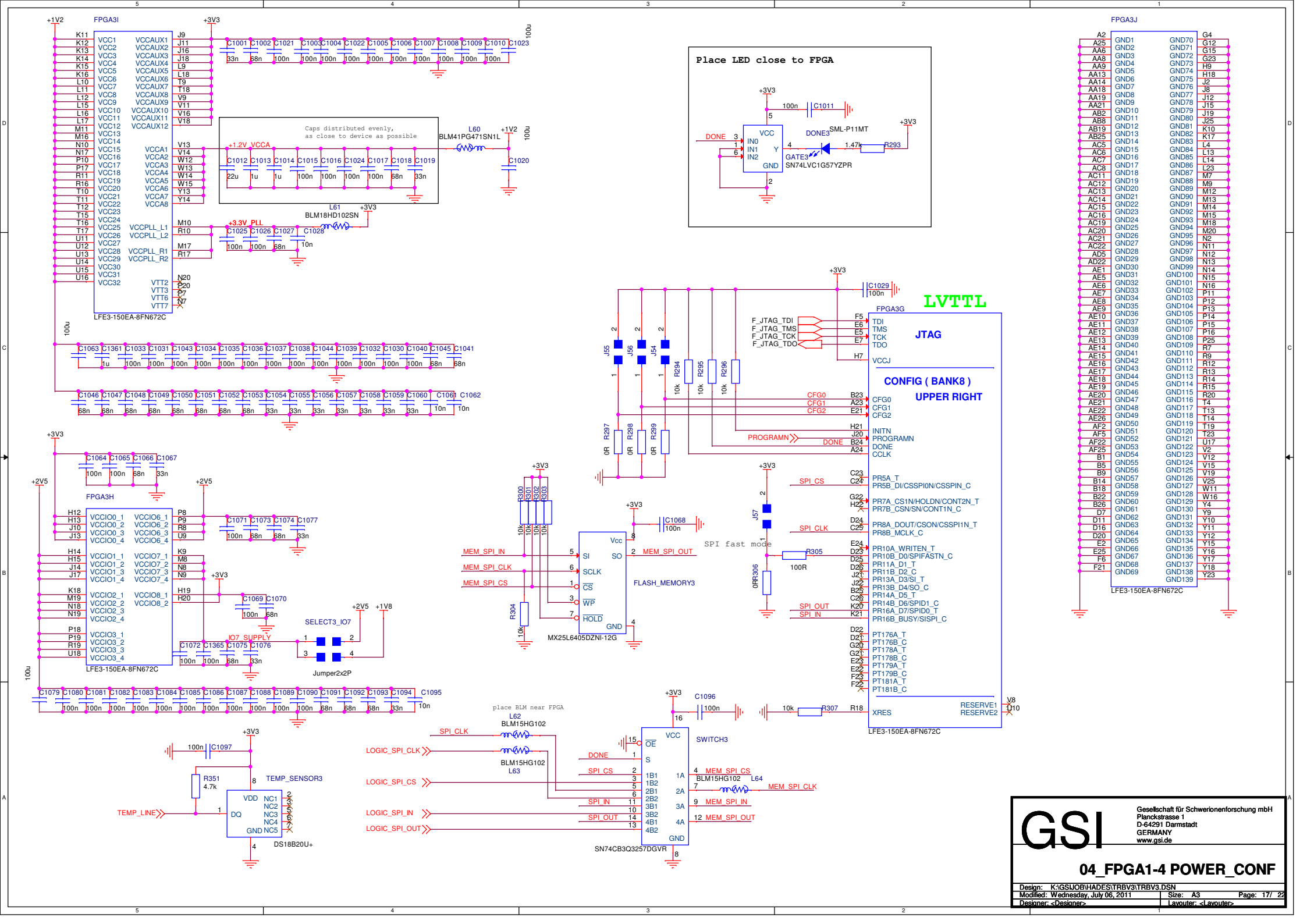

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04_FPGA1-4 POWER_CONF

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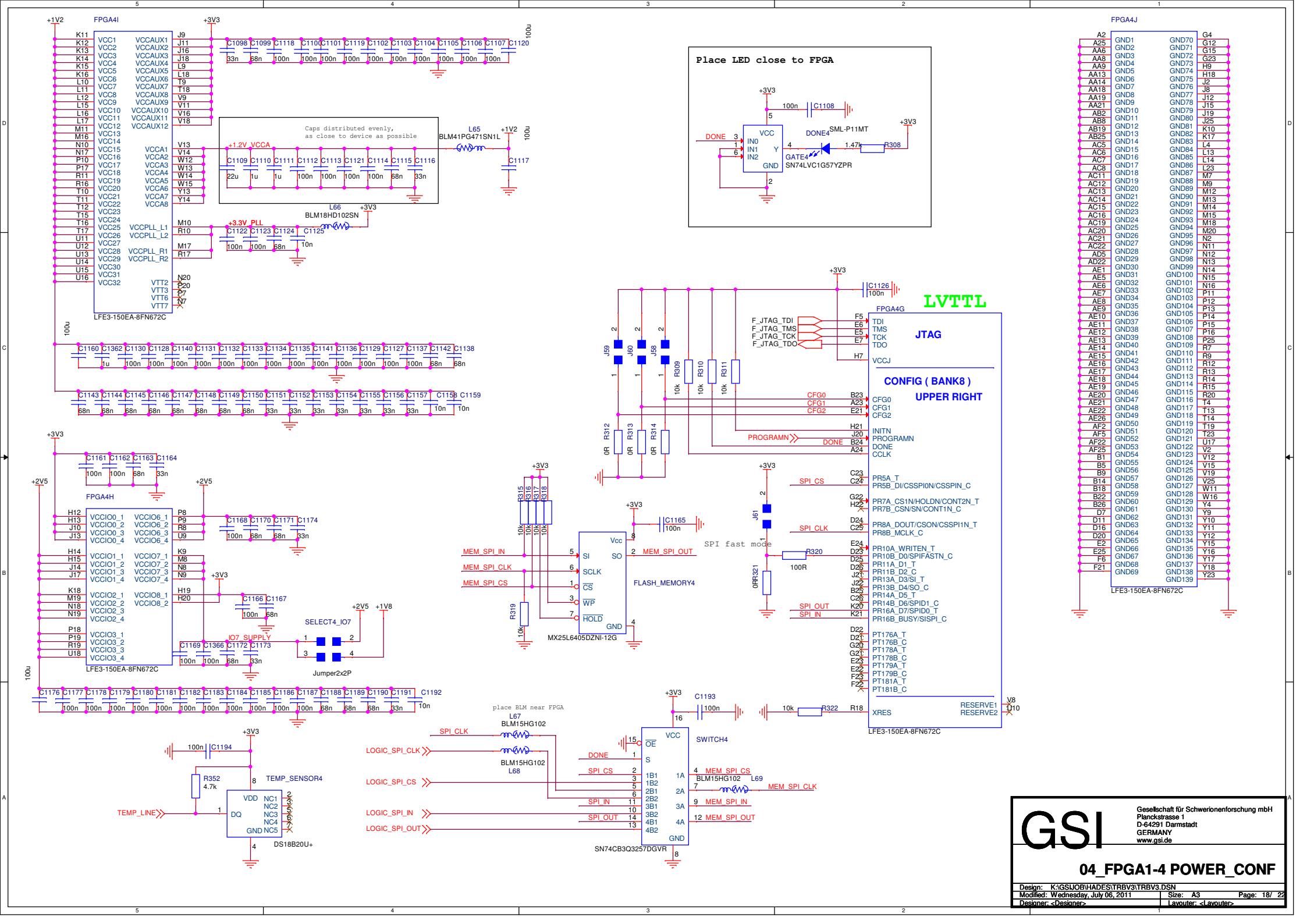
Modified: Wednesday, July 06, 2011	Size: A3	Page: 17/ 22
Designer: <Designer>	Layouter: <Layouter>	



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04_FPGA1-4 POWER_CONF

Design: K:\GSI\JOB\HADES\TRBV3\TRBV3.DSN			
Modified: Wednesday, July 06, 2011	Size: A3	Page: 18/ 22	
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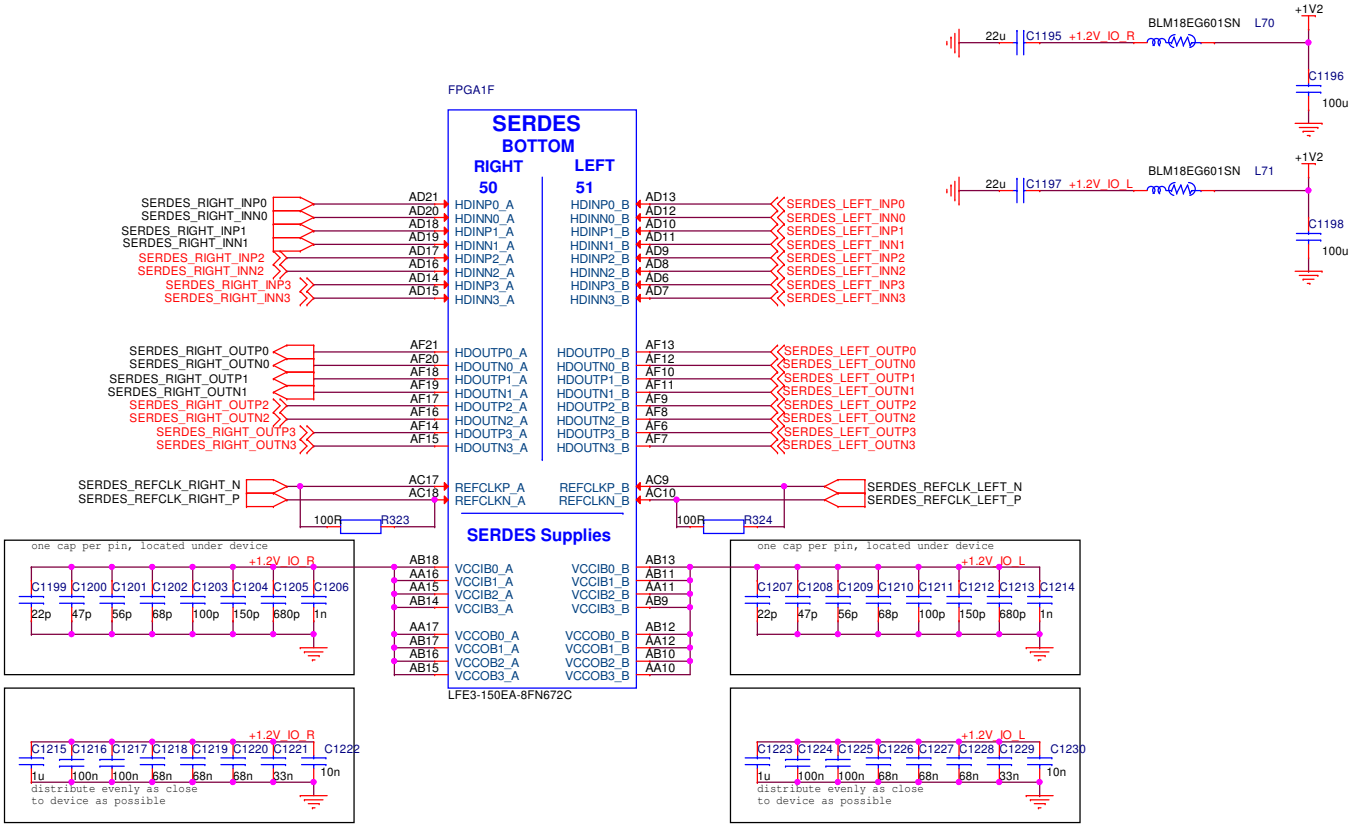

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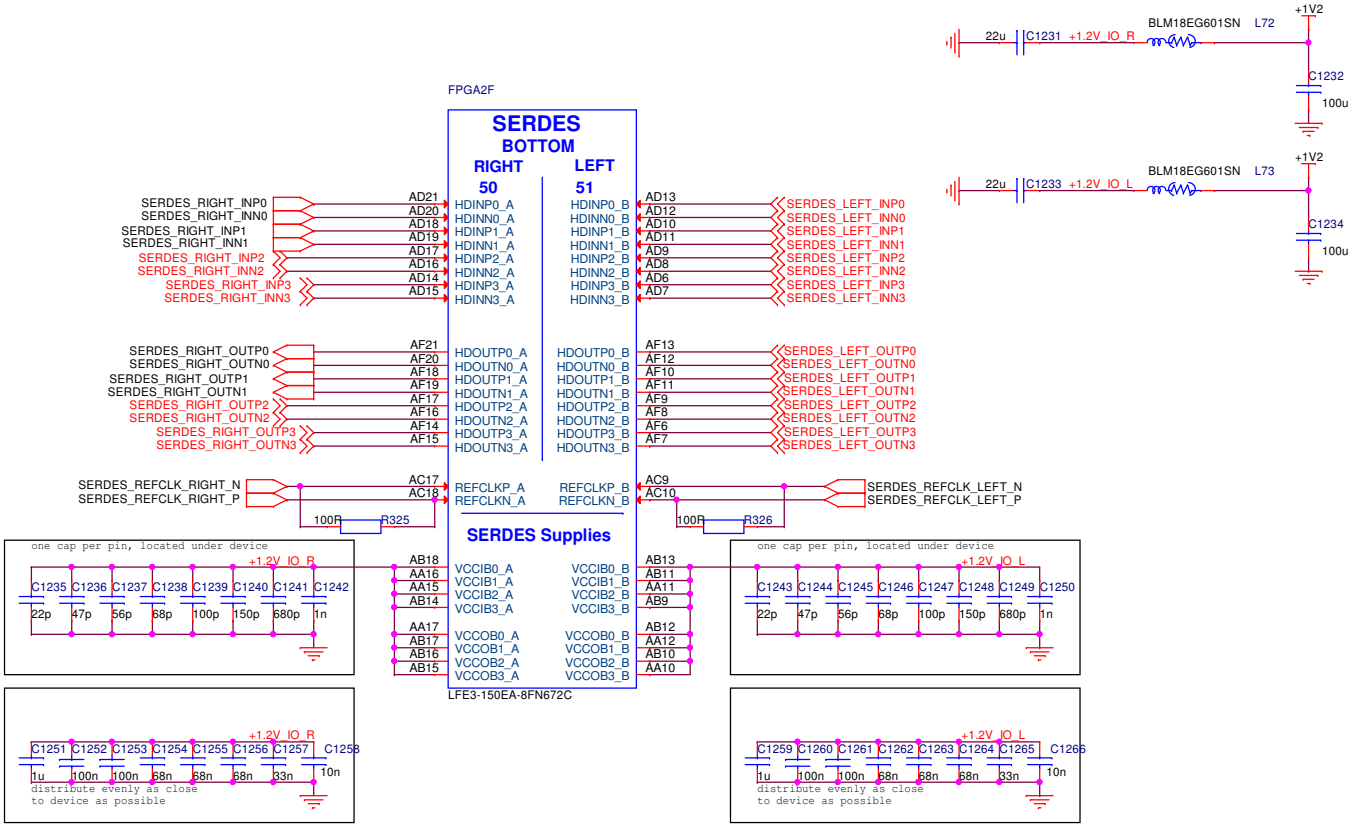
04_FPGA1-4 SERDES

Design: K:\GSI\JOB\HADES\TRBV3\TRBV3.DSN		
Modified: Wednesday, July 06, 2011	Size: A3	Page: 19/ 22
Designer: <Designer>	Layouter: <Layouter>	



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04_FPGA1-4 SERDES

Design: K:\GSI\JOB\HADES\TRBV3\TRBV3.DSN		
Modified: Wednesday, July 06, 2011	Size: A3	Page: 20/ 22
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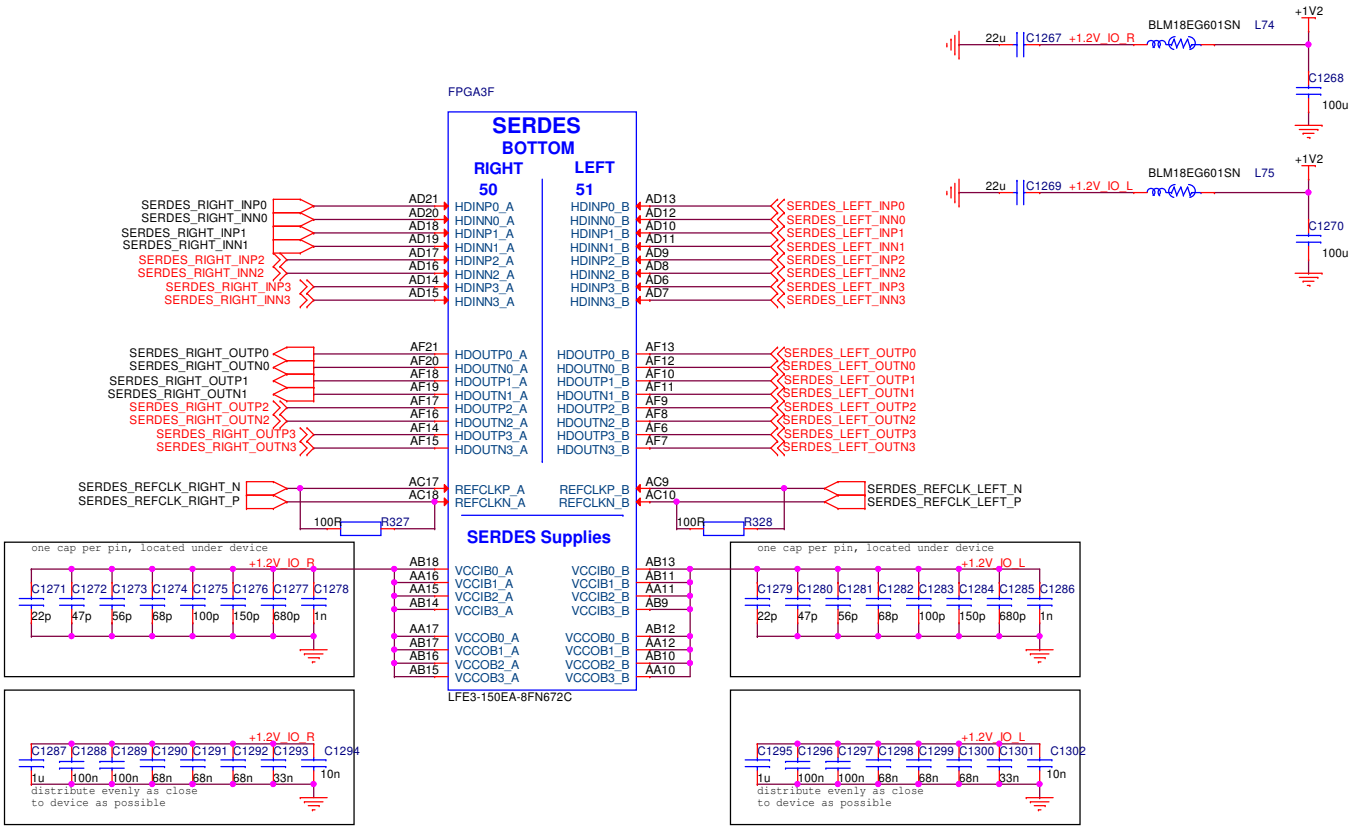

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Design: K:\GSI\JOB\HADES\TRBV3\TRBV3.DSN		
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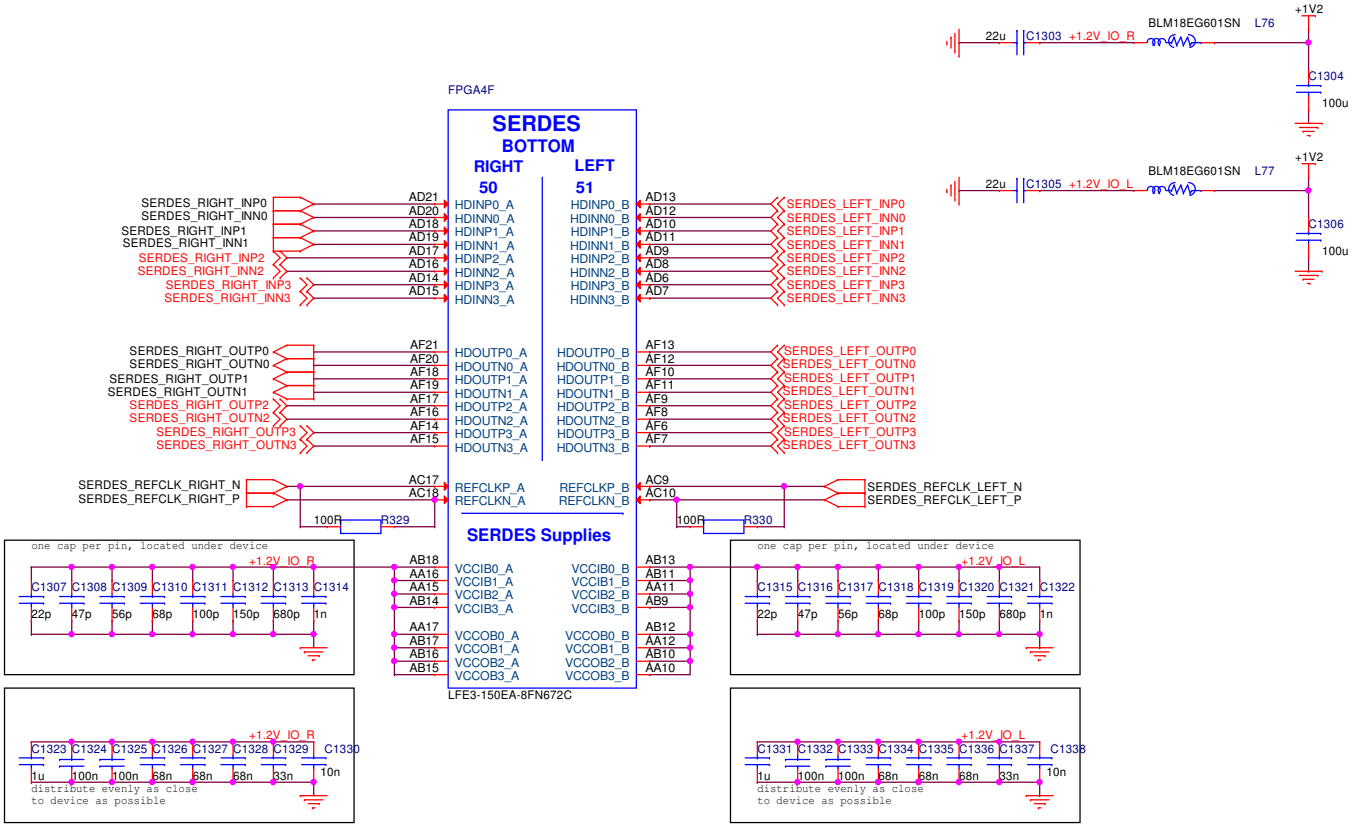

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04_FPGA1-4 SERDES

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Designer: <Designer>	Layouter: <Layouter>	