Field Programmable Gate Array Based Data Digitisation with Commercial Elements

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Outline

- Motivation
- Time digitisation in FPGAs
- Signal discrimination using FPGAs
- Amplitude digitisation with FPGAs
- Charge digitisation with FPGAs
- Summary
Motivation & Idea

• Use commercial off the shelf FPGAs as FEE
  - Easily available, industrial quality design, package and documentation
  - Upgrade included (new silicon on the roadmap of the vendor)
  - Vendor independent

• How to achieve that goal?
  - We “misuse” digital FPGAs in the asynchronous and analogue domain for:
    - Precise Time to Digital Conversion (TDC)
    - Deploying **COmplex, com**MErcial FPGAs as discriminators, DACs, ADC and QDC only adding a minimal number of external components

• The design: **Keep It Small & Simple: Come & Kiss**
Precise TDCs in FPGAs

- TDC time resolution down to 3.6 ps RMS (between two channels) using the wave union method [Jinyuan Wu] are possible
  - No cut on tails!
- Tradeoff for number of channels, time resolution and dead time can be adjusted to the needs of the application
  - 64 channels in a FPGA
  - ~10 ps RMS time resolution
- TDCs in FPGAs work much better than expected (e.g. LVDS receivers): Let’s use them for more applications!

Published IEEE 2011, E.Bayer et al.
Time Digitisation in FPGA using TDCs implemented in FPGAs

- TRB3 with 4 FPGA-TDCs with a total of 256+4 channels
- ~20 ps time resolution
- 50 MHz max. hit rate
- 300 KHz max. data readout trigger rate
- TrbNetwork for internal communication: See talk of Jan Michel
- Direct GbE connection for data and slow control; no CPU on board, all implemented in FPGA
- Usable for large system as well as stand alone system: just 48V and GbE are needed to take data
- Can be used as a pure digital board, for example as a data/trigger hub
- Applications: The time information encoded in the discriminated detector signal can be measured with FPGA-TDCs: Leading edge and pulse width
Signal Discrimination using FPGA

Input LVDS buffers as discriminators

- The signals from the detector are pre-amplified with commercial amplifiers (MMICs)

- Input LVDS buffers in FPGAs are used as discriminators – Lattice MachXO2 is used

- The leading edge time and Time over Threshold is encoded in the digital pulse generated at the output LVDS buffers

- The thresholds are set by using the FPGA as DAC via PWM and low pass filter

- All the FEE is directly at the detector and only digital signals are are sent out for measurement

- For precise time measurements of the digital pulse, the TDC implemented in FPGA is used (TRB3)
Signal Discrimination using FPGA
Input LVDS buffers as discriminators

- 500 μV, 6 ns width, analogue signal as input to PCB
- Amplified by factor 40, discriminated at the FPGA-LVDS receiver and sent out to TRB3 as nice LVDS signal
- Threshold is set on the reference LVDS input via a PWM + low-pass with a resolution of <100 μV
- FEE cost (without PCB+connectors) per channel only 0,56€ (16 channel version)
- Performance will be verified in upcoming experiment with 2400 channels PMT/MCP-PMT for large input signals
Time Digitisation in FPGA
FEE & 65 channel TDC on a board plugged to the detector

- 64 signals from detector
- Amplification
- Thresholds
- Input signal discrimination
- Time measurement
- Data readout

- Trigger signal is digitised for reference time (65th channel)
- Data readout through 2GBit/s optical link
- 5 cm times 16 cm to be plugged on the back of an MCP-PMT
- Same FPGA design as on TRB3
- Very high density for FEE & 65 channel TDC + DAQ + Power
Time Digitisation in FPGA
FEE & TDC on the same board

- Time difference between pulser output signals is measured
  - 84 ps time resolution
- Layout errors cause small oscillation on output of amplifiers which destroy the good time resolution
- Performance in beam to be measured in October
Amplitude Digitisation in FPGA concept

- generate ramp on reference pin, measure time until ref. crosses signal
- 10bit ADC, 50MSPS needs 20ps time resolution
- Advantage: many channels in one FPGA (one ramp generator), no data transfer to the FPGA, low power
- Question: What performance can be really reached?
measurements with externally generated signals show that:
- the ADC concepts works
- the measured TDC time resolution for 26ns ramps is compatible with a TDC with 10 bits resolution and 20 MSPS

An integrated solution with on board ramp generator has to be implemented and evaluated.

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<th>ch2 level [mV]</th>
<th>mean</th>
<th>Jitter (RMS)</th>
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</tr>
<tr>
<td>1600.00</td>
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Charge Measurement with FPGAs
QDC-concept

- Idea: Modified Wilkinson ADC
  - Integrate input signal with a capacitor
  - Discharge via current source → fast crossing of zero
  - Measure time to reach zero $\sim Q$

**Diagram:**
- **Amplifier**
- **Integrator (C)**
- **Current source (large R)**
- **Discriminator Fast signal**
- **Switch + Delay**
- **Discriminator Integrated Signal**
- **FPGA**
- **TDC Leading Time, ToT**
- **TDC width $\sim$ integral**
QDC Prototype

- First results with offline correction: 0.2% charge resolution, dynamic range: 50

- Applications: Calorimeter, ...

Prototype Board (4 channels) for TRB 2

Size determined by connectors and TRB 2 infrastructure

Input:
1mA peak
Integrator
Discr.
Width ca. 68ns

Maximum input:
2mA peak, close to saturation
Integrator Discr.:
Width ca. 100ns
Conclusion & Outlook

- A multi-purpose FPGA based TDC module with 256 channels and a time resolution <20ps RMS has been developed.
- With the integrated trigger system and GbE all you need is power and ethernet cable to run a DAQ.
- FPGA based discriminator boards as well as highly integrated full-system solutions to be plugged on the detector have been built: lab results are very promising, to be verified in upcoming experiments with beam.
- Advantages: “simple”, from the shelf, flexible, TDC and DAQ is finished and read to use.
- Disadvantage: larger than a tailored ASIC solution, performance of LVDS discriminators not as good as dedicated discriminators.
- Double edge detection in single TDC channel is currently being implemented.
- ADC design using precise TDCs is being implemented.
- TDC-based QDC prototype has been successfully tested, system for Calorimeter application is currently in design phase.
Thank you for your attention!
References

Backup Slides
TDC in FPGA
Tapped Delay Line Method

- Tapped delay line is used for fine time measurements – suits well with the FPGA architecture
- Delay elements are realised by LUTs
- Fast carry chain structure forms the delay line
- Registers are used to sample the delay line
TDC in FPGA
Architecture of the TDC

Delay line is realised with Full Adders [3]

Slice diagram with LUTs programmed as Full Adders

TDC Architecture
Laboratory Test Results

- Time difference measured between 2 channels
- $\Delta t = (t_{\text{coarse1}} - t_{\text{coarse2}}) - (t_{\text{fine1}} - t_{\text{fine2}})$
- RMS measured: 10.34 ps against the same clock
- Resolution: $10.34 \text{ ps} / \sqrt{2} = 7.3 \text{ ps RMS}$
Architecture of Time-to-Digital Converter

Lattice ECP2M FPGA Slice Diagram, PFU Diagram and Floorplan
Architectural Effects of FPGA

- Effect of primary clock line in the FPGA
- Effect of longer inter-slice routings
- Effect of PFU architecture
Architectural Effects of FPGA

- Effect of primary clock line in the FPGA
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Architectural Effects of FPGA

**Bin width histogram of a channel with shorter routings**
- Mean: ~10 ps
- Max: ~35 ps

**Bin width histogram of a channel with longer routings**
- Mean: ~15 ps
- Max: ~45 ps
Architectural Effects of FPGA

- Effect of primary clock line in the FPGA
- Effect of longer inter-slice routings
- Effect of PFU architecture
Wave Union Launcher

- More than one delay line is necessary in order to reduce the effect of wide bins
- Wave union launcher is implemented
- Bin widths & non-linearities are reduced
Wave Union Launcher

- More virtual bins
- Narrower bins
- Homogeneous bin distribution

Bins: ~240  
Mean: ~20 ps  
Max: ~45 ps

Bins: ~520  
Mean: ~10 ps  
Max: ~35 ps
Statistical Error & Resolution

- Time difference measured between 2 channels
  \[ \Delta t = (t_{\text{coarse1}} - t_{\text{coarse2}}) - (t_{\text{fine1}} - t_{\text{fine2}}) \]
- RMS measured: 10.34 ps against same clock
- Resolution: \( \frac{10.34 \text{ ps}}{\sqrt{2}} = 7.3 \text{ ps} \)
- Effect of 2 transitions:
  \( \frac{14.82 \text{ ps}}{10.34 \text{ ps}} = 1.43 \text{ factor} \)