TDC readout prototype: test from measurements

Authors:
Marek Pałka
Radosław Trebacz
TDC readout prototype: test from measurements

- Description of TDC board:

  - Board destination:
    - HADES – RPC detector (EU FP6 construction contract nr 515876).
  
  - Main parts of board:
    - TDC,
    - FPGA,
    - ETRAX,
    - RAM’s and FIFO,
    - Etrax.
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- Speed measurements:

  Maximum speed transfer through ethernet: 4.07 MB/s

  Maximum FPGA frequency estimated by Synplify Pro: 87.8 MHz
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- Integral and differential nonlinearity
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- Crosstalk

Crosstalk measurements - ejected channel is firing 10 ns after

Crosstalk measurement - adjacent channel is firing at the very same time as the second
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- Crosstalk

Crosstalk measurement - adjacent channel is firing at the very same time as the second - after 2 hours

<table>
<thead>
<tr>
<th>Channels</th>
<th>Counts</th>
</tr>
</thead>
<tbody>
<tr>
<td>516</td>
<td>0</td>
</tr>
<tr>
<td>517</td>
<td>12000</td>
</tr>
<tr>
<td>518</td>
<td>4000</td>
</tr>
<tr>
<td>519</td>
<td>2000</td>
</tr>
</tbody>
</table>

Crosstalk measurement - adjacent channel is firing at the very same time as the first

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- Summation
  - System is during tests now and it is operating,
  - In November there will be RPC detector test and our board,
  - Designed board is flexible.