MAPS pixel readout based on the HADES TRB concept

Ingo Fröhlich

University of Frankfurt

JOHANN WOLFGANG GOETHE

UNIVERSITÄT

FRANKFURT AM MAIN

Introduction

- ## Monolitic Active Pixel Sensors (MAPS)
  - ### Candidate for inner part of the STS detector

  High resistivity diode

  Amplifier (Source follower)

  M2 Select

  $C_{Parasitic}$

  M3 Output

  - ### MIMOSA11 prototype testing done @ "technology lab" – IKF, Frankfurt [1]
    - #### Test-Setup using USB hardware & analysis software from IReS / IPHC

[1] see talk of M. Winter

Test setup at IKF

[1]
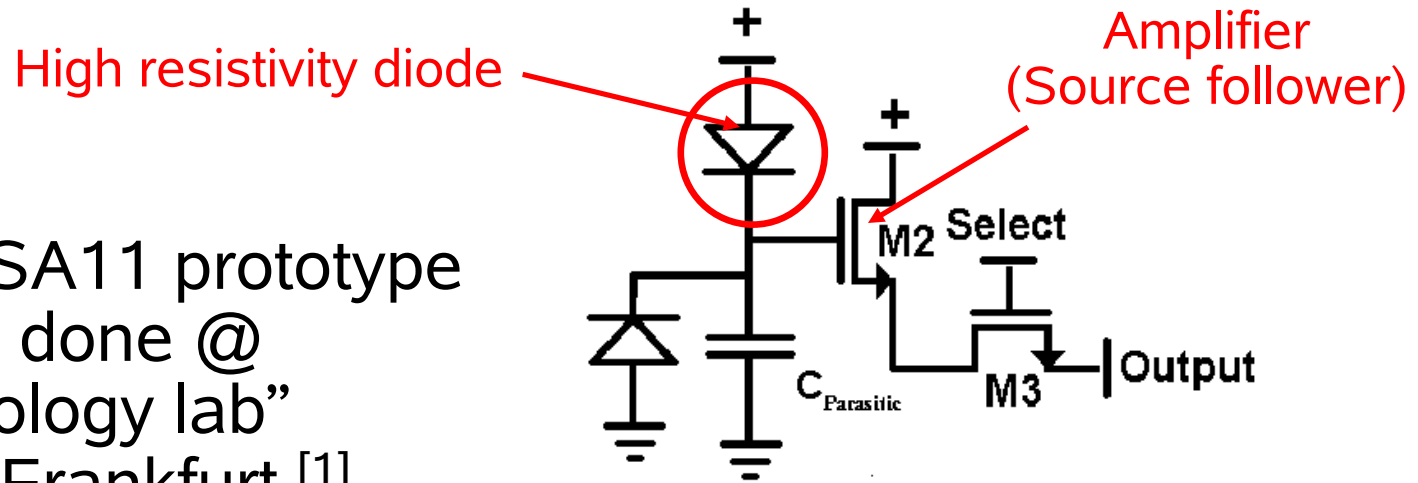
- Tests done with focus on radiation hardness [2]
  - Using USB readout board designed by IReS/ IPHC - Strasbourg
- Analysis done offline
  - No data reduction
- ToDo:
  - Tests for online data reduction algorithms
  - Study of integration of many MIMOSAS
  - In-Beam test with existing detector
- **Needs readout hardware for large scale experiment**
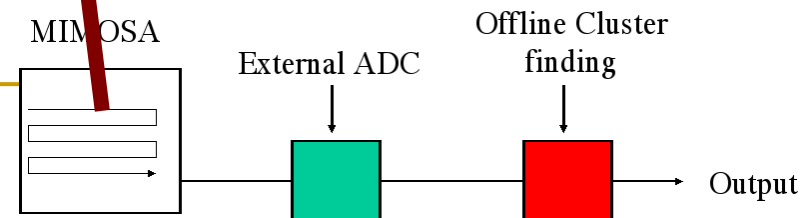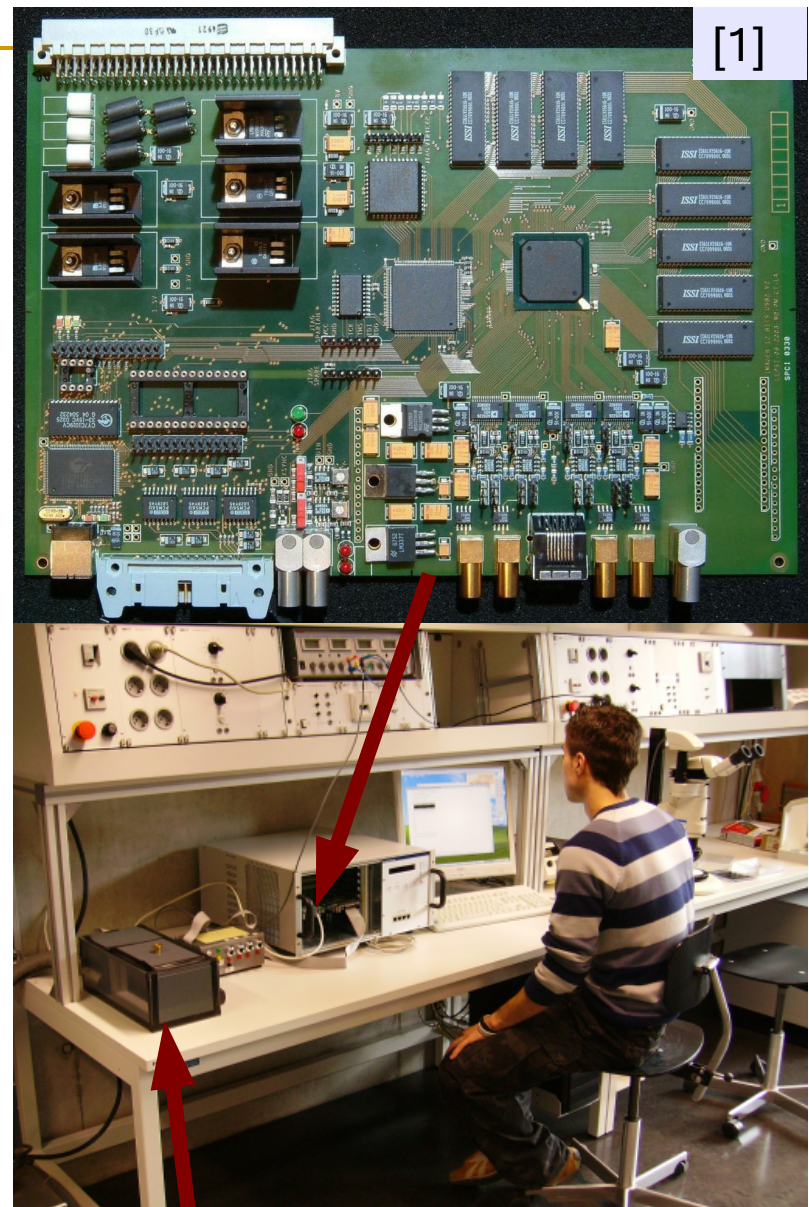
[1] Photo made by Gilles Claus, IReS / IHPC
[2] Work done by S. Amar-Youcef

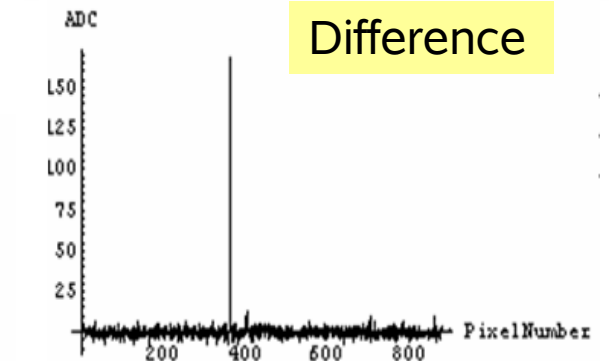MIMOSA   External ADC   Offline Cluster finding   Output

Data from Test-Setup

- MAPS: Detection of ionizing particles based on charge loss
- Subtraction of 2 frames
  - CDS=correlated double sampling
  - Done offline after all frames have been taken
  - Requires some disk space
- Future full system tests require GSI based readout (e.g. HADES)
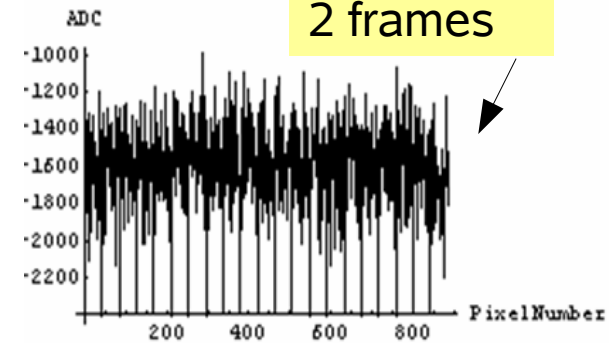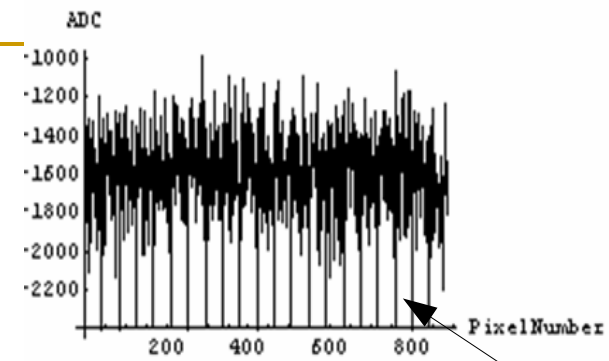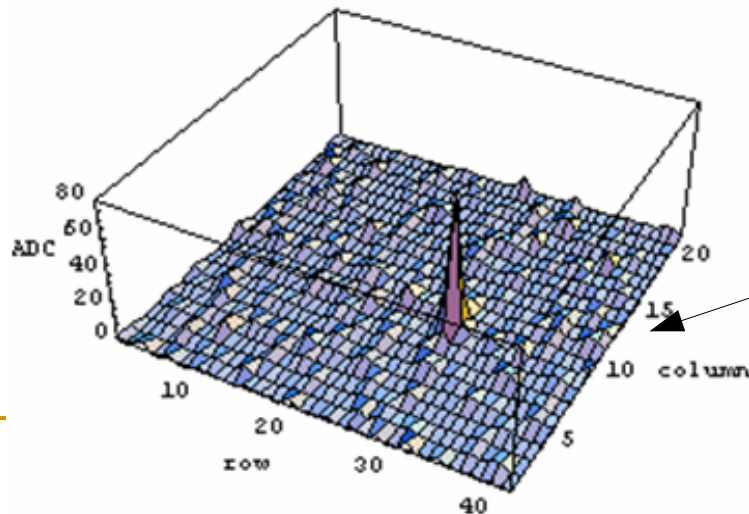
2 frames

Difference

Needed online for a longer test
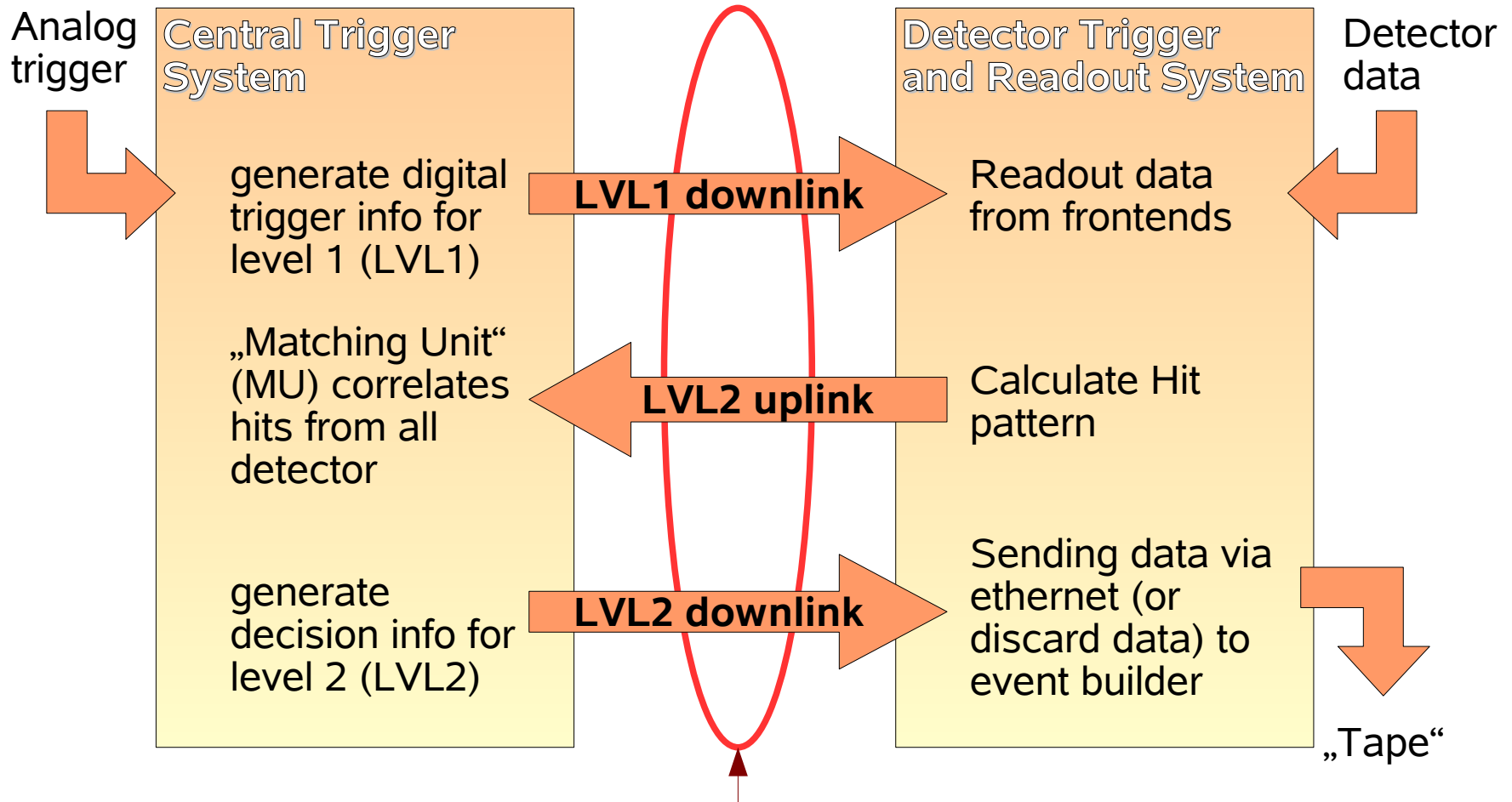
HADES-TRB

„Triggered Readout Board"

- **HADES could be a candidate for an in-beam test**

- **Parts of the HADES-DAQ will be redesigned:**

- **TRB (Triggered Readout Board)**
  - Standalone & ethernet based
  - Can be adapted to different requirements
  - Allow for online data analysis & reduction
  - TRBv1 for HADES-RPC [1] is existing and tested

[1] see talk of D. Gonzales

HADES readout (simplified)

Analog trigger

Detector data

Central Trigger System

Detector Trigger and Readout System

generate digital trigger info for level 1 (LVL1)

LVL1 downlink →

Readout data from frontends

„Matching Unit" (MU) correlates hits from all detector

← LVL2 uplink

Calculate Hit pattern

generate decision info for level 2 (LVL2)

LVL2 downlink →

Sending data via ethernet (or discard data) to event builder
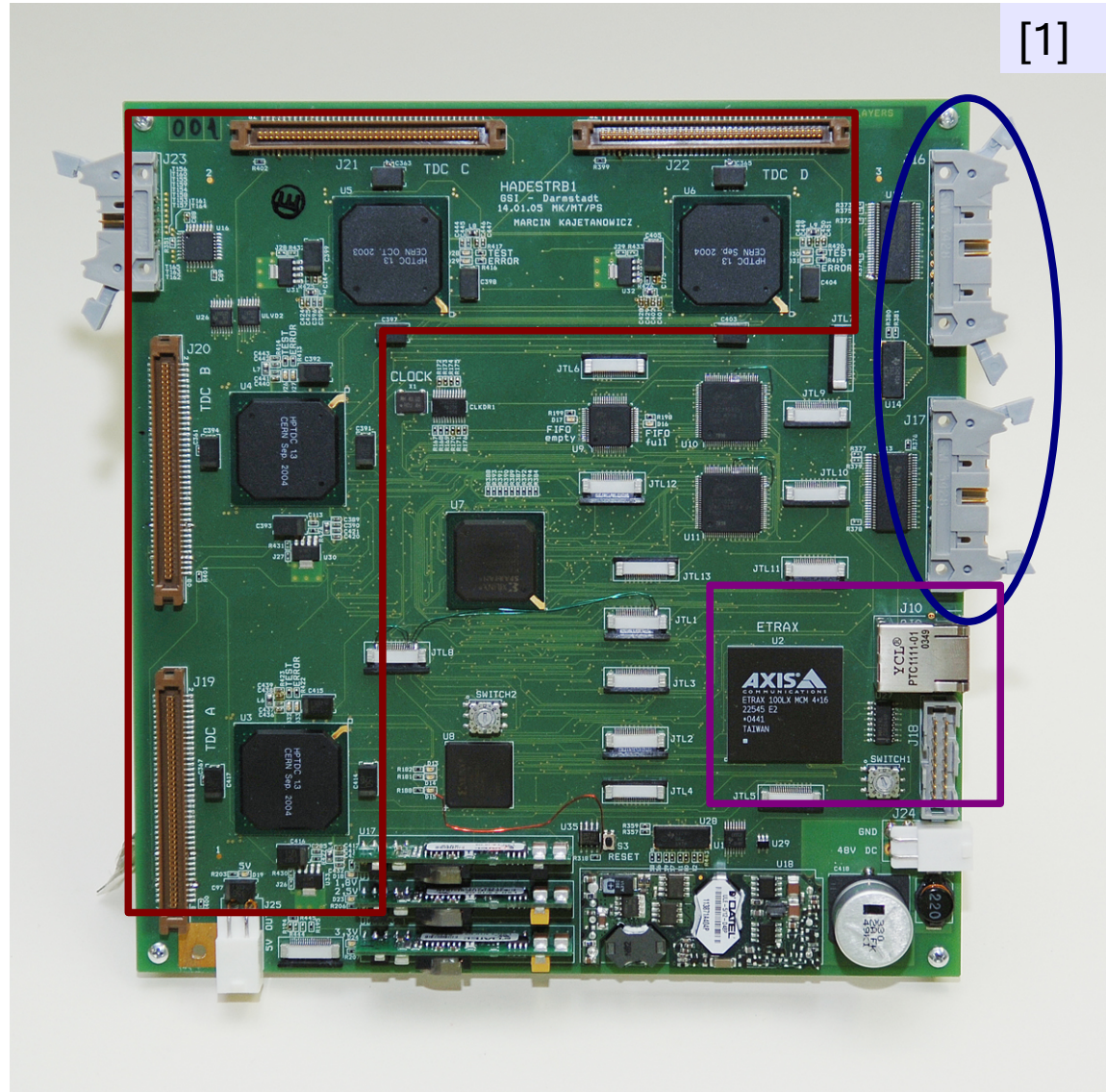
„Tape"

- Communication done via 3 flat cables

TRB v1.0

- **128 channel TDC based on HPTDC [2]**
- On-board DAQ functionality via
  - ETRAX (Linux single chip computer) [3]
  - 100MBit interface
- Access to HADES LVL1 & LVL2 bus (only uplink part)
- Main purpose: Readout for the new HADES RPC
- First tests during beam time have been done

[1] M. Traxler , D. Gil, M. Kajetanowicz, K. Korcyl, M. Palka, P. Salabura, P. Skott, R. Trebacz: GSI Report 2006
[2] HPTDC, Jorgen Christiansen, Digital Microelectronics Group, CERN   [3] www.axis.com
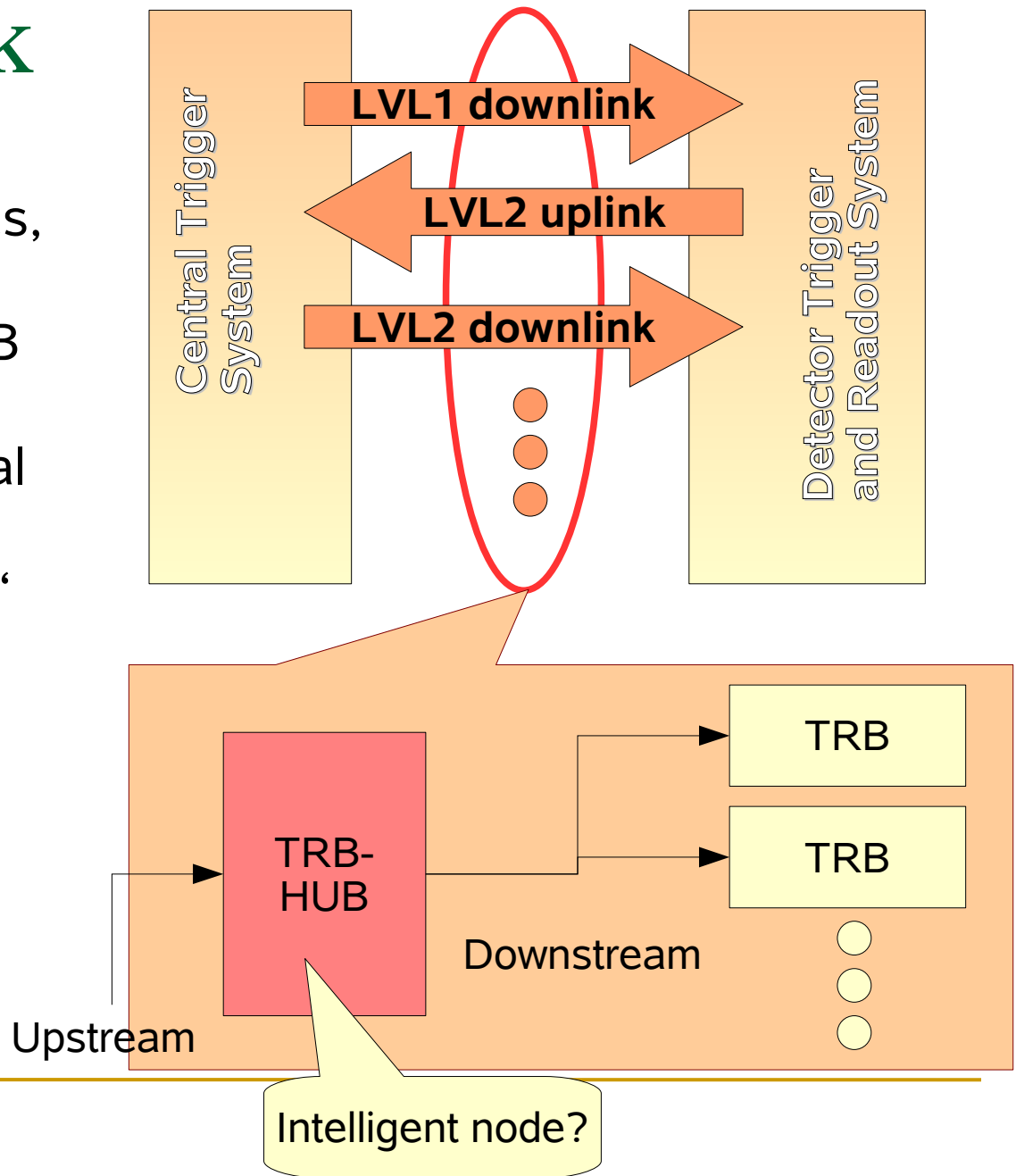
TRB v2.0 (currently designed) [1]

- Faster ETRAX
- Online hit pattern calculation
  - Adapt existing Time-Of-Flight algorithm to RPC
- Needs new hardware
  - TigerSHARC TS201, 24MBit memory, 500MHz, fast LinkPort transfer
    - DSP = Digital Signal Processor (can be programmed via C-Language)
  - XILINX Virtex4
    - Programmable logic resources
- Needs uplink communication
  - Transport of found hits back to the Central Trigger System

TRB-Network

- Bidirectional optical link, TLK1501 SerDes, up to 1.5GBit/s
  - Requirement: HUB latency 150ns
  - 16 individual virtual channels
  - Can combine „old" cables into one protocol
  - Flexible for future extensions, new trigger schemes
- Allow integration of new detectors

Central Trigger System

Detector Trigger and Readout System

LVL1 downlink

LVL2 uplink

LVL2 downlink

TRB-HUB

TRB

TRB

Upstream

Downstream

Intelligent node?

Plans for MAPS Readout

- Build reference tracking system for in-beam tests
  - DAQ compatible with HADES
  - The TRB (+ TRB-network) allows to use the HADES trigger distribution & readout software
  - System integration
  - Special features for MAPS:
    - Replace TDCs by 12-Bit ADCs (e.g. 4 per board)
- Studies of online data processing
  - Reduction of data
  - Aspects of tracking
  - Tests can be done in FPGA & DSP

Summary

- Use a existing DAQ system for the MAPS prototype:
  - Important step to go from a test setup to a full system
- TRBv1 is existing and has been successfully tested
- TRBv2 will have online resources
  - DSP („normal C")
  - XILINX Virtex4 („logic design")
- Tests needed for the MAPS-Readout
  - Will be done at the technology lab / Frankfurt