TrbNet: Full Endpoint

- The central entity for all endpoints is trb_net16_endpoint_hades_full.vhd
- It includes all controlling of the three used channels
  - Lvl1 trigger
  - Data readout
  - Slow Control
- Only one additional entity has to be connected: The approbriate media interface (files named trb_net16_med_...)

TrbNet: Full Endpoint Port Map – part I

- Clock & Reset Signals

```
CLK    : in std_logic;
RESET  : in std_logic;
CLK_EN : in std_logic;
```

- Connect these ports to the media interface (e.g. Optical interface)

```
MED_DATAREADY_OUT   : out std_logic;
MED_DATA_OUT        : out std_logic_vector(15 downto 0);
MED_PACKET_NUM_OUT  : out std_logic_vector( 2 downto 0);
MED_READ_IN         : in  std_logic;
MED_DATAREADY_IN    : in  std_logic;
MED_DATA_IN         : in  std_logic_vector(15 downto 0);
MED_PACKET_NUM_IN   : in  std_logic_vector( 2 downto 0);
MED_READ_OUT        : out std_logic;
MED_STAT_OP_IN      : in  std_logic_vector(15 downto 0);
MED_CTRL_OP_OUT     : out std_logic_vector(15 downto 0);
```

- Connection to temperature sensor

```
REGIO_ONEWIRE_INOUT        : inout std_logic;
```

TrbNet: Full Endpoint Port Map – 1st lvl trigger

- Trigger Received – stays high until trigger is released

```
LVL1_TRG_RECEIVED_OUT     : out std_logic;
```

- Trigger information, valid while TRG_RECEIVED is high

```
LVL1_TRG_TYPE_OUT         : out std_logic_vector( 3 downto 0);
LVL1_TRG_NUMBER_OUT       : out std_logic_vector(15 downto 0);
LVL1_TRG_CODE_OUT         : out std_logic_vector( 7 downto 0);
LVL1_TRG_INFORMATION_OUT  : out std_logic_vector( 7 downto 0);
```

- Trigger release & basic status information

```
LVL1_ERROR_PATTERN_IN     : in  std_logic_vector(31 downto 0);
LVL1_TRG_RELEASE_IN       : in  std_logic;
```

- Old busy signal is inherent to the network protocol
- Trigger should be released when it is sure that the device will be able to accept a new trigger 1µs later
- All trigger information has to be stored until the data is read out

`Wiki: TriggerLvl1Information`

TrbNet: Full Endpoint Port Map – Data Readout

- Start signal & Number of the requested event

```
  IPU_NUMBER_OUT           : out std_logic_vector (15 downto 0);
  IPU_INFORMATION_OUT      : out std_logic_vector ( 7 downto 0);
  IPU_START_READOUT_OUT    : out std_logic;
```

- Data port – data format as described in the pdf (wiki)

```
IPU_DATA_IN             : in  std_logic_vector (31 downto 0);
IPU_DATAREADY_IN        : in  std_logic;
IPU_READOUT_FINISHED_IN : in  std_logic;
IPU_READ_OUT            : out std_logic;
```

- Additional Information to form the network packet

```
IPU_LENGTH_IN           : in  std_logic_vector (15 downto 0);
IPU_ERROR_PATTERN_IN    : in  std_logic_vector (31 downto 0);
```

`Wiki: TrbNetIPUChannel`

TrbNet: Full Endpoint Port Map – Slow Control

- Standardized Status & Control Registers

`Wiki: CommonStatusRegister`

```
  REGIO_COMMON_STAT_REG_IN  : in  std_logic_vector(2*32-1 downto 0);
  REGIO_COMMON_CTRL_REG_OUT : out std_logic_vector(1*32-1 downto 0);
```

- Simple registers, user-defineable

```
  REGIO_REGISTERS_IN  : in  std_logic_vector(32*2**(NUM_STAT)-1 downto 0);
  REGIO_REGISTERS_OUT : out std_logic_vector(32*2**(NUM_CTRL)-1 downto 0);
```

- Internal data port for user defined purposes

`Wiki: TrbNetRegIO`

```
  REGIO_ADDR_OUT            : out std_logic_vector(15 downto 0);
  REGIO_READ_ENABLE_OUT     : out std_logic;
  REGIO_WRITE_ENABLE_OUT    : out std_logic;
  REGIO_DATA_OUT            : out std_logic_vector(31 downto 0);
  REGIO_TIMEOUT_OUT         : out std_logic;

  REGIO_DATA_IN             : in  std_logic_vector(31 downto 0);
  REGIO_DATAREADY_IN        : in  std_logic;
  REGIO_NO_MORE_DATA_IN     : in  std_logic;
  REGIO_WRITE_ACK_IN        : in  std_logic;
  REGIO_UNKNOWN_ADDR_IN     : in  std_logic;
```

TrbNet: Full Endpoint - Generics

- Most of the values can be kept at their default state, only the ones to be changed are shown here
- Select valid broadcast addresses

`Wiki: TrbNetAddresses`

```
  BROADCAST_BITMASK          : std_logic_vector(7 downto 0) := x"FF";
```

- Configure user registers

`Wiki: TrbNetRegIO`

```
  REGIO_NUM_STAT_REGS        : integer := 3;
  REGIO_NUM_CTRL_REGS        : integer := 3;
  REGIO_USED_CTRL_REGS       : std_logic_vector := "00000001";
  REGIO_USED_CTRL_BITMASK    : std_logic_vector := (others => '1');
```

- Information about board, design version & time

`Wiki: TrbNetRegIO`

```
  REGIO_INIT_BOARD_INFO   : std_logic_vector(31 downto 0) := x"1111_2222";
  REGIO_INIT_ENDPOINT_ID  : std_logic_vector(15 downto 0) := x"0001";
  REGIO_COMPILE_TIME      : std_logic_vector(31 downto 0) := x"00000000";
  REGIO_COMPILE_VERSION   : std_logic_vector(15 downto 0) := x"0001";
  REGIO_HARDWARE_VERSION  : std_logic_vector(31 downto 0) := x"12345678";
```