Advanced JTAG Configuration Tips for Xilinx FPGAs

Agenda

- Basics of JTAG
- Basic Causes of Configuration Failure & Designing Bullet-proof JTAG Chains.
- Troubleshooting 101
- Summary

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- **Basics of JTAG**
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FPGA Developer on holiday…..

IEEE 1149.1 – aka "JTAG"

- Defines a five wire serial interface known as the TAP, or Test Access Port.

- Consists of the signals TCK, TMS, TDI, TDI, and TRST (optional).

- The TAP serves several purposes, including programming and boundary-scan testing.

IEEE 1149.1 – Test Access Port

- Every fully compliant JTAG device includes a shift register composed of boundary scan cells, a 4 or 5 wire Test Access Port, and a state-machine controller.

- The TAP pins are:

    TCK – Clock signal, separate from other clocks to the IC. This clock is used to clock data in and out of the TAP controller.

    TMS – TAP State Machine Mode Select signal.

    TDI – Data input to the TAP controller.

    TDO – Data output from the TAP controller.

    TRST – TAP asynchronous reset.

# IEEE 1149.1 – Test Access Port

- The TAP allows access to internal registers associated with the TAP controller

- Bypass – used to bypass the device. A one bit register.

- Instruction – used to shift instructions to the TAP controller. 5 or more bits

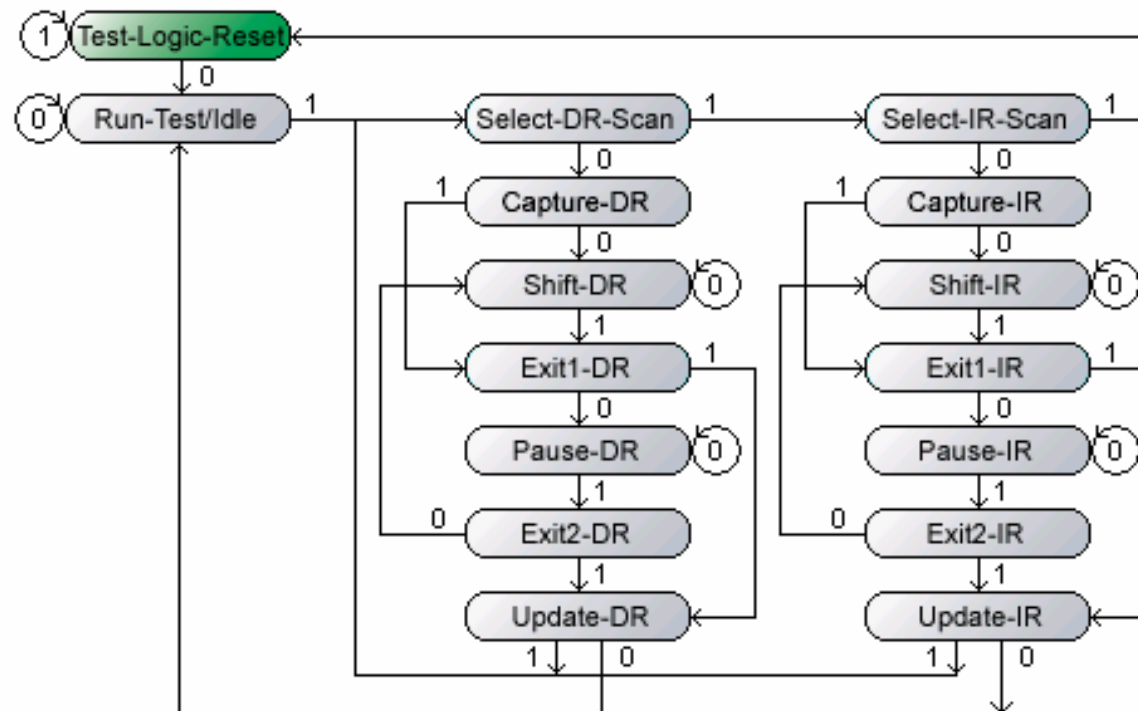- Data – used to shift data to and from the TAP controller.
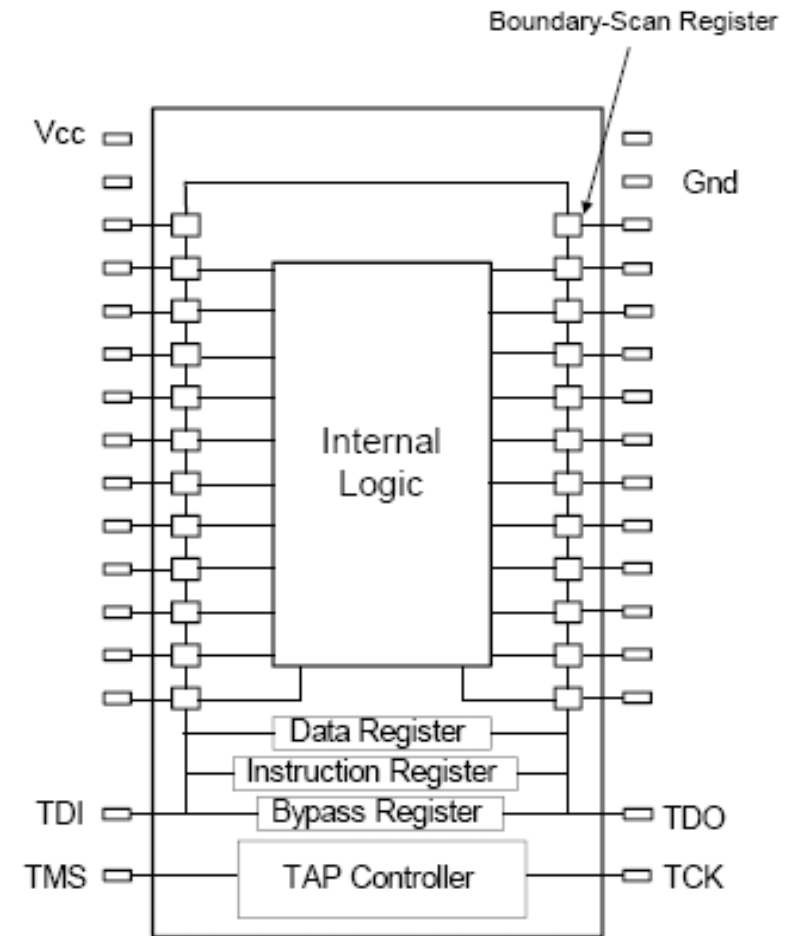
Xilinx TAP Controller State Machine

- State transitions are shown below and are controlled by the state of TMS (logic 0 or logic 1).
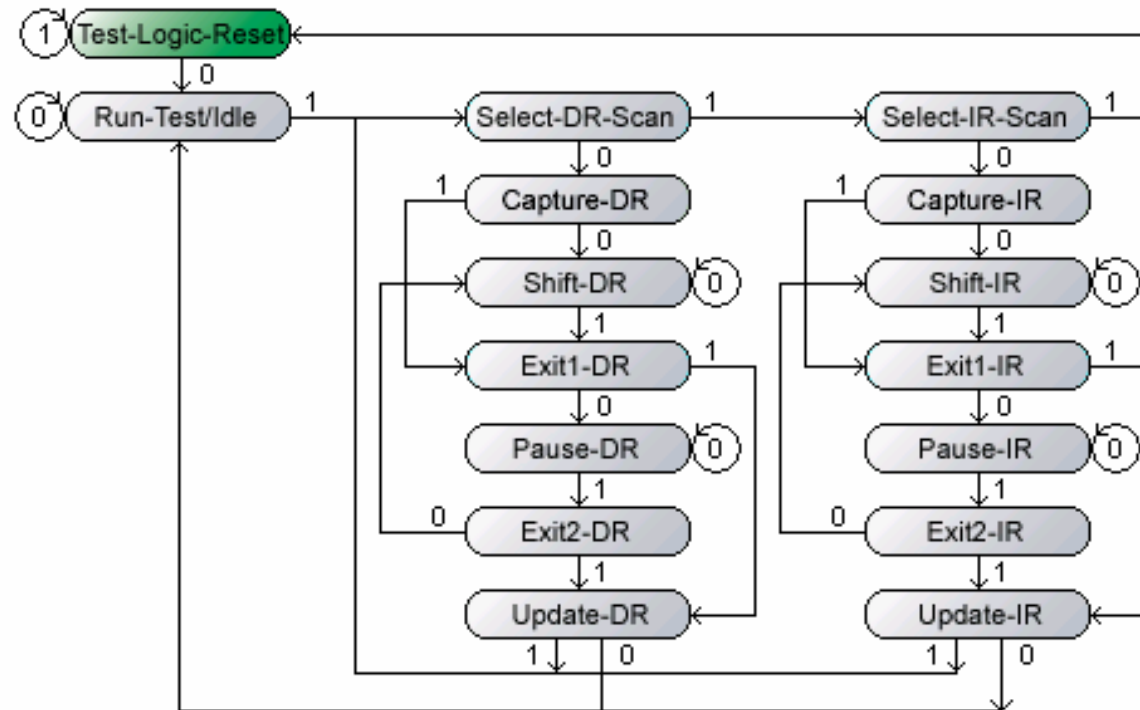
Xilinx TAP Controller State Machine

- The flow through the middle of the diagram is for the Data Register, the flow on the right is for the instruction register.

Xilinx TAP Controller State Machine

- When the device is powered on, the TAP controller is reset and automatically loads the IDCODE instruction into the instruction register. Therefore, if you read the data register immediately after TAP reset, you will read back the IDCODE for the device.

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The JTAG Chain….

- The JTAG chain connects each subsequent device in a daisy chained fashion.

- All devices are driven by the TCK and TMS signals from the programmer (USB, P3, P4 or user).

- TDO of the first device connects to TDI of the downstream device.
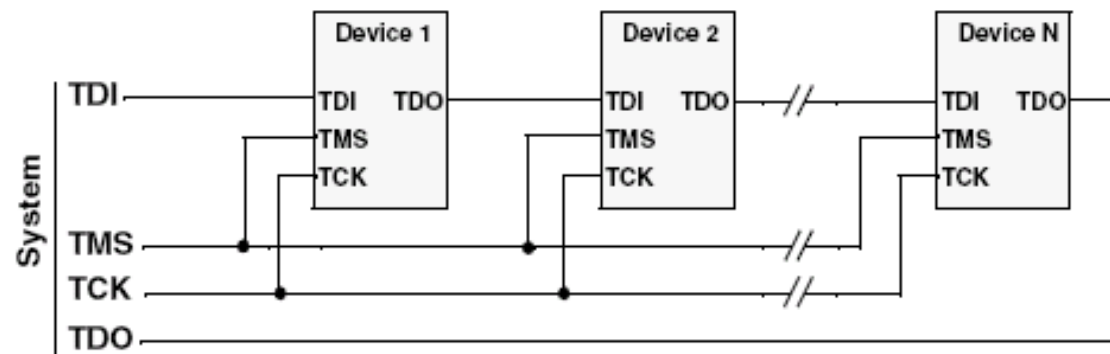
Data goes out….

- In order for this to work effectively, data must propagate through the system in one half cycle of TCK, otherwise, chaos will rule.

- TMS and TDI written onto the chain from the master (Impact via P4 or USB) on the falling edge of TCK.

- TMS and TDI are sampled by the FPGA or CPLD or the rising edge of TCK.
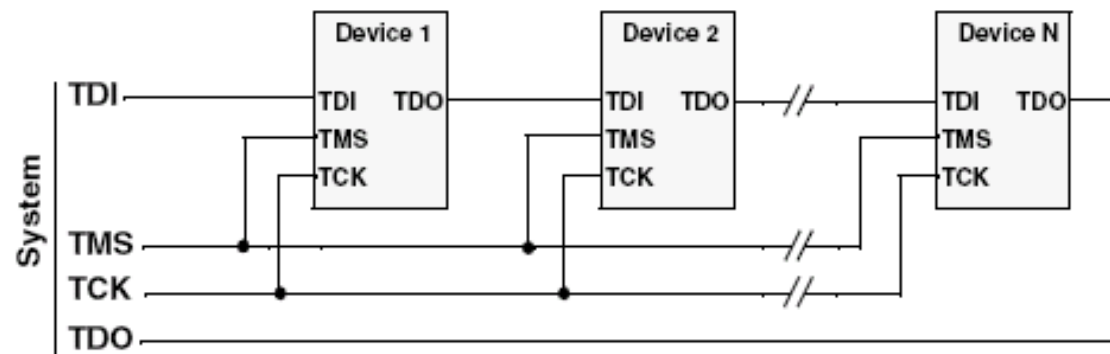
Data comes in…

- Likewise, TDO is written on the falling edge and is sampled on the rising edge.

- Setup times inherent to the downstream device (FPGA, CPLD, Cable or other) must be met in order to reliably read the data at the receiver.

- If setup times are not accounted for, the user may not be able to read the chain at full speed.
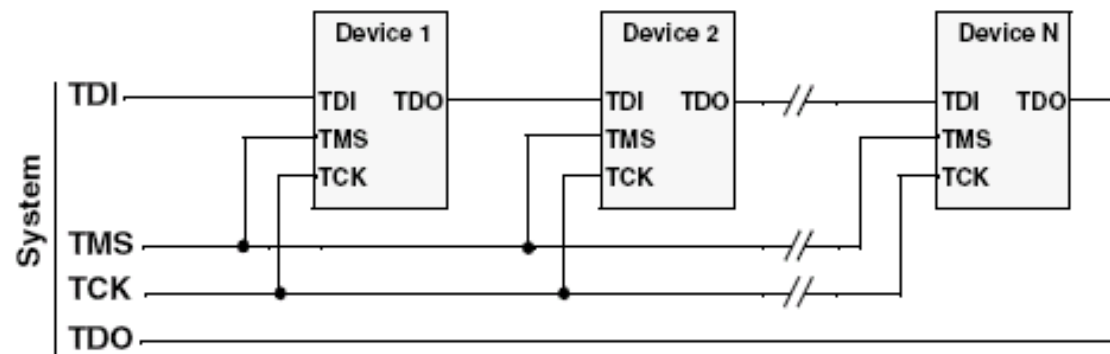
Platform USB propagation delay times

- The propagation delay times of the Platform USB cable need to be accounted for in the design of your JTAG chain. These delays can be found in DS300 – the Platform Cable USB Product Specification.

- http://www.xilinx.com/bvdocs/publications/ds300.pdf
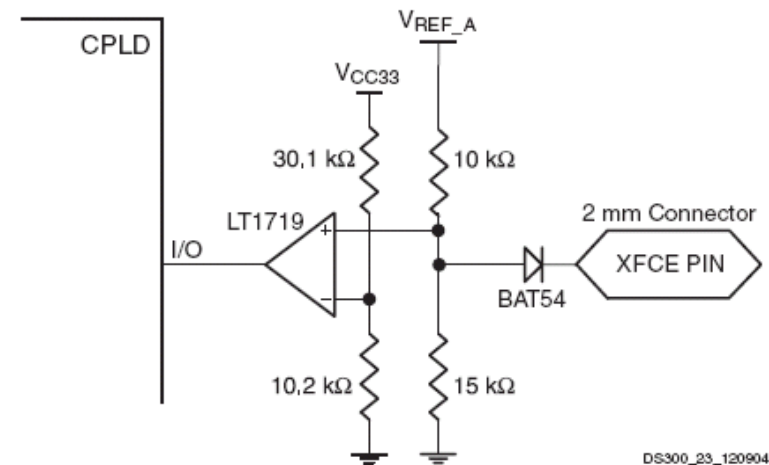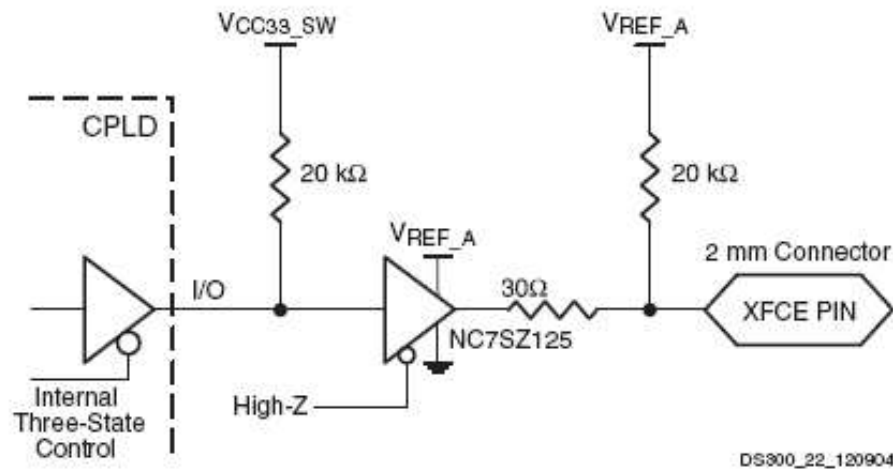
The mysterious Vref pin…..

- What is this pin for?
- What should I connect it to?
- What happens if I connect it incorrectly?

The mysterious Vref pin…..

- The figures below illustrate the circuits used inside the Platform USB cable to transmit the TCK, TMS and TDI signals and to receive the TDO signal.

- Note that Vref is used as a reference to power these circuits.

The mysterious Vref pin…..

- If you analyze the TDO input circuit, you will see that it operates in current mode and detects a logic 0 on TDO when the input voltage produces a current of ~ 166uA.

- Using an incorrect Vref would change the threshold Voltage as well as the threshold current.

- Vref should be the same as the JTAG voltage on the device.
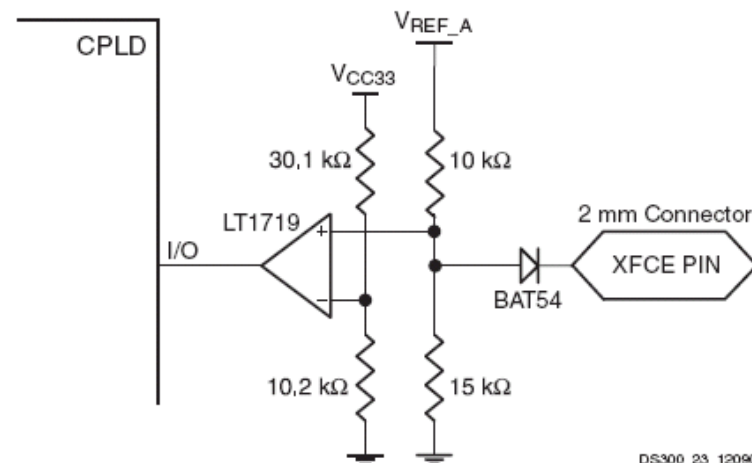
The mysterious Vref pin…..

- In the case of a Spartan 3 device, the Vref voltage is equal to Vccaux (2.5V).
- In the case of a Virtex 4 device, the JTAG Vref voltage is determined by Vcco0 on the FPGA.

Distribution of TCK and TMS signals

- TMS and TCK are very susceptible to misuse due to the fact that they must travel across the board to connect with multiple devices.

- Routing must be kept short and free of stubs. Direct routes between devices are an absolute requirement. A treed routing structure on the PCB is not appropriate and will greatly reduce the likelihood of a workable design.
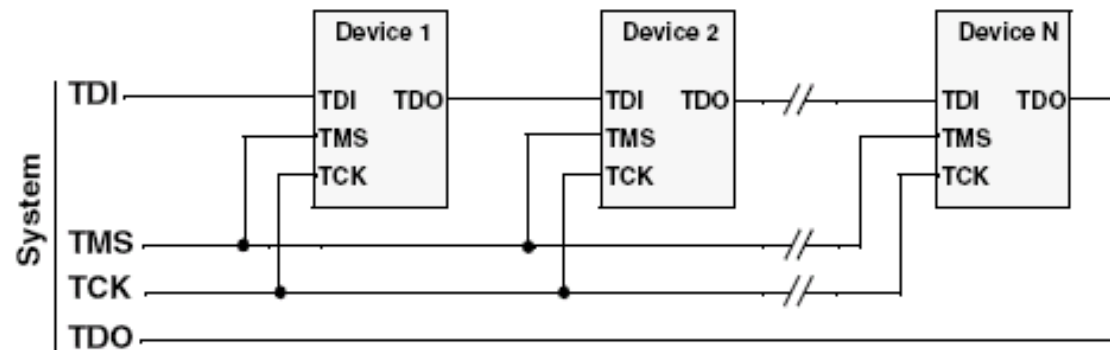
Distribution of TCK and TMS signals

- Most designers look at TCK and TMS as low frequency signals. This is only somewhat true.

- You must consider that these are signals driven by an FPGA designed to produce edge rates for signals greater than 300MHz in frequency.

- While the signals may change at slow rates, the buffers produce, and the detection circuits within the FPGA respond to, very fast transitions.

- Poor signal integrity on the TCK signal is one of the most likely causes of JTAG failure. The TCK is one of the most difficult to deal with as it must route to every device.

Distribution of TCK and TMS signals

- If you have a single FPGA on your board, you want the JTAG header as close to the FPGA as possible.

- If you have multiple FPGAs, you should consider buffering the TCK and TMS signals.

- The 2mm ribbon header used with the P4 and USB cables is designed to provide a fixed impedance and provides alternating ground and signal lines throughout the cable to afford better performance with high-speed FPGAs.

Slave Serial	JTAG				
INIT	NC	14	□ □	13	GND
NC	NC	12	□ □	11	GND
DIN	TDI	10	□ □	9	GND
DONE	TDO	8	□ □	7	GND
CCLK	TCK	6	□ □	5	GND
PROG	TMS	4	□ □	3	GND
V$_{REF}$	V$_{REF}$	2	□ □	1	GND

0.0797" (2 mm)

0.0787" TYP.

0.472"   0.656"

0.020" (0.5 mm) SQ. TYP.

ds300_16_111804
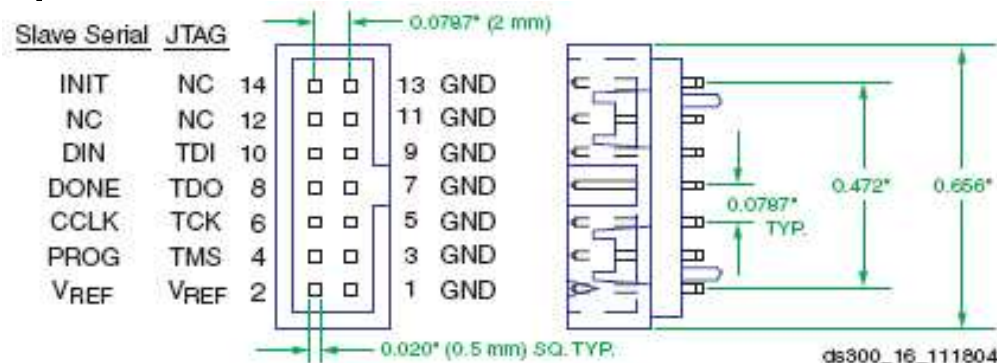
Distribution of TCK and TMS signals

- Differential signaling affords better control of propagation delay across the board and greatly reduces the affects of crosstalk and noise.

- Adding differential buffers to the TCK line on your board should improve performance and reduce noise pick-up from surrounding circuitry.

DS300_24_110804
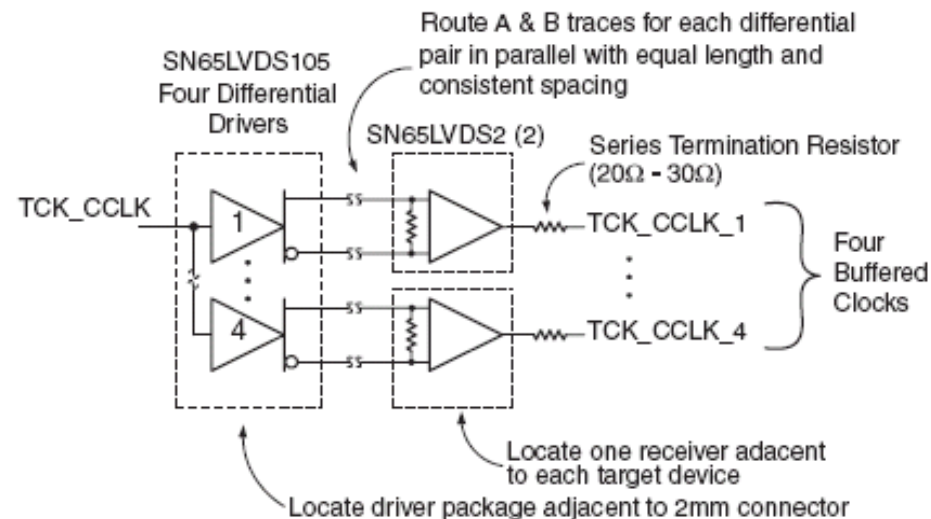
Distribution of TCK and TMS signals

- Route the JTAG signals together and away from other high-frequency signals. Provide a ground path return and route the signals using defined impedance routes.

- Consider terminating the JTAG signals to avoid ringing, particularly TCK.

- Several types of terminations can be used, but note that the Platform USB cable does already include a 30 Ohm source series termination on the outputs. For this reason, AC termination may be the best topology to use on your PCB. Simulation is the key to success.

- Keep the design flexible, allowing you to populate or not populate components such as buffers and terminations when it comes time for production.

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Troubleshooting 101

- Check to ensure that the cable works with an known good board such as an evaluation board.

- Run IDCODE looping within Impact 10000 iterations to test the integrity of the chain. This isn't a foolproof test, but it is a good indicator of potential issues.

- If IDCODE looping still does not function, try shifting out the IDCODE manually using Impact's debug function. If you are able to obtain the IDCODE this way, the problem is with the hardware design.

- Download a trial copy of Universal Scan and confirm whether or not the JTAG on your board is working as expected.

Troubleshooting 101

- Look at the signals with a scope – determine if TDO is arriving at the JTAG header with enough time margin to meet the set-up time requirements of the JTAG cable.

- Do the signals look clean, free of noise and ringing?

- If you are working with an open chassis, consider that some of the problems may be due to induced or coupled noise feeding into the cable.

- The Platform USB cable is internally shielded, but the cable leading to your PCB is not. Consider installing a ferrite cable clamp on the ribbon cable to eliminate induced high-frequency noise, or consider adding small ferrite beads to the JTAG signals at the header on the PCB to remove coupled noise.

Summary

- JTAG is an IEEE standard which affords both boundary scan and also programming of device on the PCB.
- There are many potential causes of failure in JTAG chains, particularly as voltages and lithographies are reduced. It is important that you avoid these pitfalls.
- If you do encounter difficulties, there are several techniques that you can explore in an effort to find the source of the problem, or eliminate it as an issue directly related to the Xilinx toolchain.

A few of many references….

- V4 Configuration Guide: http://www.xilinx.com/bvdocs/userguides/ug071.pdf
- Signal Integrity Central: http://www.xilinx.com/products/design_resources/signal_integrity/index.htm
- Ultracad.com: http://www.ultracad.com/calc.htm
- Platform USB Specification: http://www.xilinx.com/bvdocs/publications/ds300.pdf
- Universal Scan: http://www.universalscan.com/
- XAPP361: http://www.xilinx.com/bvdocs/appnotes/xapp361.pdf
- XAPP069: http://www.xilinx.com/bvdocs/appnotes/xapp069.pdf
- Xilinx JTAG landing page: http://www.xilinx.com/xlnx/xweb/xil_publications_display.jsp?iLanguageID=1&category=-1209876&sGlobalNavPick=PRODUCTS&sSecondaryNavPick=Design+Tools
- IEEE: http://standards.ieee.org/reading/ieee/std/testtech/1149.1-2001.pdf

Demo

- Demonstrate IDCODE looping
- Demonstrate manual read of IDCODE
- Demonstrate Universal Scan