128-channels amplifier-discriminator module (HADES TRB ADDon TOF).

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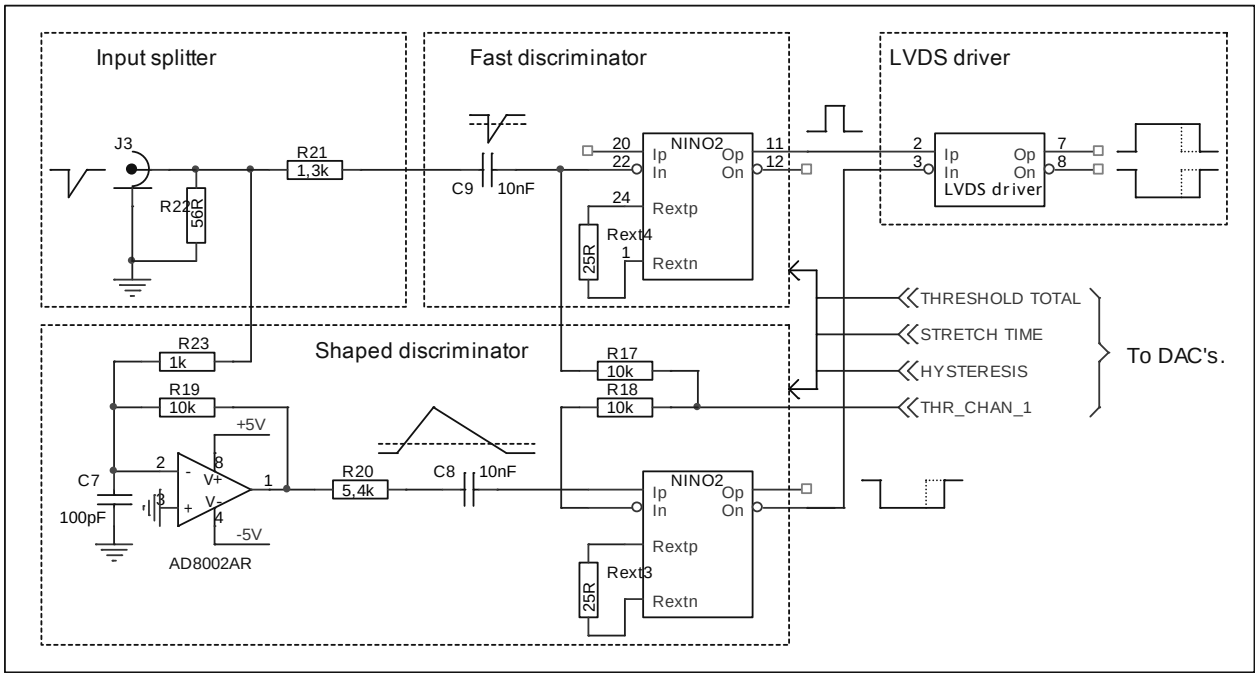
The 128-channel Time over Threshold (TOT) front-end amplifier-discriminator module (HADES_128_TOT) for HADES experiment is an amplifier-discriminator optimized for PMT TOF applications with TOT method of time walk correction and also particle identification. The use of 8-channels ASIC NINO integrated circuits, which design at CERN for ALICE TOF system is provide excellent timing performance and a power dissipation of less than 80mW per ADDon TOF channel.

Tabl. 1. *Common parameters of ADDon TOF module.*

Parameter	Value
Number of channels	128
Input impedance	50 Ω
Output signals standard	LVDS
Rise time (fast channel)	< 1 ns
Input voltage dynamic range	< 5 V
Cross talking factor	< 1/100
Leading edge timing jitter	< 25 ps rms
Trailing edge timing jitter	< 1000 ps rms
Output signal width range	25 - 120 ns
Threshold value range	(10 – 110)mV
Individual threshold range	- 20mV / +20mV
Stretch timer range	1ns – 50us
Hysteresis range	0 – 13%
Input referred threshold skew	< 5 %
Power consumption per channel	< 80 mW

1. The channel of amplifier-discriminator structure.



The channel of HADES_128_TOT amplifier-discriminator based on two NINO ASIC channels. 8-channels NINO ASIC was design for TOT (Time over Threshold) method time walk

correction. Fast NINO discriminator (FAST part) is provides leading edge of output pulse. Trailing edge of output pulse is given from shaped discriminator (SLOW part), realized on second NINO channel, combined with shaper unite.

Using especial shaper provide persistent of pulse width (TOT) dependence from PM amplitudes.

Fig.4 One channel of HADES_128_TOT amplifier-discriminator schematic.

1. STRUCTURE and CONTROL SIGNALS.

Structure of module 128-channel HADES_128_TOT amplifier-discriminator showed on Fig1.

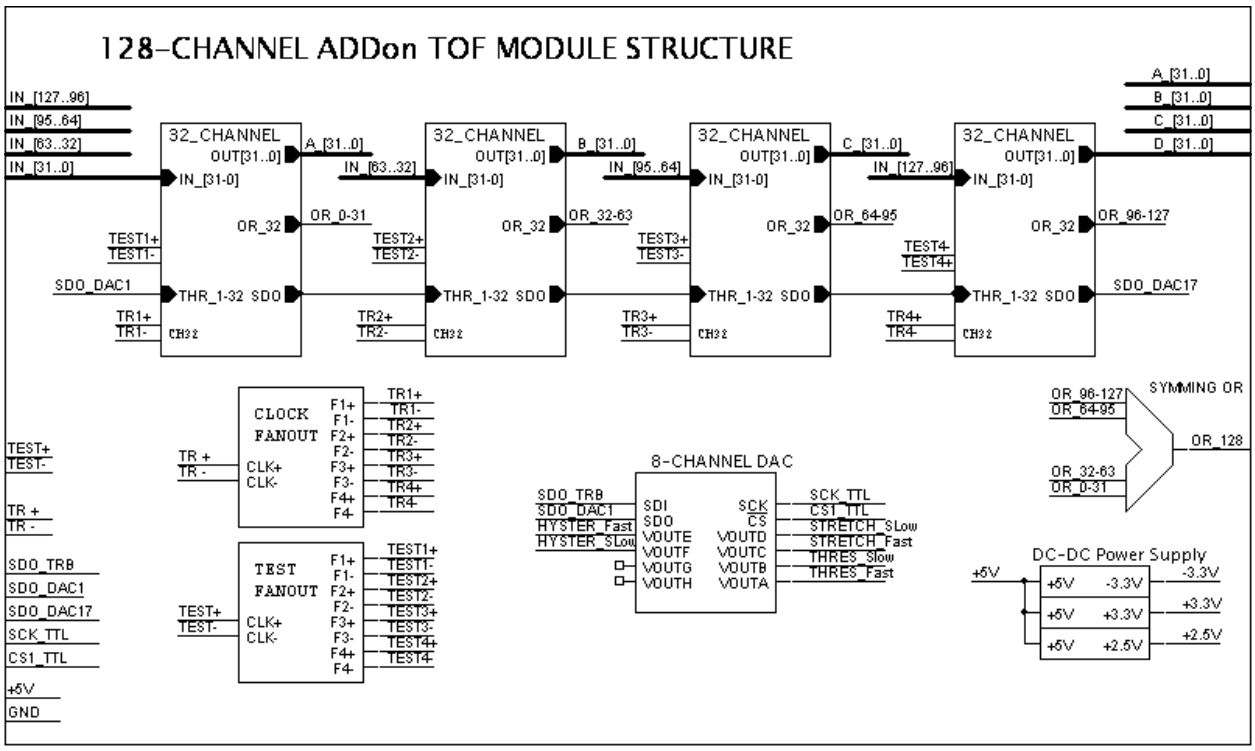
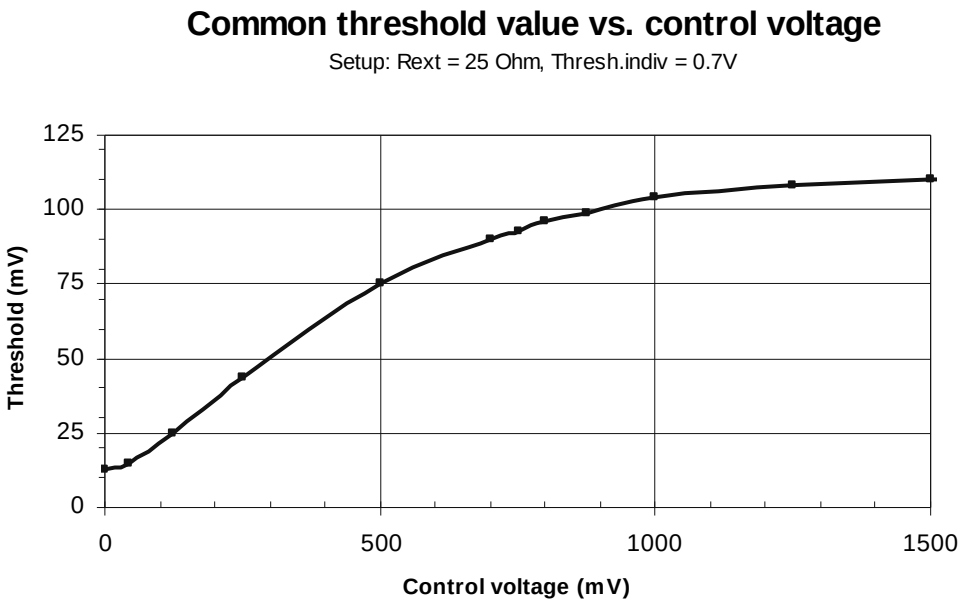


Fig.1 HADES_128_TOT module structure.

Module consists of:

- Four identical 32-channel discriminators parts,
- Common board internal DAC for TOTAL THRESHOLD, HYSTERESIS and STRETCHER controls,
- 16 DAC's for control THRESHOLD by 128 CHANNELS individually,
- Analog multiplicity schematic with 128-OR function (analog summing of 128-th digital levels), negative output polarity of "OR_128" signal,
- TEST fanout schematic for monitoring all 128 discriminator channels,
- TIME REFERENCE fanout schematic for generate timing signal by each 32nd channel,
- POWER SUPPLY DC-DC converters,
- Temperature sensor.

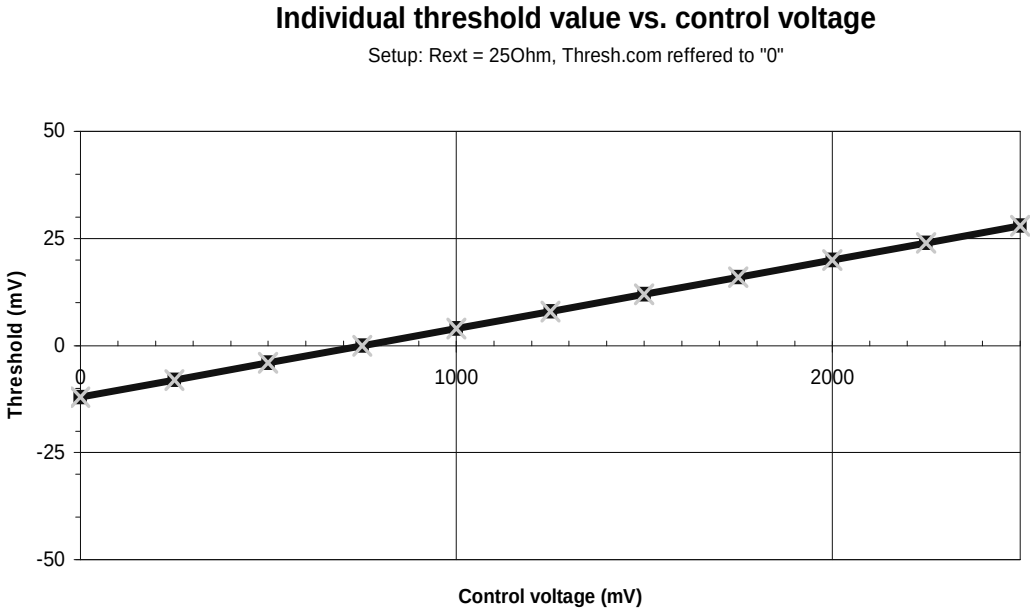
2. COMMON THRESHOLD settings.



Separate THRESHOLD control signals for FAST and SLOW parts:

- THRESHOLD FAST common signal for all 128 channels,
- THRESHOLD SLOW common signal for all 128 channels,
- Output DAC's voltage range (0 – 2.5)V correspond to threshold range (0 – 110) mV,
- Used DAC1, part A (FAST), part B (SLOW).

INDIVIDUAL THRESHOLDS 128 signals coming for FAST and SLOW parts.



- Output DAC's voltage range (0 – 2.5) V correspond to input referred threshold range from (- 35mV) to (+50mV) from total threshold level.
- Used DAC's (2 – 17).

3. STRETCH TIME settings.

Separate STRETCH TIME control signals for FAST and SLOW parts:

- STRETCH TIME FAST common signal for all 128 channels
- STRETCH TIME SLOW common signal for all 128 channels
- Used DAC1, part C (FAST), part D (SLOW)
- Output DAC control voltage range is (0.5 – 2.5) V, corresponding time range showed on figure2.

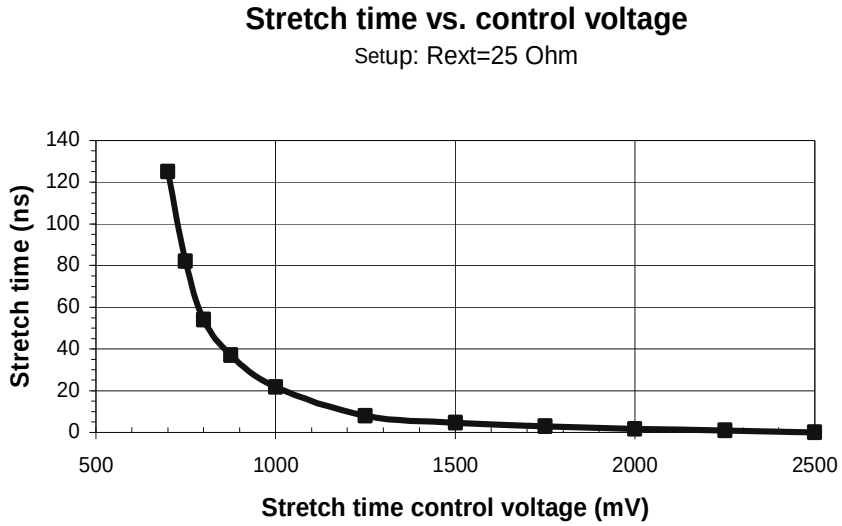


Fig.2 Stretch time vs. control voltage.

- Use DAC1, part C (FAST), part D (SLOW).
- Usual STRETCH TIME is 10ns correspond to control voltage +1.2V.

4. HYSTERESIS common settings.

Separate HYSTERESIS control signals for FAST and SLOW parts:

- HYSTERESIS FAST common signal for all 128 channels,
- HYSTERESIS SLOW common signal for all 128 channels,
- Output DAC's control voltage range is (0.5 – 2.5) V, referred hysteresis range (0 – 13) %
- Used DAC1, part E (FAST), part F (SLOW),
- Default HYSTERESIS value is 1-2% corresponds to control voltage +1.2V.

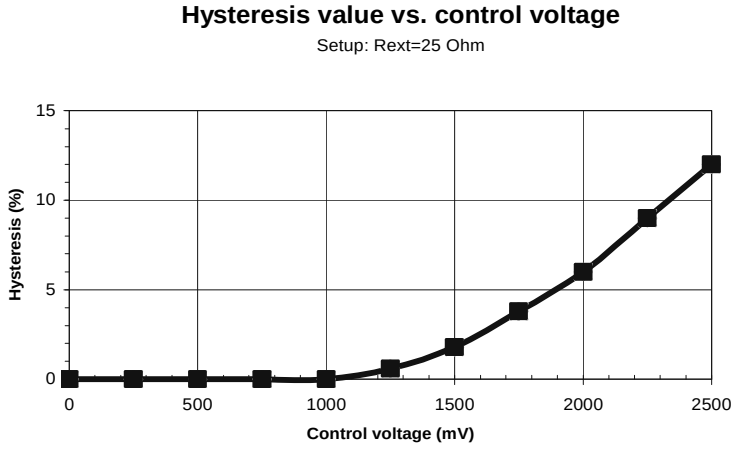


Fig.3 Hysteresis value vs. control voltage.

5. TIME REFERENCE.

External TIME REFERENCE signal on LVDS levels is receive from TYCO connector, fanouting and corresponds for each 32-chammel module for adding to 32 channel by function OR (each 32nd channel of connectors JTDC1, JTDC2, JTDC3, JTDC4).

6. TESTING (monitoring of all channels).

For testing all 128 channel discriminators use internal TRB control lines AD0_L60 and AD0_L61/ from JTRB1 connector on LVDS levels.

Received TEST signal use for generate testing pulses for all 128 channels by active fanouting to each 8 channel parts and passive splitting inside 8 channel schematic.

7. DAC's control lines.

All 17 DAC's are using control lines from TRB module: SDO_TRB, SDO_DAC1, SDO_DAC17, SCK_TTL, and CS1_TTL.

Temperature sensor is connecting to line FS_PE9 of JTRB2 connector.

8. INPUT and OUTPUT CONNECTORS.

For connect to PMT used 50 ohm micro coaxial connectors MMCX.

Each 32-channel outputs are connect to output connectors A,B,C and D which named like correspond TRB input connectors:

- Channel's 1 – 32 are connect to JTDC1 (A_HIT_IN (31 - 0)),
- Channel's 33 – 64 are connect to JTDC2 (B_HIT_IN (31 - 0)),
- Channel's 65 – 96 are connect to JTDC3 (C_HIT_IN (31 - 0)),
- Channel's 97 – 128 are connect to JTDC4 (D_HIT_IN (31 - 0)).

9. Generator test results of 64-channel prototype board are presented on Fig.5. and Fig.6. For generator testing used pulse with 5ns rise time and internal jitter ~ 25-30ps.

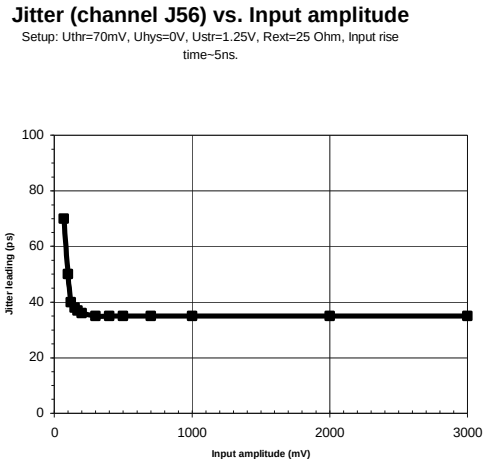


Fig. 5

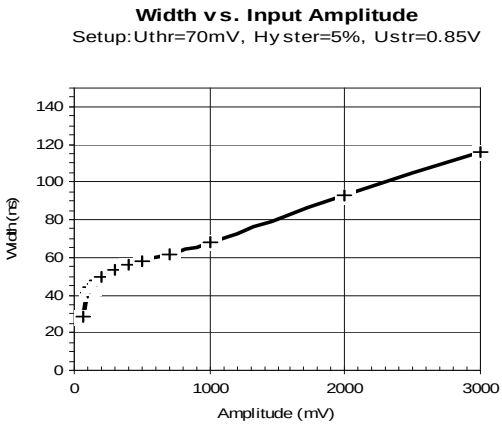


Fig. 6

10. Power consumption:

- External power supply +5V (1,8A).
- Internal power dissipation: +3.3V (0,5A), +2,5V (1,3A), -3,3V (0,35A).