DAQ: Status of Upgrade / Tasks

Outline

- Overview of DAQ Upgrade
  - Motivation
  - Architecture
  - Projects / People
  - Hardware: Readout and IPU-boards
    - TRB V1, Dev-Board (HadCom), TRB V2
    - TOF-Readout/IPU, MDC-Readout/IPU
    - Trigger Distribution / TRB-Network
- EU-Contract and BMBF money
- Discussion
  - Tasks for participants
  - Schedule / Estimates

Motivation: bad performance!

	max LVL1	max LVL2	LVL2 trigger downscaling factor
pulser rate	17 kHz	4-5 kHz	10-20
p+p	8-6 kHz	1-3 kHz	10-20
Ar+KCl	3-4 kHz	1-2 kHz	3

- DAQ performance not sufficient for large systems
  - LVL1 and LVL2 transfer
- LVL2 trigger not efficient (high reduction rate) anymore
- maintenance
  - zoo of hardware is hard to handle
  - decaying and obsolete components
  - does not scale easily (Trigger-Bus/Hub, MU)
    - how to integrate the RPC detector

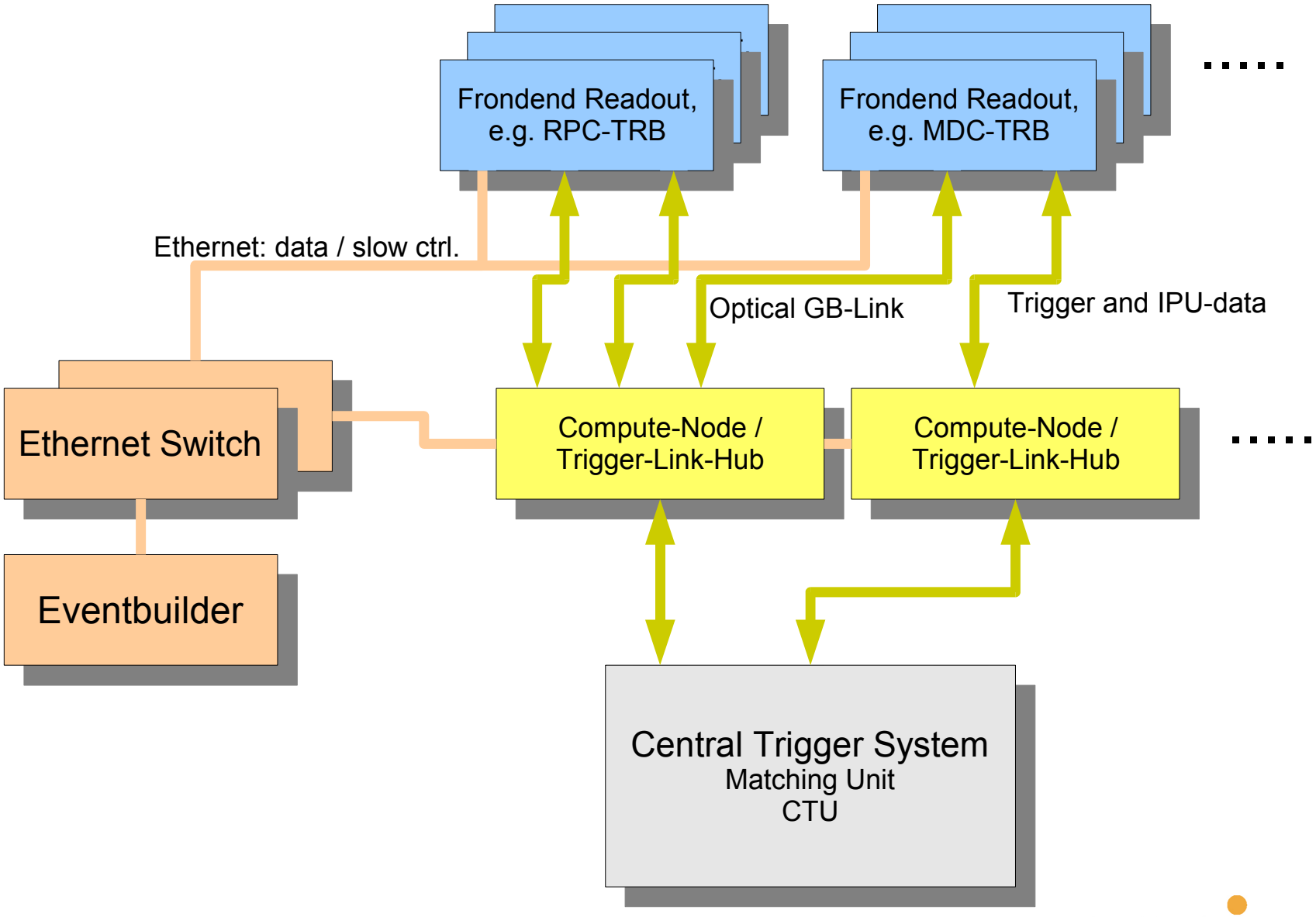
Mission Statement
List of Projects for DAQ upgrade

Objective: 20 kHz primary data rate to ensure measuring rare decays in heavy systems

MU	TOF	Common Readout	MDC	RICH	RPC
Matching Unit Concentrator	Replacement TOF readout-board	Replacement of old VME-CPUs	Higher bandwidth digital readout electronics	New analog amps for higher sensitivity / less noise	TDC-board with readout
Matching Unit Version 2	more powerful TOF-IPU	Parallel working Eventbuilders	Integration of track information to LVL2 trigger	Fast digital readout / more powerful IPU for lower fake-rate	IPU for RPC

FP6-HADES3
FP6-HADES1
not FP6 (BMBF)

Architecture of new DAQ



Projects: Boards and Software

- RPC-Readout: TRB V1 [done]
- ETRAX_DEV1 / HadCom [done]
- TRB V2 [layout finished]
- GP-Add-On [schematics]
- MDC Add-On [schematics]
- RICH-Add-On [will start soon?]
- MDC driver card [open topic]
- EventBuilder Software [work started]
- RICH-Ring-finder (higher reduc.) [work started]
- LVL2 Trigger Algorithm (Meta) [??]
- TrbNet (Trigger and IPU Net) [work started]
- MDC cluster search algo. [??]
- TOF-wall FEE (TOT) [FEE concept ready, ???]
- MU V2 [Basic functionality tested]
- ....

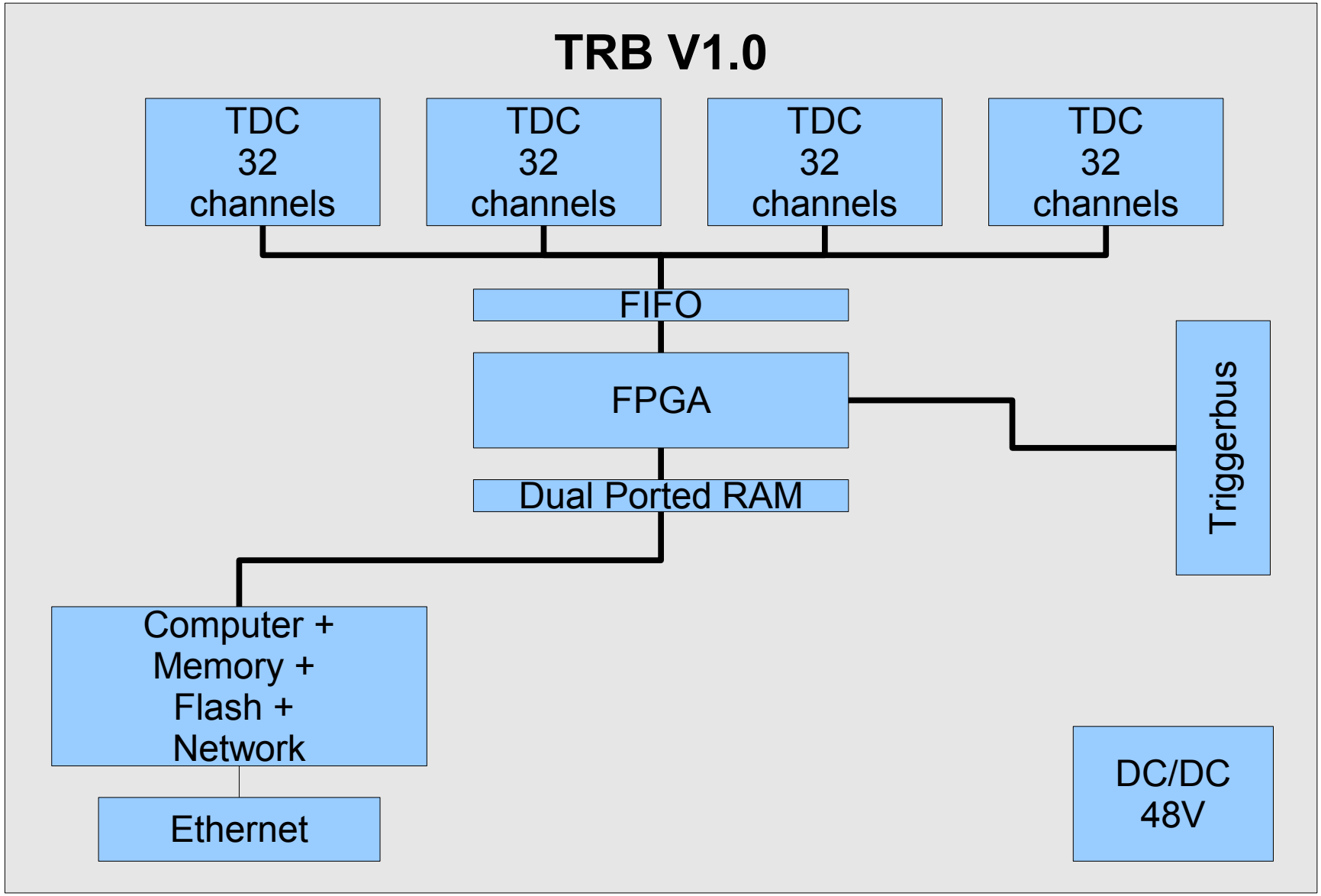
Involved People I

- Ingo Fröhlich
  - TRB-Network, TOF-Readout and IPU, Hardware-design
- Marek Pałka
  - TRB V1, DEV-Board (2 GBit/s Links), TRB V2 (FPGA for readout)
- Radek Trebacz
  - Programming of ETRAX-Processor and Co-Processor (DAQ-readout)
- Attilio Tarantola
  - MDC-readout and MDC-IPU
- Marcin Kajetanowicz
  - Hardware design and schematics

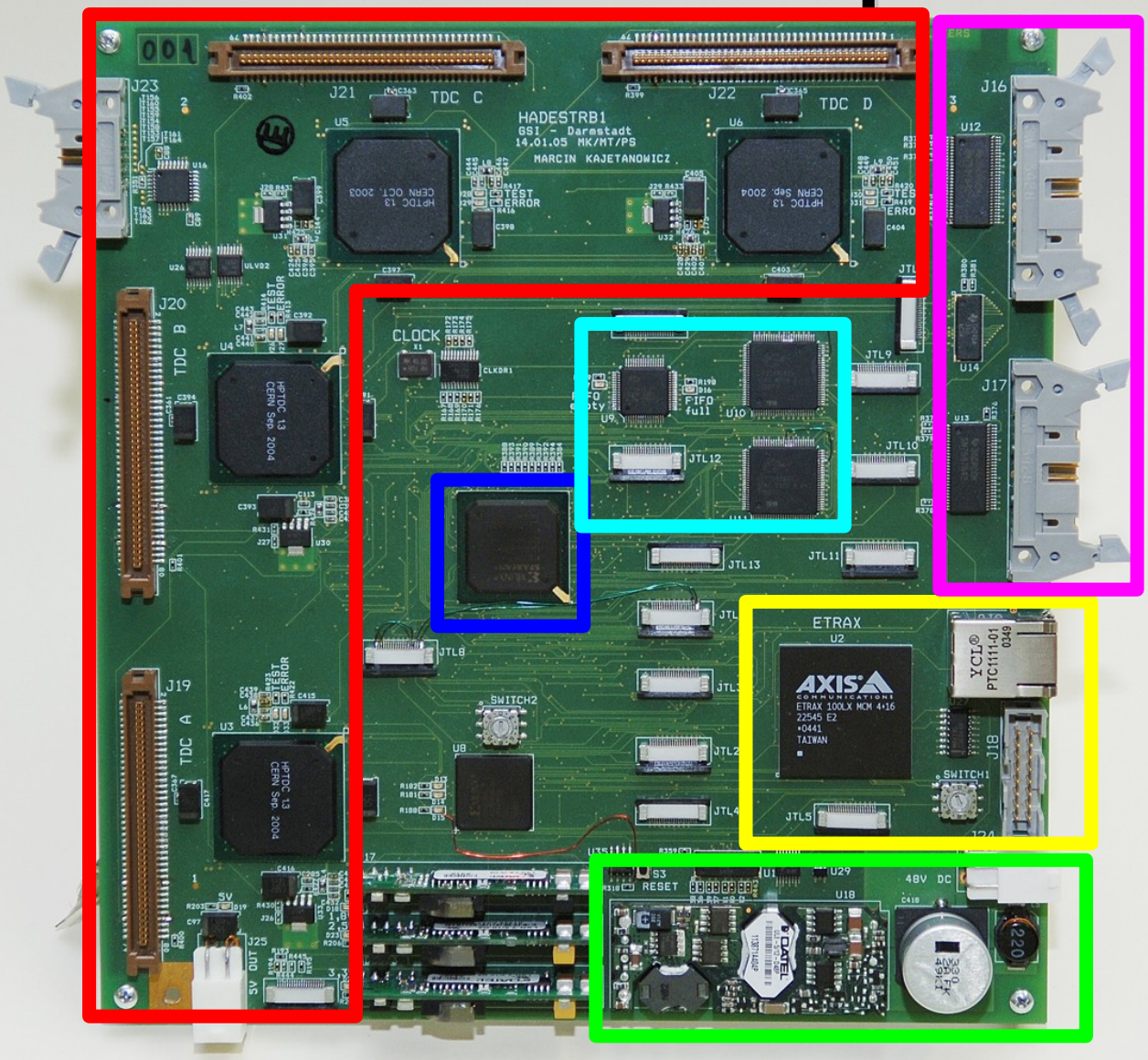
Involved People II

- Sergey Yurevich
  - DAQ-Software (EventBuilder upgrade)
  - RICH-IPU Algorithm, VHDL?
- Christoph Schrader
  - learning, TRB-Network, ...
- Michael Traxler
  - Hardware-Design, Coordination
- Michael Böhmer
  - RICH-Readout, IPU
- Peter Skott
  - Layout

Architecture TRB1, just readout



TRB Module and components

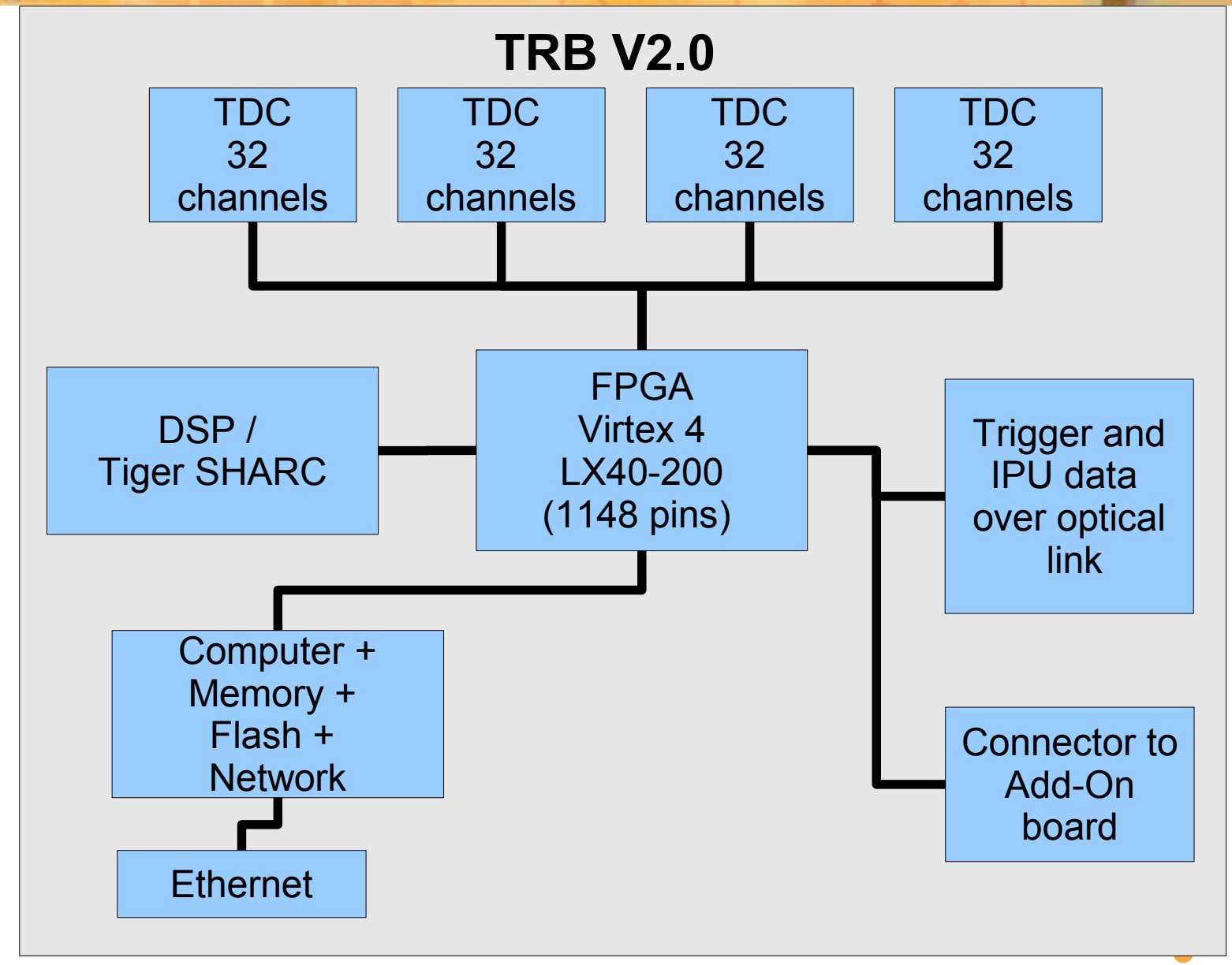


- 4*32 channels TDC, HPTDC
- 80 pin twisted pair cable, KEL connector
- Single Chip Computer with Ethernet
- FPGA
- DC/DC 48V, isolated
- Memory

Results for TRBv1

- **Performance:**
  - LVL1 readout of 60 TDC-words/event: 35kHz
  - LVL1 readout: only header and trailer: 80kHz
  - LVL2 readout of 60 words/event: 5-6kHz
  - LVL2 readout of empty events: 18-19kHz
  - all without DMA, no optimization in FPGA
- **TDC-Resolution**
  - sigma between 2 channels (4 TDCs): 38ps
  - no signs of crosstalk on TRB (has to be verified with more careful measurement)
  - RPC-detector channel resolution: 80ps

TRB V2 Block Diagram



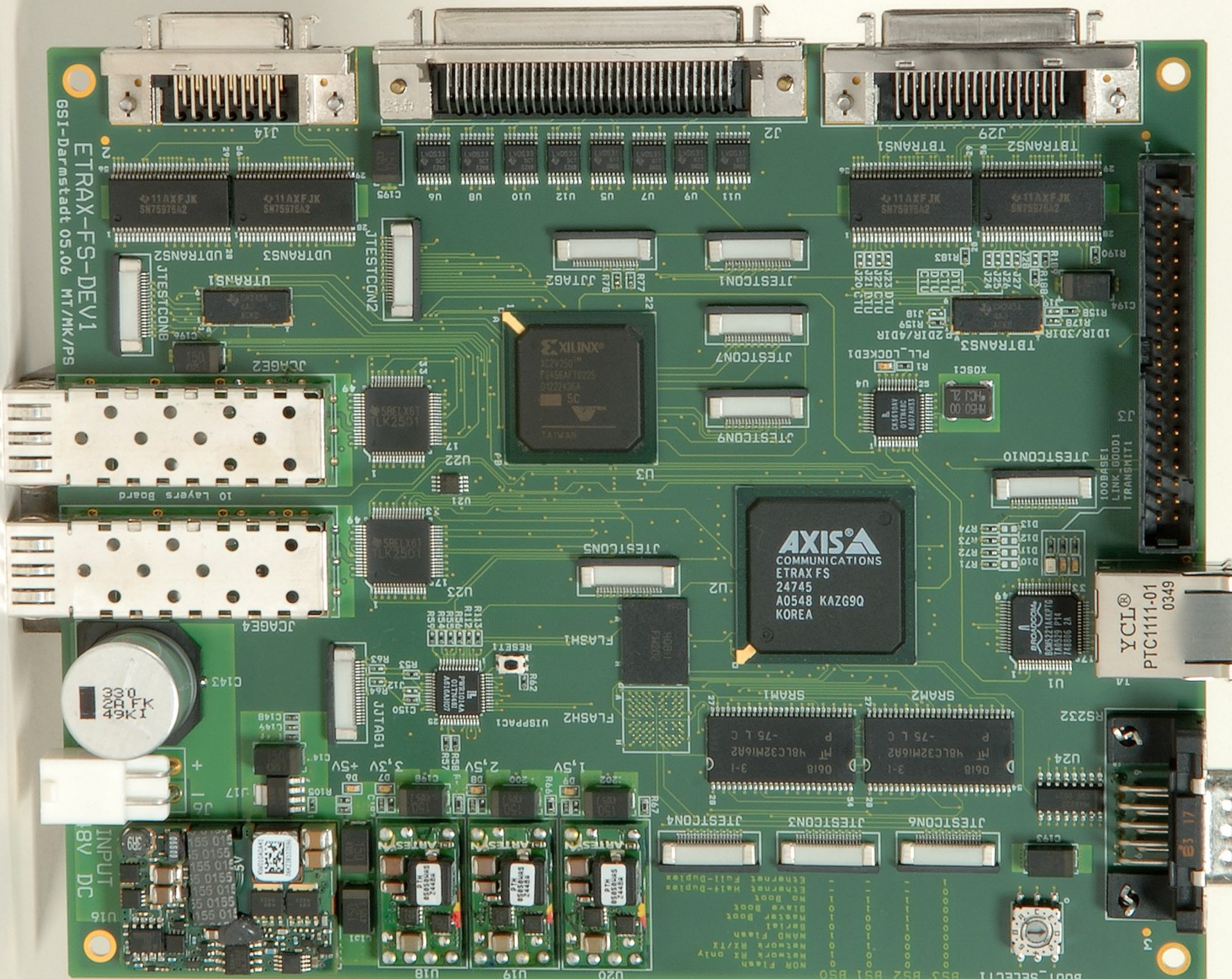
ETRAX_FS_DEV1 / HadCom on the way to TRBv2

Purpose:

- Validate ETRAX-FS (3 I/O-Co-Processors)
- Translate between old-Trigger-bus and new optical trigger-bus
- Connectivity to Concurrent-VME-CPU (Acromag)

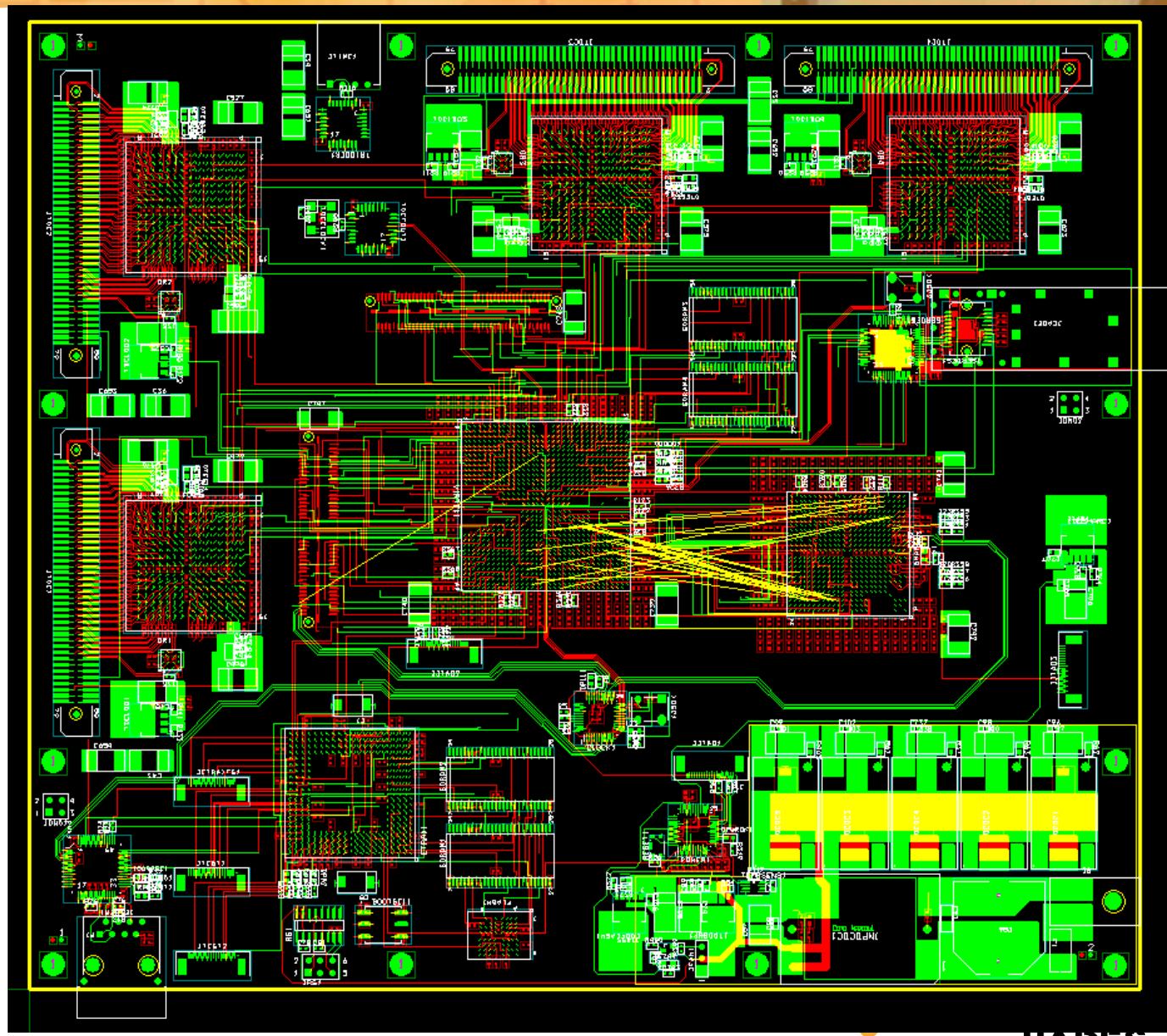
Status:

- 10 assembled boards available (5 with 2 flash-chips)
- Booting of Linux, Flash-Boot working now
- 2 times 2 Gbit/s Optical Links are working without errors for 3 days (50m cable, Marek)
- Driver / Code for Co-Processor worked on in Krakow and GSI (Radek and Attilio)
- ready for TRBv2

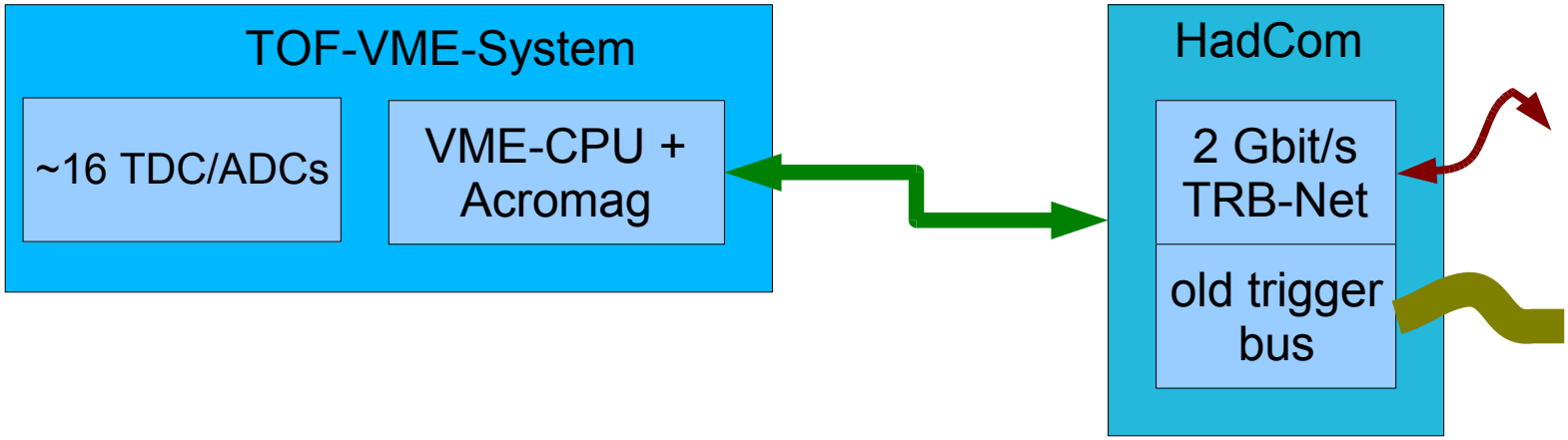

ETRAX-FS-DEV1
GSI-Darmstadt 05.06 MT/MK/PS
XILINX
AXIS
COMMUNICATIONS
ETRAX FS
24745
A0548 KAZG9Q
KOREA
YCL®
PTC1111-01
0349
330
2A FK
49KI
10 Layers Board
INPUT
8V DC

TRBv2, status

- schematics grown with experience of HadCom
- layout almost finished
- PCB available in mid-November
- Assembly finished: beg. December
- TRBv1 functionality: July 2007
- Full featured: beg. 2008



TOF readout / concept / status



Concurrent VME-CPU + Acromag PCI card + HadCom

- intermediate step: TOF-FEE could be TRB compatible
- Concurrent CPU + Acromag card: „hello world“
- HadCom: ready to be used
- VME-CPU can be upgraded easily
- Time estimate / priority ?

MDC-readout / TRBv2 Add-On Board / concept / status

Concept:

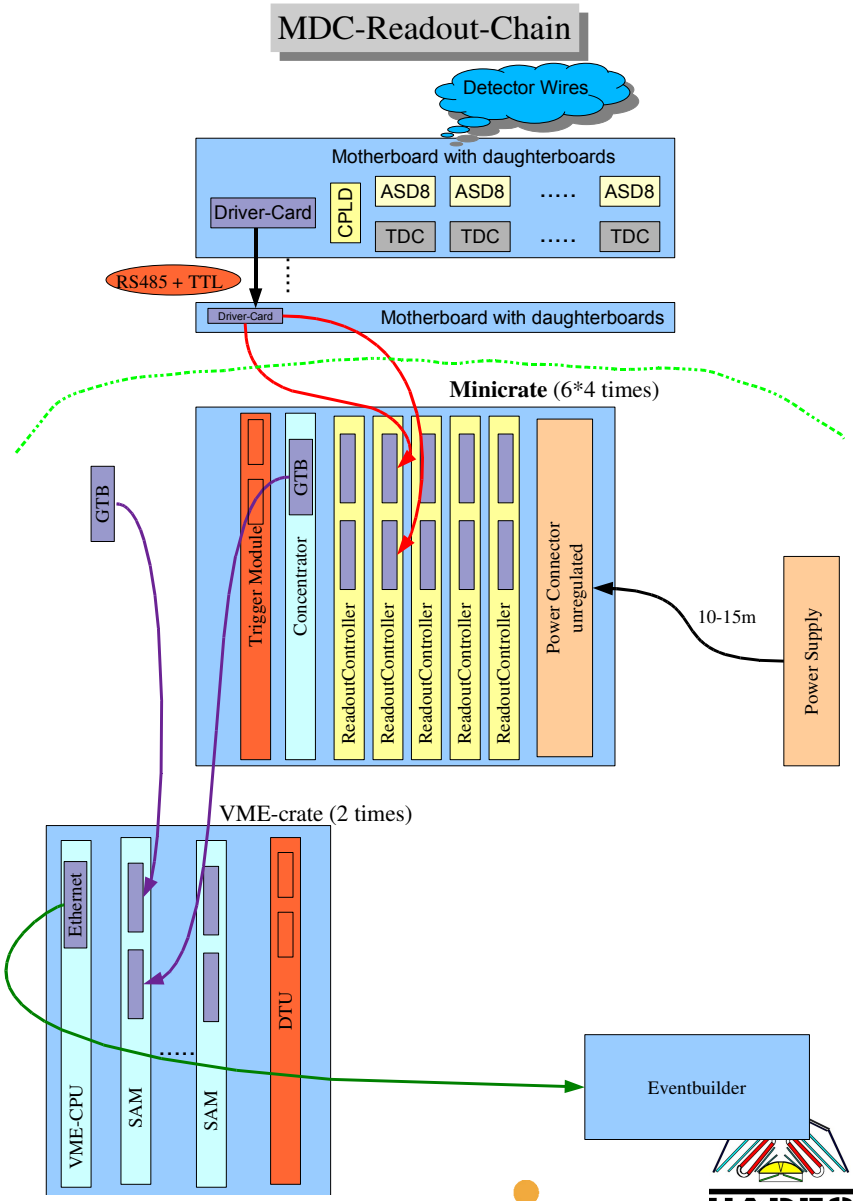
- Replacement of:
  - mini-VME-crate
    - RC, Concentrator, TriggerModule
  - readout VME-crate
    - DTU, SAMs, VME-CPU
- with: TRBv2 Add-On-board

Status: (Attilio)

- Schematics: 95%
- MDC-Test-Setup: not ready
- State-Machines (paper): done

Future:

- MDC-Driver Cards



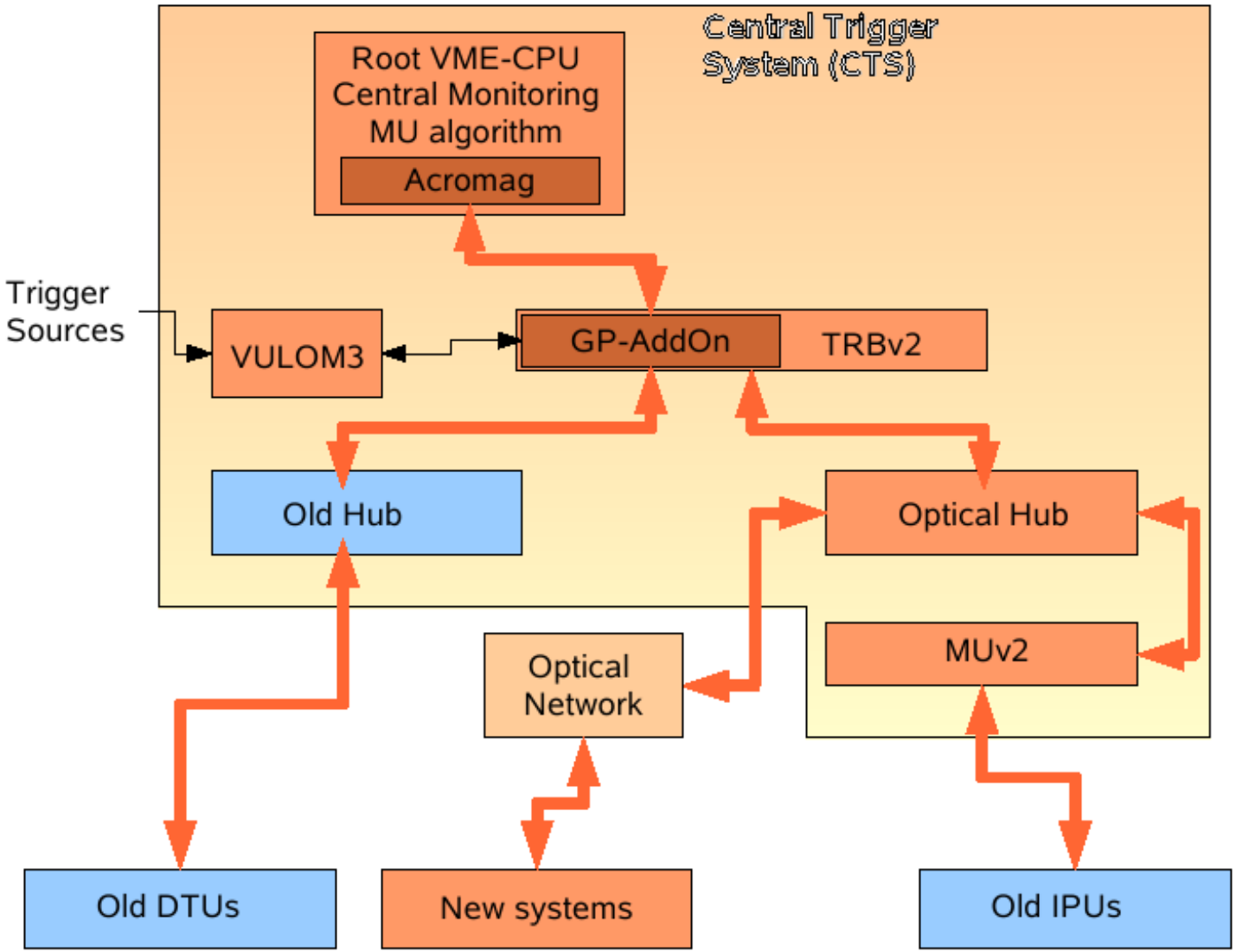
TRB-Net / Trigger-IPU-Network

- One common data and trigger transport „library“ for all subsystems
  - problems are solved only once for all systems
- Flexible Communication Protocol
  - Low latency for Trigger-Purposes
  - Stream mode for IPU data
  - 16 channels for sharing one medium
- Ingo
  - status / time-estimate / needed support
- Trigger-Hub
  - 10 (15) inputs / 1 output
  - FPGA-LatticeSC (16 times 3-Gbit/s-Serdes)
  - schematics will be started soon: Add-On to TRBv2 ?

Other boards / tasks

- General Purpose Add-On-board
  - Schematics finished
  - TRBv2 connection to Acromag + old TriggerBus (Hub)
- RICH Ring online finder: (Sergey)
  - surveying data, already ideas?
- RICH readout and RICH-IPU
  - TRB Add-On
  - Serial communication from RICH-FEE-backplanes to RICH-Readout
  - Michael B.
    - ideas / commitment / time estimate

Central Trigger System (CTS) in a "mixed mode"



Unsolved problems / no commitment

- Manpower for VULOM (VME-Universal-Logic-Module)?
- TOF-FEE (TOT-measurement): Any commitment?
  – the concept is similar to the Forward-Wall FEE
- MDC-cluster search online algorithm
  – occupancy in MDC for Au+Au ?
- LVL2 Trigger Algorithm in Meta
  – Matching Window optimization ?
  – occupancy in meta for Au+Au ?
- if LVL2 fails: LVL2 data rate must be high enough to take everything....
- things I forgot ....

EU-Contract / Money: Where we are now?

- Money spent (**invest**) by me on the account of others in 12 month (2005-10-01 till 2006-10-01):

53610 (DAQ)	**13,000**	**100,000**
53608 (RPC-LIP)	3,200	240,000
53608 (RPC-USC)	3,600	100,000
53608 (RPC-JU)	35,000	130,000
53608 (RPC-GSI)	4,500	80,000
Sum (RPC)	**46,300**	650,000

- cost estimate:
  - RPC: 30 times TRBv2: 30 x 1.6k€ + 2k€ offset = 50k€
  - Hubs: 10 x 700€ + 2000€ offset = 9k€
  - GP-Add-On: 5 x 400€ + 1000€ = 3k€
  - Accessories: = 10k€

Let's do things better...
Mission Statement

Things to learn from HADES-experiences:

- Don't allow a zoo of digital-hardware for every subsystem
- Think in modules rather than boards
  - team members work on modules not on boards
  - teams work together to get the whole system running rather than their board (who is guilty: MDC or RICH?)
- Data transport issues are at least 10 times more demanding / time-consuming than the algorithm to implement (maybe connected to the zoo of hardware)
- Think more about Low-Voltage Power-Distribution

more things?

Discussion

Time schedule