Proposal for a MDC-ToF Discriminator and Trigger Board

W. Koenig, January 14th 2007, Version 1.1

In order to include the inner MDC (Plane 2) in the trigger system, several boundary conditions have to be considered:

- Adjusting thresholds for MDC field wire signals needs monitoring of the analogue signals as well as easy to use remote threshold adjustment (Epics).
- Timing constraints for the 1st level trigger are tight. Signal delays have to be kept at a minimum.
- Sectorwise coincidence with ToF/Tofino needs to be implemented and monitoring of the relative timing under in beam conditions is necessary to adjust relative timing.
- Signal width has to be adjusted for proper signal overlap (MDC – ToF/Tofino). Time above threshold delivered by a leading edge discriminator does not allow for proper overlap coincidences.

In order to fulfil above constraints, a dedicated discriminator/Trigger board is proposed:

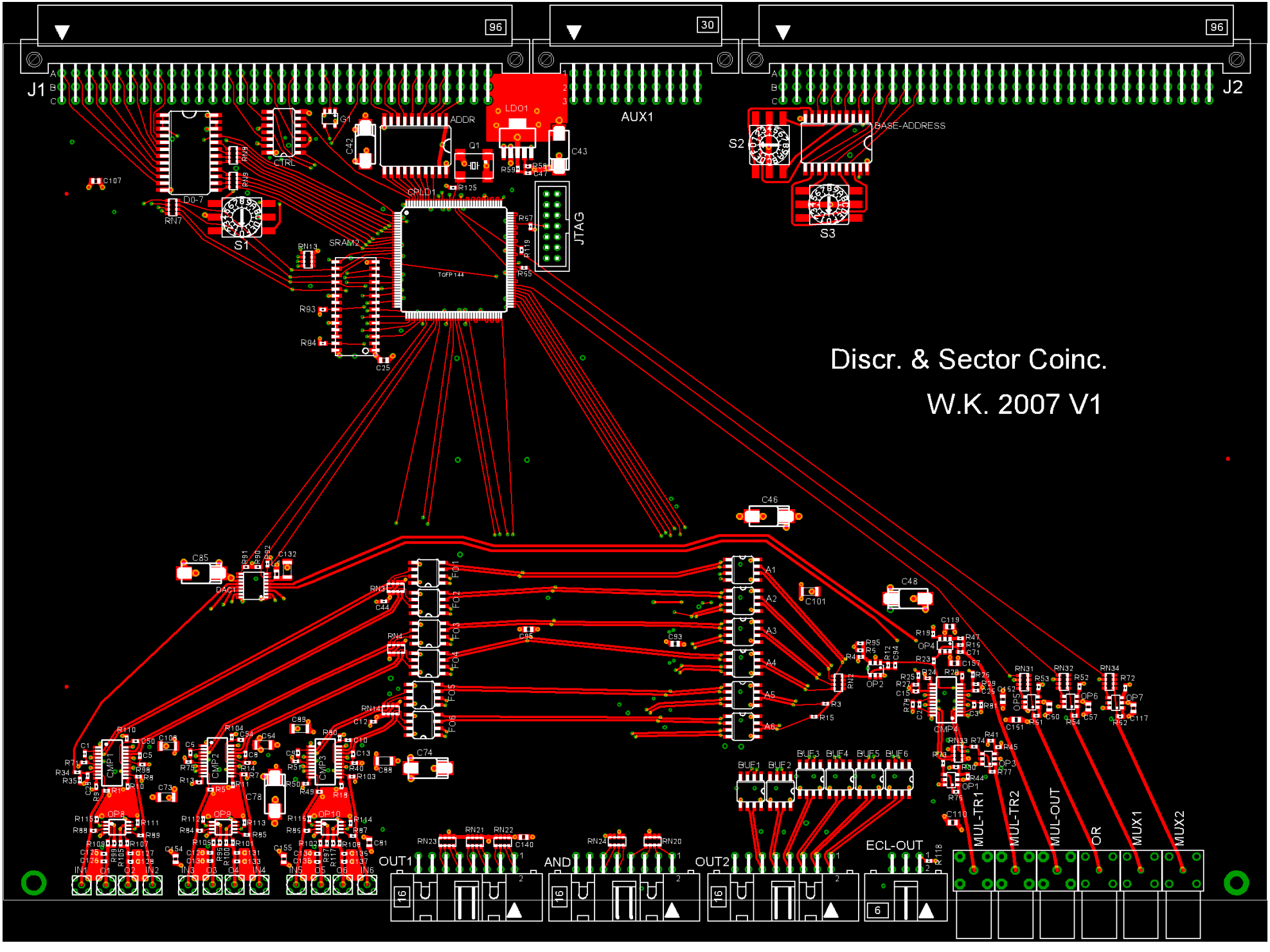
It features threshold control, signal monitoring and provides two sector multiplicity outputs..

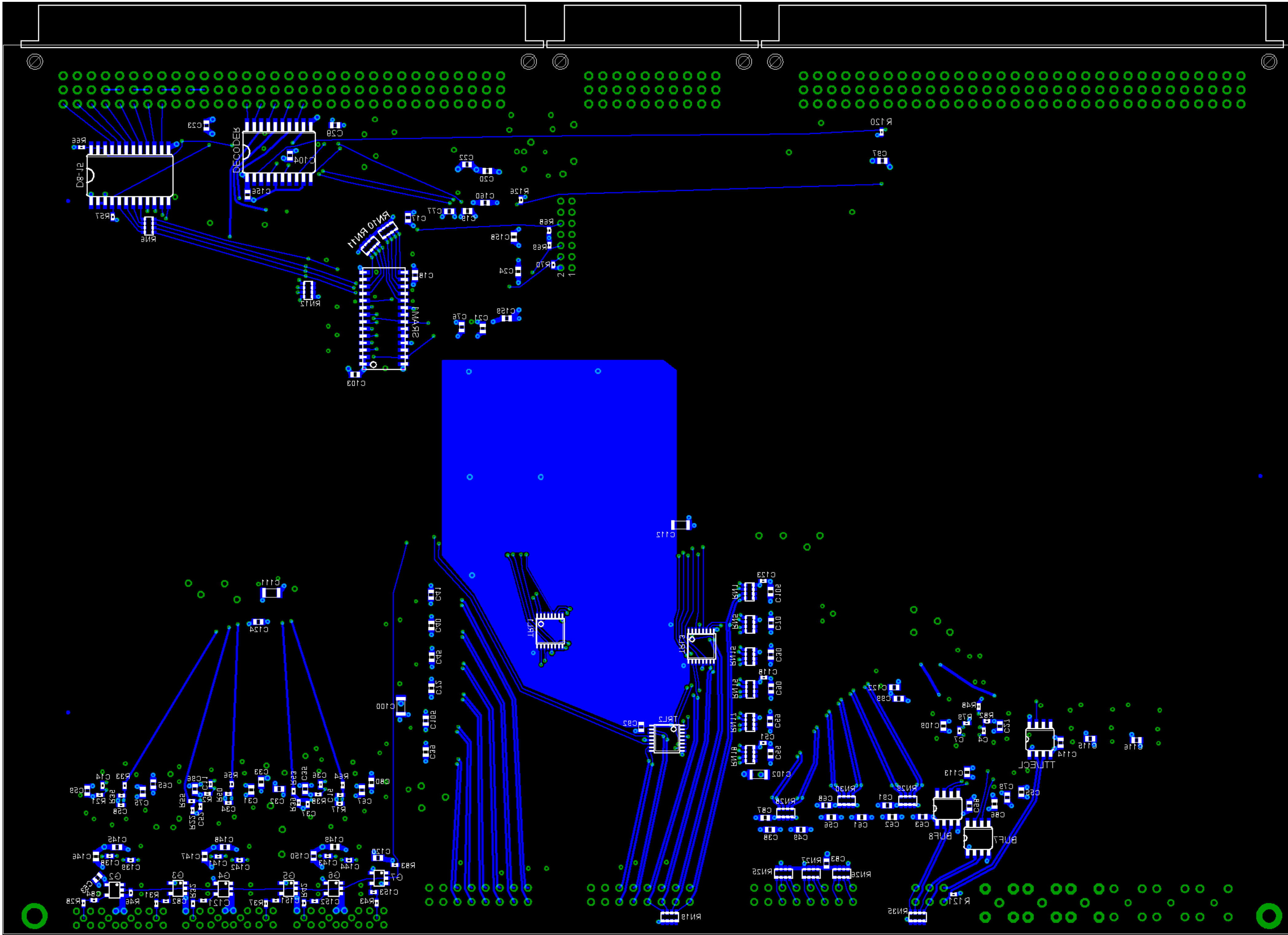
For minimized delay, the sectorwise MDC-ToF/Tofino coincidence is realized in hardware (ECL). In addition, signal processing and monitoring is provided by a (more flexible) CPLD. The board is based on existing components already used in a different context.

Concept:

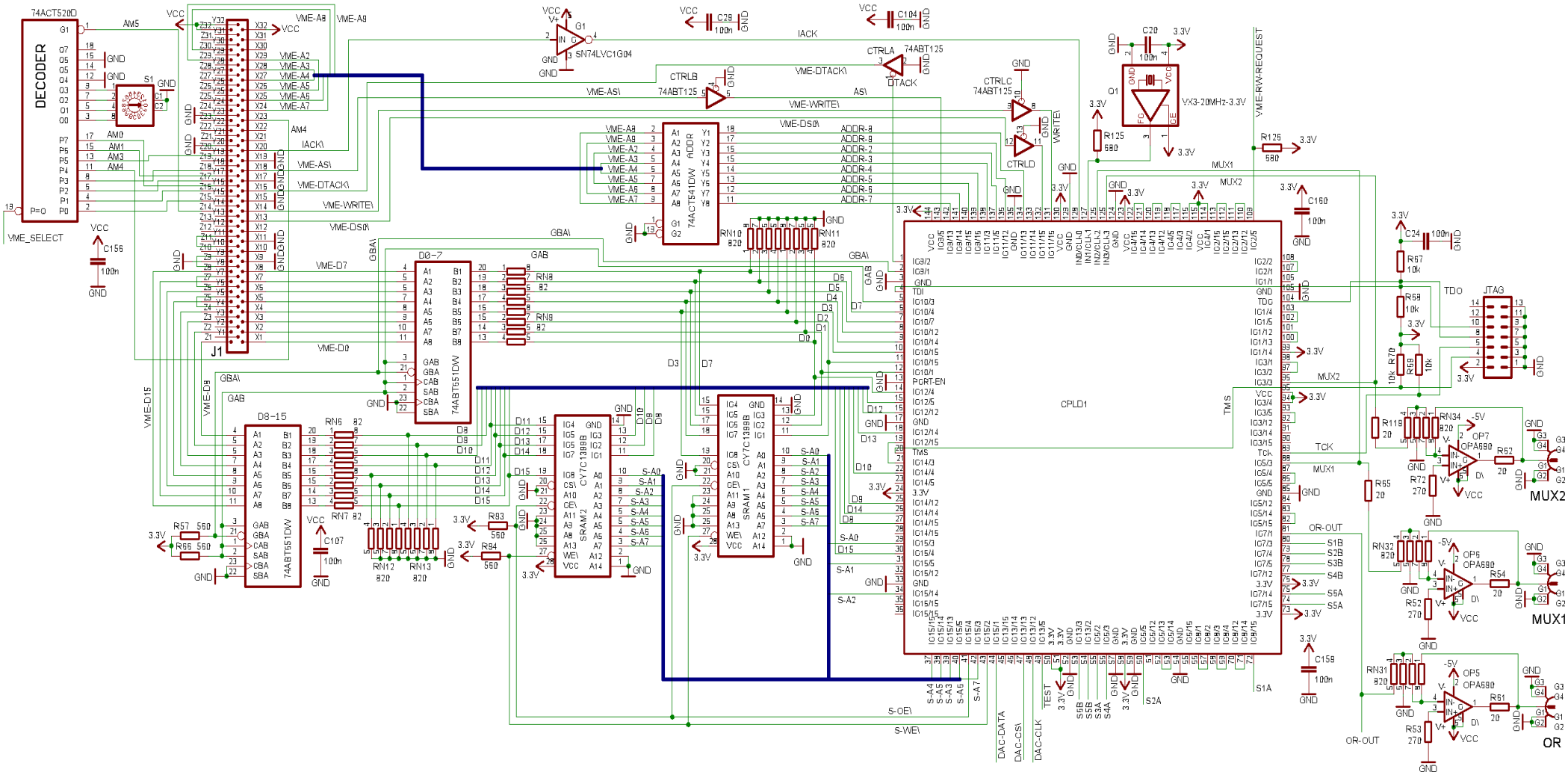
- The signals from the 6 layers of each plane are summed via analogue summing. This avoids individual discriminators (36/plane) as well as further discrimination of layer multiplicity (another discriminator). Analogue summing minimizes timing jitter by averaging over the signal arrival times of the 6 layers.
- The resulting 6 sector signals are fed into leading edge discriminators which provide a minimum signal width (100 ns).
- The analogue signals are in addition forwarded to analogue outputs via an Op-Amp which decouples input and output.
- The logic signals are combined sectorwise with the corresponding ToF/Tofino signals (AND). The resulting logic signals are fed into a multiplicity unit (0.3V/sector)
- Two discriminators allow to select sector multiplicity (e.g. M1 is an OR of all sectors).
- In addition the logic signals of MDC sectors as well as ToF/Tofino sectors are forwarded to a CPLD. It performs the following operations:
  - Two multiplexers allow to check any of the 12 inputs with respect to any other (timing, signal width, rate). Sectorwise and global MDC-ToF/Tofino coincidences can be monitored as well. In addition, the multiplexer outputs are connected to two internal scalers which can be read via Epics
  - A third output performs a logical AND between MDC and ToF/Tofino followed by an OR of all sectors. It allows for a programmable trigger signal using other logic as well. However, it has an additional delay as compared to the pure hardware solution.

Top View of the Discriminator/Trigger VME board





Schematics of the VME Interface and Slow Control Part

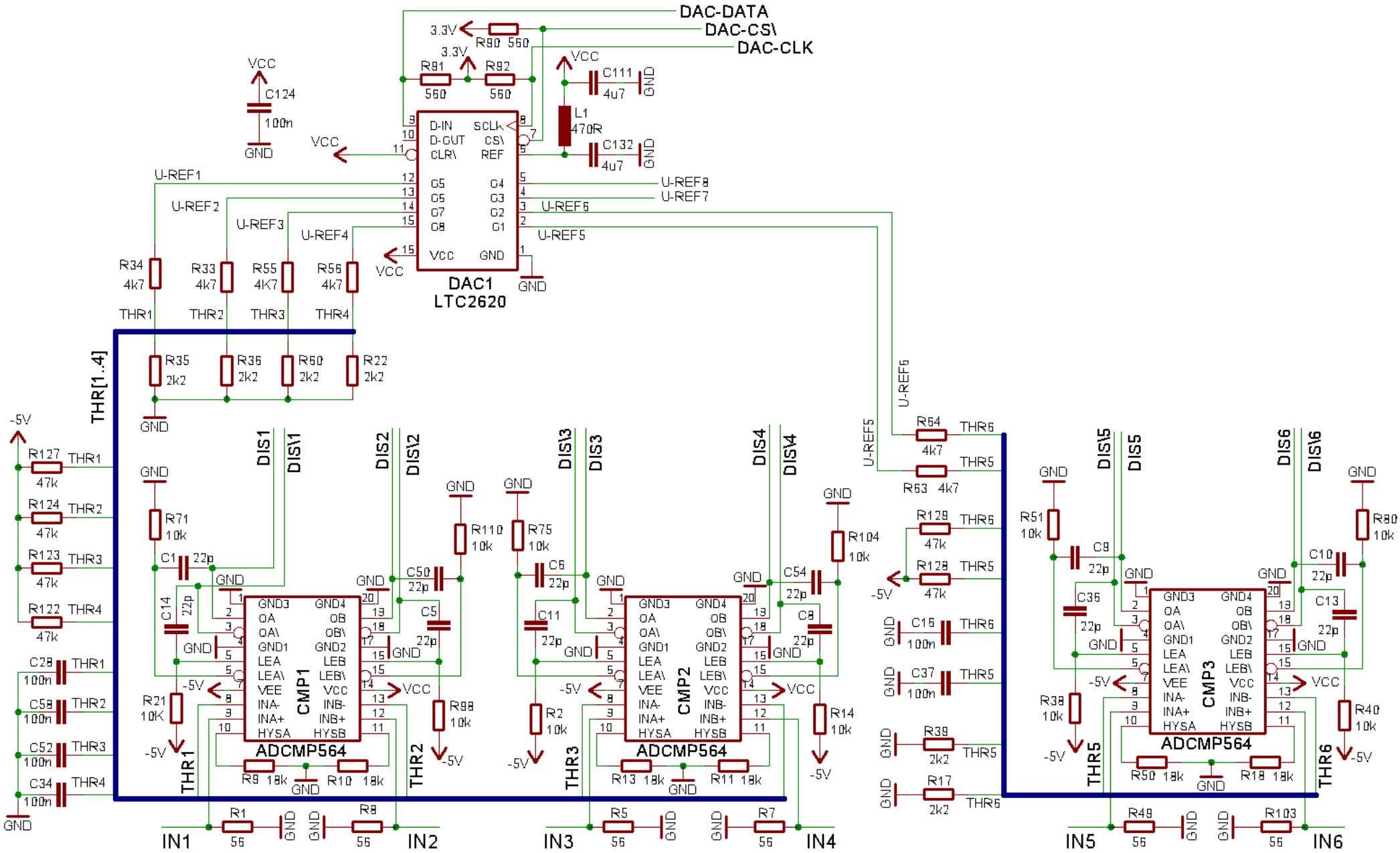


Left: VME IO connector, Address comparator and VME Transceiver.

Middle: 2*8 Bit SRAM for readback of thresholds, multiplexer and test-signal settings.

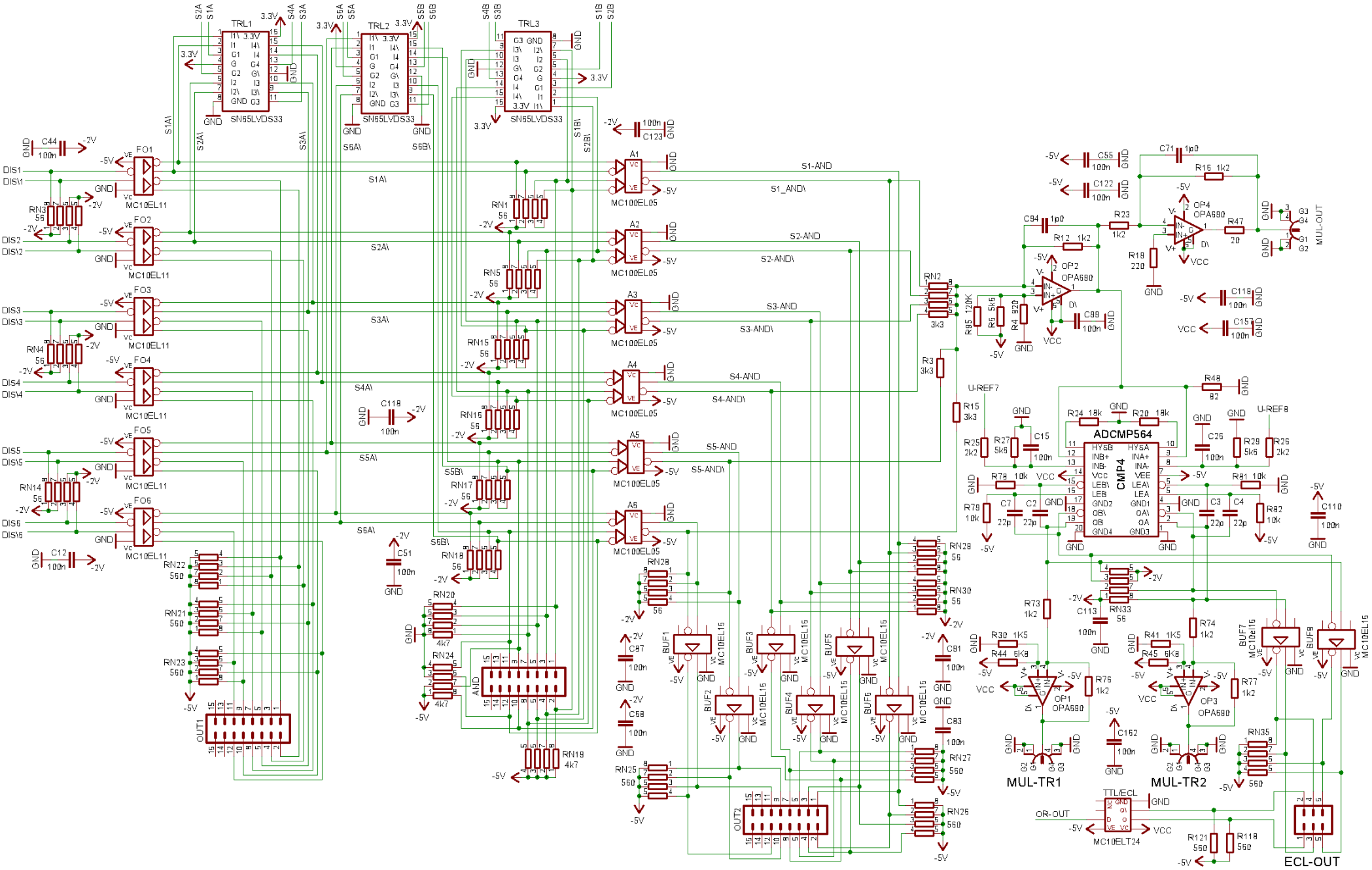
Right: CPLD (Xilinx XCR3128XL-7) and Multiplexer/Trigger output drivers.

Discriminators for MDC fieldwire signals (after analogue summing within one sector)



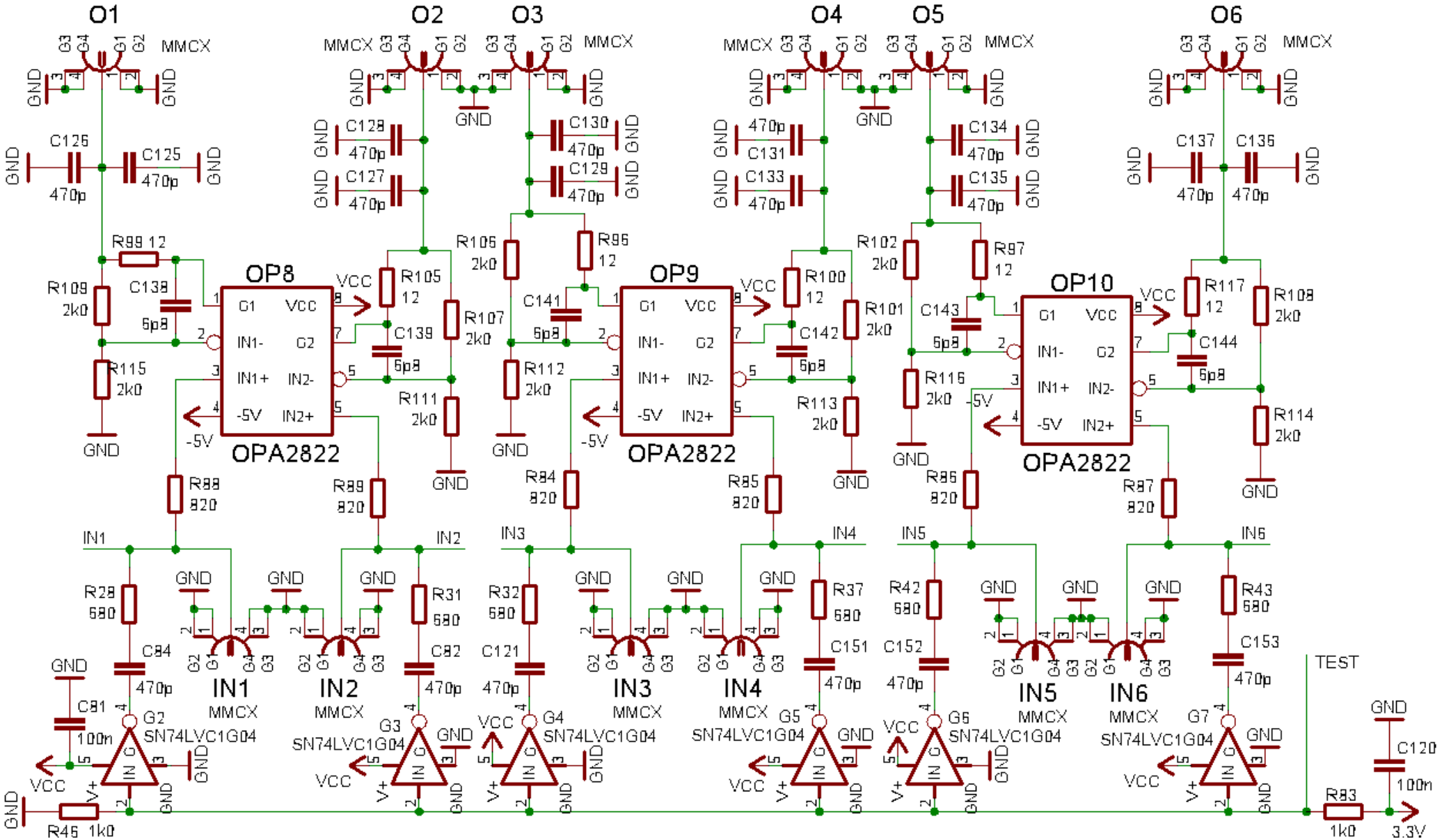
Upper part: 8 fold DAC for threshold control. **Lower part:** Discriminators with Latch

Schematics of the Trigger part (MDC - ToF/Tofino sectorwise coincidence)



Left: MDC Input and Output Buffers. **Middle:** ToF/Tofino input, AND with MDC and Output
Right: Multiplicity unit, multiplicity discriminators and output drivers. **Top:** CPLD interface

Analogue inputs and outputs, test signal distribution



Upper Part: Analogue outputs. **Middle Part:** Op-Amps driving analogue outputs.
Lower Part: Analogue inputs and test signal distribution.

Detailed Description: Multiplexer Output

Mux1: Address Hex 100

Data	Output
0	MDC Sector 1
1	MDC Sector 2
2	MDC Sector 3
3	MDC Sector 4
4	MDC Sector 5
5	MDC Sector 6
6	TOF Sector 1
7	TOF Sector 2
8	TOF Sector 3
9	TOF Sector 4
10	TOF Sector 5
11	TOF Sector 6
12	Sector OR (MDC and TOF) (fixed Width1 or Width2)
13	Sector OR (MDC)
14	Sector OR (TOF)
15	Test Pulse

Mux2: Address Hex 180

Data	Output
0	MDC Sector 1
1	MDC Sector 2
2	MDC Sector 3
3	MDC Sector 4
4	MDC Sector 5
5	MDC Sector 6
6	TOF Sector 1
7	TOF Sector 2
8	TOF Sector 3
9	TOF Sector 4
10	TOF Sector 5
11	TOF Sector 6
12	Sector OR (MDC and TOF) (overlap coincidence)
13	Sector 1 (MDC and TOF)
14	Sector 2 (MDC and TOF)
15	Sector 3 (MDC and TOF)
16	Sector 4 (MDC and TOF)
17	Sector 5 (MDC and TOF)
18	Sector 6 (MDC and TOF)

Detailed Description: Setting Thresholds

MDC Sector	Address	Data	Value
1	010	0 - 4096	-0.15V - +1.4V
2	014	0 - 4096	-0.15V - +1.4V
3	018	0 - 4096	-0.15V - +1.4V
4	01C	0 - 4096	-0.15V - +1.4V
5	000	0 - 4096	-0.15V - +1.4V
6	004	0 - 4096	-0.15V - +1.4V
Multiplicity	**Address**	**Data**	**Value**
MUL-TRIG1	008	0 - 4096	-0.5V - +3.0V (app. 300 mV/sector)
MUL-TRIG2	00C	0 - 4096	-0.5V - +3.0V (app. 300 mV/sector)

Detailed Description: Test Pulse, Scaler Readout

Test Pulse: VME Address Hex 200

Data	Frequency
0	Off
1	10MHz
2	5 MHz
3	2.5 MHz
4	1.25 MHz
5	625 kHz
6	312.5 kHz
7	156.25 kHz
8	78.125 kHz
9	39.0625 kHz
10	19.531 kHz
11	9.7656 kHz
12	4.8828 kHz
13	2.4414 kHz
14	1.2207 kHz
15	610.35 Hz

Scaler readout:

Scalers count multiplexer outputs 1 and 2

Select prescaling: VME Address Hex 20

Data	Prescaling Factor
0	32
1	2

Clear Scaler: VME Address Hex 4x, Write

Read Scaler: VME Address Hex 40/44, Read

Scaler 1: Address Hex 40

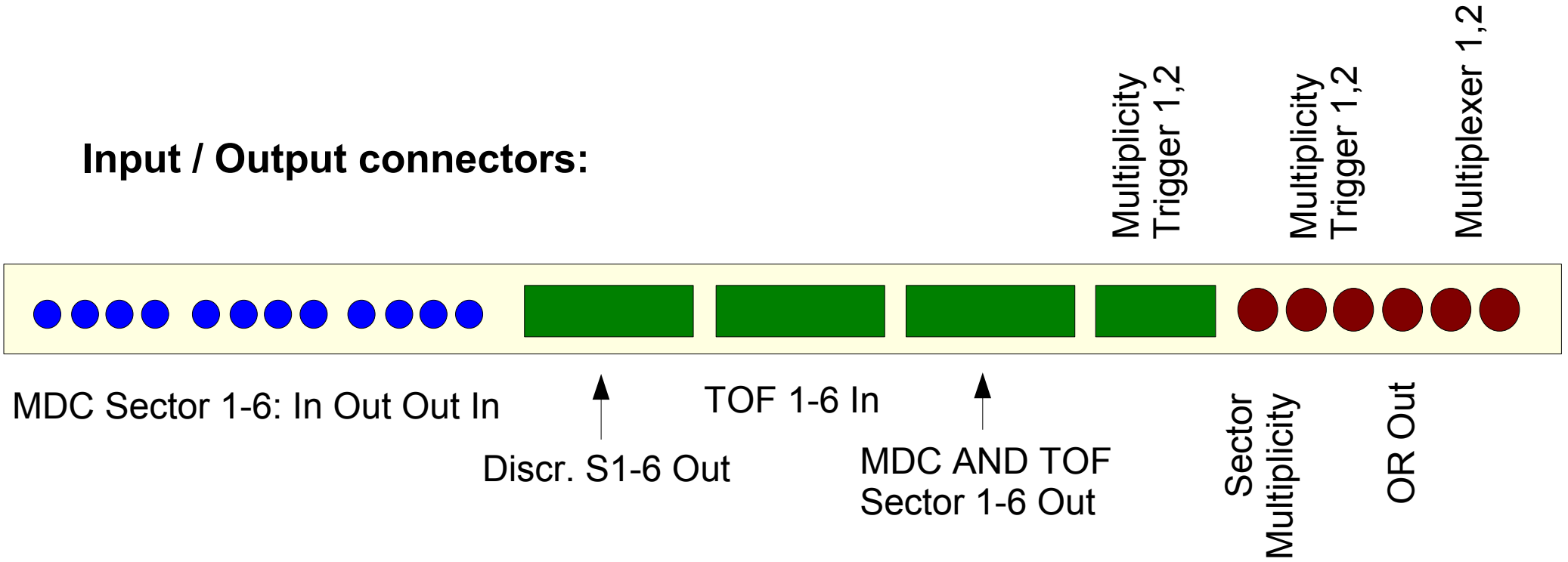
Scaler 2: Address Hex 44

(counting is inhibited during a read cycle)

Pulse width of Trigger Output (Sector OR, sectorwise MDC/TOF AND)

Address: Hex 30	
Data	**Output Width**
0	long
1	short

Input / Output connectors:



Blue: MMCX connectors, **Green:** ECL Twisted Pair connectors, **Red:** Lemo connectors (NIM)