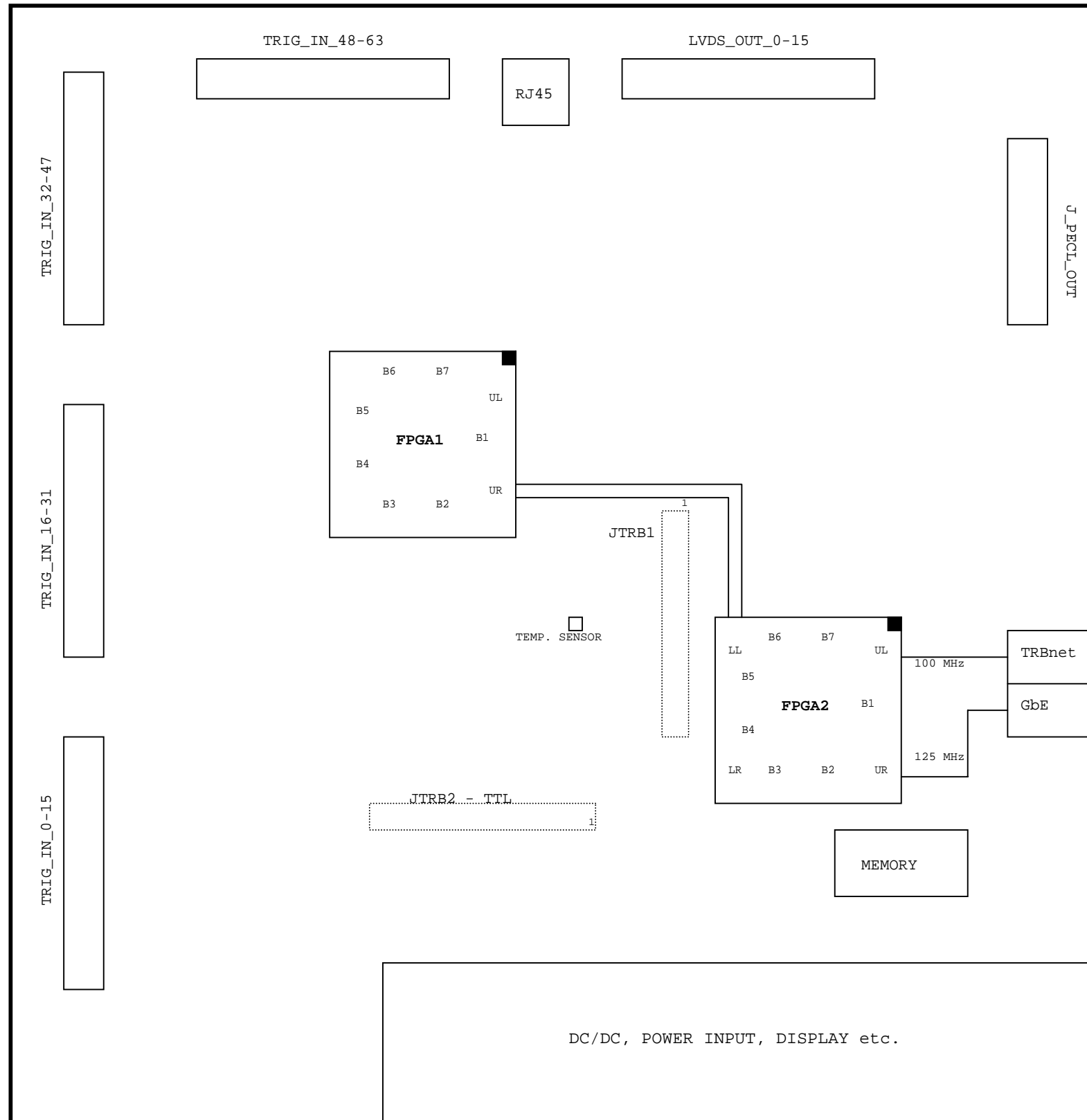
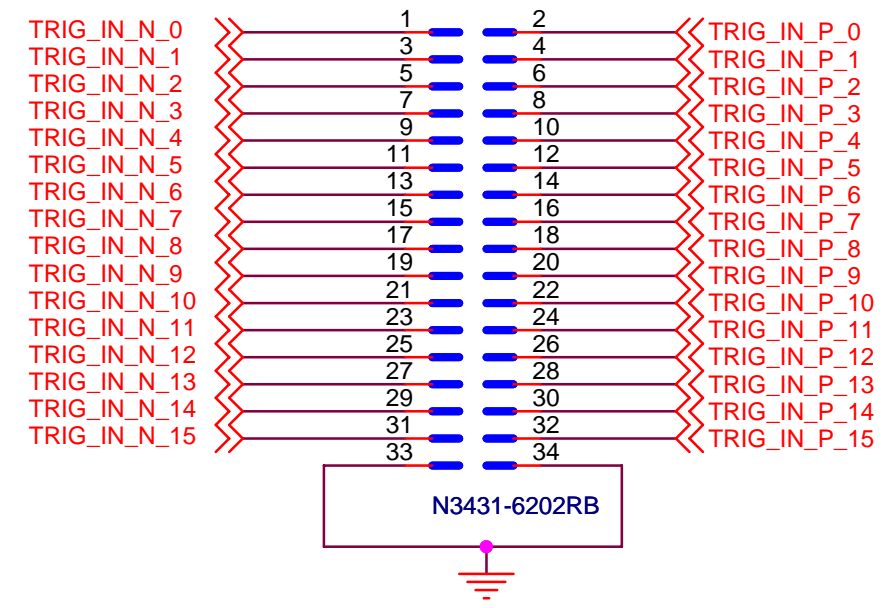


TOP VIEW (COMPONENT SIDE) (on PCB design most likely bottom view...)

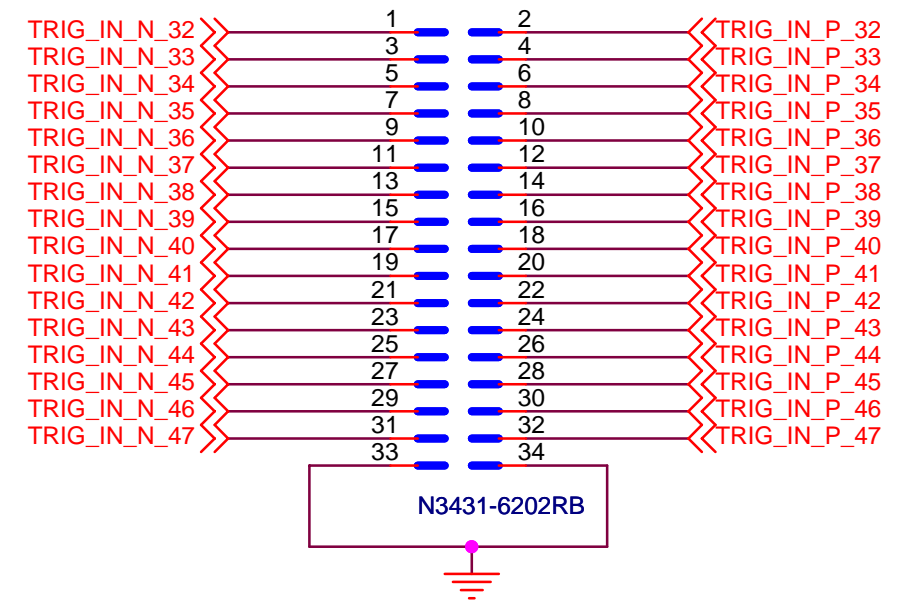


Title			00_LAYOUT		
Size	Document Number	Rev			
A3	<Doc>	<RevC>			
Date:	Monday, April 19, 2010	Sheet	1	of	16

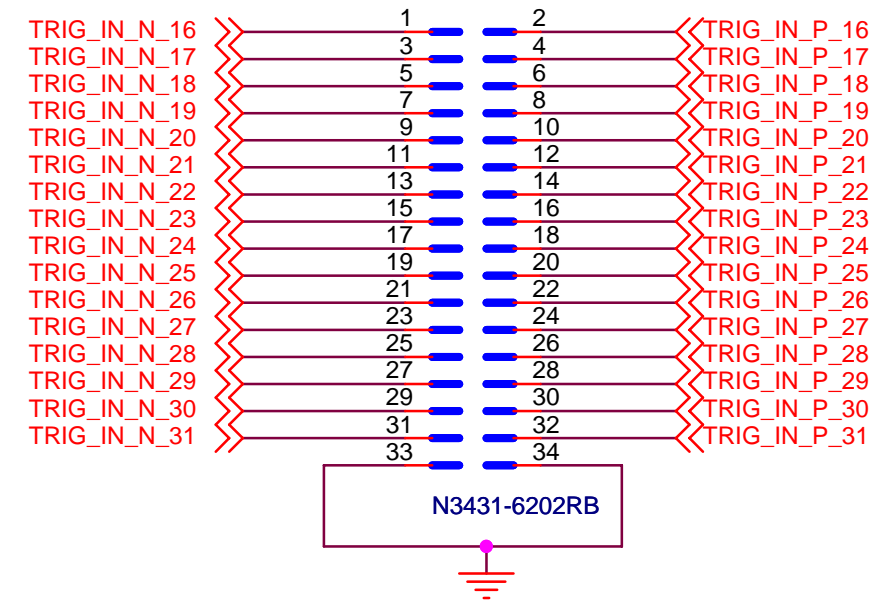
JTRIGGER1



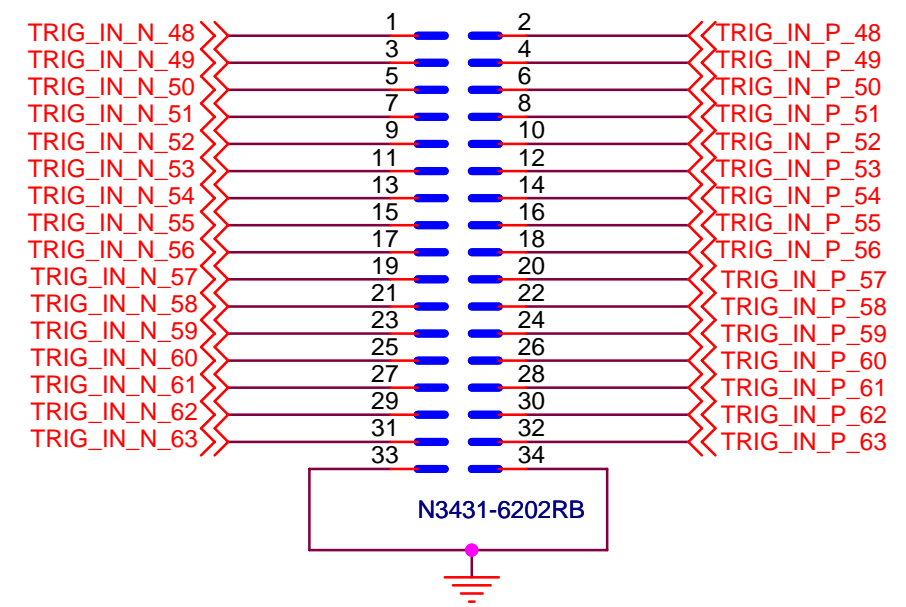
JTRIGGER3



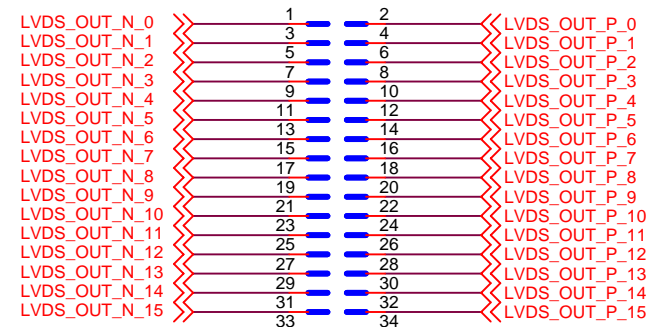
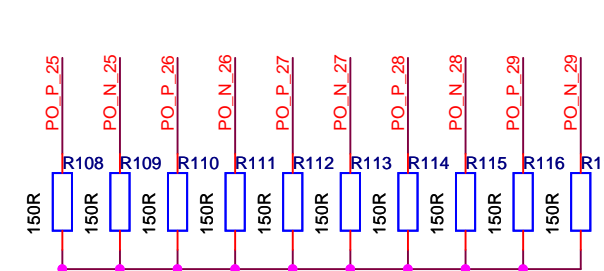
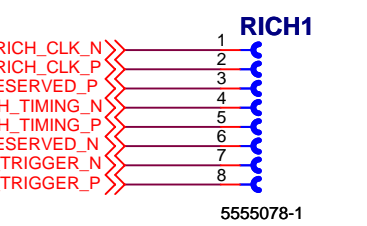
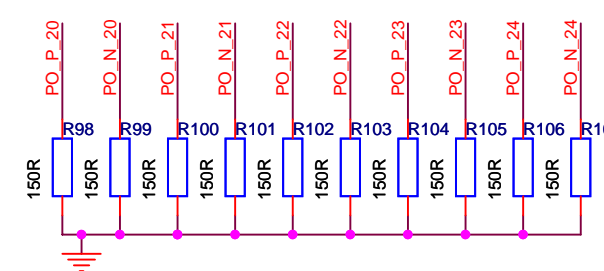
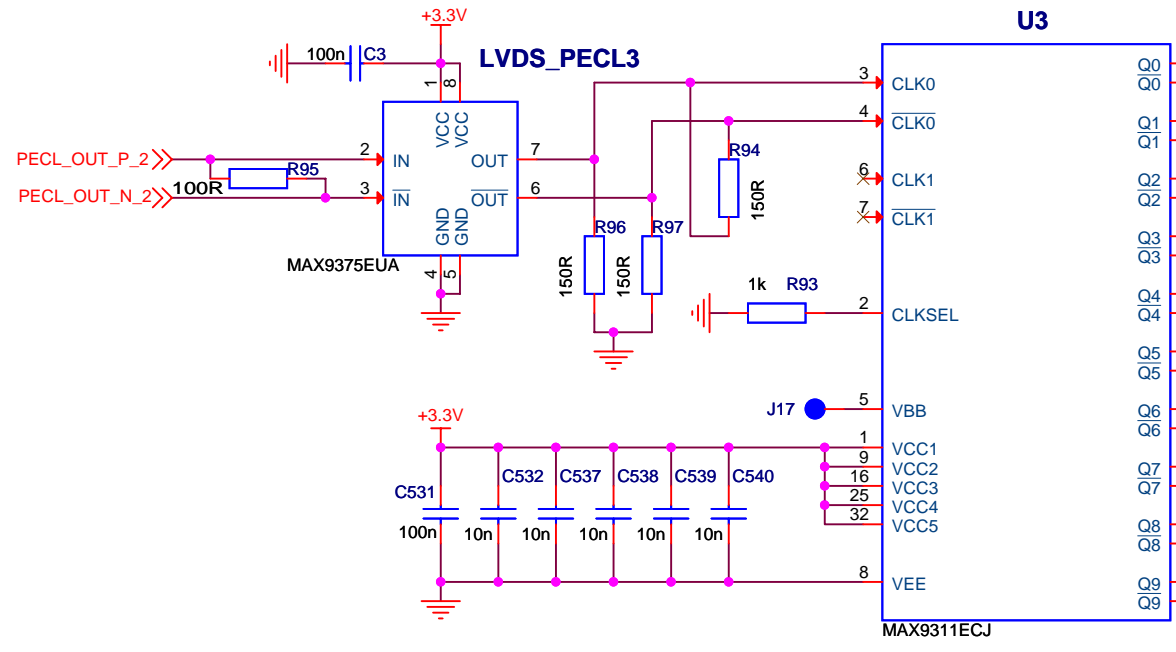
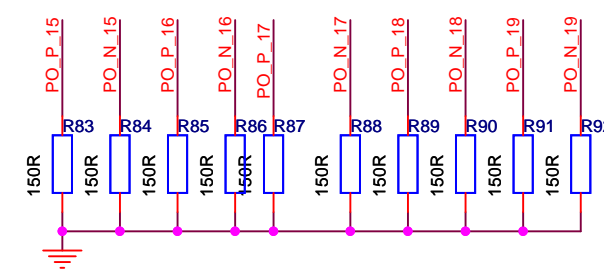
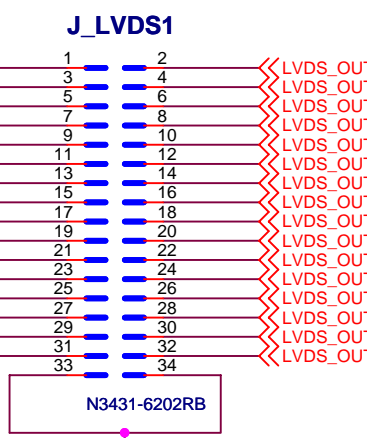
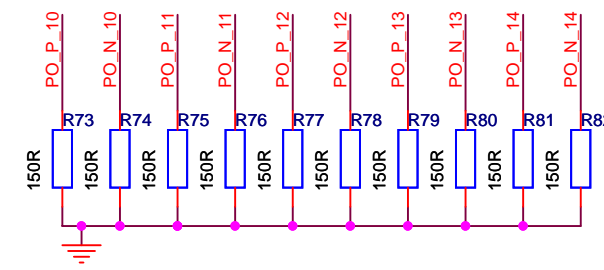
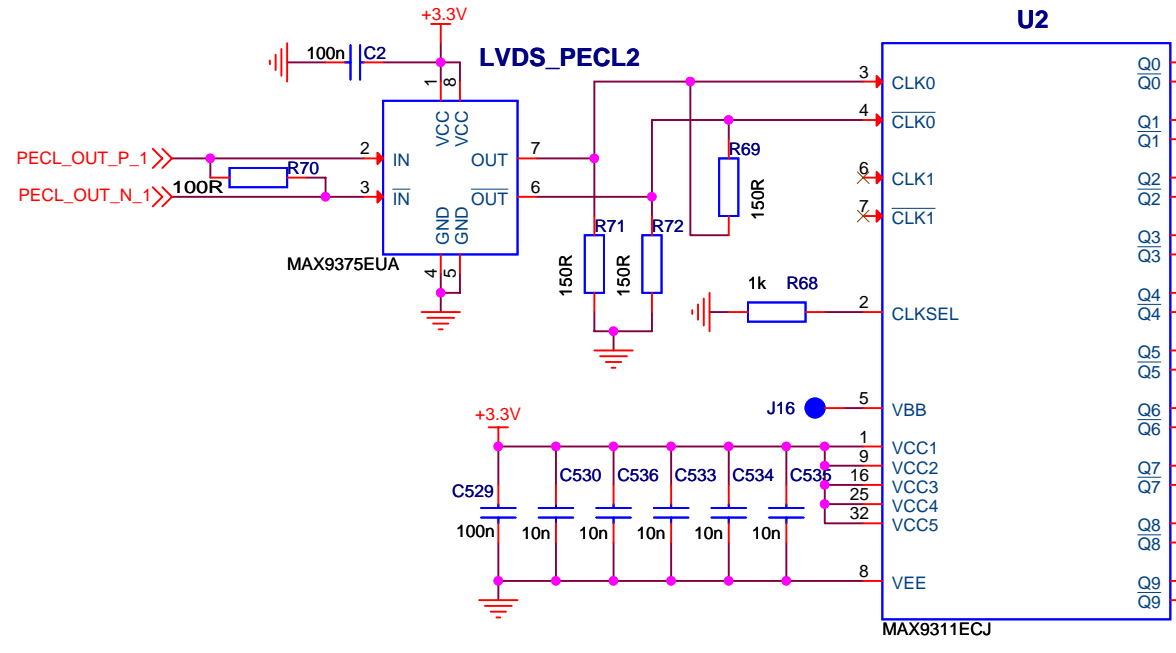
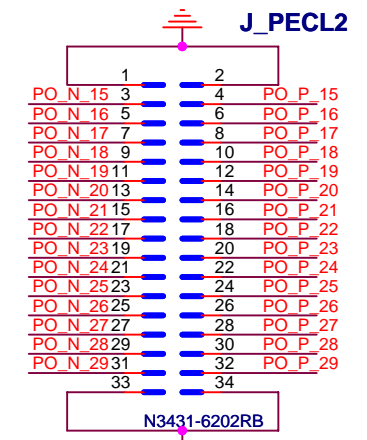
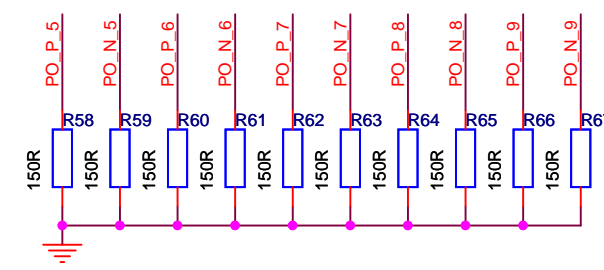
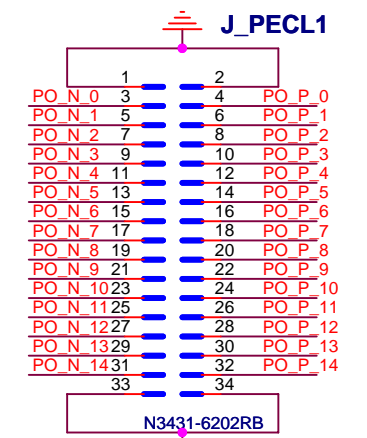
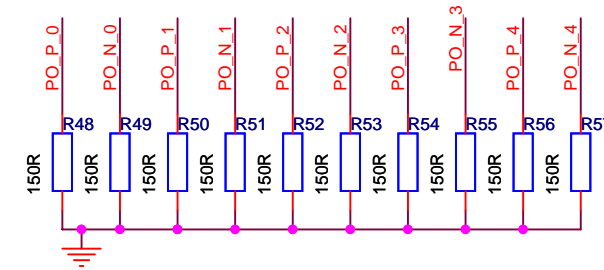
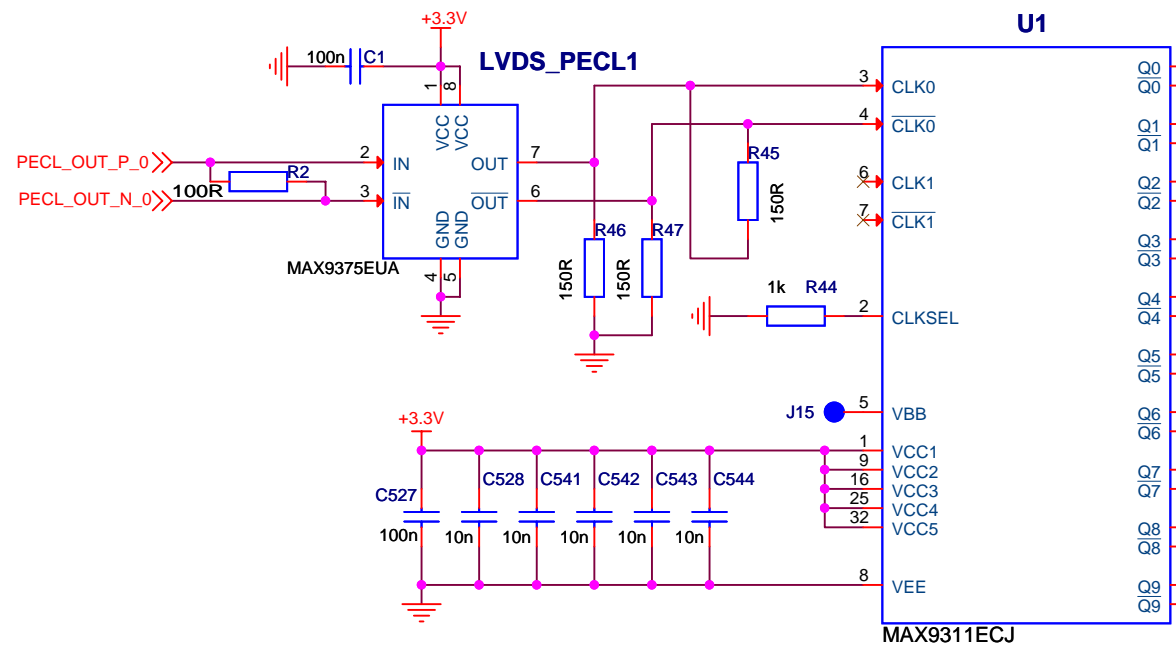
JTRIGGER2



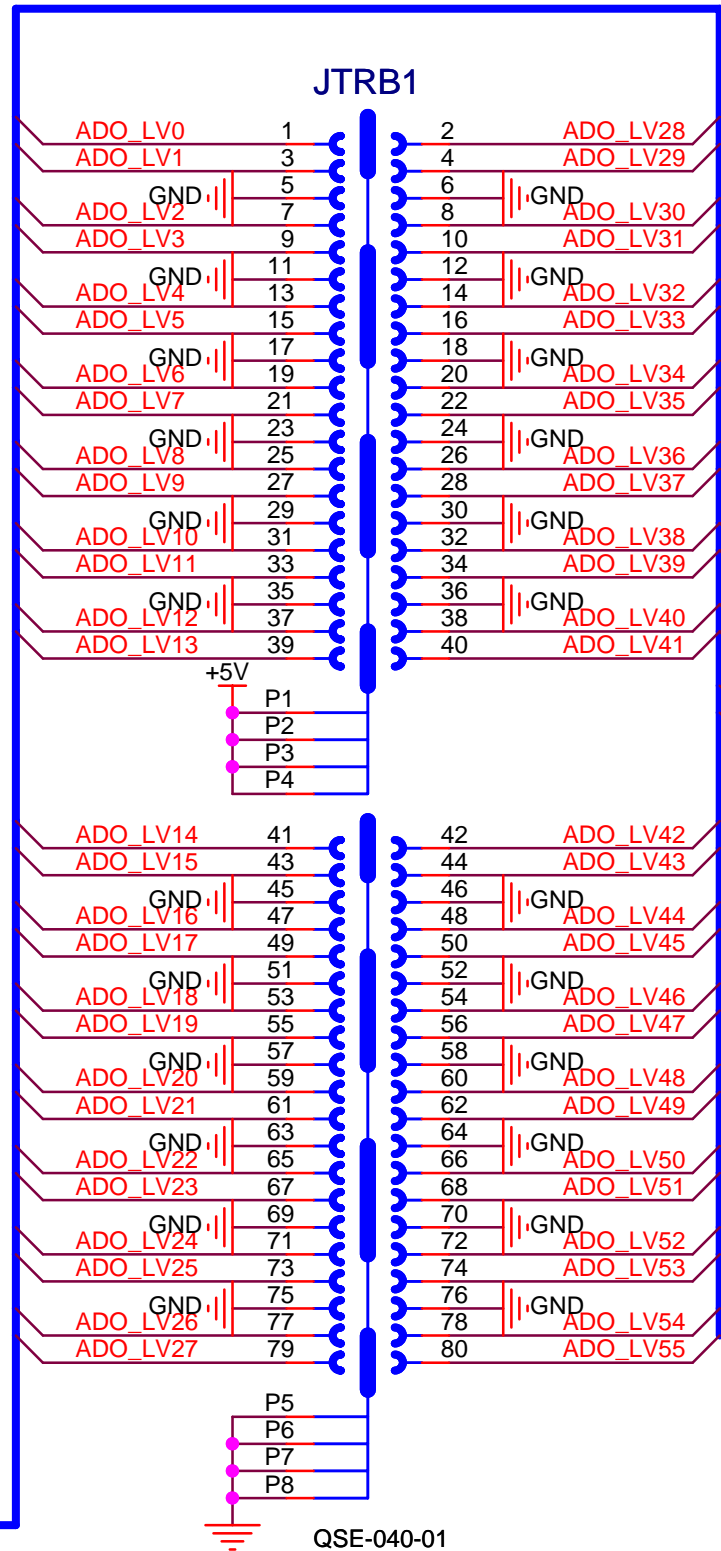
JTRIGGER4



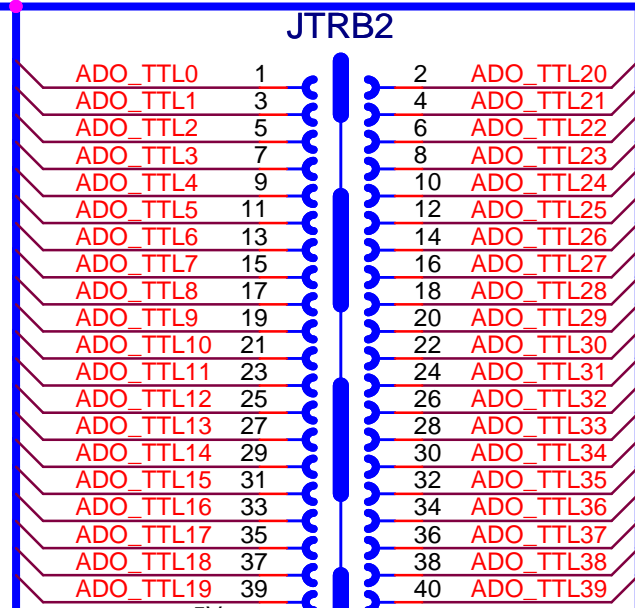
Title			01_INPUTS		
Size	Document Number	Rev			
A4	<Doc>	<RevCo			
Date:	Monday, April 19, 2010	Sheet	2	of	16



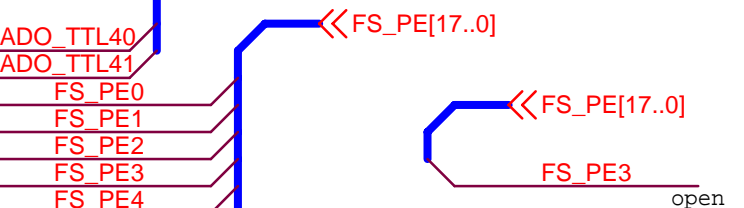
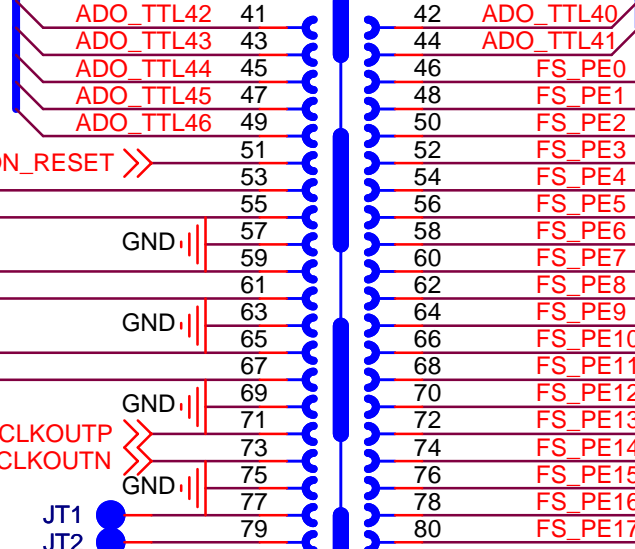
Even numbers: positive
 Odd numbers: negative



ADO_TTL[46..0]



JTAG interface:
 (seen from TRB)
 TDI - TDO from FPGA on TRB (FS_PE0 high Z)
 TMS - FS_PE1
 TCK - FS_PE2
 TDO - FS_PE4



goes to FPGA
 global clock input

ADO_CLKOUTP
 ADO_CLKOUTN

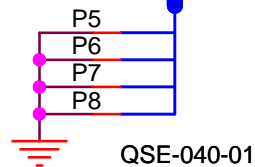


FS_PE16 (SCL) and FS_PE17 (SDA)
 used to control ispPAC-POWER chip

FS_PE12 - FS_PE15 connected to
 IN1 - IN4 in ispPAC-POWER chip
 general purpose inputs

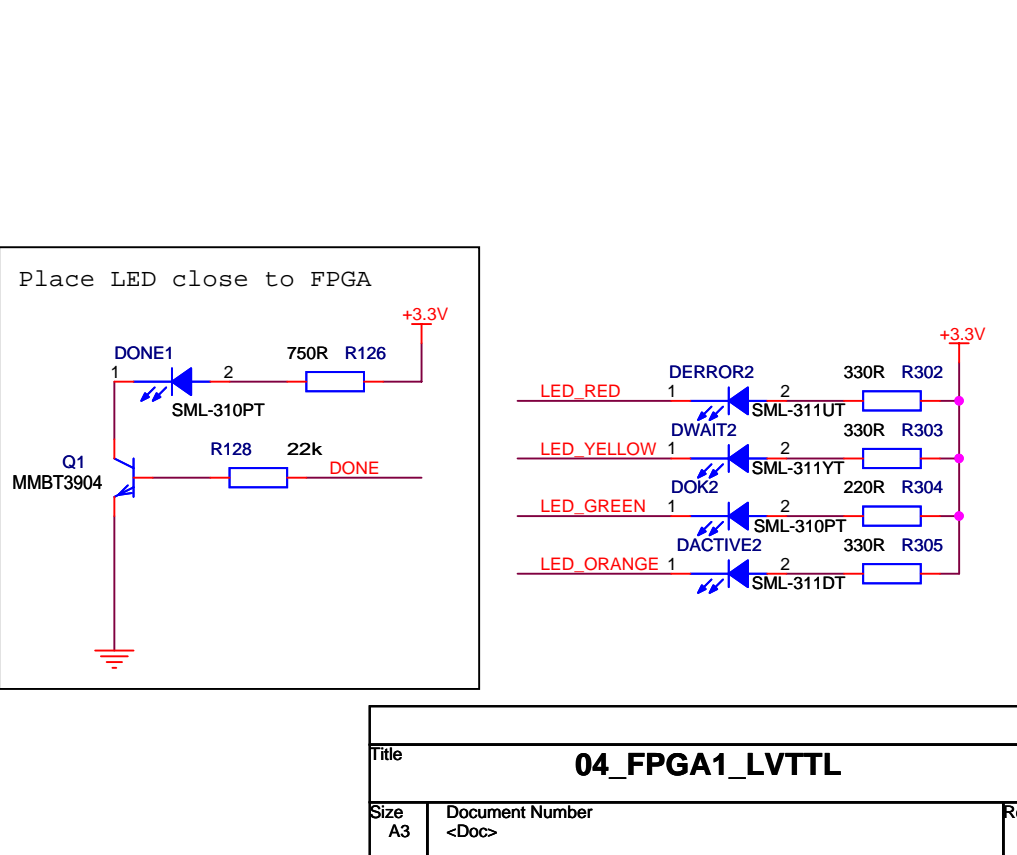
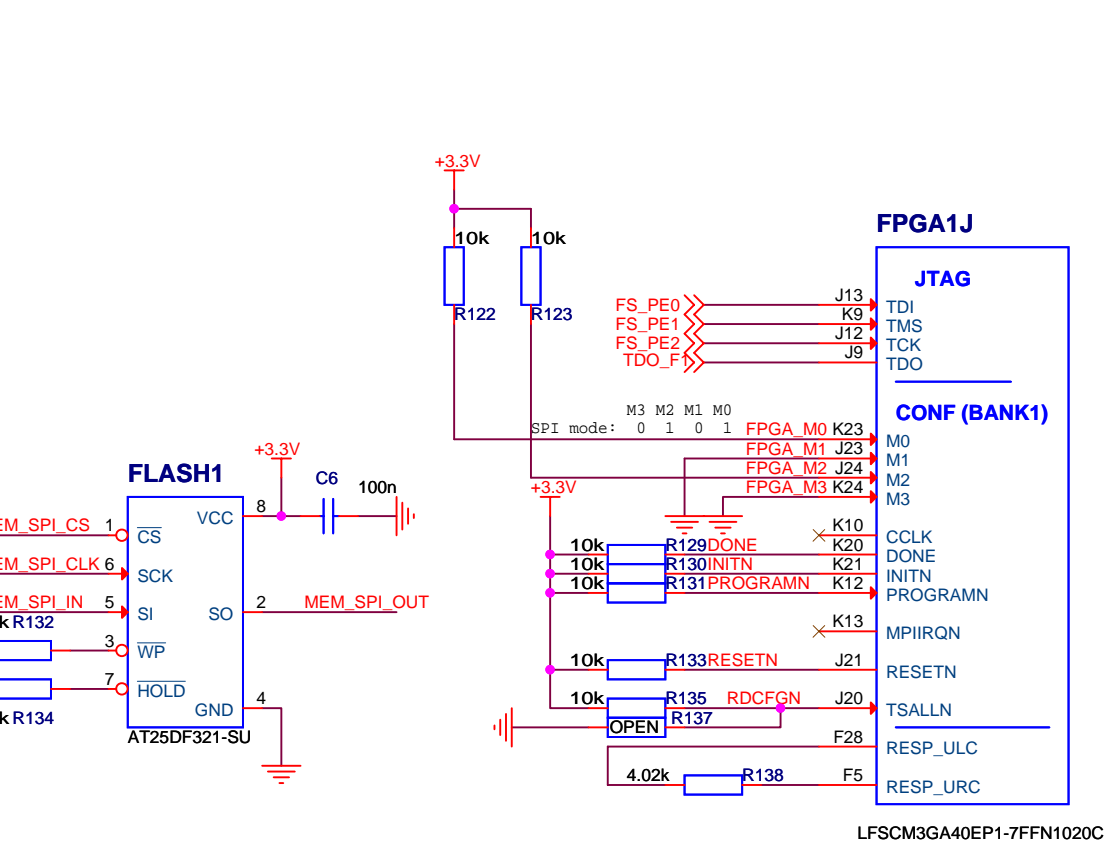
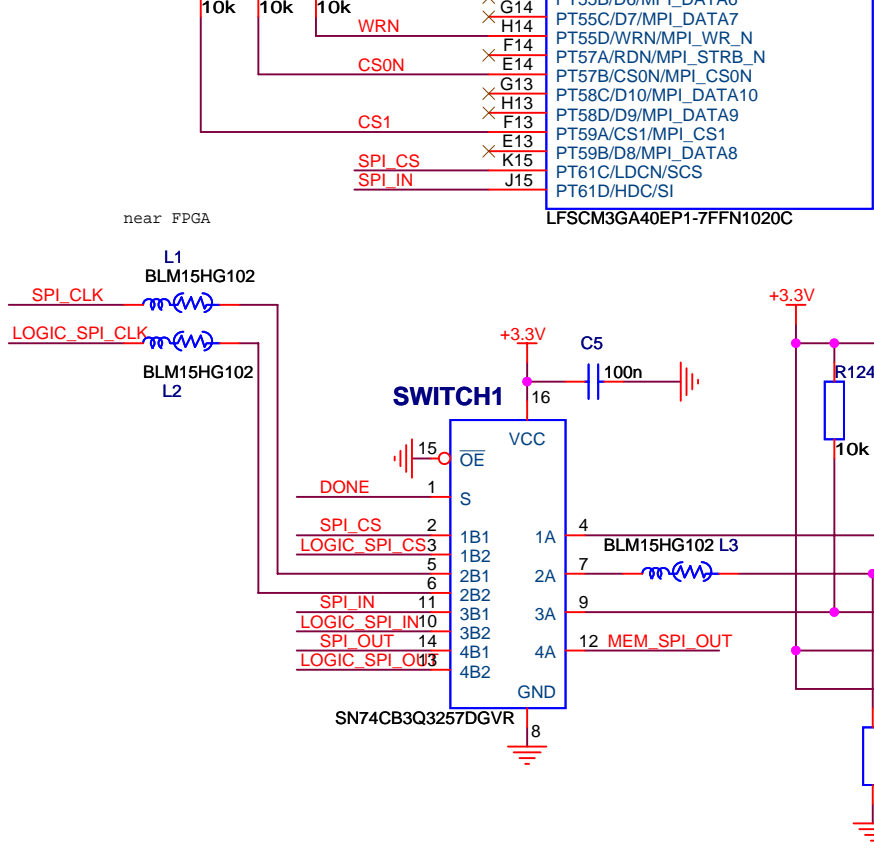
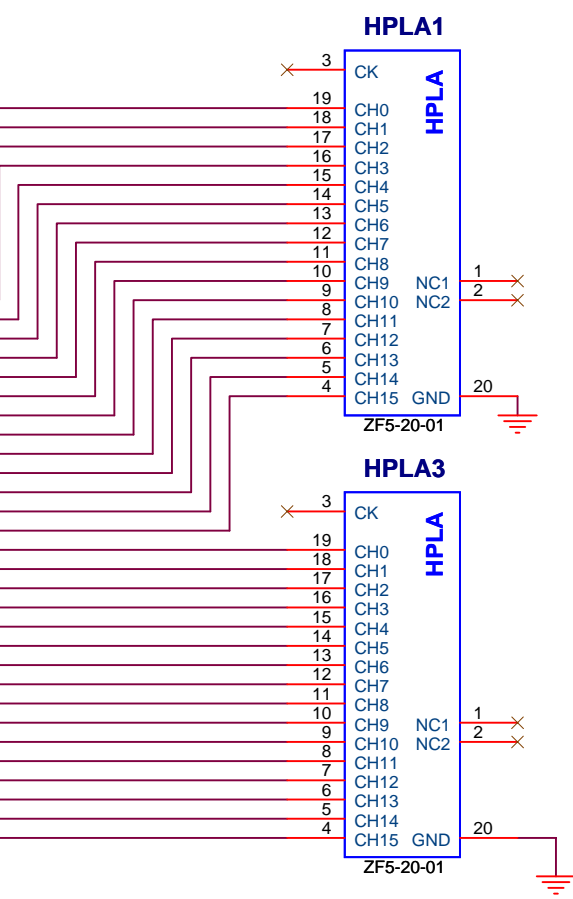
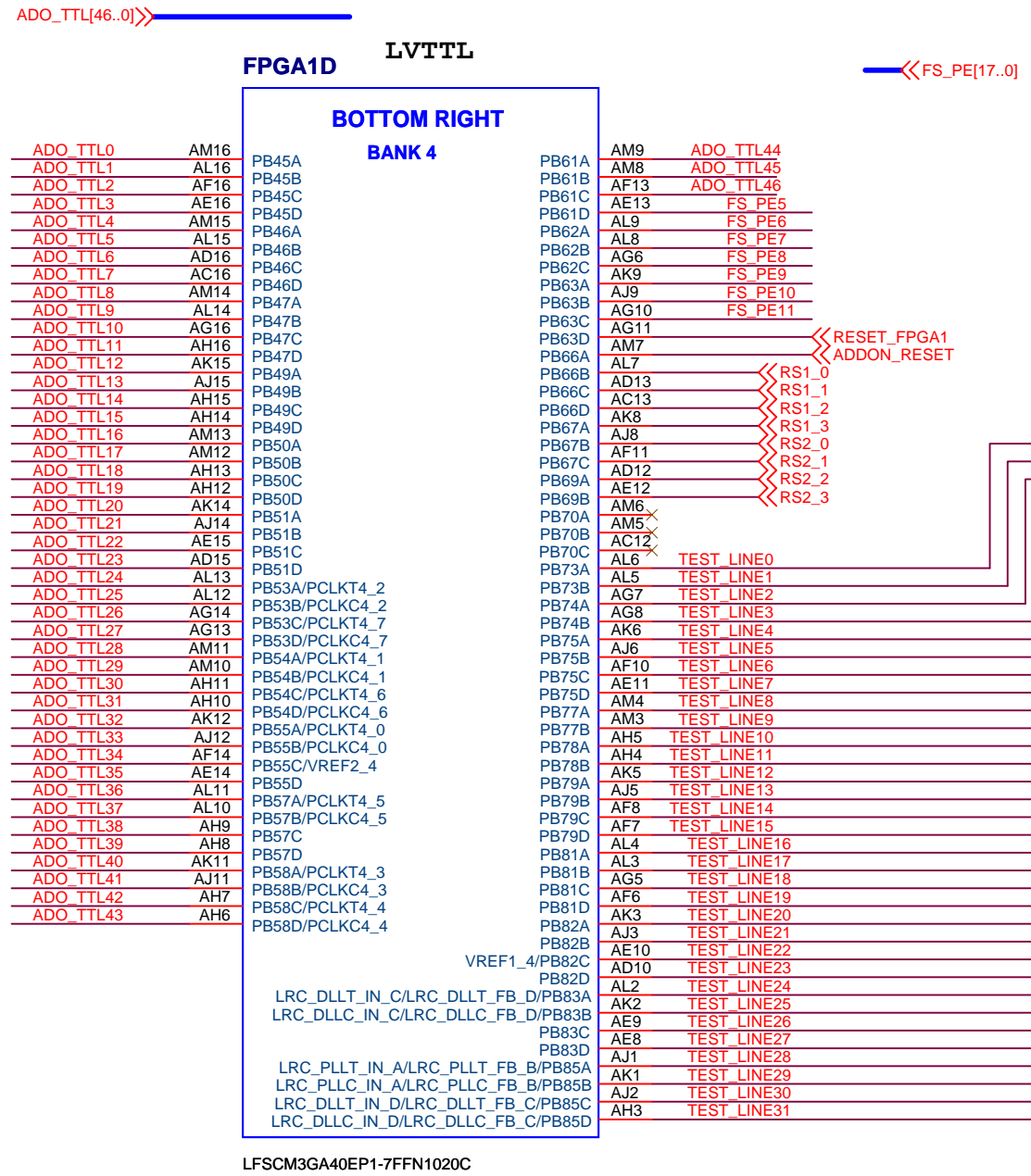
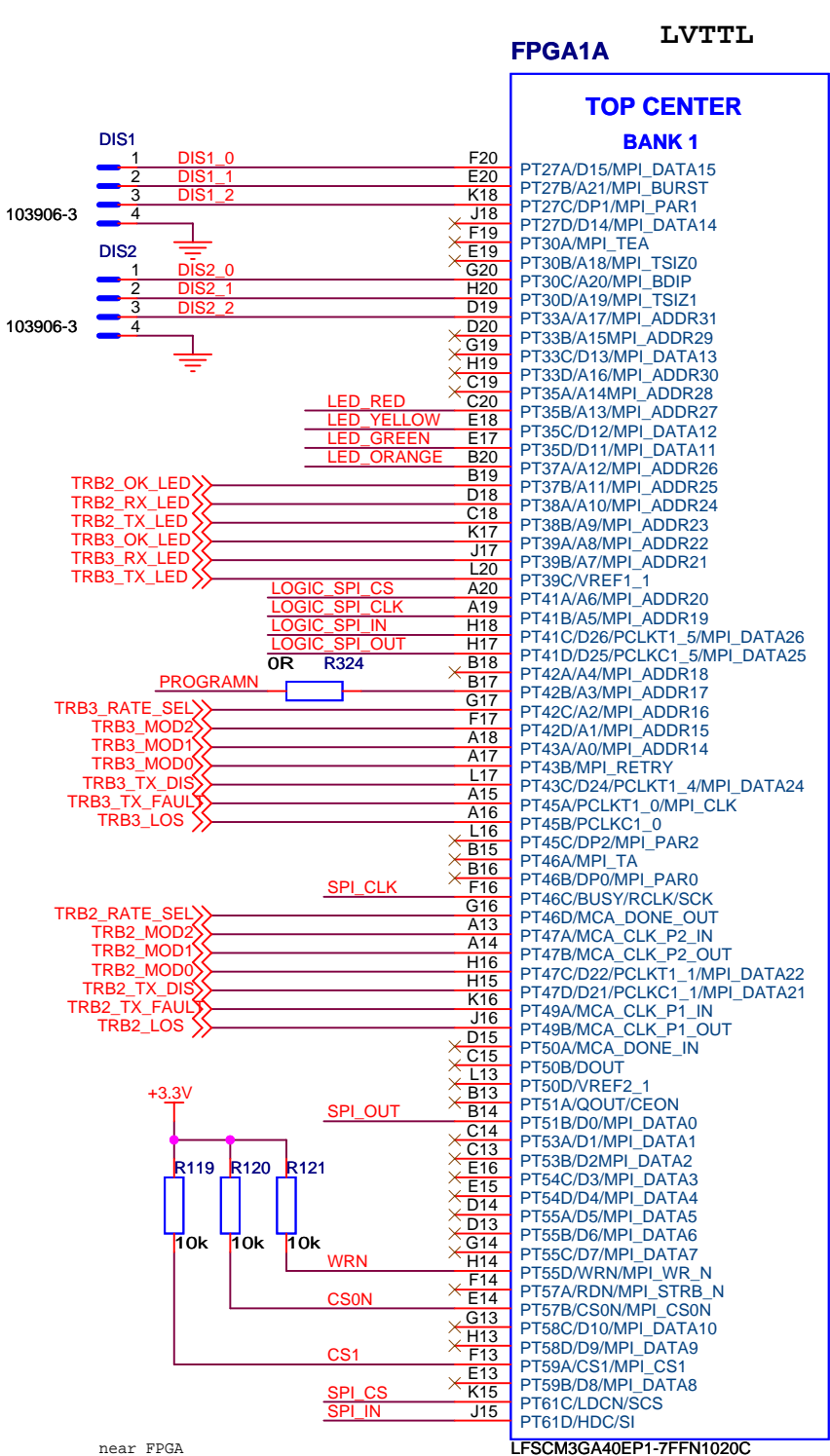
FS_PE11 - temperature control

ADO_LV[61..0]



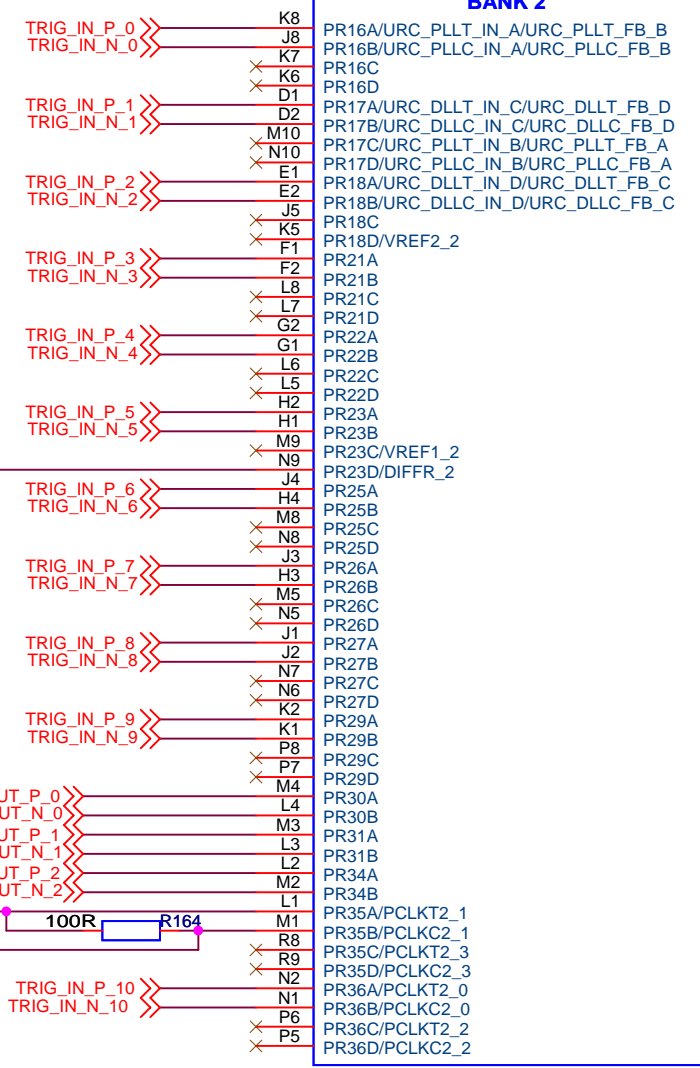
QSE-040-01

Title			03_TRB_CONNECTORS		
Size	Document Number				Rev
A4	<Doc>				<RevCo
Date:	Monday, April 19, 2010			Sheet	4 of 16



FPGA1B LVDS

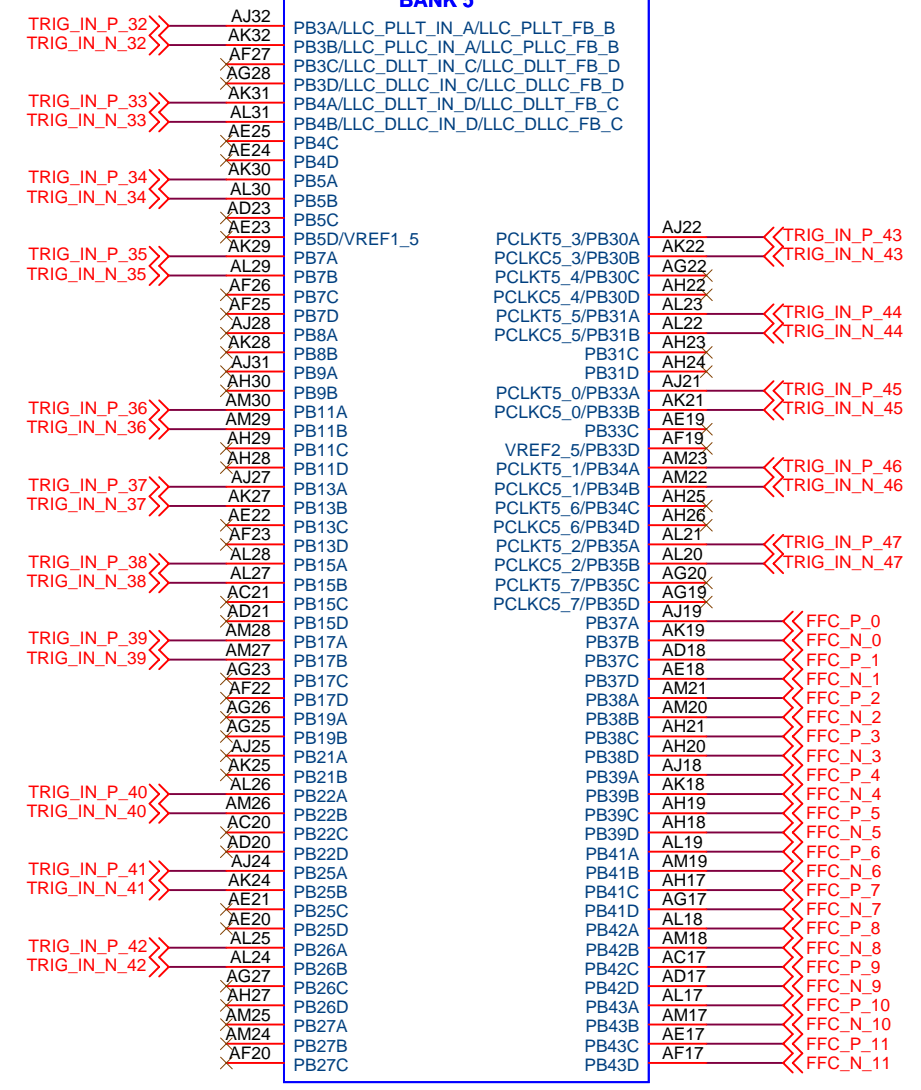
UPPER RIGHT
BANK 2



LFSCM3GA40EP1-7FFN1020C

FPGA1E LVDS

BOTTOM LEFT
BANK 5



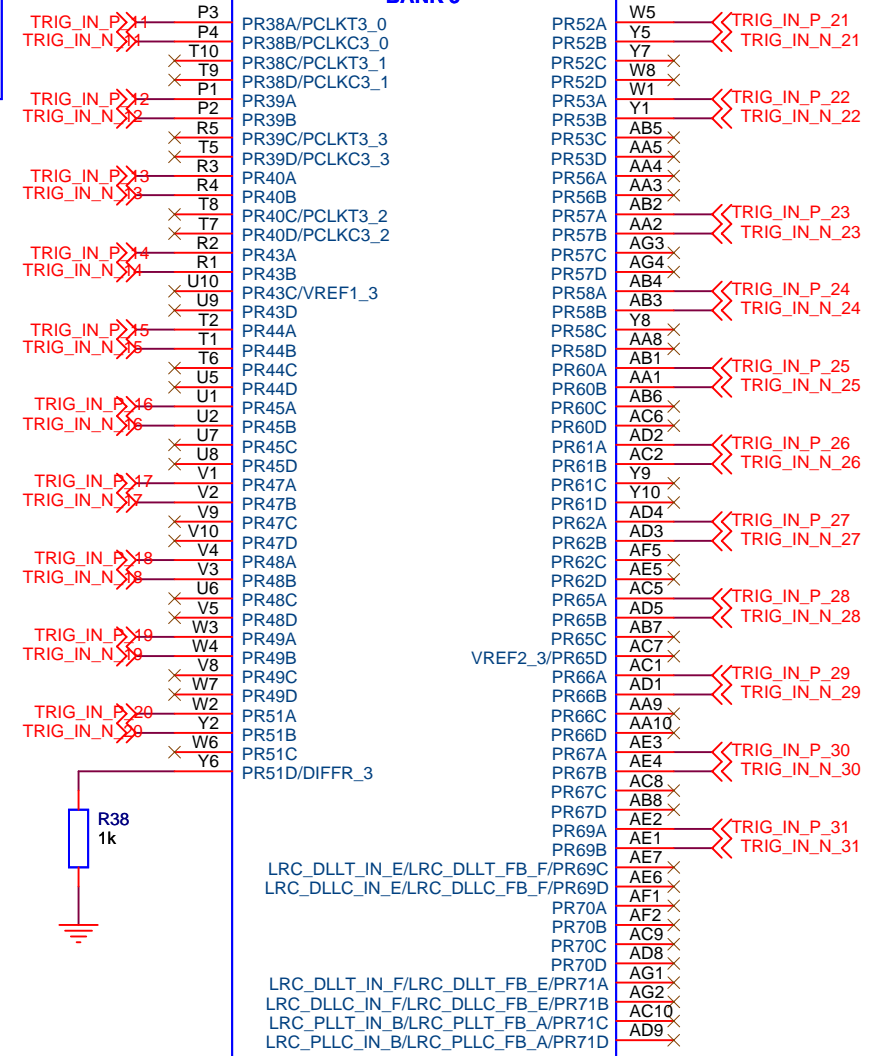
LFSCM3GA40EP1-7FFN1020C

FFC P 1		R327	FFC N 1
FFC P 3	100R	R328	FFC N 3
FFC P 5	100R	R329	FFC N 5
FFC P 7	100R	R330	FFC N 7
FFC P 9	100R	R331	FFC N 9
FFC P 11	100R	R332	FFC N 11

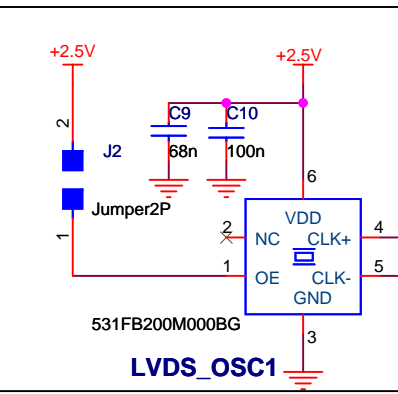
Optional resistors
do not solder

FPGA1C LVDS

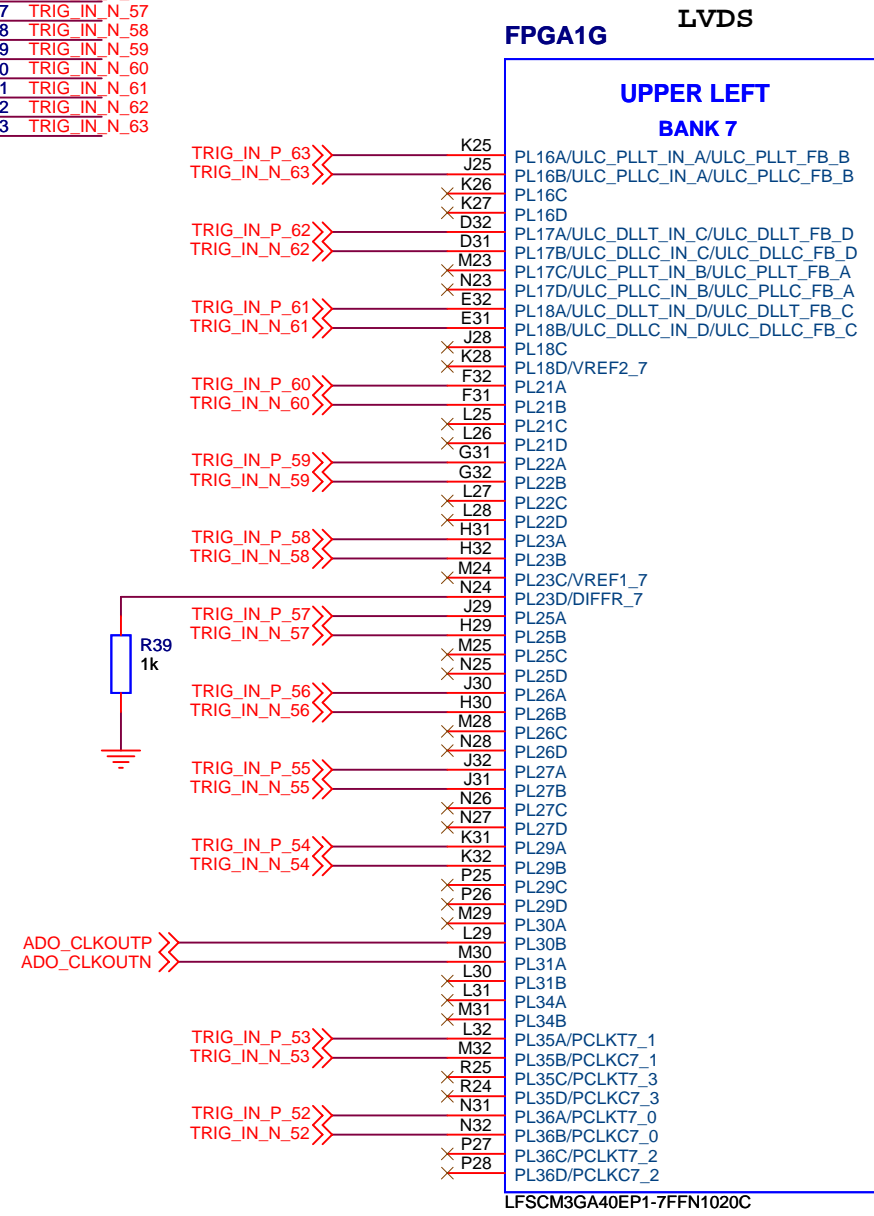
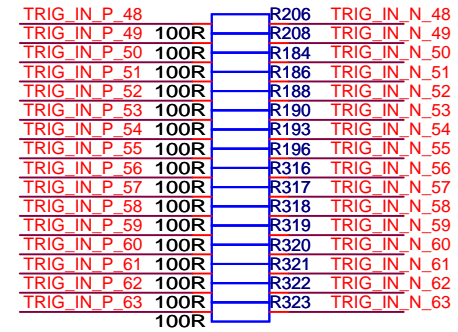
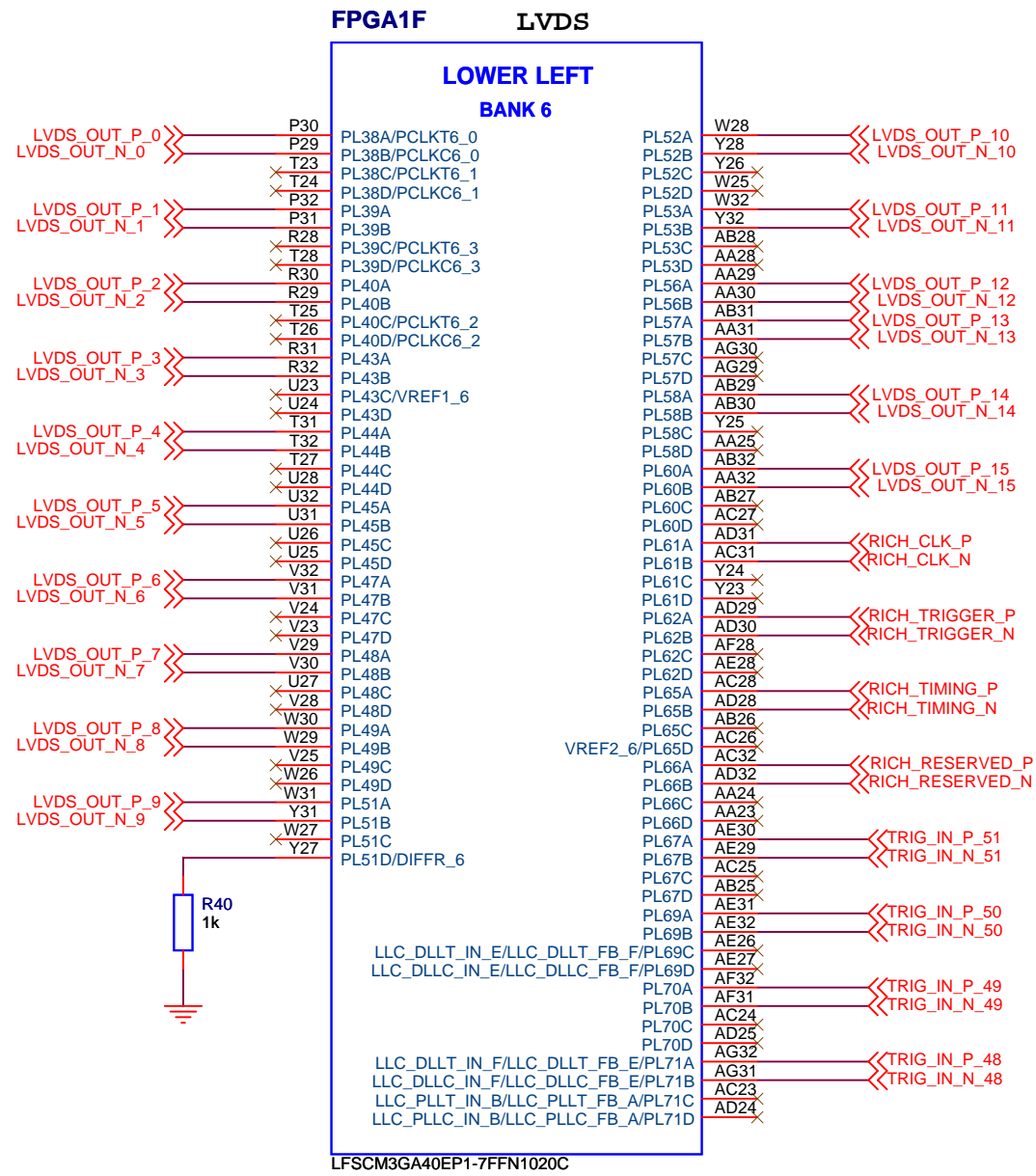
LOWER RIGHT
BANK 3

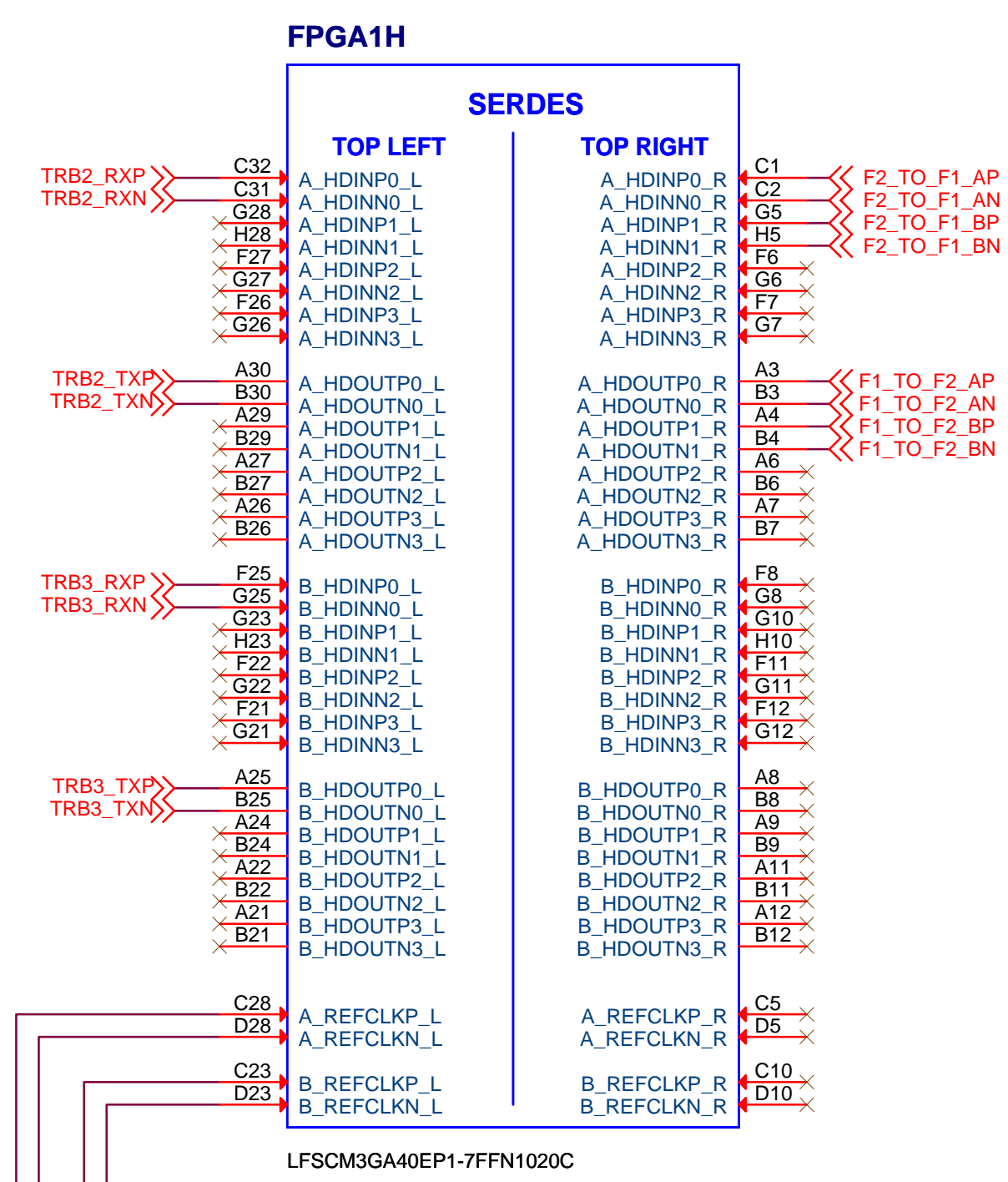
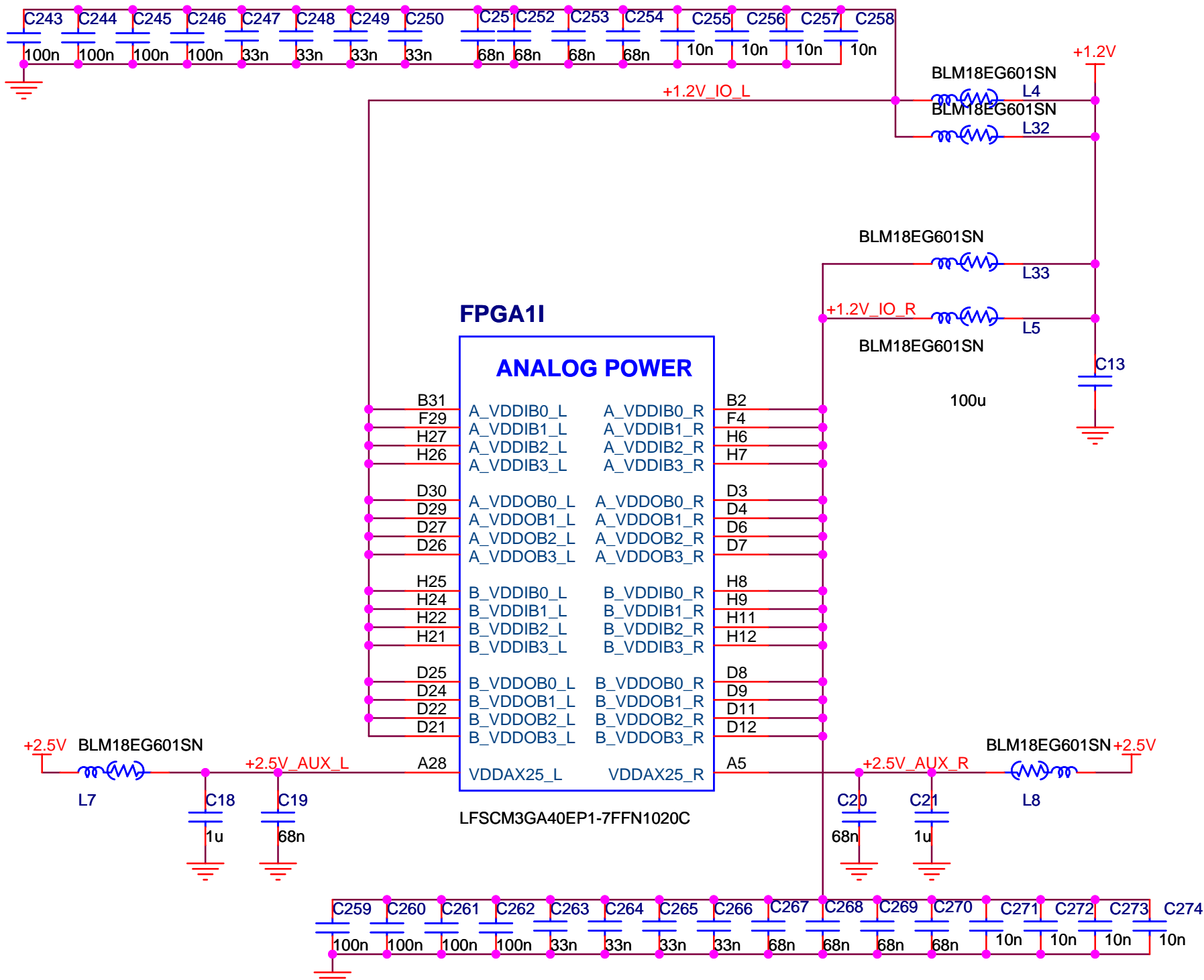


LFSCM3GA40EP1-7FFN1020C



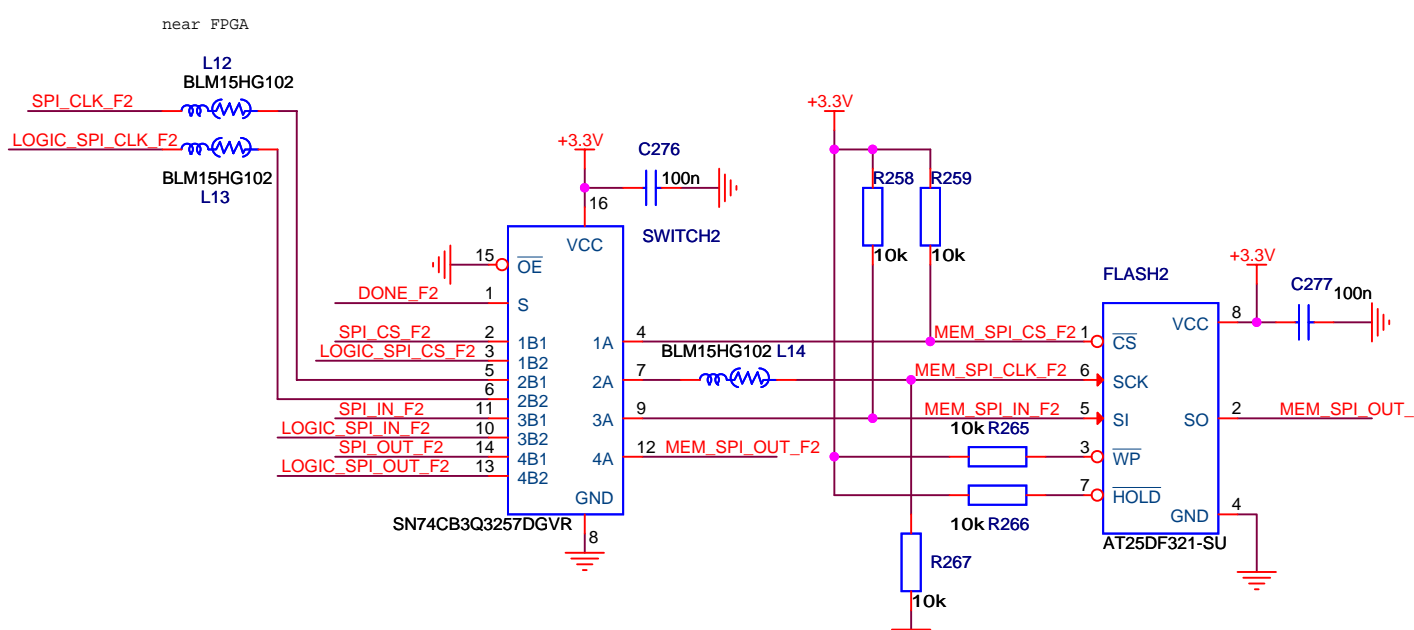
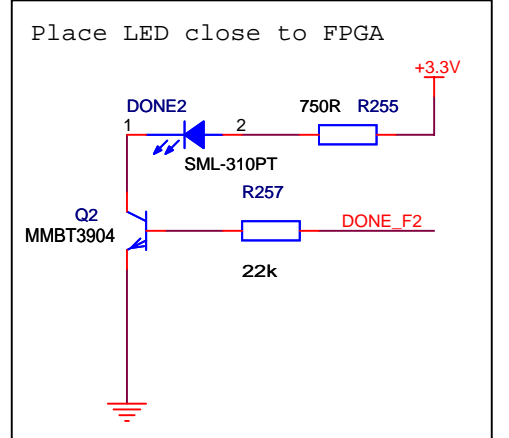
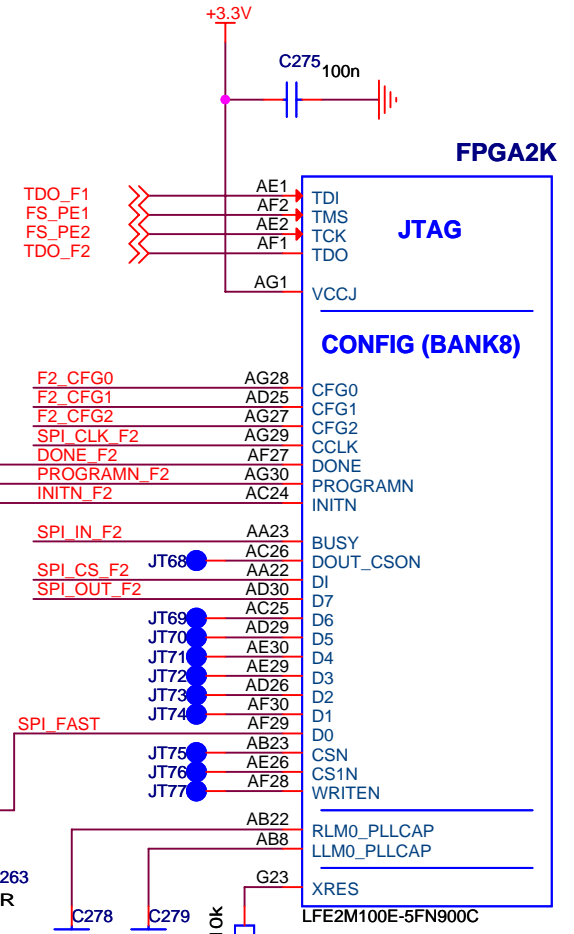
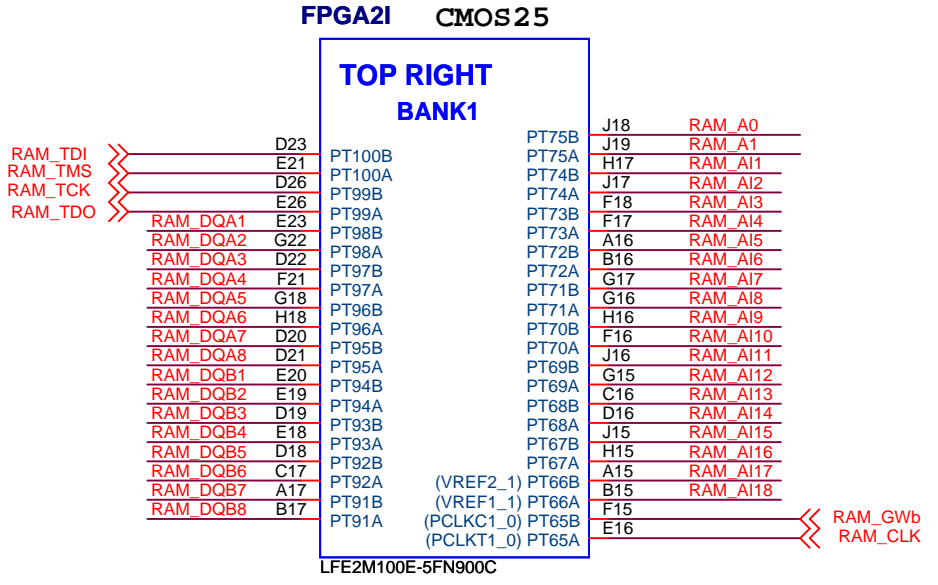
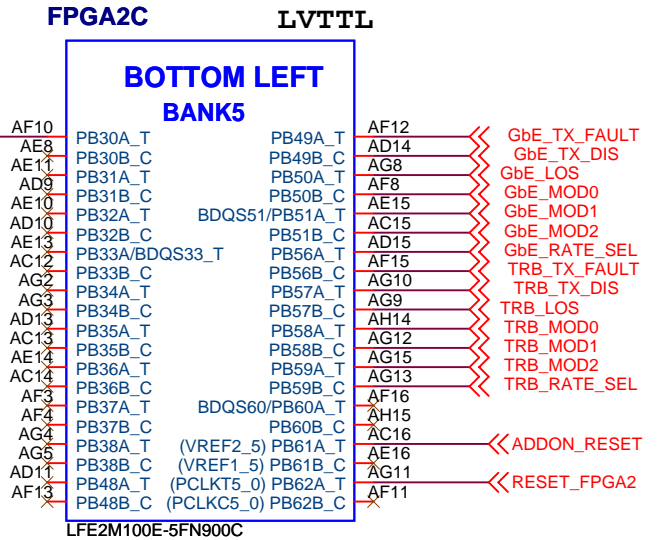
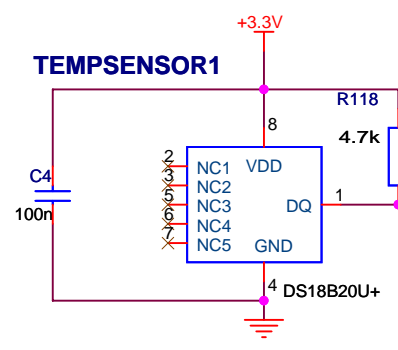
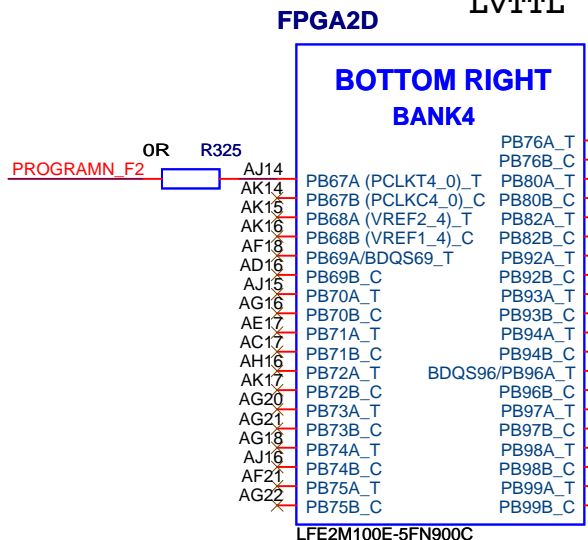
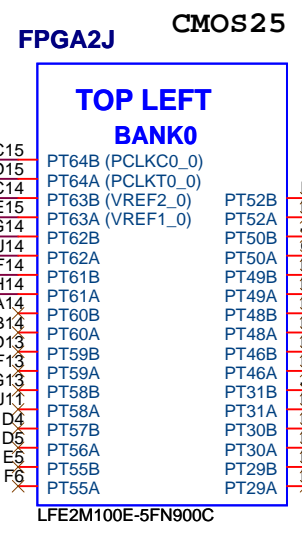
TRIG_IN_P_0		R139	TRIG_IN_N_0
TRIG_IN_P_1	100R	R140	TRIG_IN_N_1
TRIG_IN_P_2	100R	R141	TRIG_IN_N_2
TRIG_IN_P_3	100R	R143	TRIG_IN_N_3
TRIG_IN_P_4	100R	R145	TRIG_IN_N_4
TRIG_IN_P_5	100R	R147	TRIG_IN_N_5
TRIG_IN_P_6	100R	R150	TRIG_IN_N_6
TRIG_IN_P_7	100R	R152	TRIG_IN_N_7
TRIG_IN_P_8	100R	R153	TRIG_IN_N_8
TRIG_IN_P_9	100R	R155	TRIG_IN_N_9
TRIG_IN_P_10	100R	R157	TRIG_IN_N_10
TRIG_IN_P_11	100R	R159	TRIG_IN_N_11
TRIG_IN_P_12	100R	R142	TRIG_IN_N_12
TRIG_IN_P_13	100R	R144	TRIG_IN_N_13
TRIG_IN_P_14	100R	R146	TRIG_IN_N_14
TRIG_IN_P_15	100R	R148	TRIG_IN_N_15
TRIG_IN_P_16	100R	R149	TRIG_IN_N_16
TRIG_IN_P_17	100R	R151	TRIG_IN_N_17
TRIG_IN_P_18	100R	R154	TRIG_IN_N_18
TRIG_IN_P_19	100R	R156	TRIG_IN_N_19
TRIG_IN_P_20	100R	R158	TRIG_IN_N_20
TRIG_IN_P_21	100R	R160	TRIG_IN_N_21
TRIG_IN_P_22	100R	R161	TRIG_IN_N_22
TRIG_IN_P_23	100R	R162	TRIG_IN_N_23
TRIG_IN_P_24	100R	R307	TRIG_IN_N_24
TRIG_IN_P_25	100R	R308	TRIG_IN_N_25
TRIG_IN_P_26	100R	R309	TRIG_IN_N_26
TRIG_IN_P_27	100R	R310	TRIG_IN_N_27
TRIG_IN_P_28	100R	R311	TRIG_IN_N_28
TRIG_IN_P_29	100R	R312	TRIG_IN_N_29
TRIG_IN_P_30	100R	R313	TRIG_IN_N_30
TRIG_IN_P_31	100R	R314	TRIG_IN_N_31
TRIG_IN_P_32	100R	R306	TRIG_IN_N_32
TRIG_IN_P_33	100R	R315	TRIG_IN_N_33

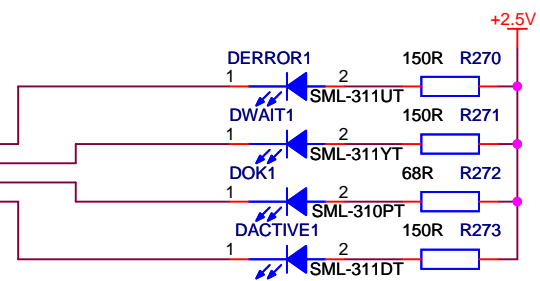
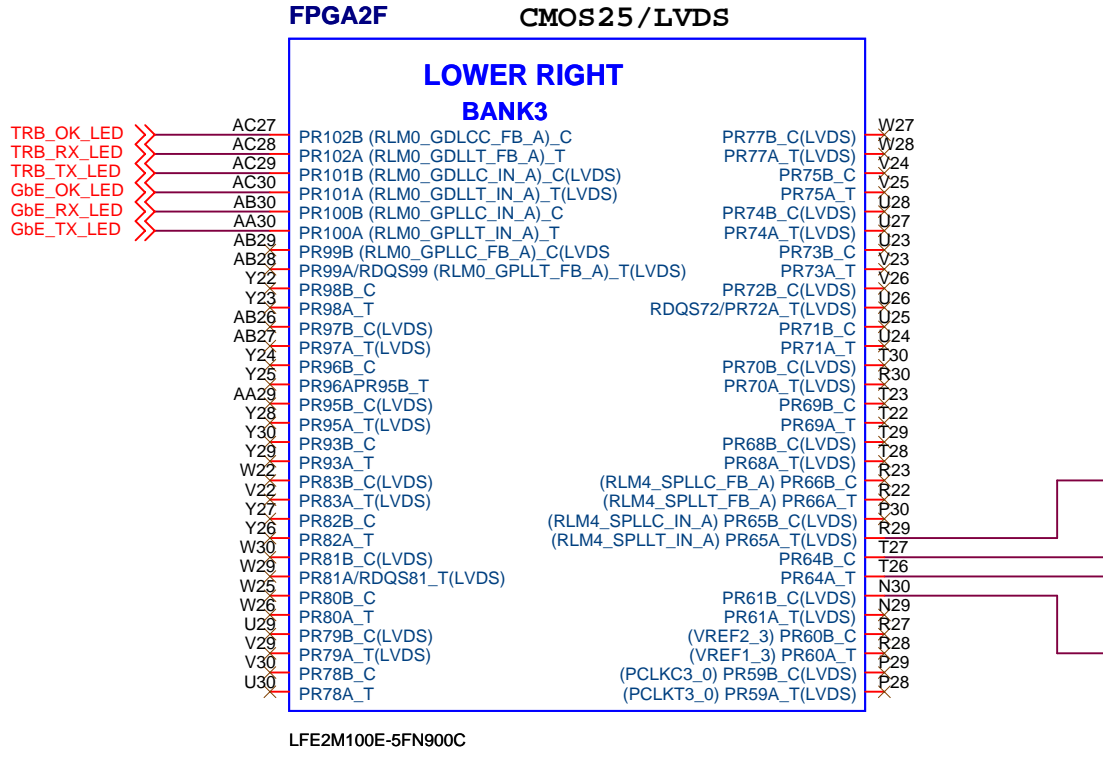
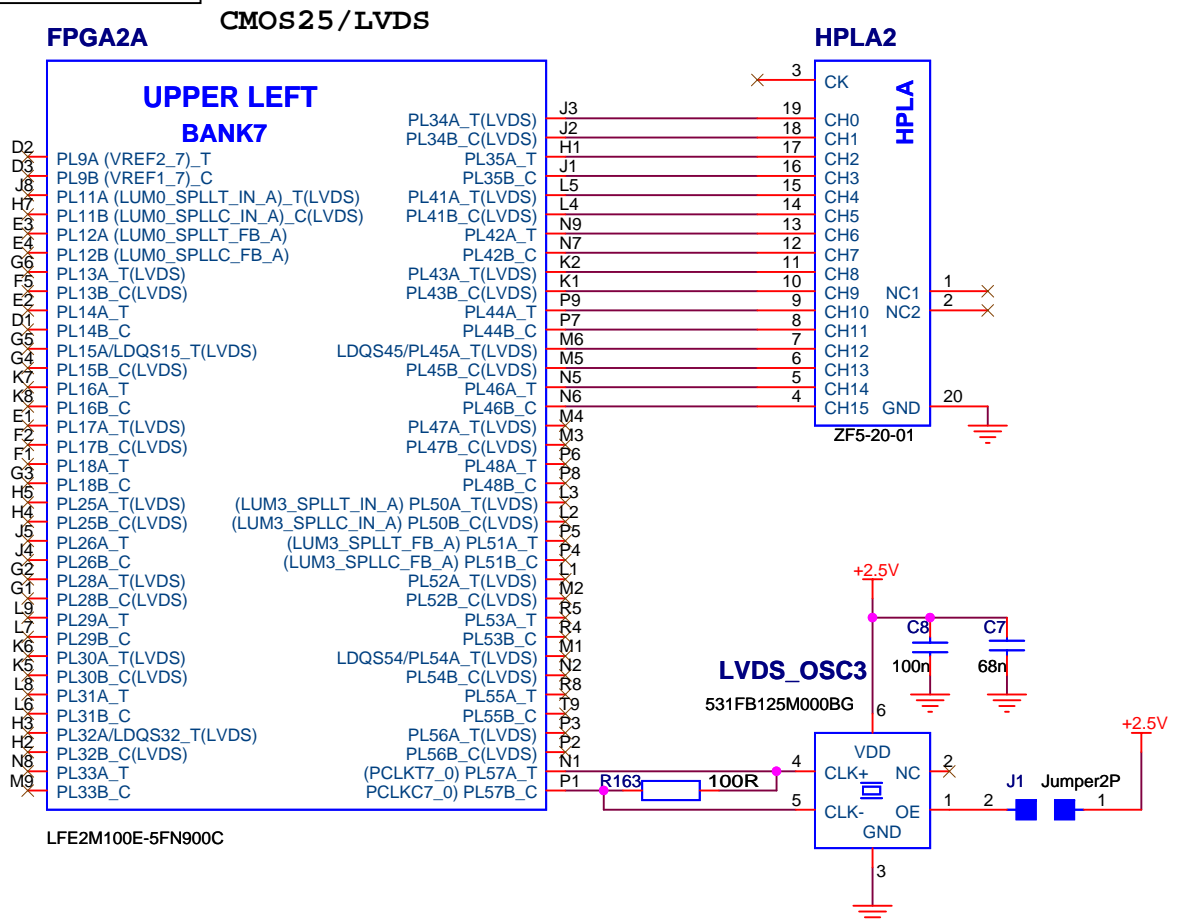
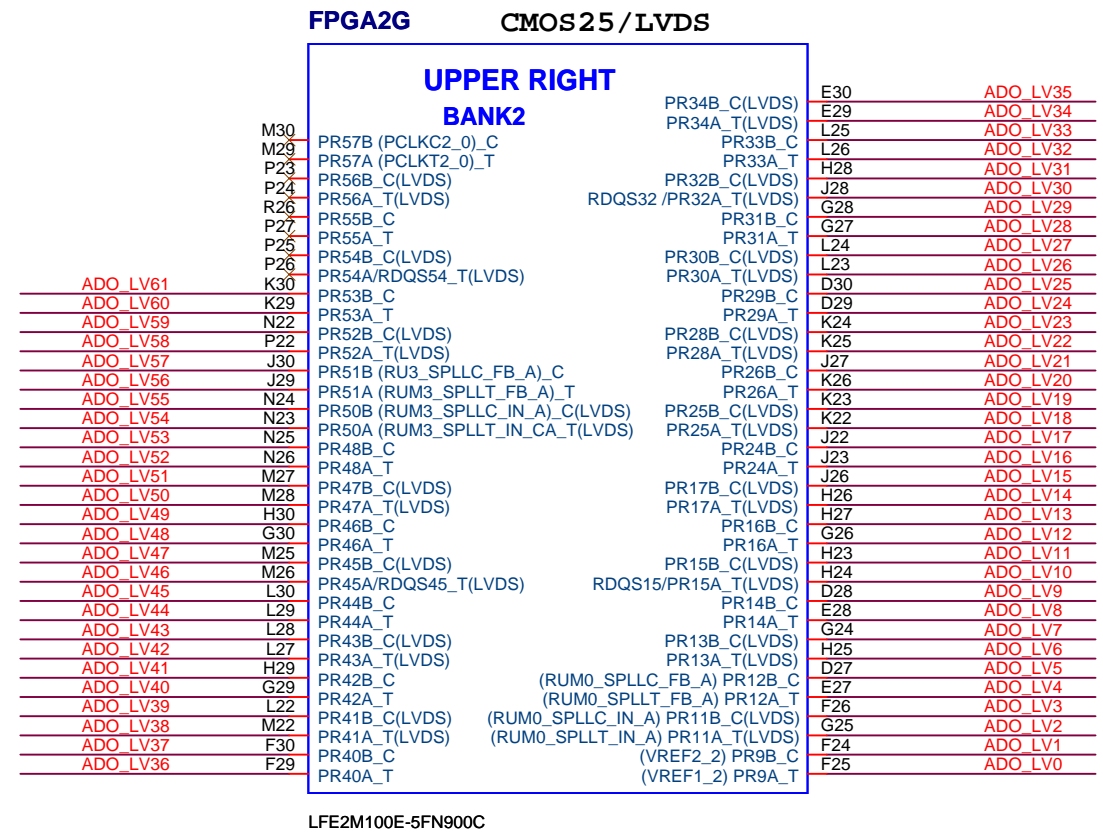
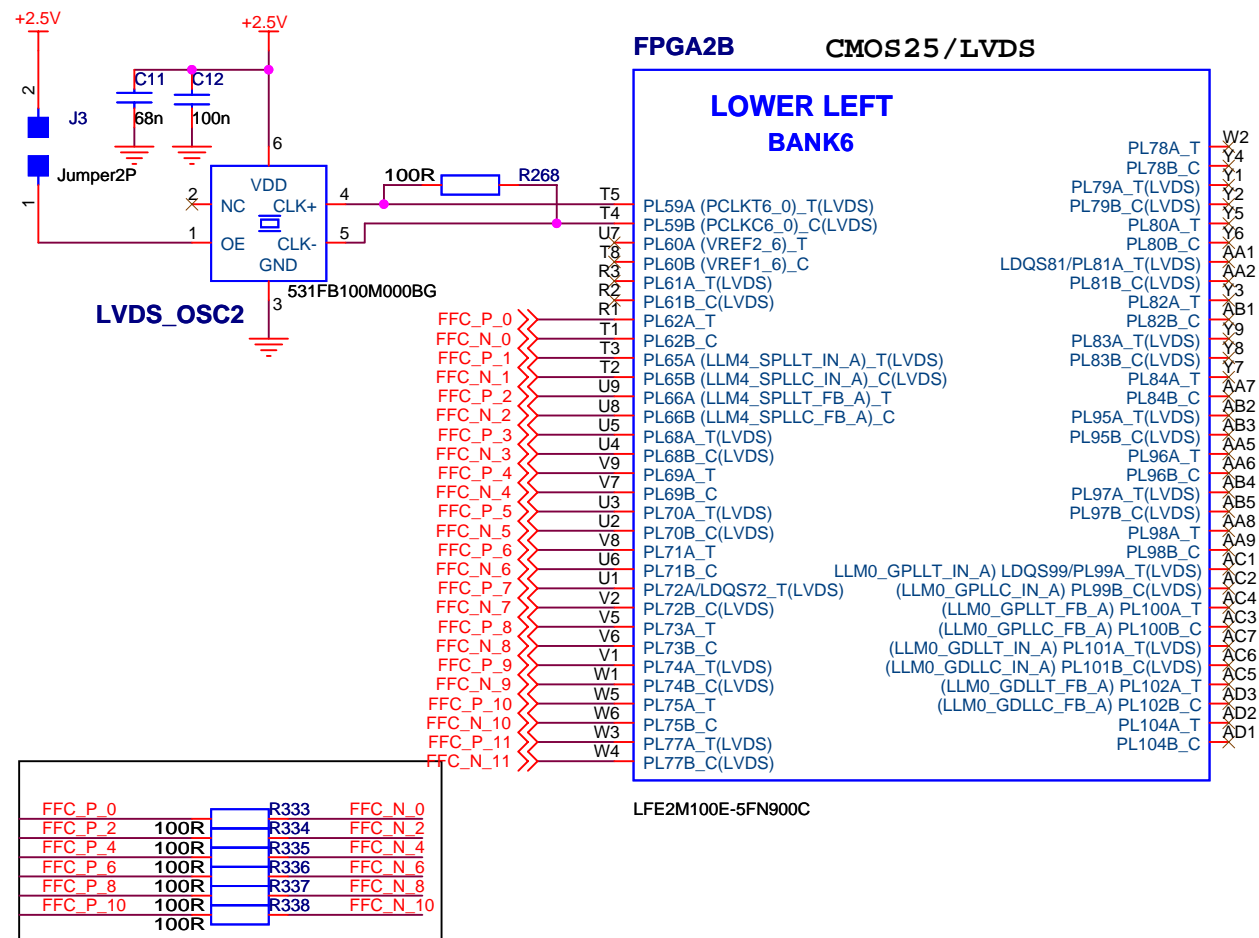


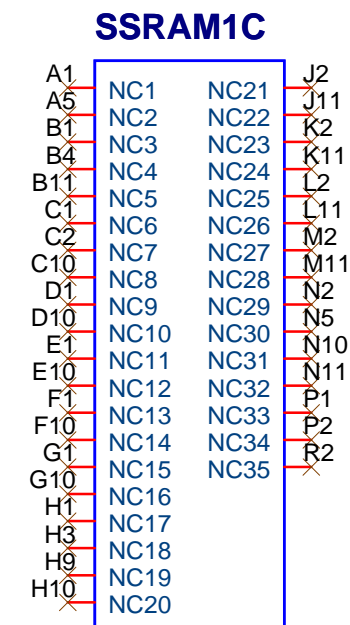
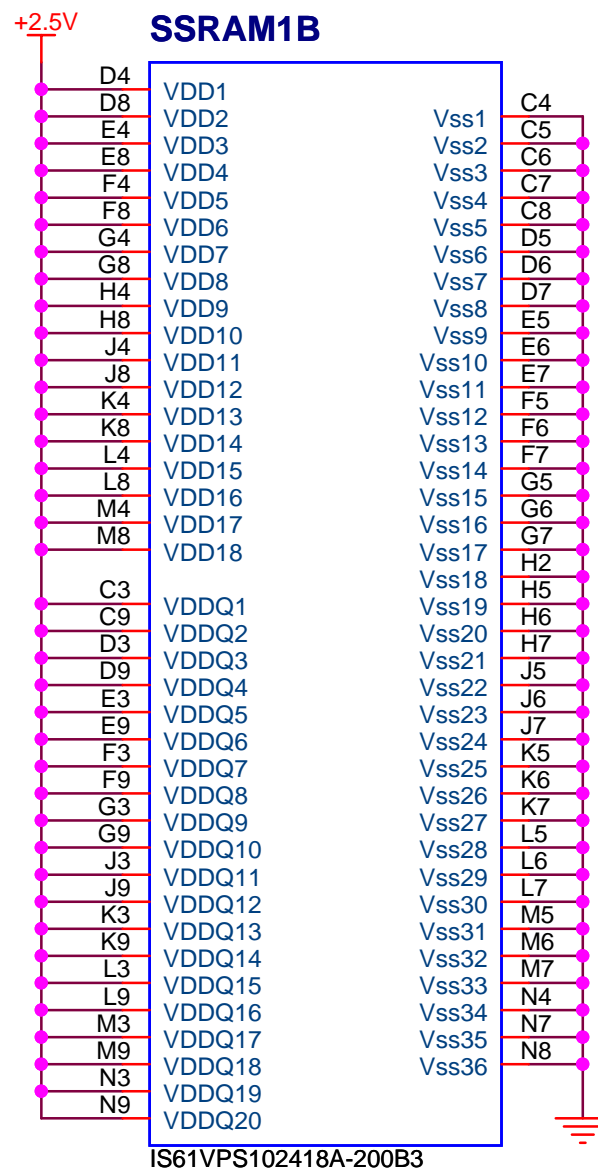
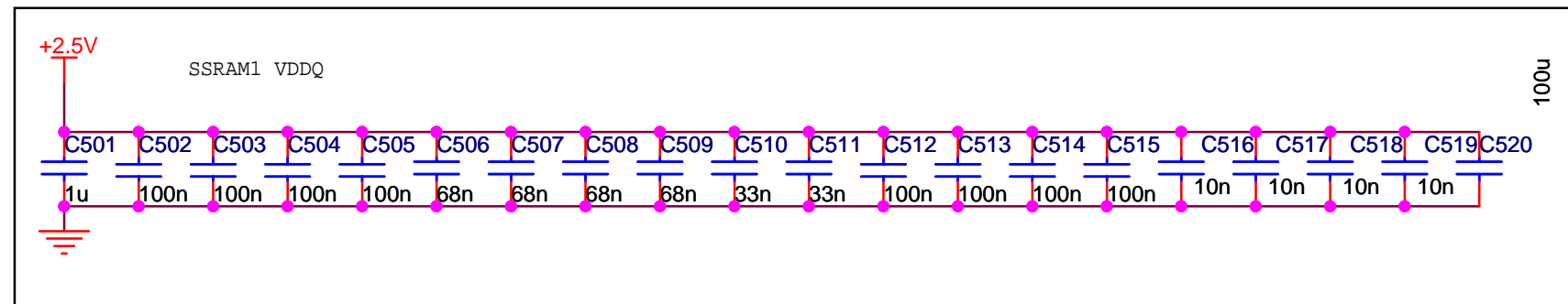
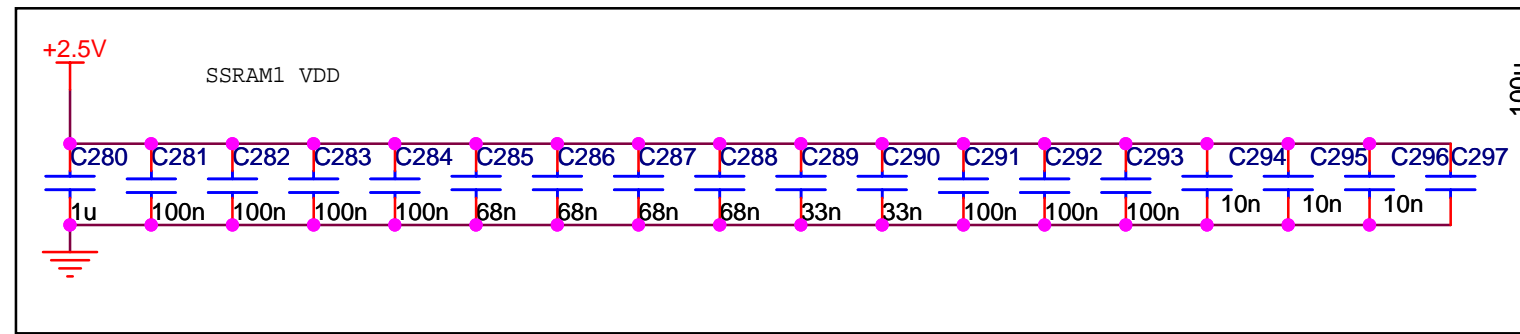
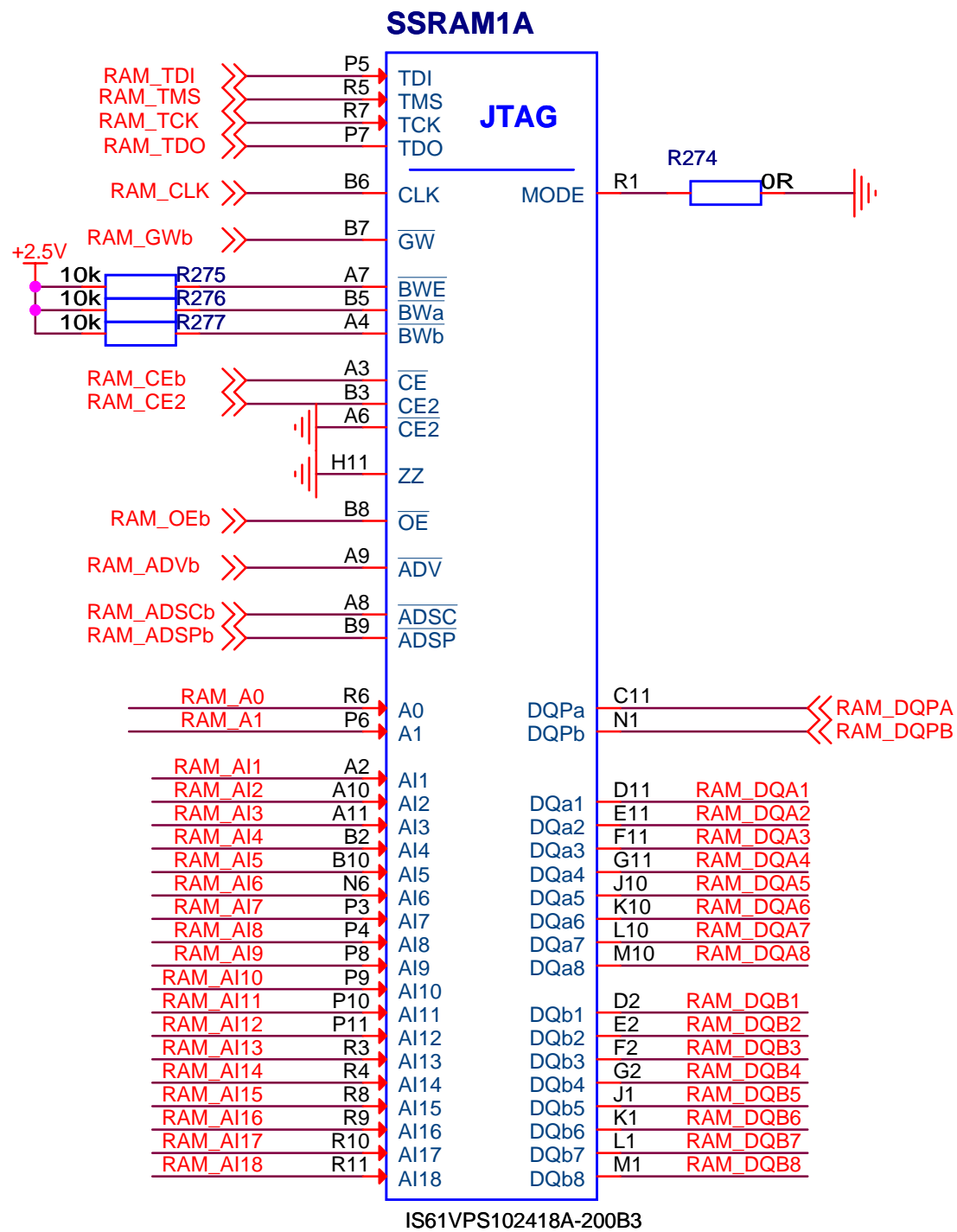


Title			07_FPGA1_SERDES		
Size	Document Number	Rev			
A4	<Doc>	<RevCo			
Date:	Monday, April 19, 2010	Sheet	8	of	16

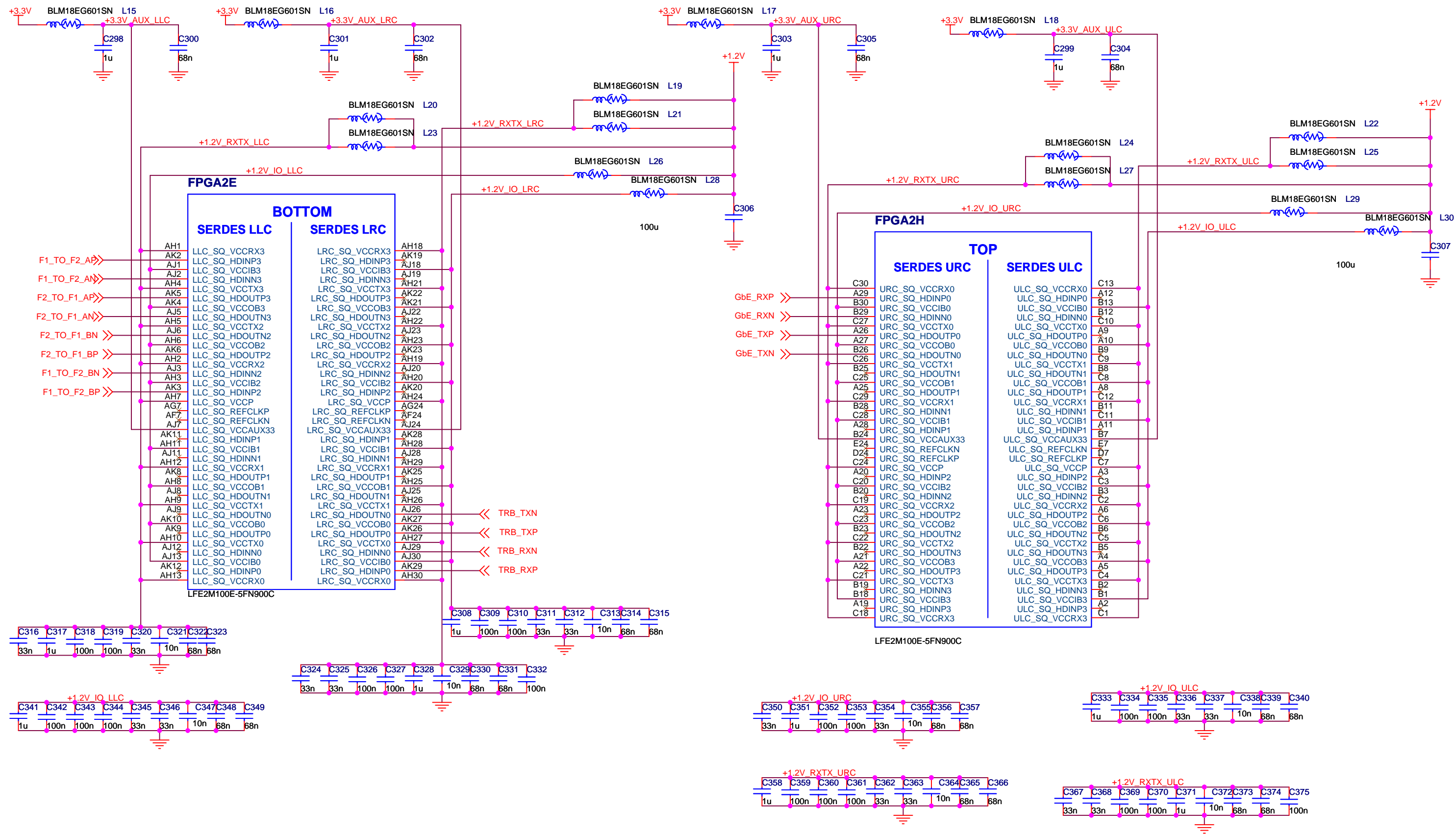
RAM_A[1..0] >>
 RAM_AI[18..1] >>
 RAM_DQA[8..1] >>
 RAM_DQB[8..1] >>



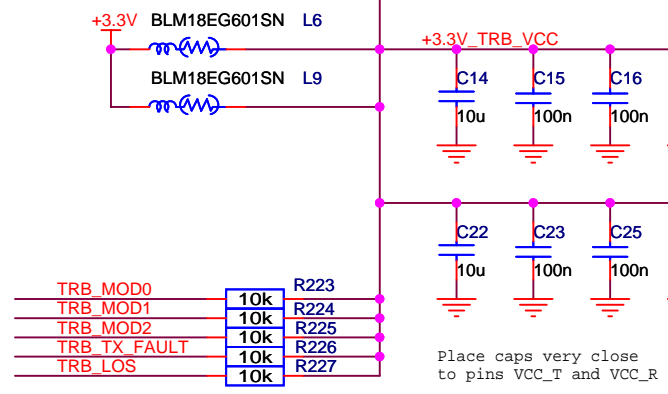
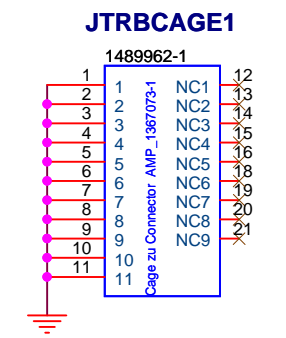
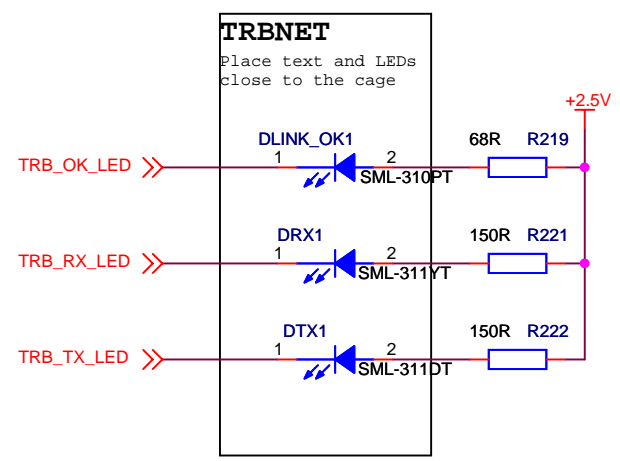




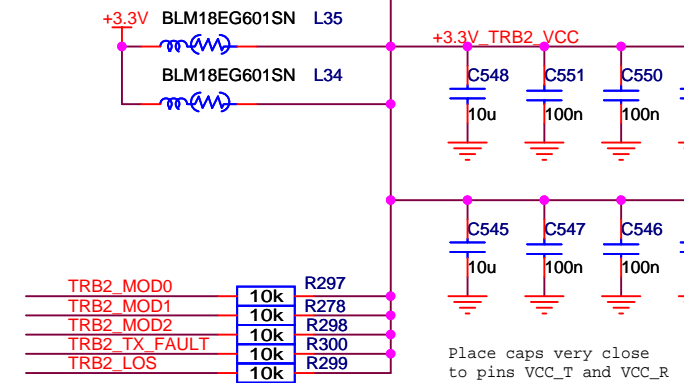
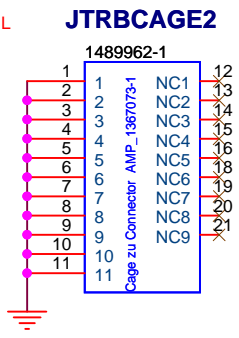
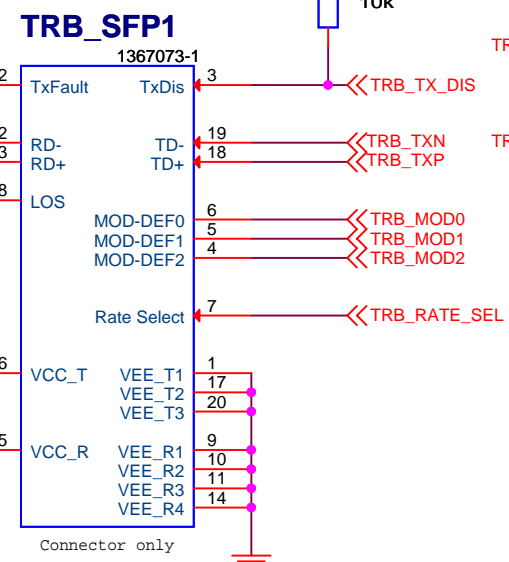
Title			10_FPGA2_MEMORY		
Size	Document Number				Rev
A4	<Doc>				<RevCo
Date:	Monday, April 19, 2010	Sheet	11	of	16



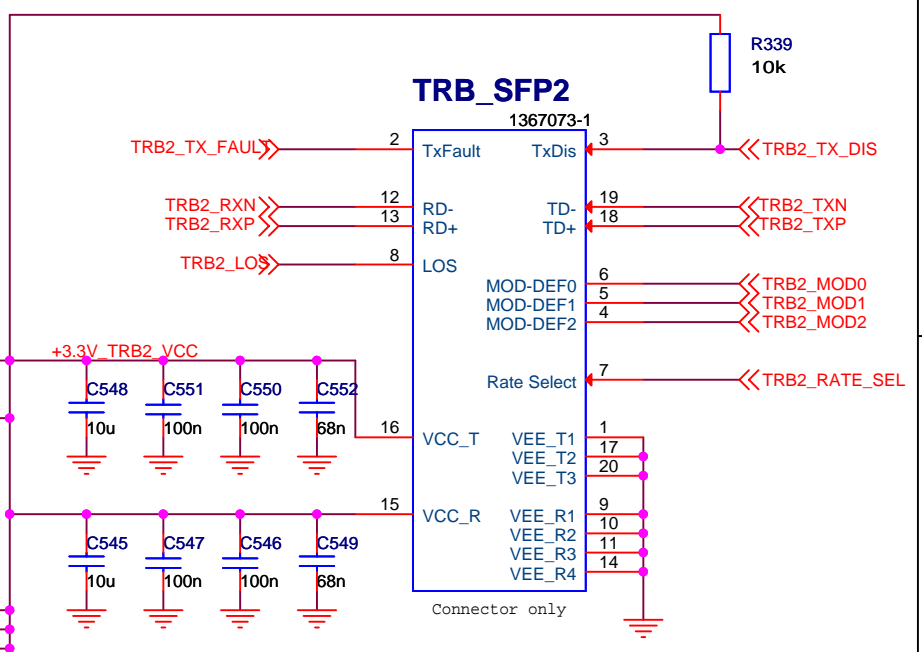
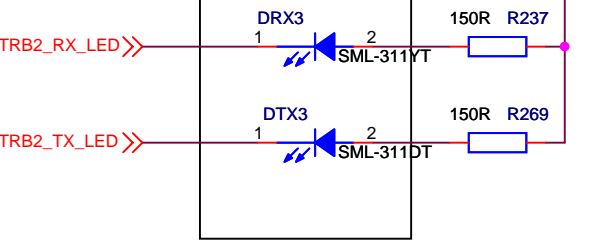
Title			11_FPGA2_SERDES		
Size	Document Number				Rev
A3	<Doc>				<RevC
Date:	Monday, April 19, 2010	Sheet	12	of	16



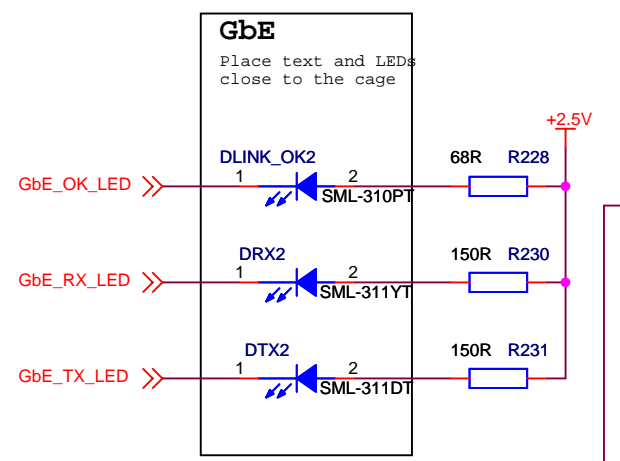
MODDEF0 is grounded by module when inserted



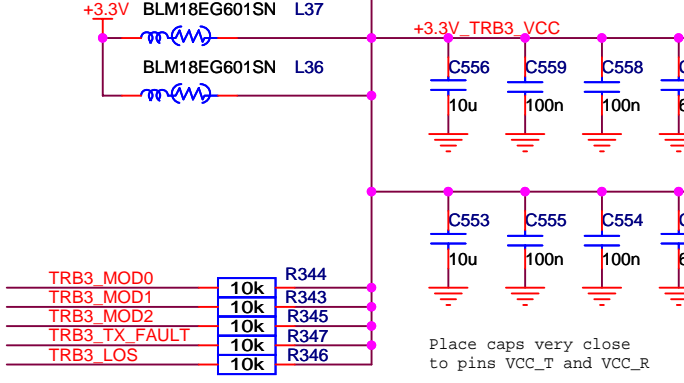
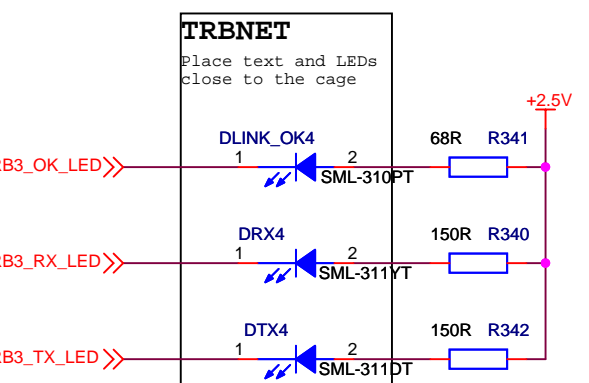
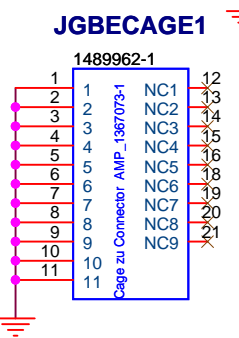
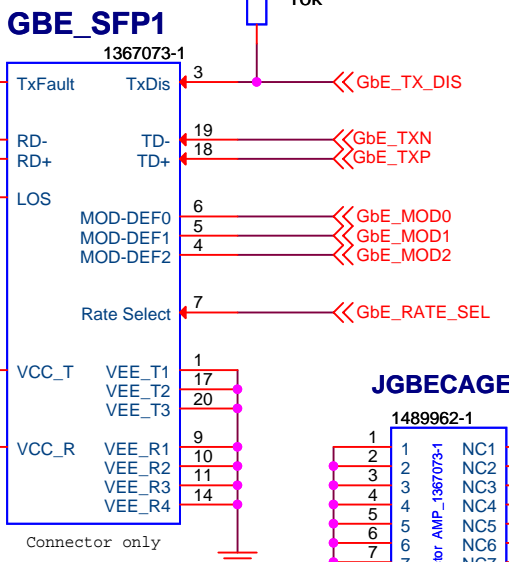
MODDEF0 is grounded by module when inserted



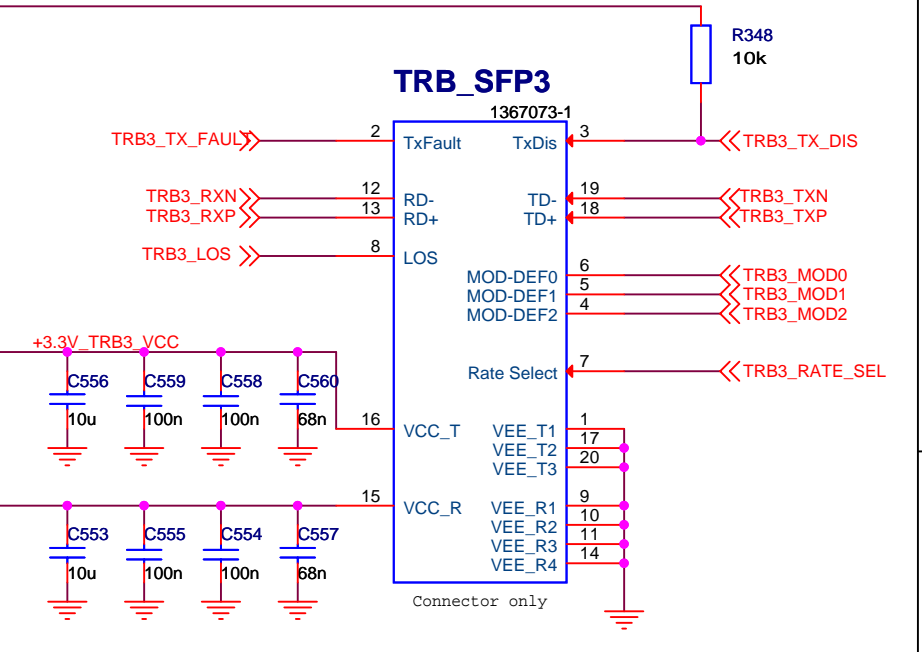
Place caps very close to pins VCC_T and VCC_R



MODDEF0 is grounded by module when inserted

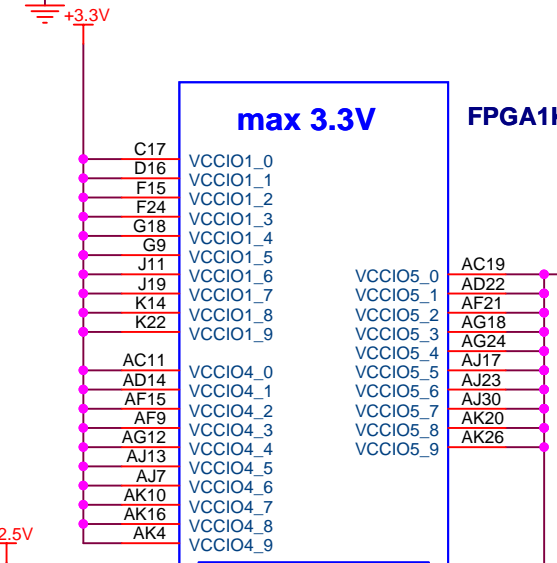
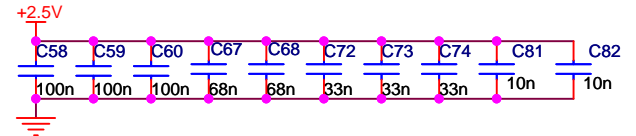
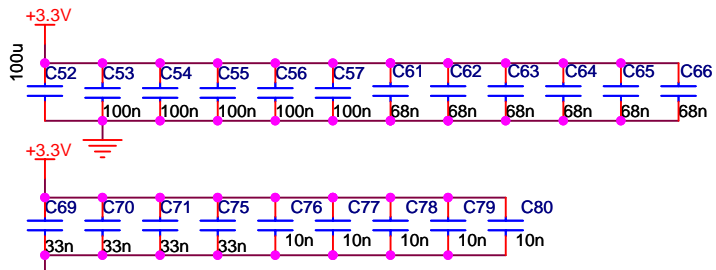


MODDEF0 is grounded by module when inserted

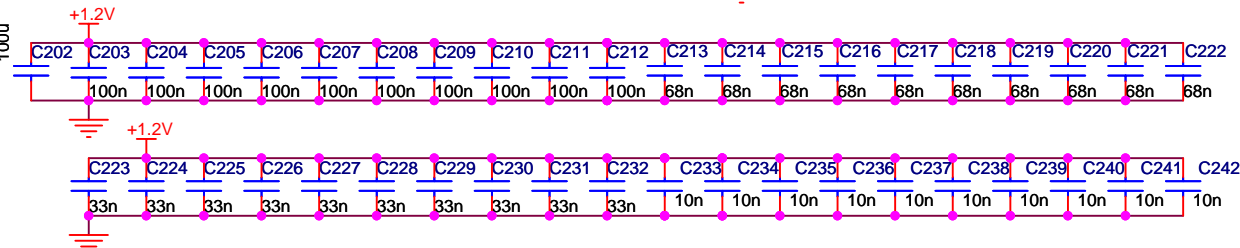
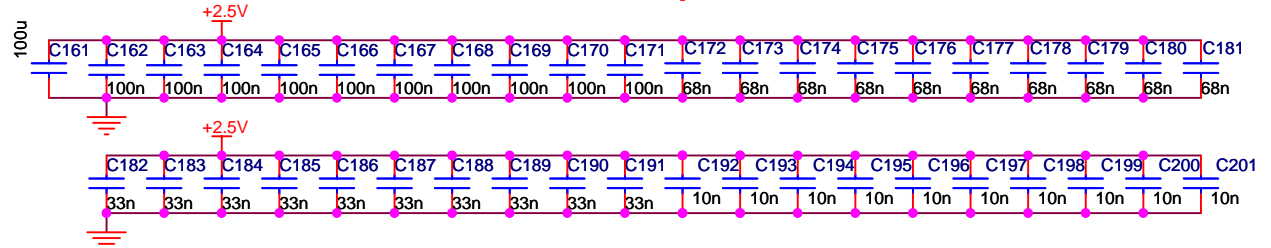
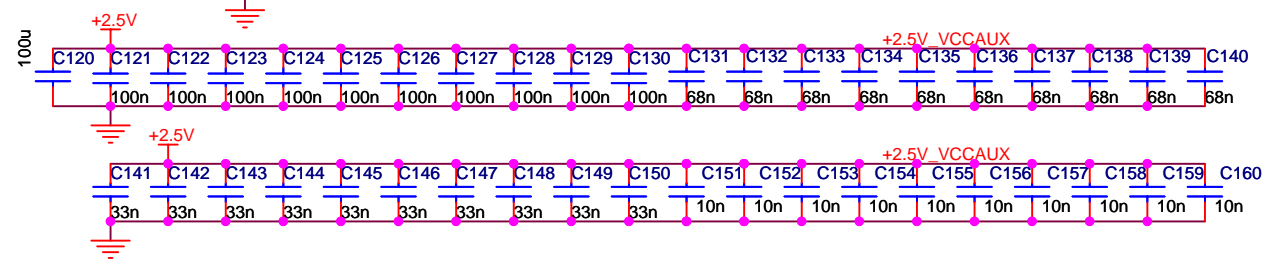
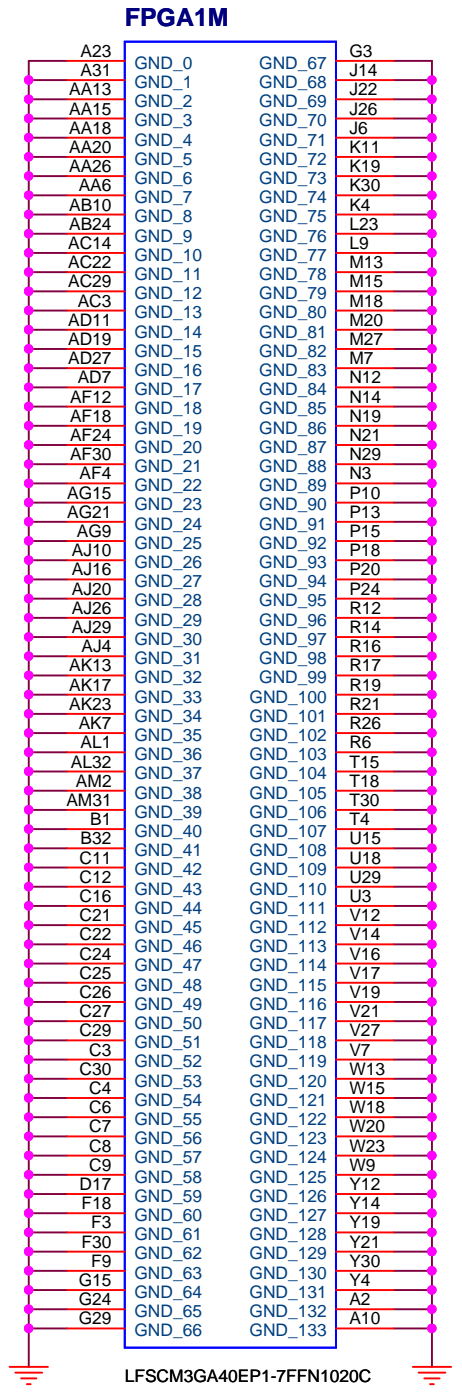
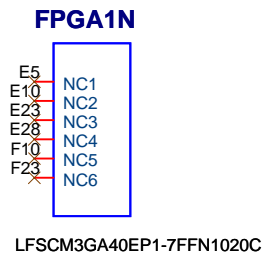
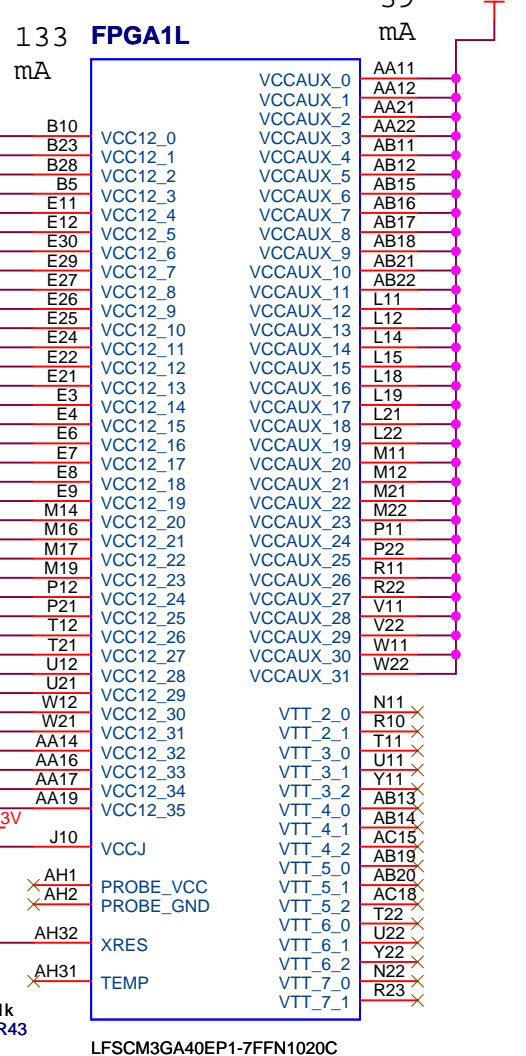
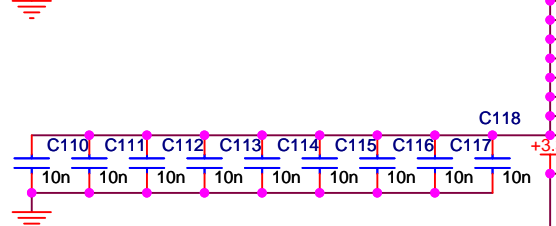
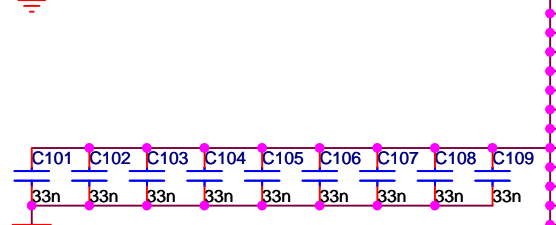
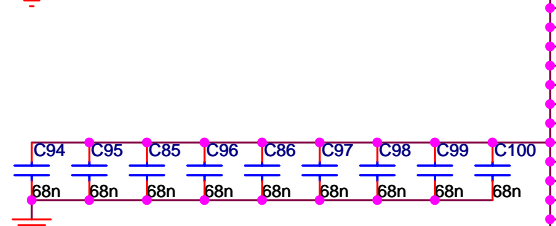
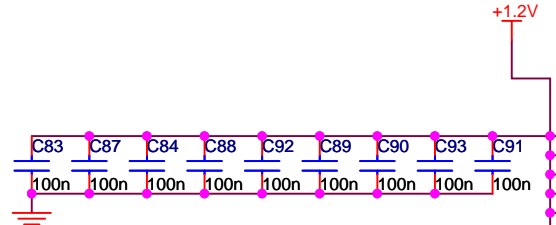
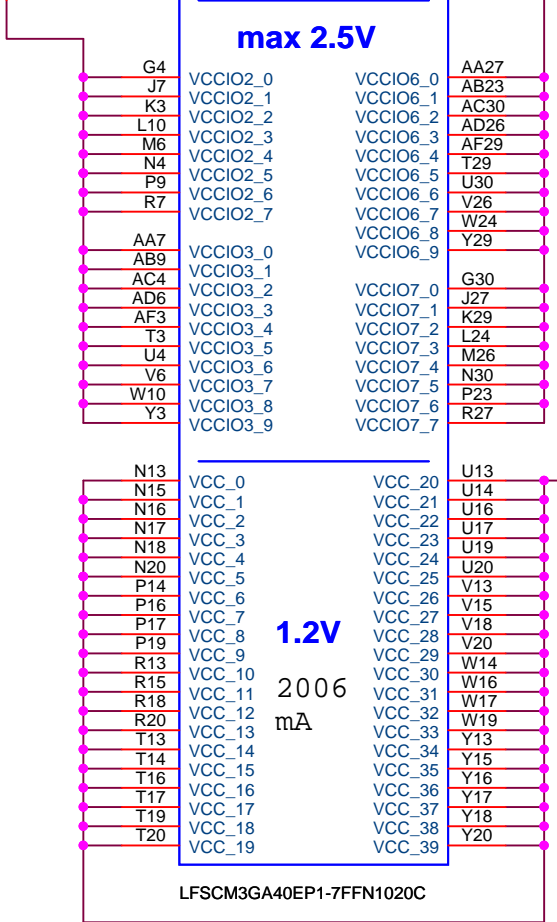


Place caps very close to pins VCC_T and VCC_R

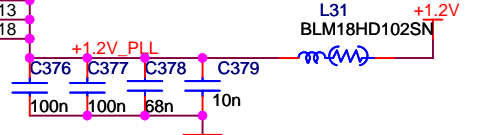
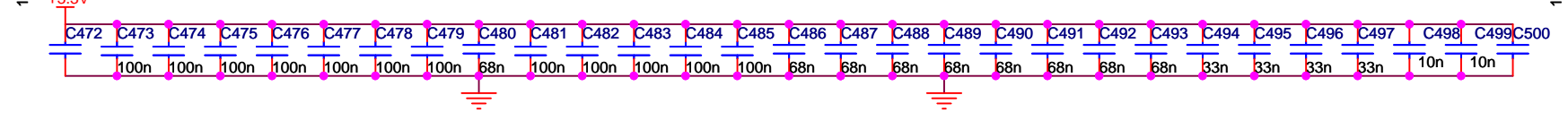
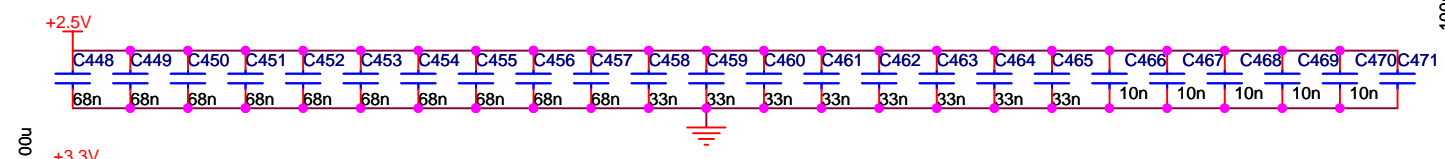
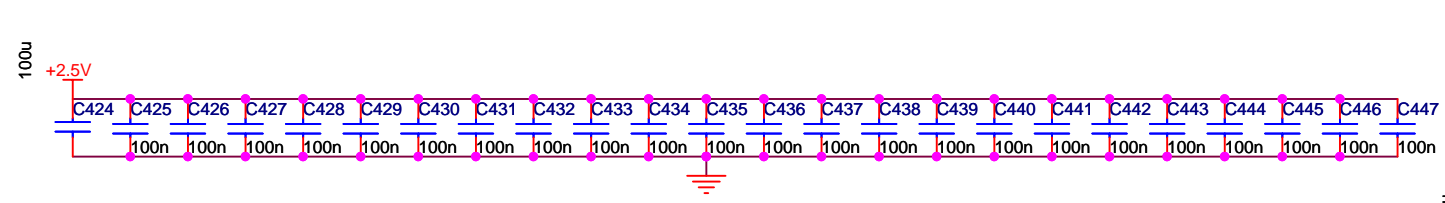
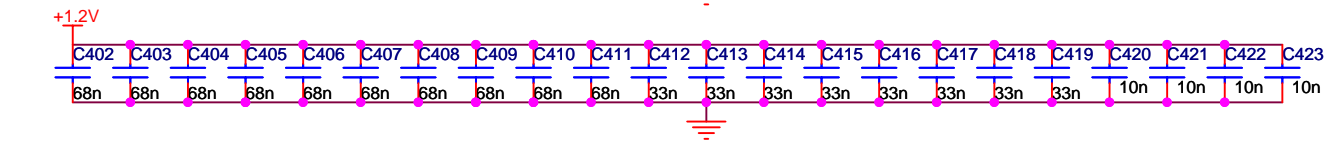
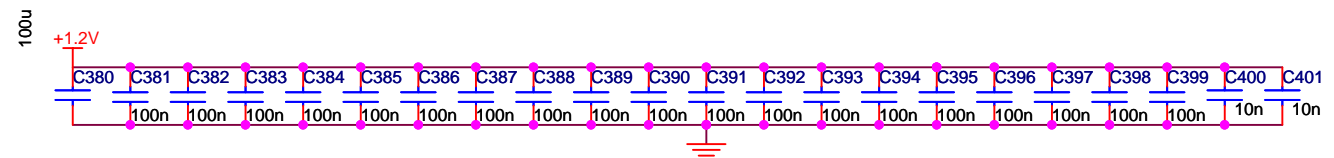
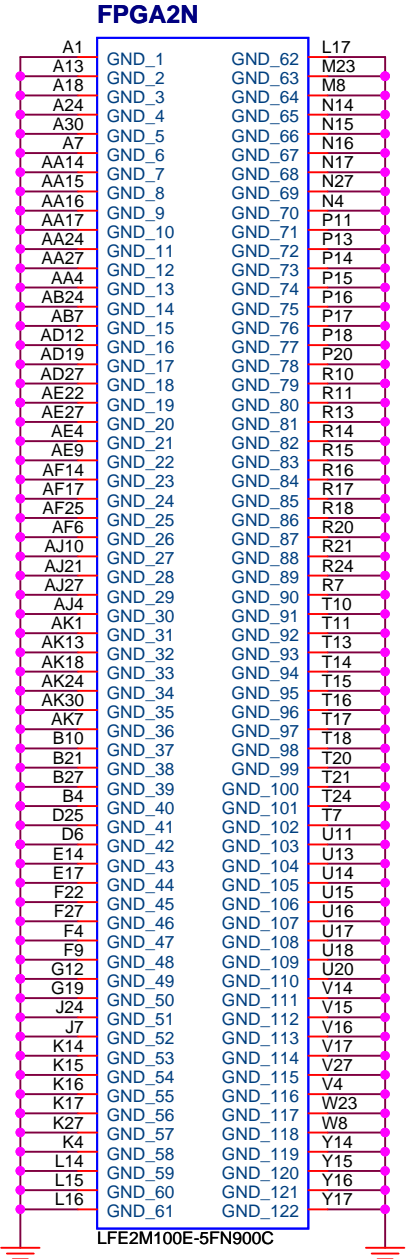
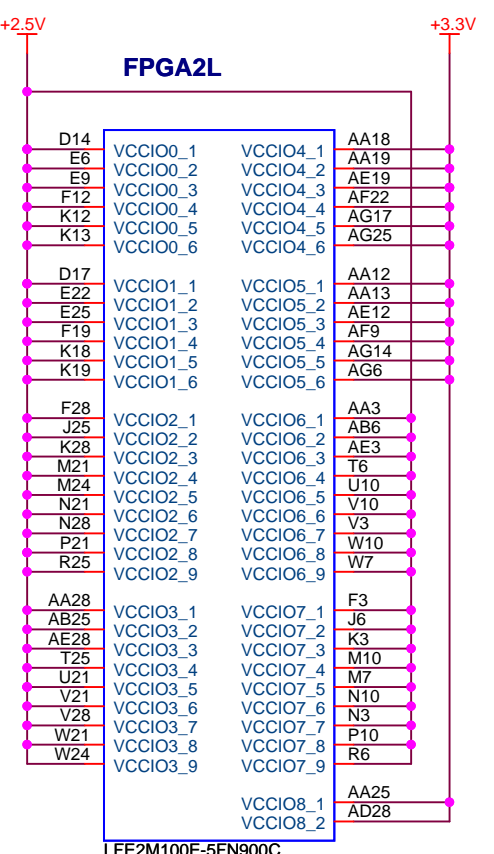
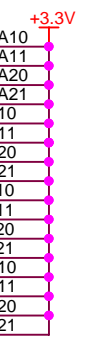
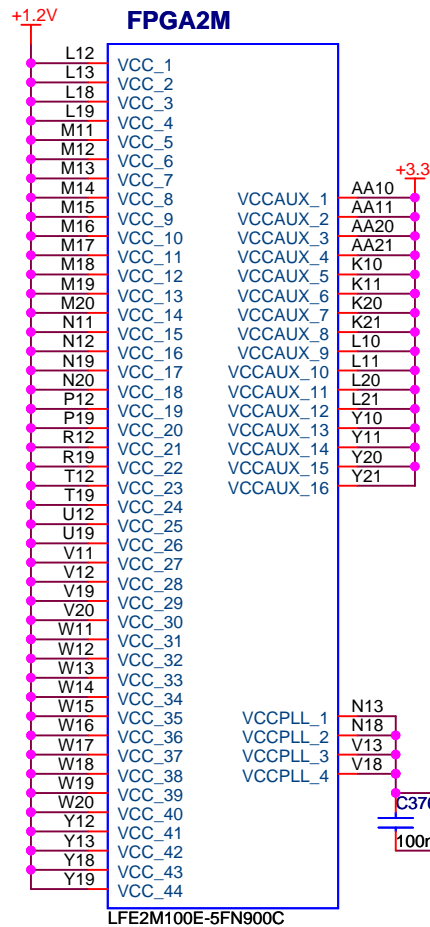
Title			12_FPGA2_SERDES		
Size	Document Number				Rev
A3	<Doc>				<RevC>
Date:	Monday, April 19, 2010		Sheet	13	of 16

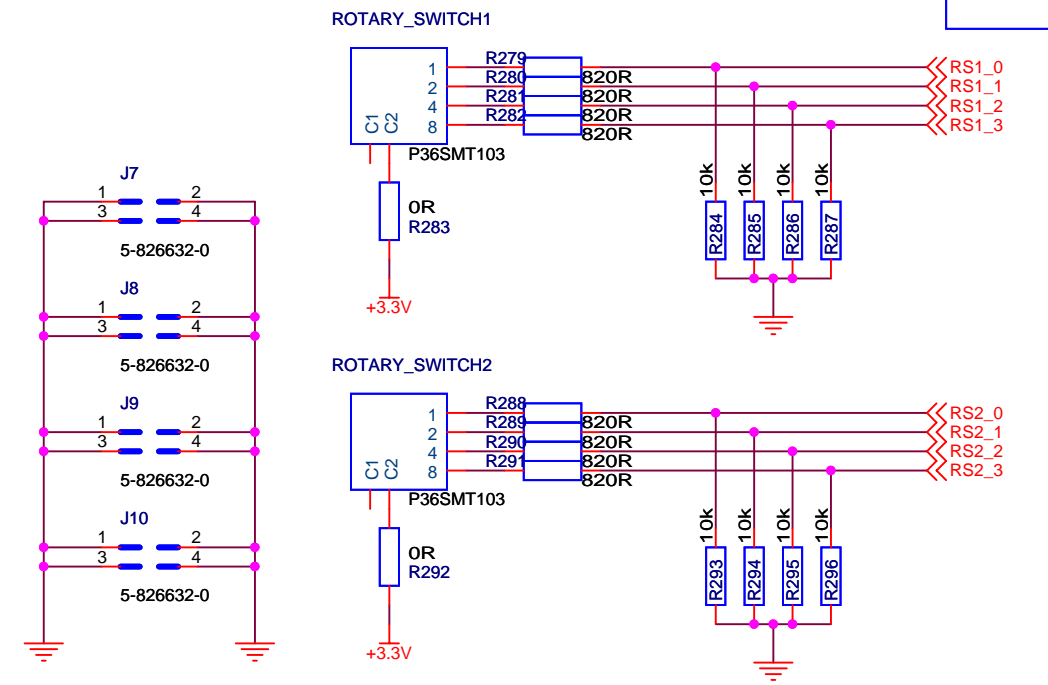
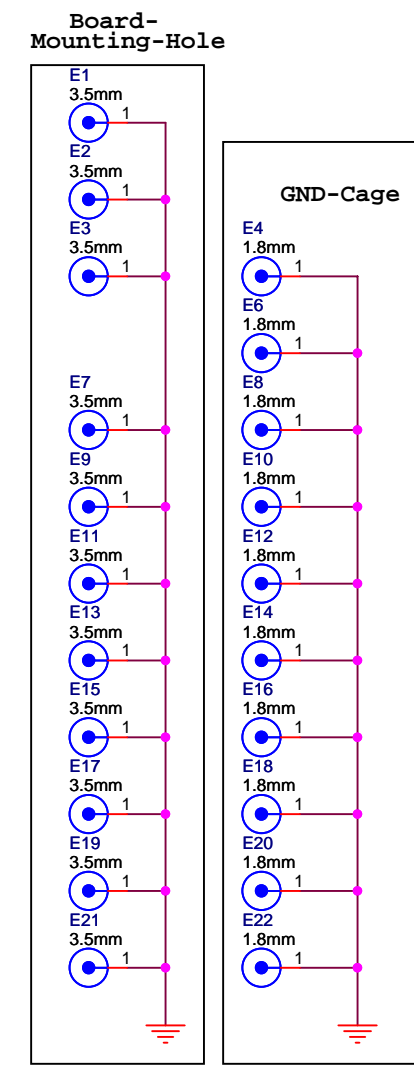
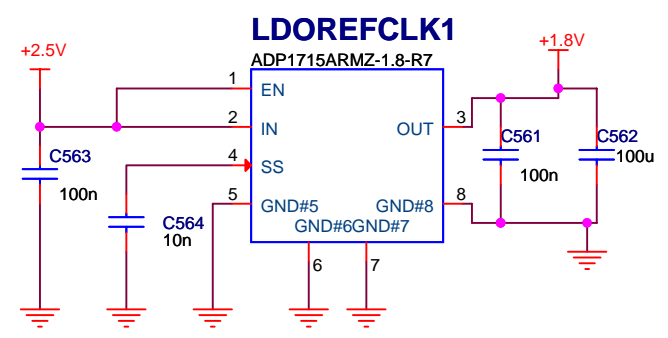
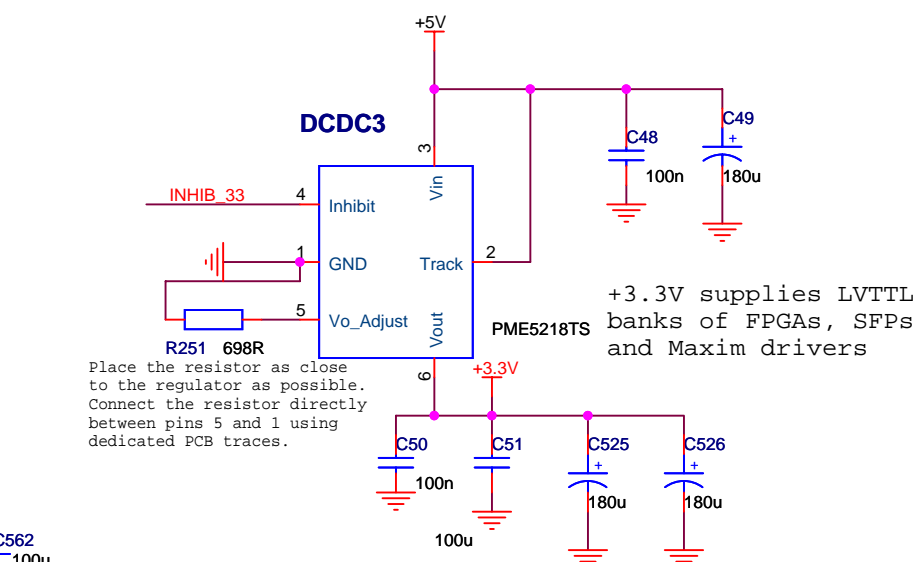
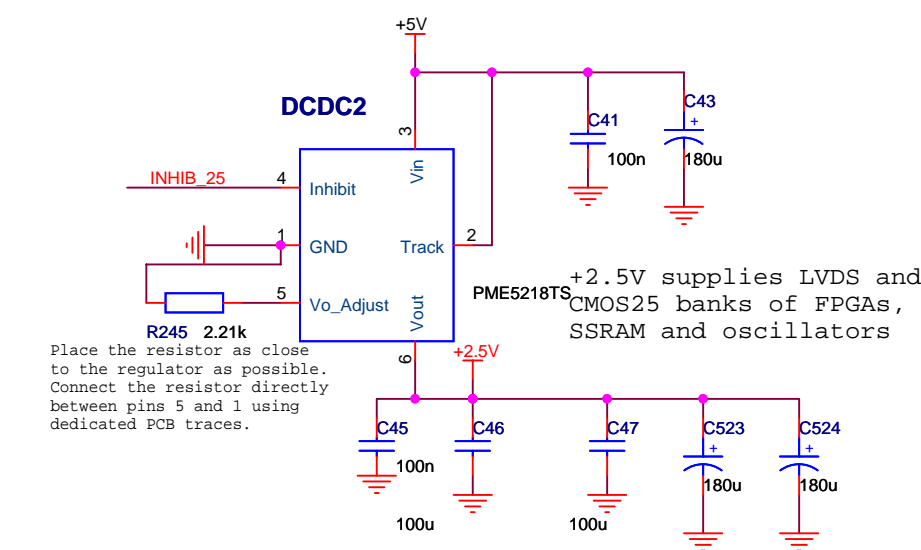
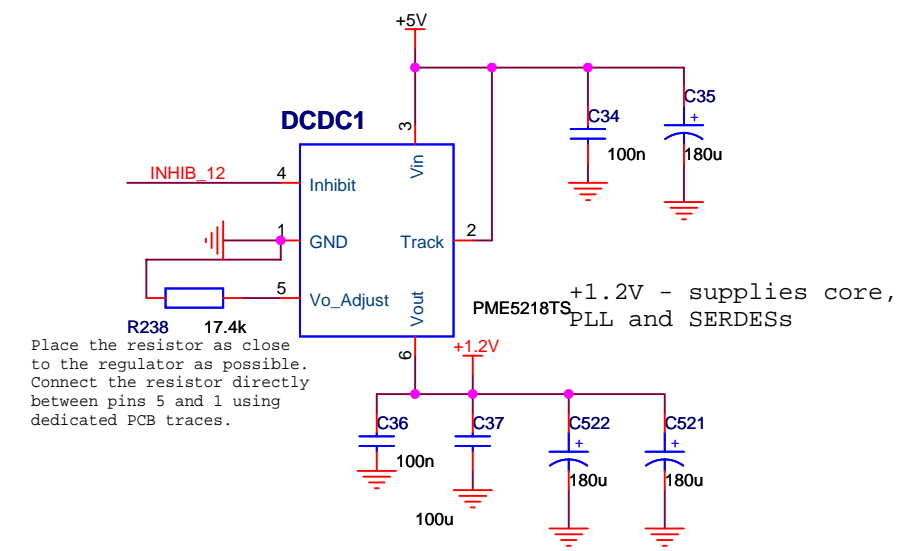
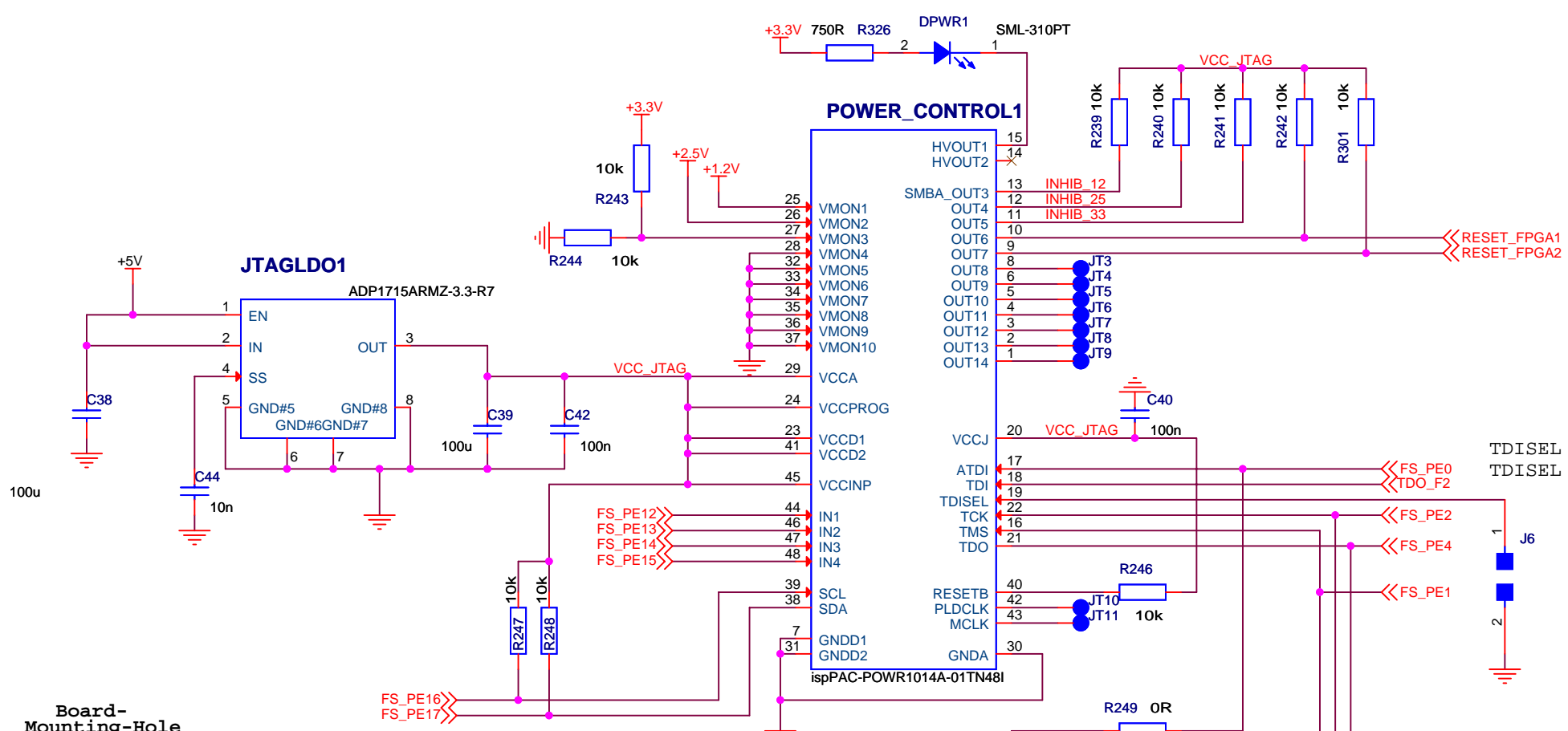


All currents from DS1004 v02.2 page 3-3



Title			13_DECOUPLING		
Size	Document Number	Rev			
A3	<Doc>	<RevC>			
Date:	Monday, April 19, 2010	Sheet	14	of	16





Title			15_POWER		
Size	Document Number		Rev		
A3	<Doc>		<RevC		
Date:	Monday, April 19, 2010	Sheet	16	of	16