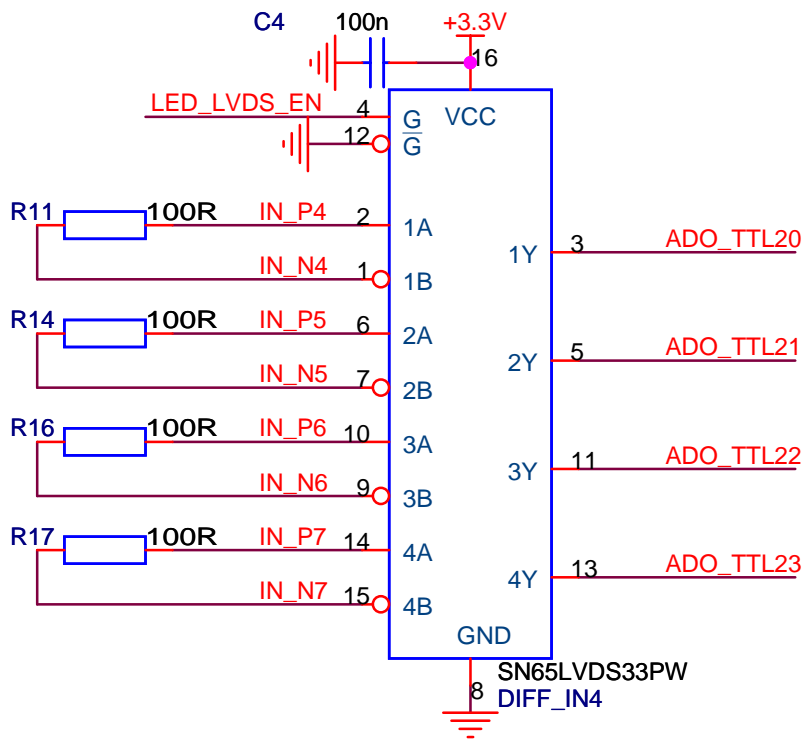


ADO\_TTL[46..0] >>>

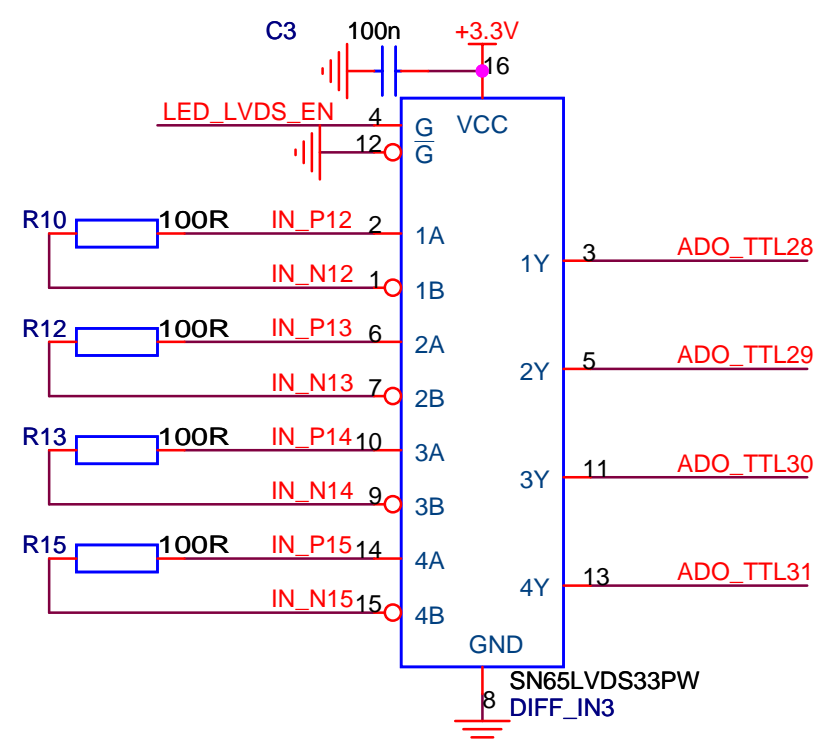
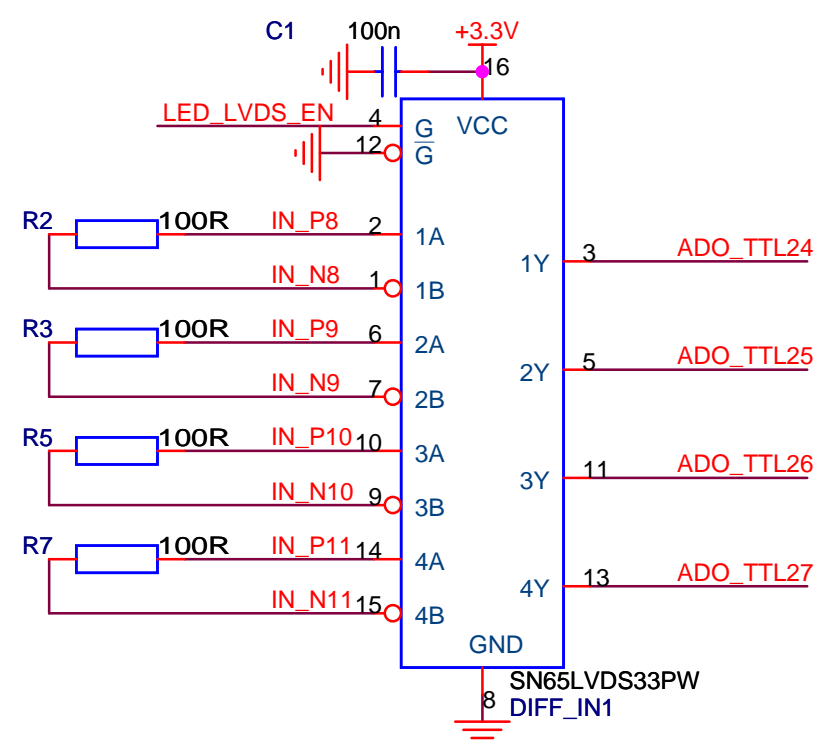


JDIF1					
IN_P0	1	2	IN_N0		
IN_P1	3	4	IN_N1		
IN_P2	5	6	IN_N2		
IN_P3	7	8	IN_N3		
IN_P4	9	10	IN_N4		
IN_P5	11	12	IN_N5		
IN_P6	13	14	IN_N6		
IN_P7	15	16	IN_N7		

3M-3408-5502

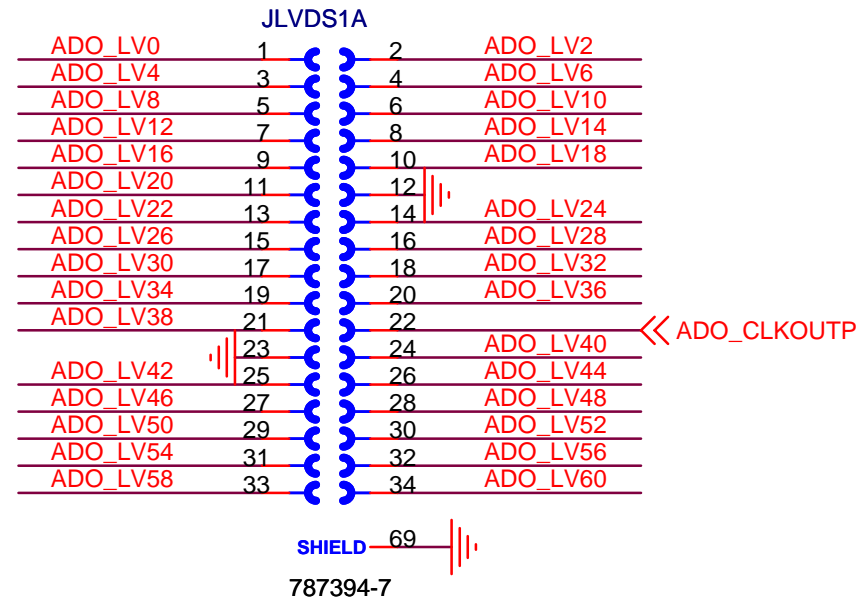
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IN_P9	3	4	IN_N9		
IN_P10	5	6	IN_N10		
IN_P11	7	8	IN_N11		
IN_P12	9	10	IN_N12		
IN_P13	11	12	IN_N13		
IN_P14	13	14	IN_N14		
IN_P15	15	16	IN_N15		

3M-3408-5502

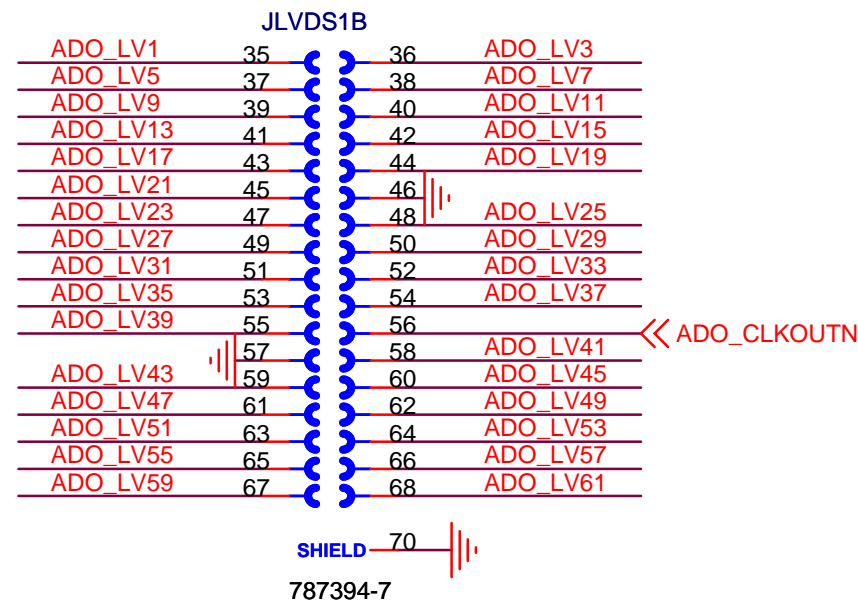


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ADO\_LV[61..0] >>

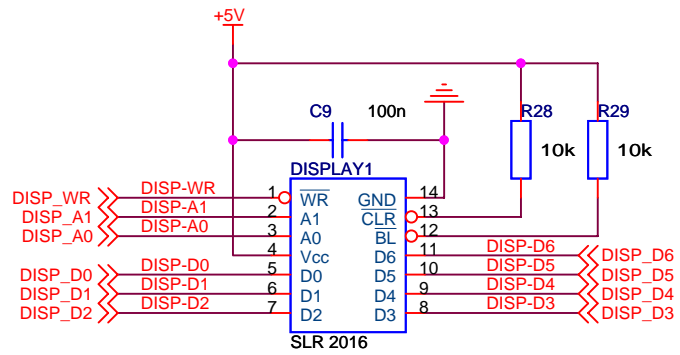
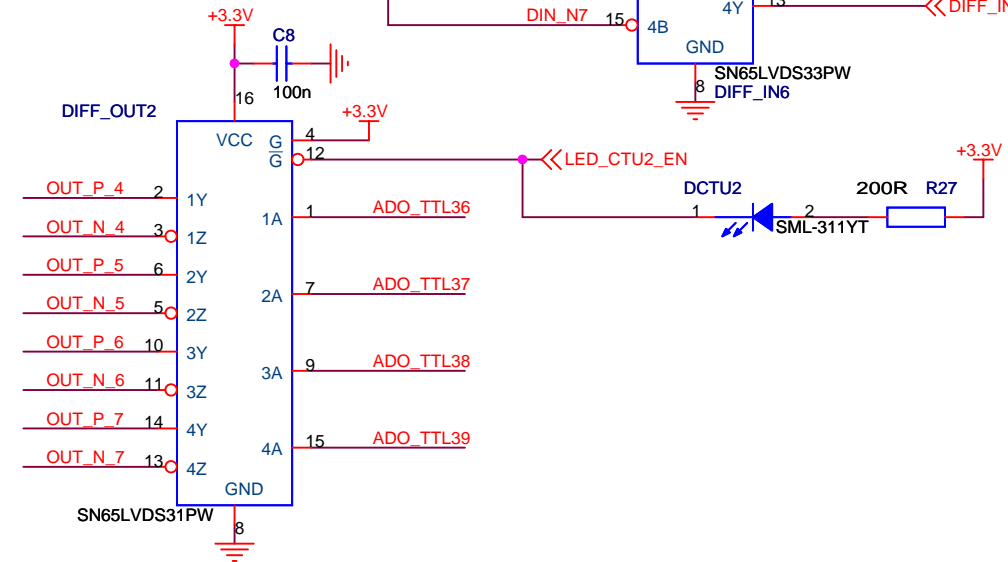
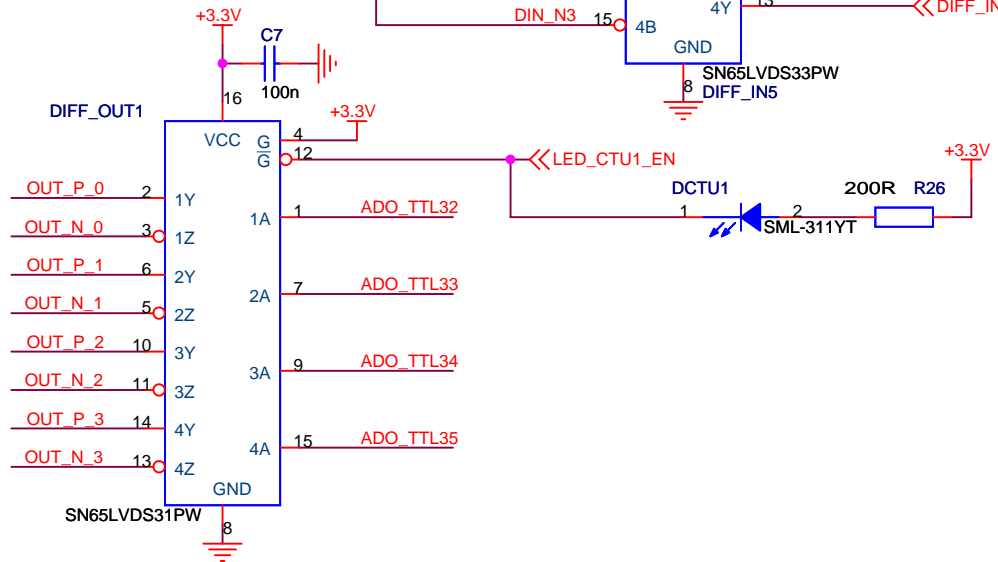
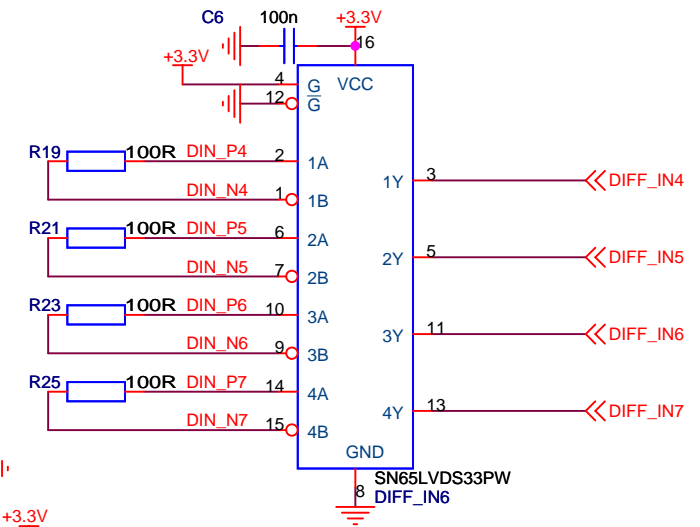
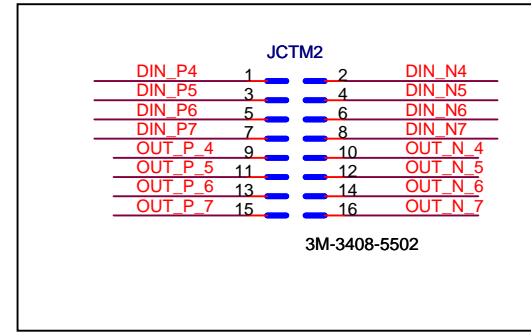
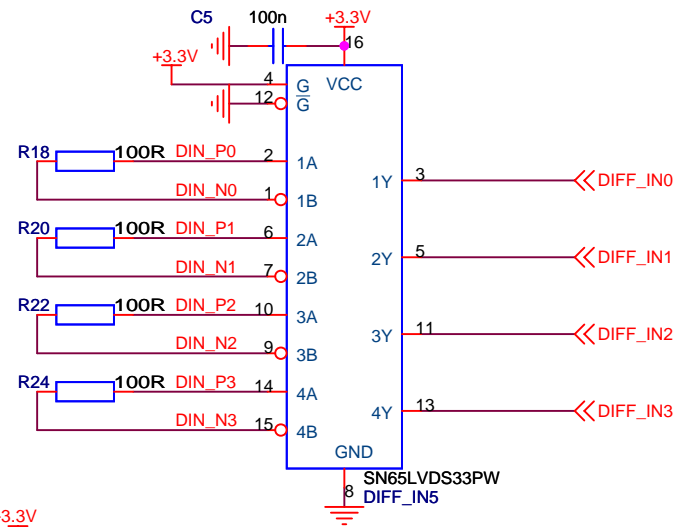
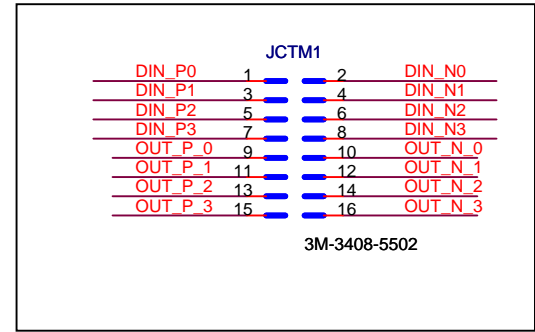
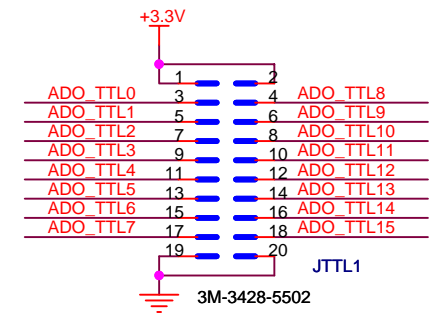
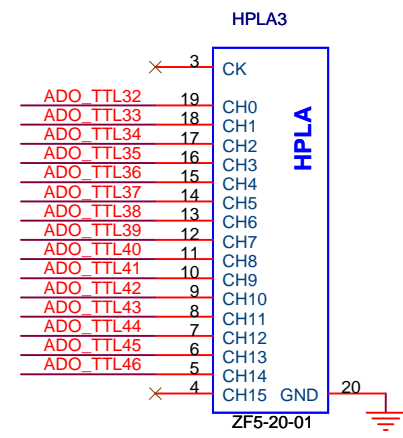
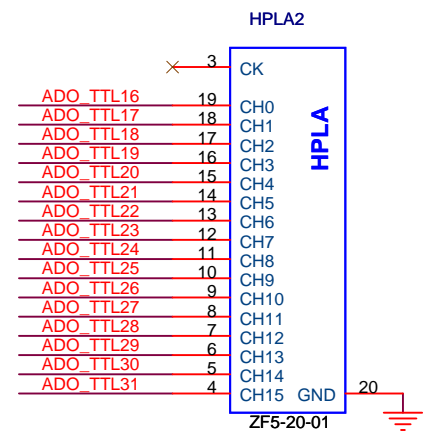
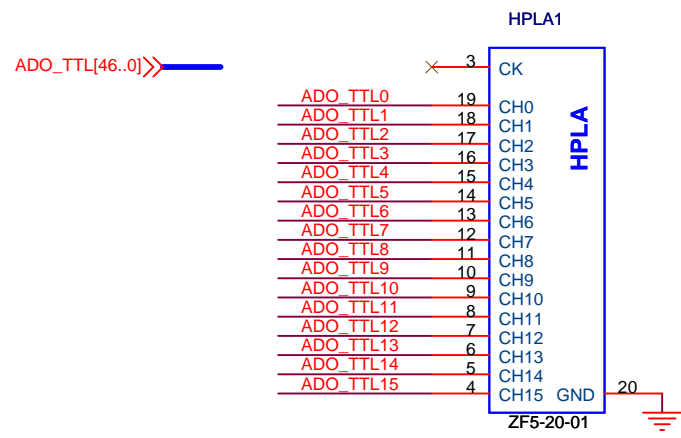


ADO\_LV0, ADO\_LV1 - pair 0 pins 1, 35  
 ADO\_LV2, ADO\_LV3 - pair 1 pins 2, 36  
 ADO\_LV4, ADO\_LV5 - pair 2 pins 3, 37  
 ADO\_LV6, ADO\_LV7 - pair 3 pins 4, 38  
 ADO\_LV8, ADO\_LV9 - pair 4 pins 5, 39  
 ADO\_LV10, ADO\_LV11 - pair 5 pins 6, 40  
 ADO\_LV12, ADO\_LV13 - pair 6 pins 7, 41  
 ADO\_LV14, ADO\_LV15 - pair 7 pins 8, 42  
 ADO\_LV16, ADO\_LV17 - pair 8 pins 9, 43  
 ADO\_LV18, ADO\_LV19 - pair 9 pins 10, 44  
 ADO\_LV20, ADO\_LV21 - pair 10 pins 11, 45  
 ADO\_LV22, ADO\_LV23 - pair 11 pins 13, 47  
 ADO\_LV24, ADO\_LV25 - pair 12 pins 14, 48  
 ADO\_LV26, ADO\_LV27 - pair 13 pins 15, 49  
 ADO\_LV28, ADO\_LV29 - pair 14 pins 16, 50  
 ADO\_LV30, ADO\_LV31 - pair 15 pins 17, 51

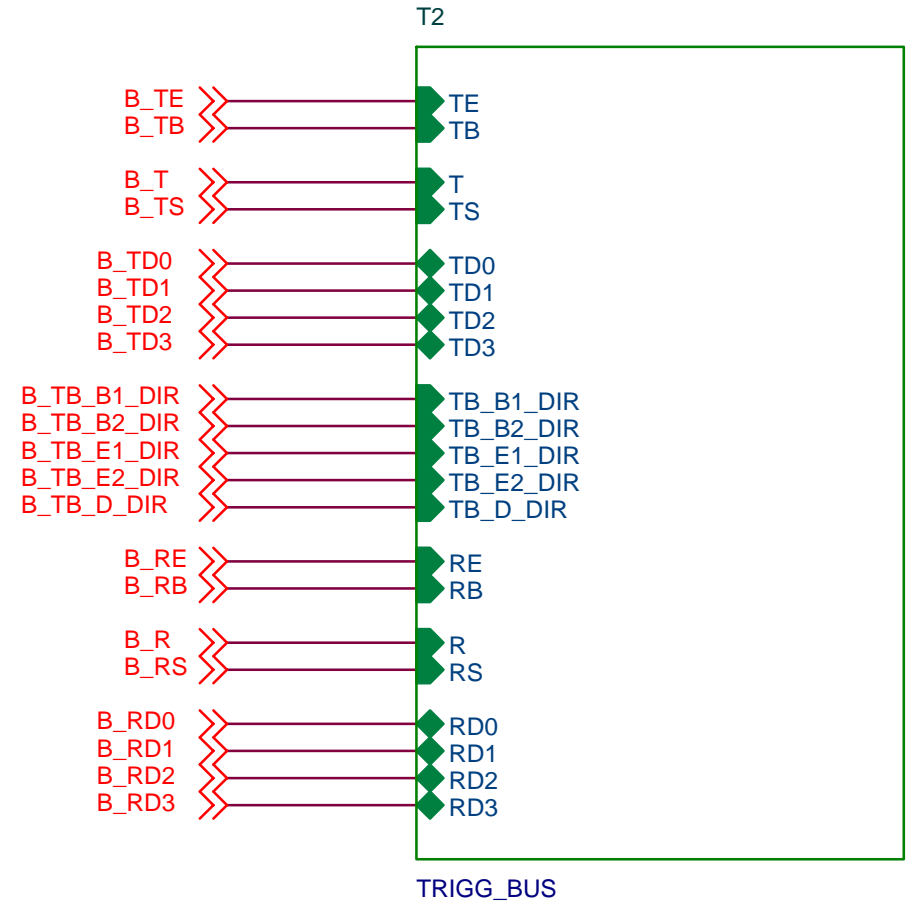
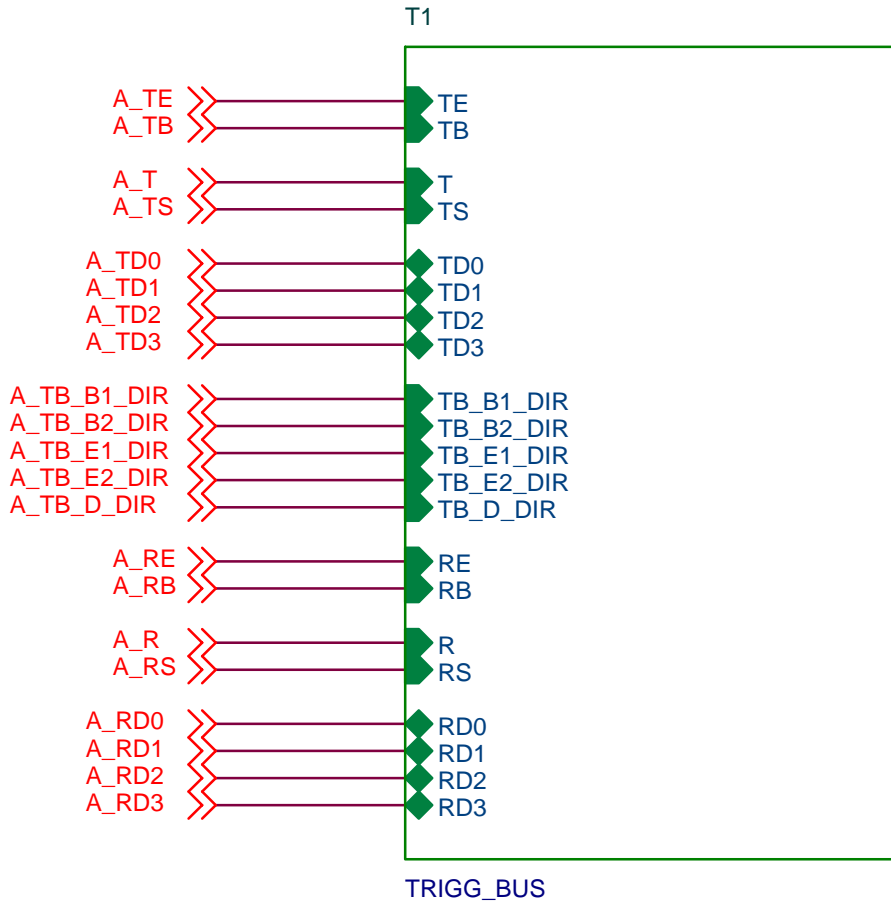


ADO\_LV32, ADO\_LV33 - pair 0 pins 18, 52  
 ADO\_LV34, ADO\_LV35 - pair 1 pins 19, 53  
 ADO\_LV36, ADO\_LV37 - pair 2 pins 20, 54  
 ADO\_LV38, ADO\_LV39 - pair 3 pins 21, 55  
 ADO\_CLKOUTP, ADO\_CLKOUTN - pair 4 pins 22, 56  
 ADO\_LV40, ADO\_LV41 - pair 5 pins 24, 58  
 ADO\_LV42, ADO\_LV43 - pair 6 pins 25, 59  
 ADO\_LV44, ADO\_LV45 - pair 7 pins 26, 60  
 ADO\_LV46, ADO\_LV47 - pair 8 pins 27, 61  
 ADO\_LV48, ADO\_LV49 - pair 9 pins 28, 62  
 ADO\_LV50, ADO\_LV51 - pair 10 pins 29, 63  
 ADO\_LV52, ADO\_LV53 - pair 11 pins 30, 64  
 ADO\_LV54, ADO\_LV55 - pair 12 pins 31, 65  
 ADO\_LV56, ADO\_LV57 - pair 13 pins 32, 66  
 ADO\_LV58, ADO\_LV59 - pair 14 pins 33, 67  
 ADO\_LV60, ADO\_LV61 - pair 15 pins 34, 68

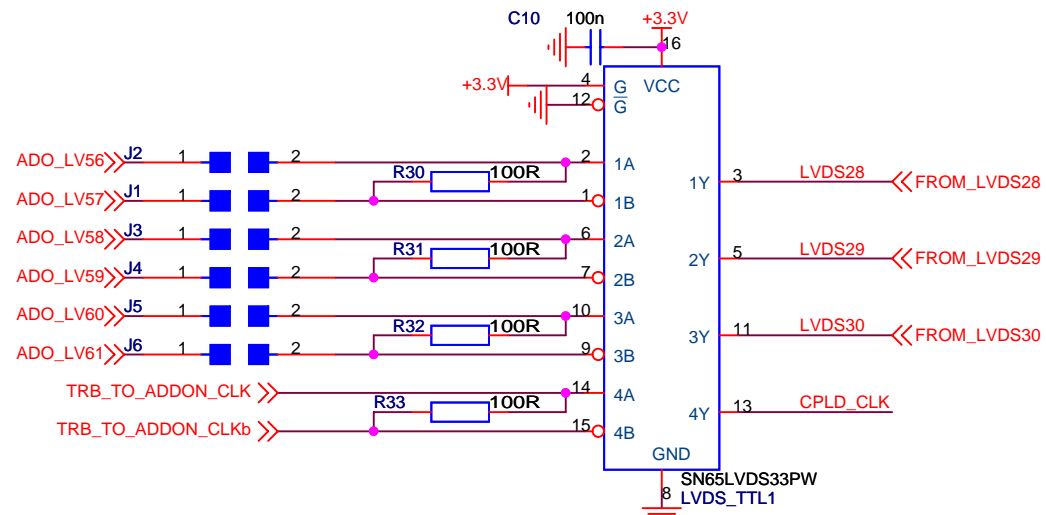
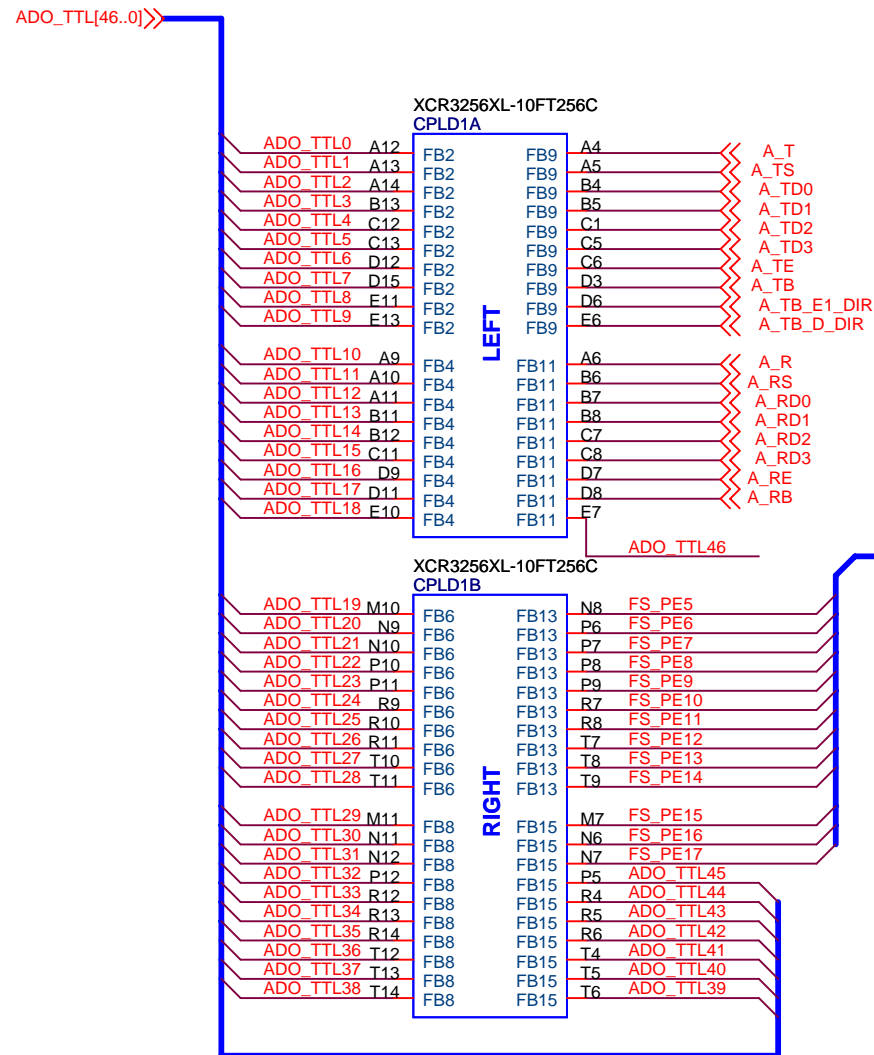
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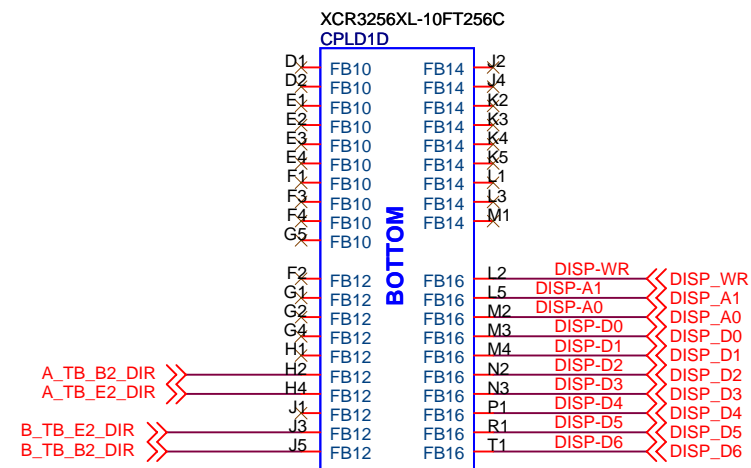
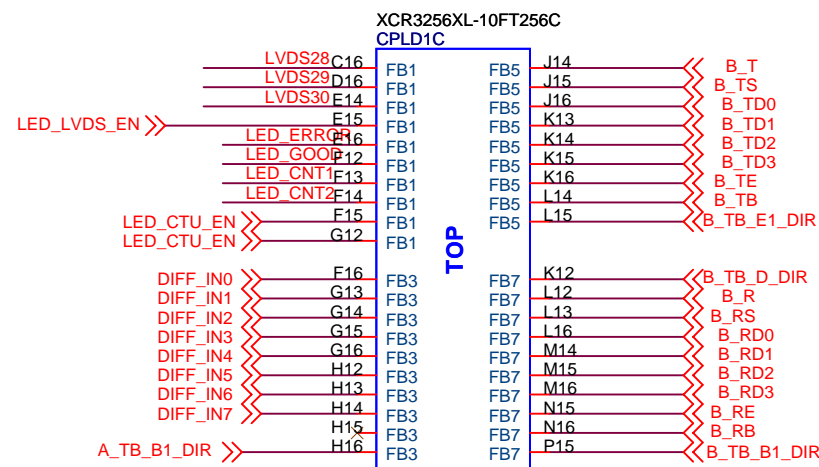
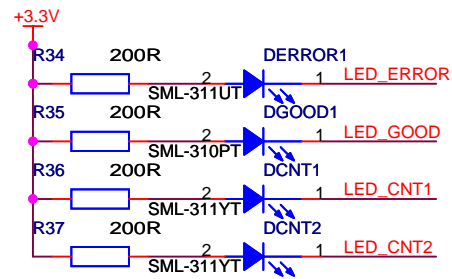
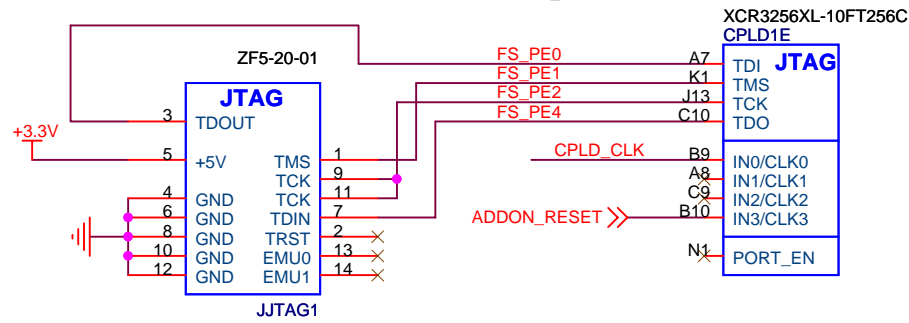
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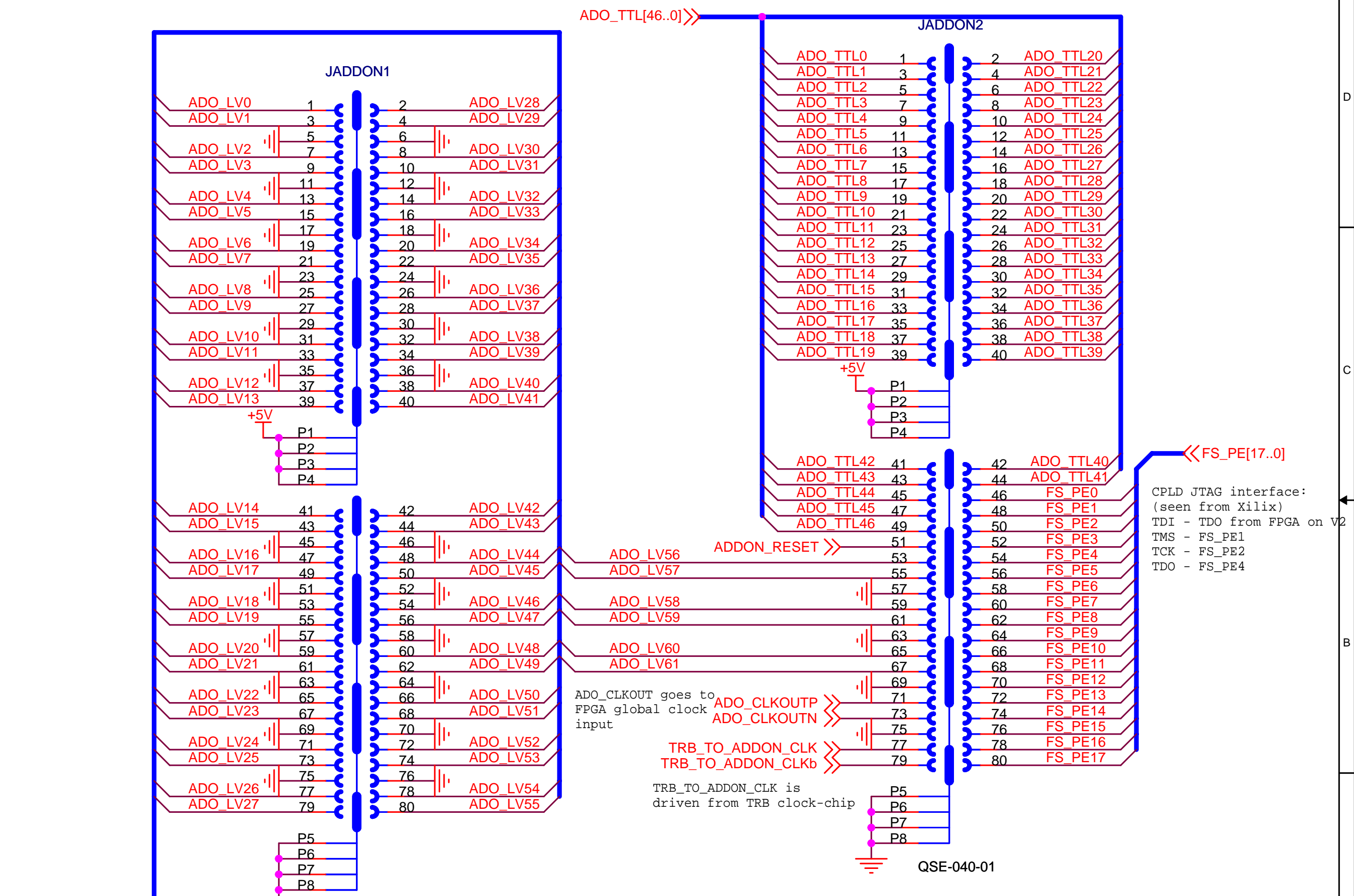


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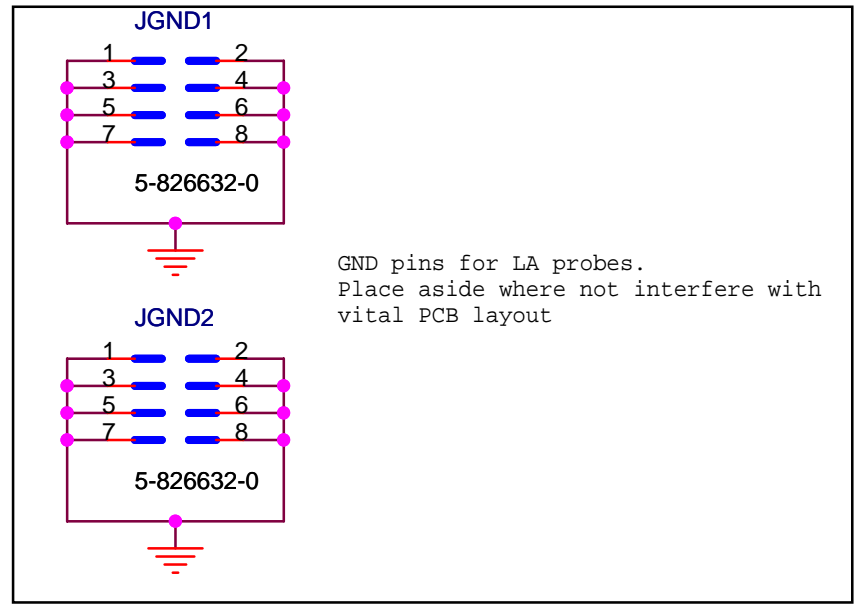
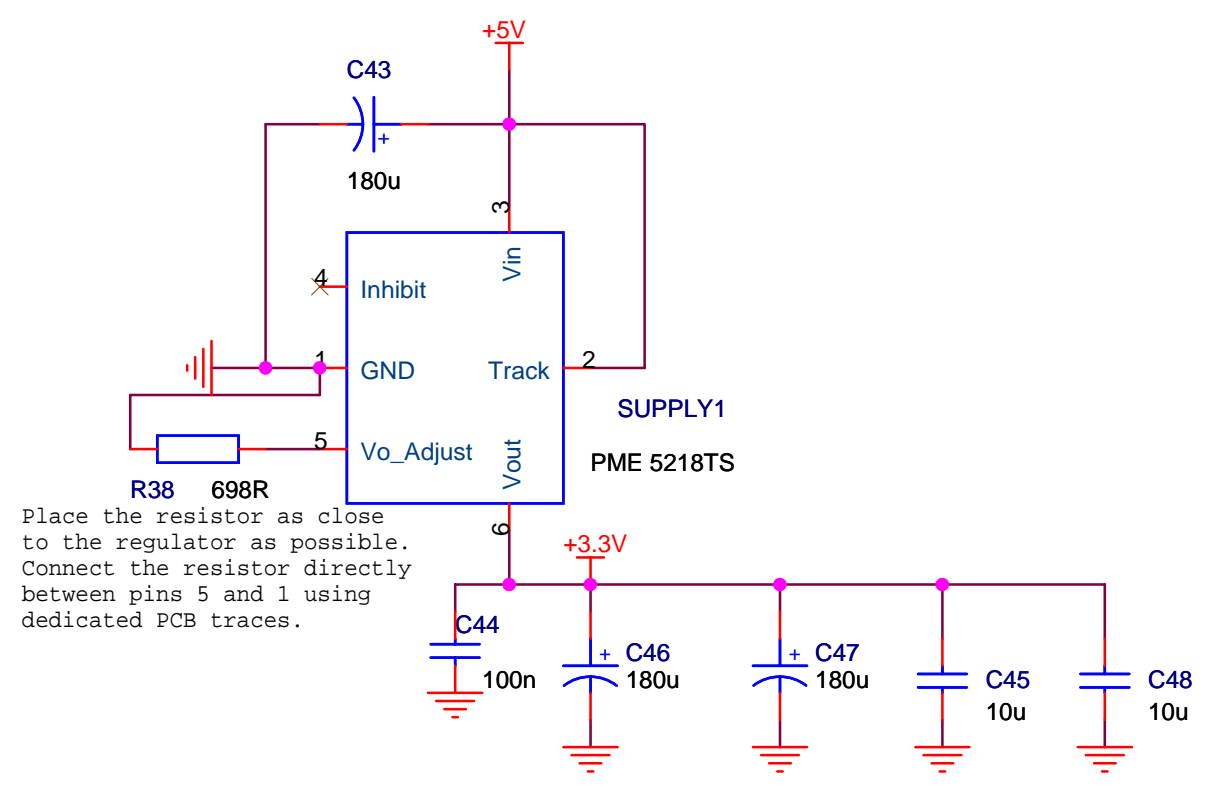
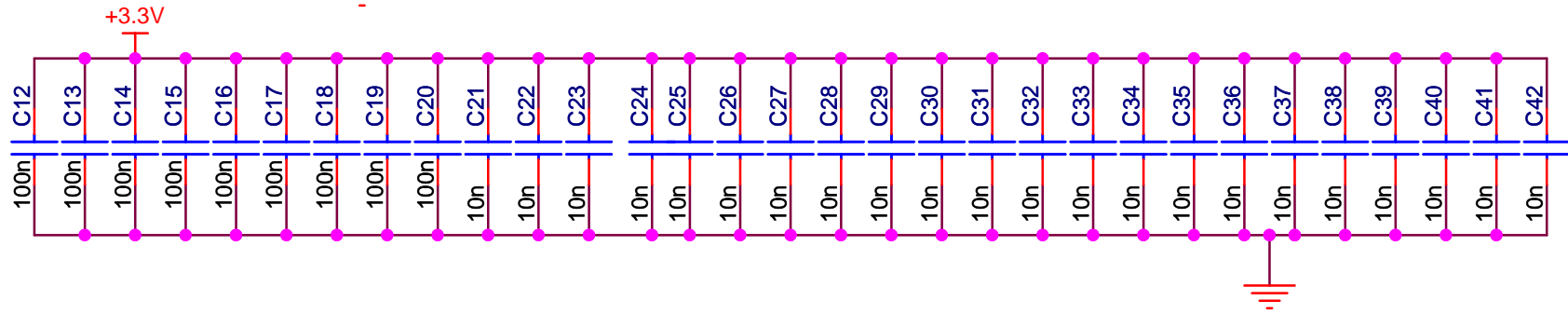
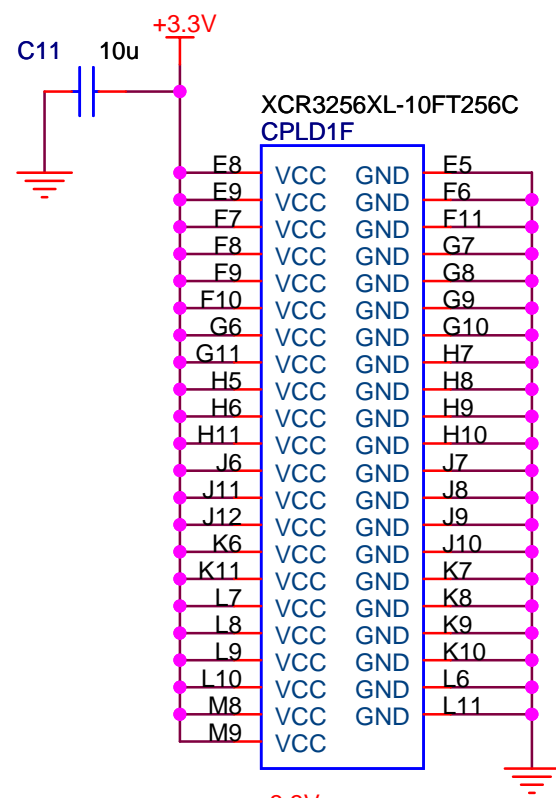
CPLD JTAG interface:  
(seen from Xilinx)  
TDI - TDO from FPGA on HadesTRBv2  
TMS - FS\_PE1  
TCK - FS\_PE2  
TDO - FS\_PE4



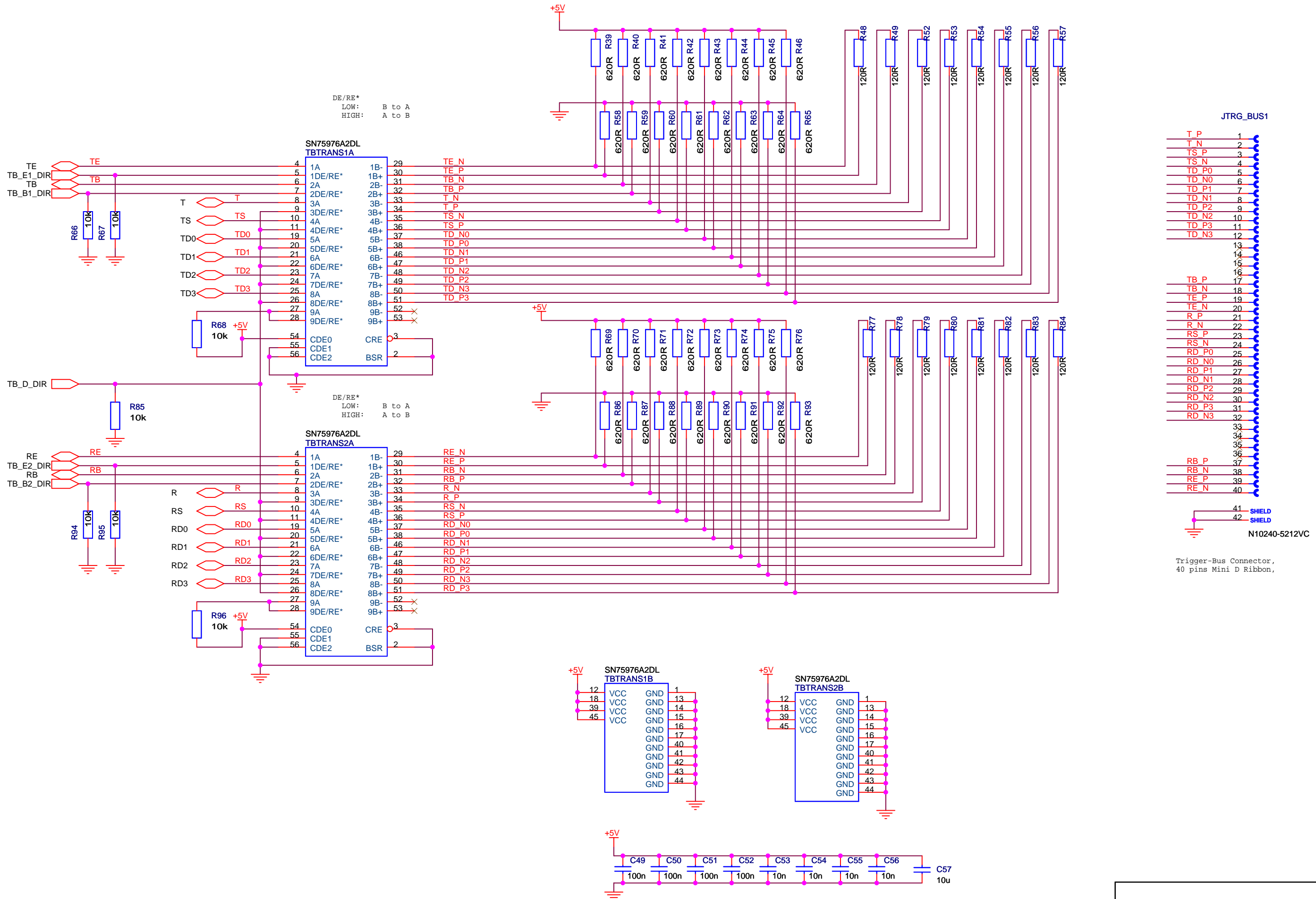


CPLD JTAG interface:  
 (seen from Xilinx)  
 TDI - TDO from FPGA on V2  
 TMS - FS\_PE1  
 TCK - FS\_PE2  
 TDO - FS\_PE4

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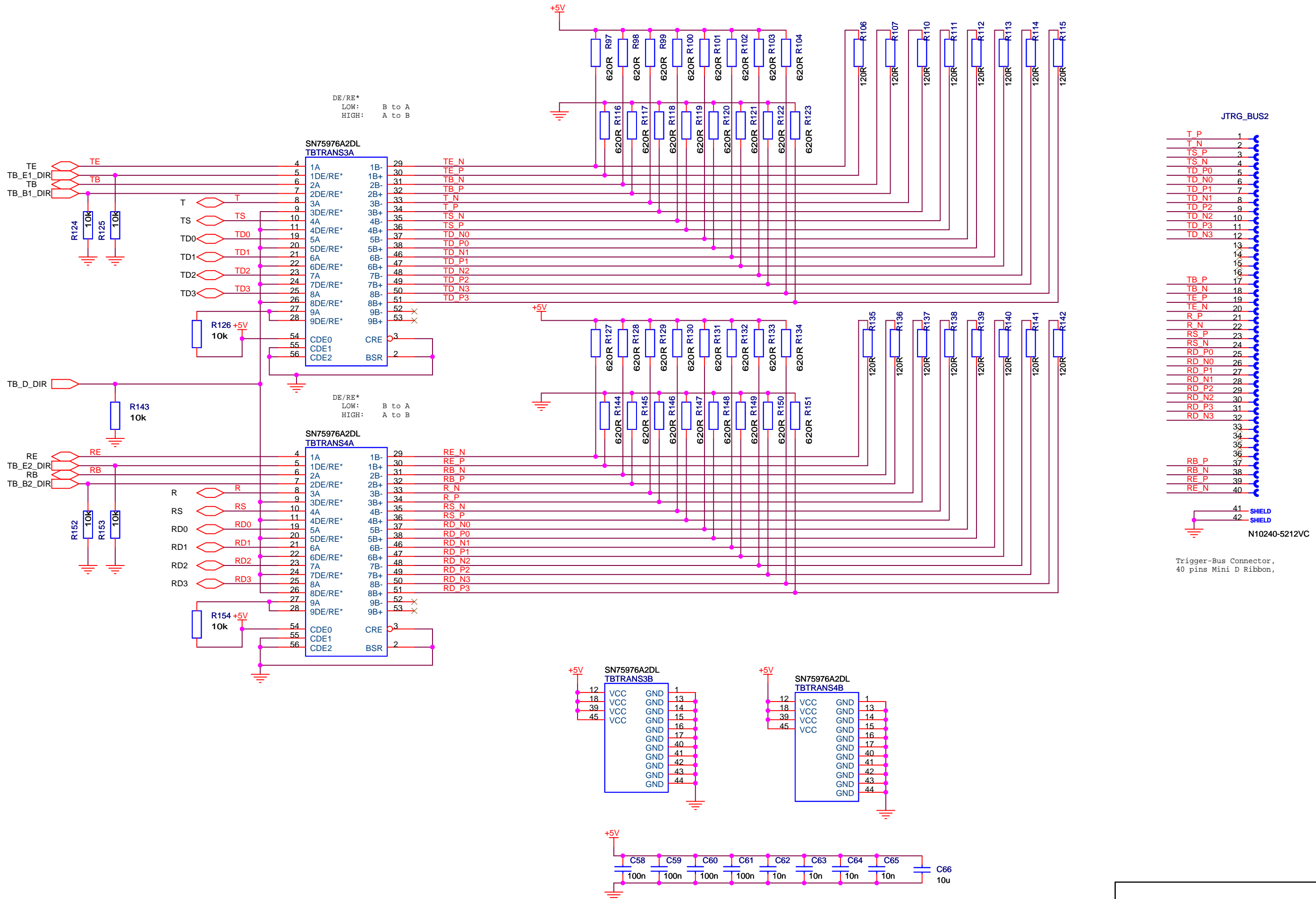


**JTRG\_BUS1**

T P	1
T N	2
TS P	3
TS N	4
TD P0	5
TD N0	6
TD P1	7
TD N1	8
TD P2	9
TD N2	10
TD P3	11
TD N3	12
	13
	14
	15
	16
TB P	17
TB N	18
TE P	19
TE N	20
R P	21
R N	22
RS P	23
RS N	24
RD P0	25
RD N0	26
RD P1	27
RD N1	28
RD P2	29
RD N2	30
RD P3	31
RD N3	32
	33
	34
	35
	36
	37
	38
	39
	40
	41 SHIELD
	42 SHIELD

N10240-5212VC  
Trigger-Bus Connector,  
40 pins Mini D Ribbon,





**JTRG\_BUS2**

T P	1
T N	2
TS P	3
TS N	4
TD P0	5
TD N0	6
TD P1	7
TD N1	8
TD P2	9
TD N2	10
TD P3	11
TD N3	12
	13
	14
	15
	16
TB P	17
TB N	18
TE P	19
TE N	20
R P	21
R N	22
RS P	23
RS N	24
RD P0	25
RD N0	26
RD P1	27
RD N1	28
RD P2	29
RD N2	30
RD P3	31
RD N3	32
	33
	34
	35
	36
RB P	37
RB N	38
RE P	39
RE N	40
	41 SHIELD
	42 SHIELD

N10240-5212VC  
Trigger-Bus Connector,  
40 pins Mini D Ribbon,