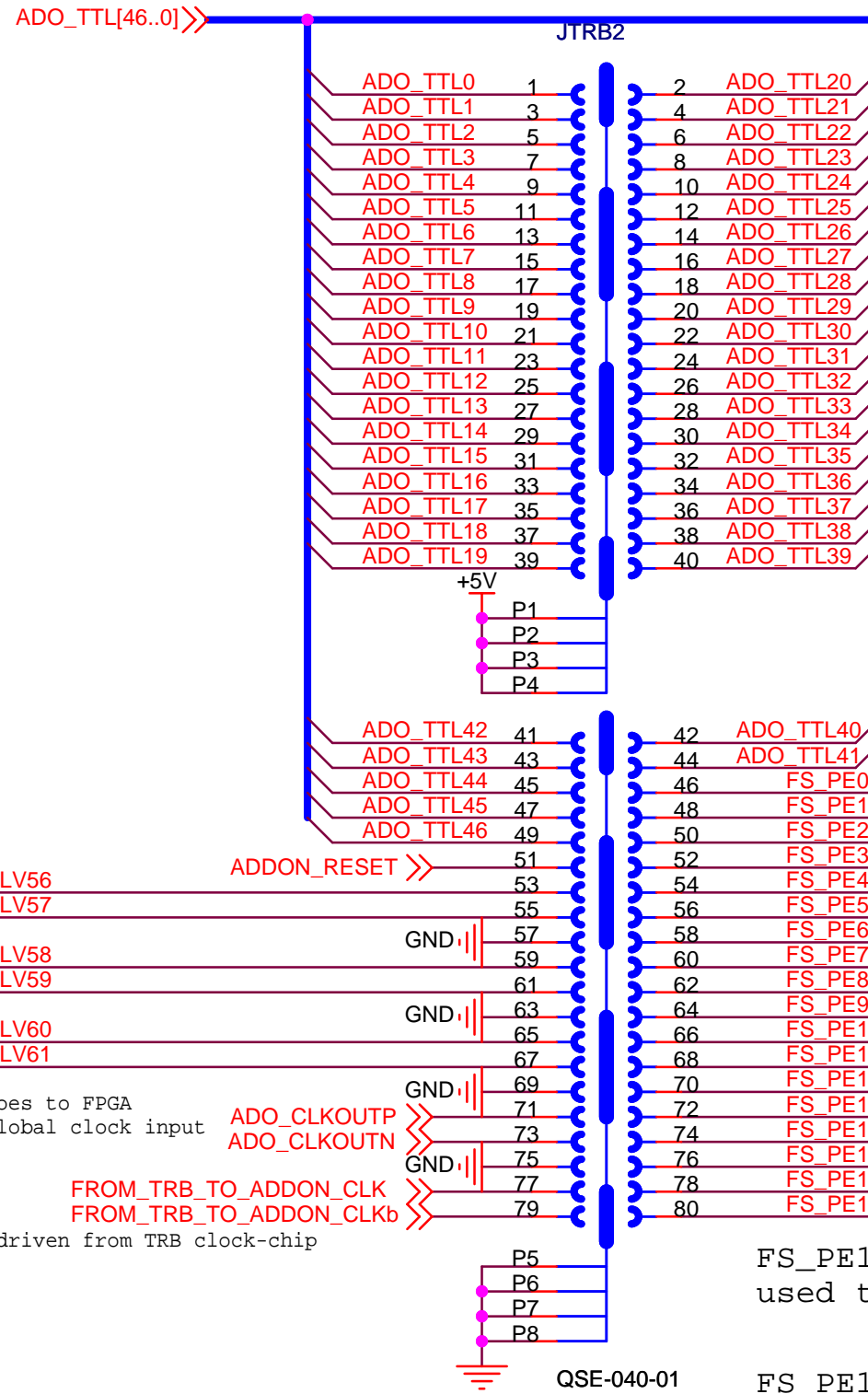
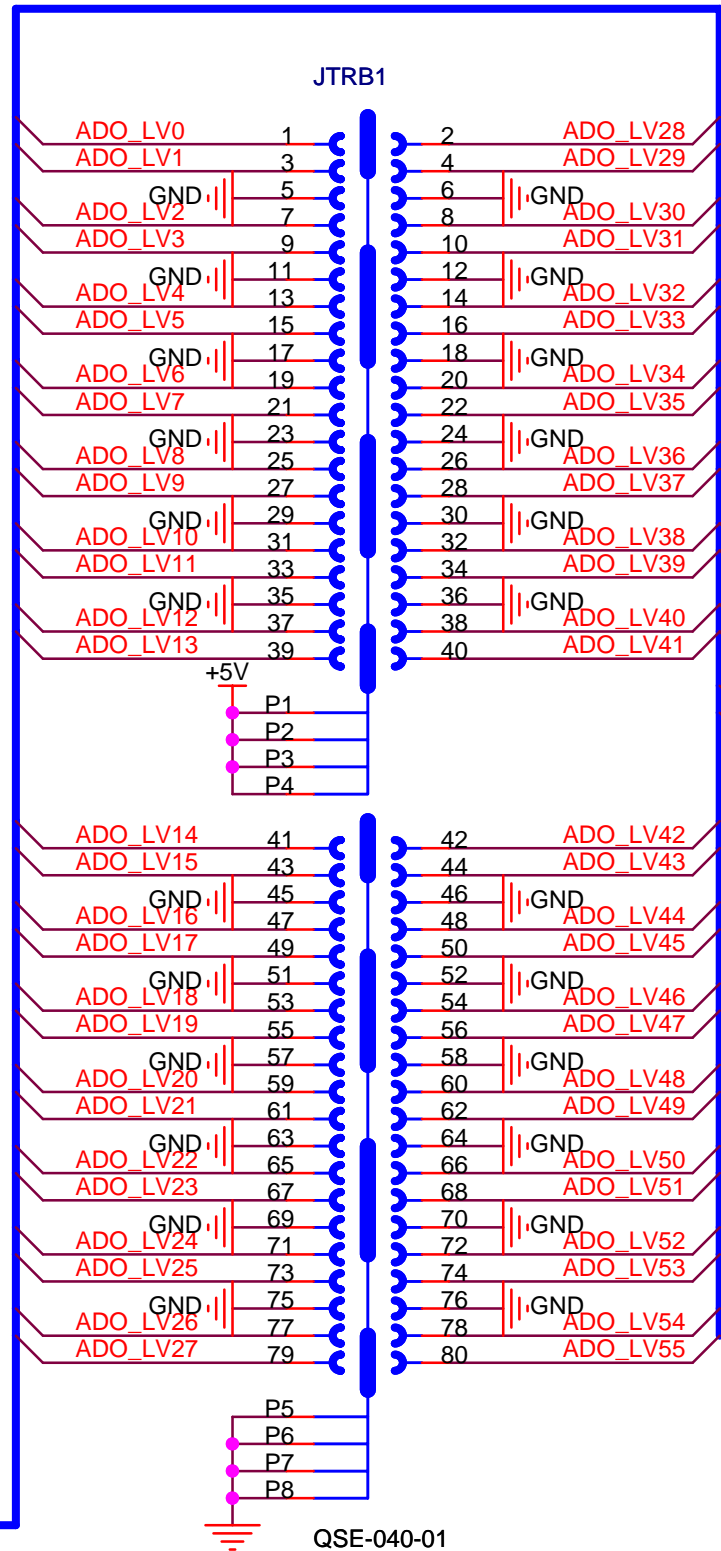


Even numbers: positive
 Odd numbers: negative



JTAG interface:
 (seen from TRB)
 TDI - TDO from FPGA on TRB (FS_PE0 high Z)
 TMS - FS_PE1
 TCK - FS_PE2
 TDO - FS_PE4

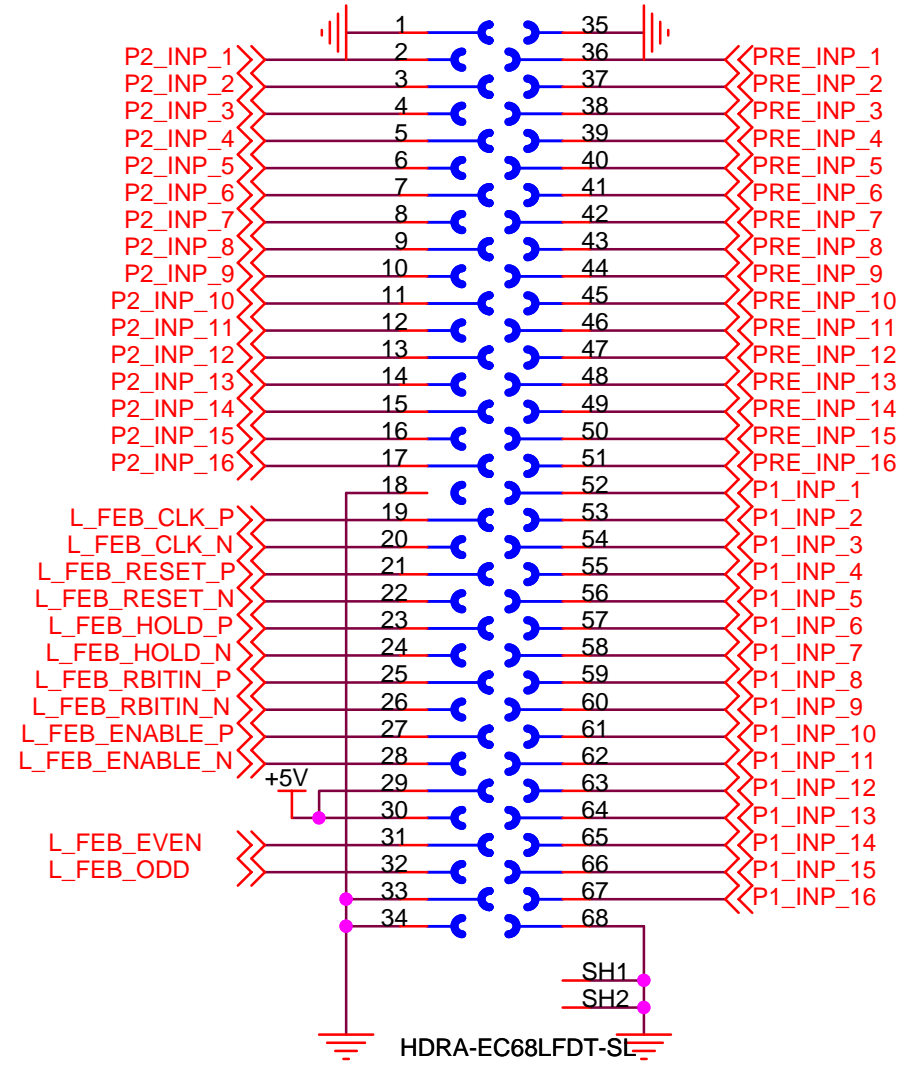
FS_PE16 (SCL) and FS_PE17 (SDA)
 used to control ispPAC-POWER chip

FS_PE12 - FS_PE15 connected to
 IN1 - IN4 in ispPAC-POWER chip
 general purpose inputs

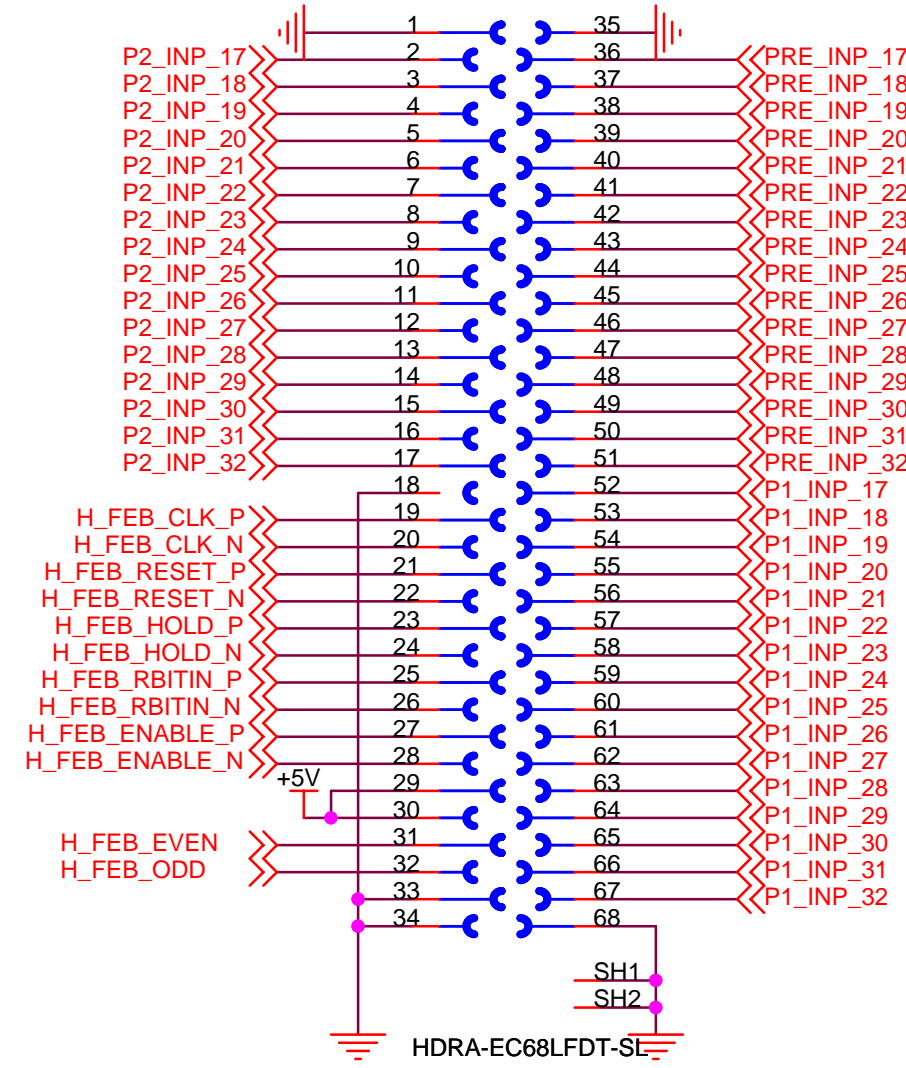
FS_PE11 - temperature control

Title			01_TRB_CONNECTORS		
Size	Document Number	Rev			
A4	<Doc>	<RevCo			
Date:	Saturday, September 08, 2007	Sheet	1	of	21

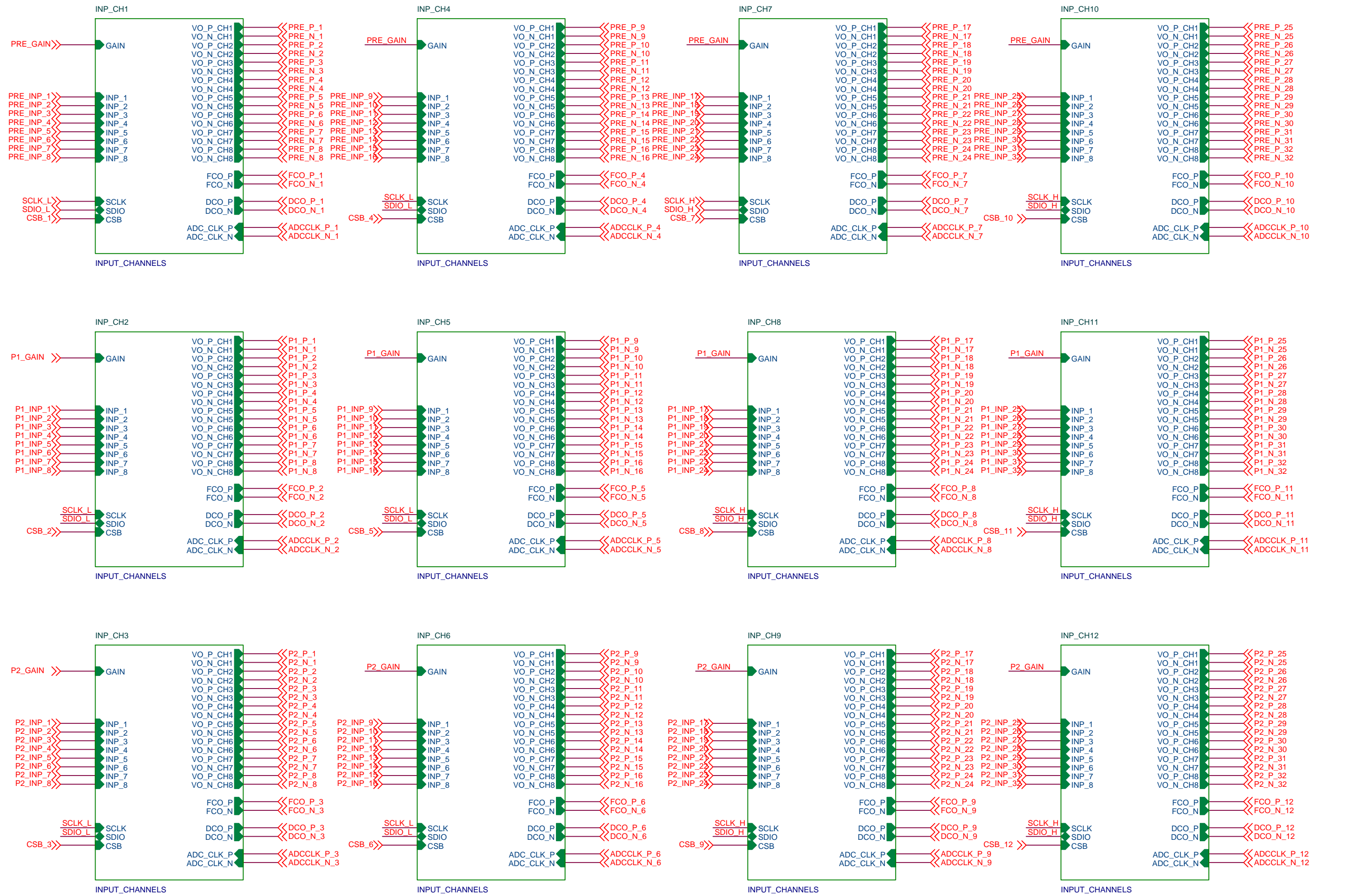
DET_LOW1



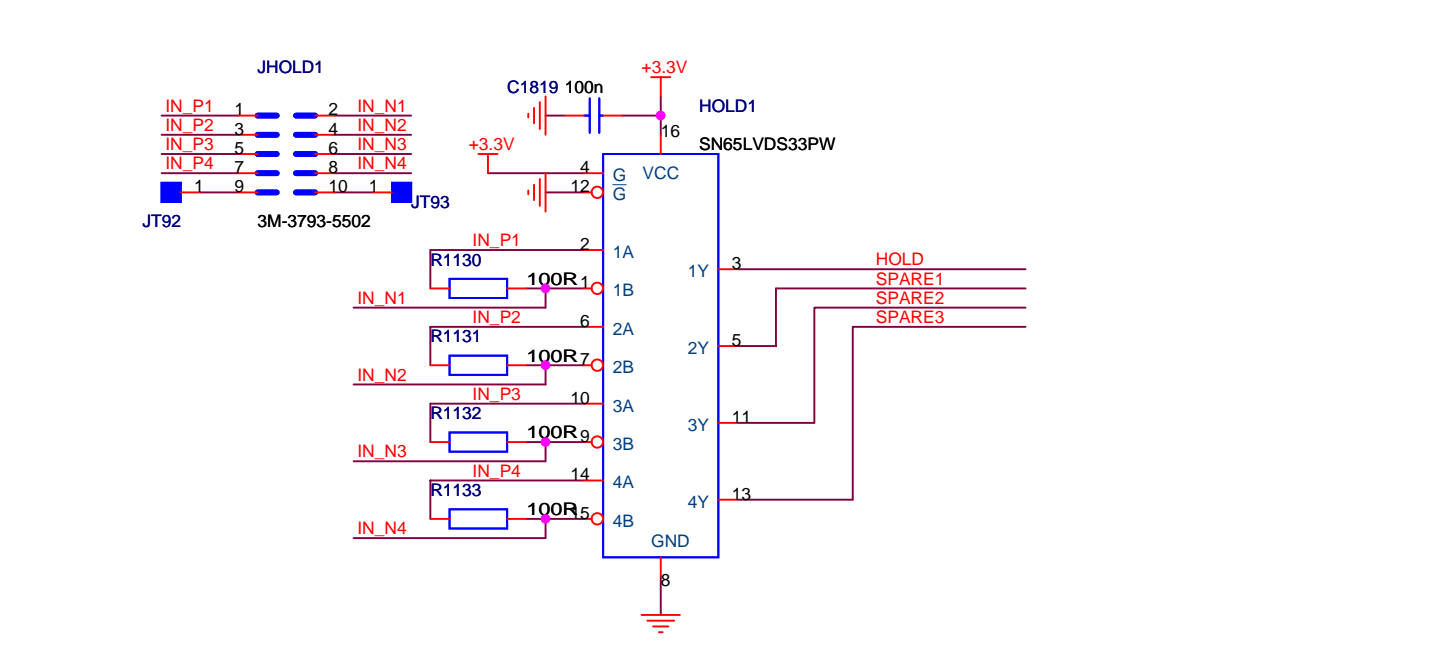
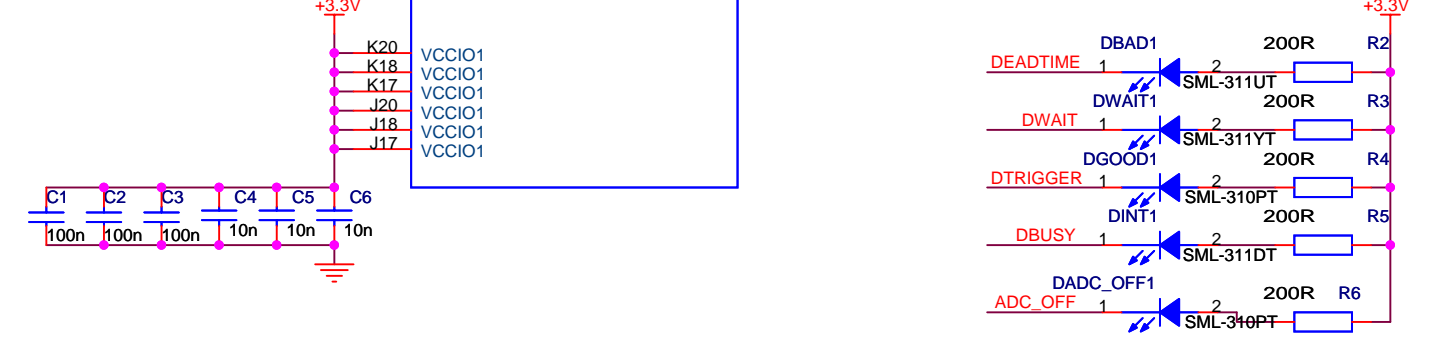
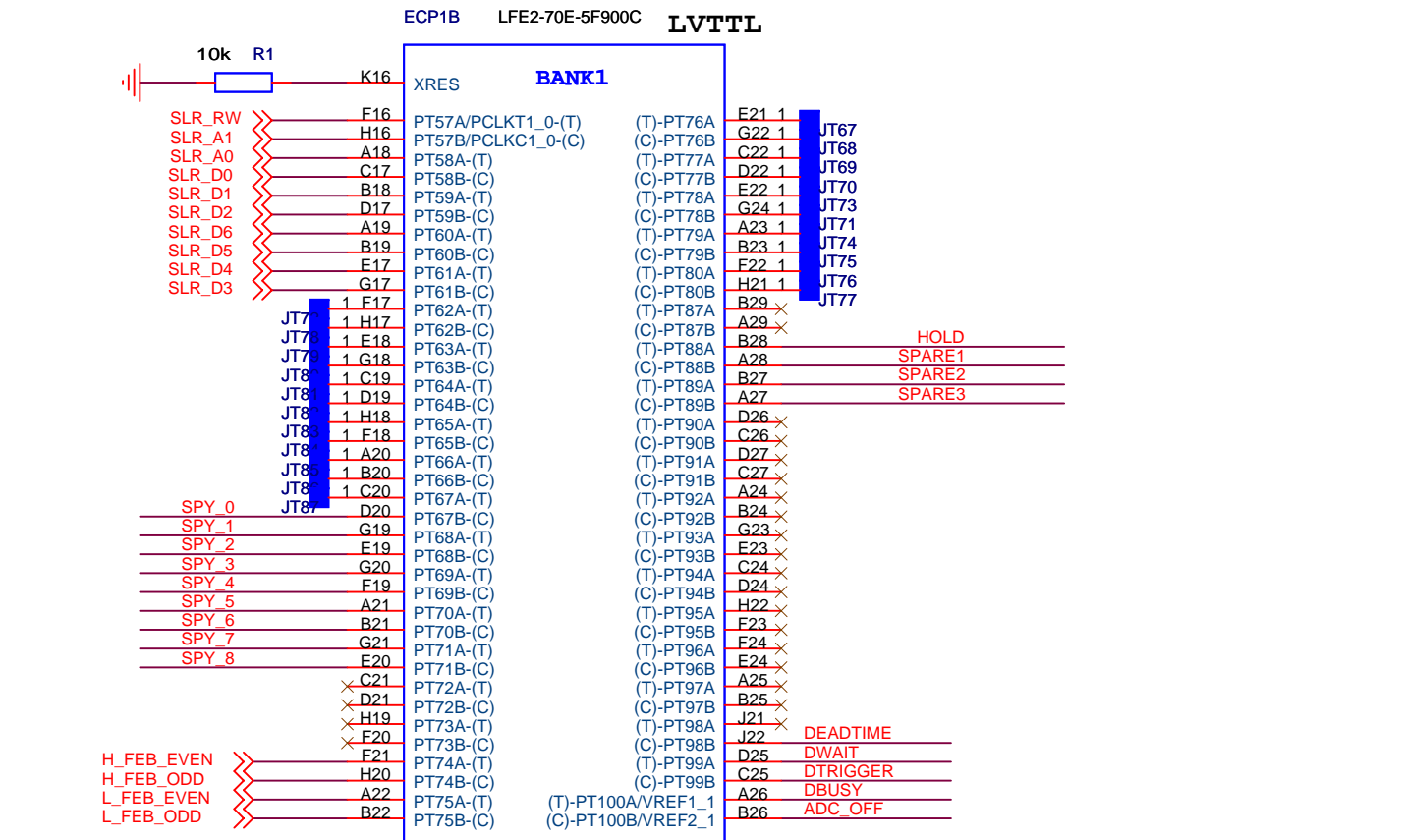
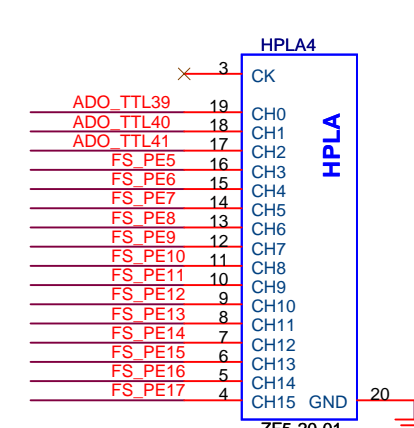
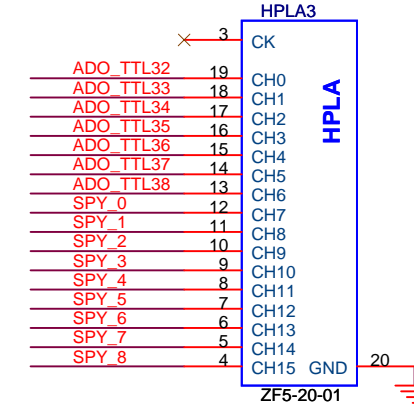
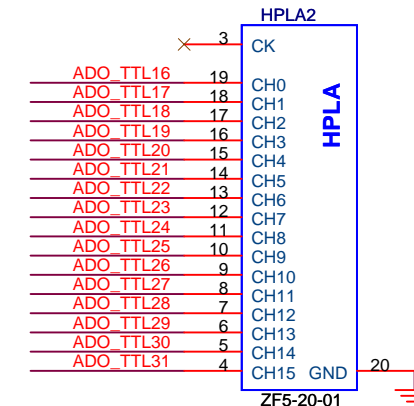
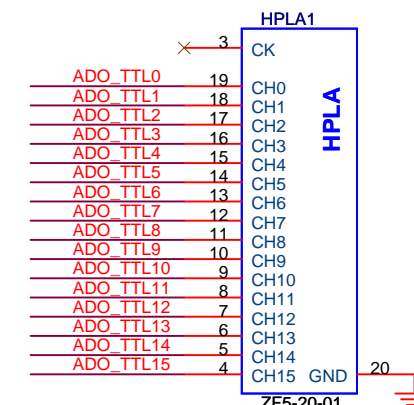
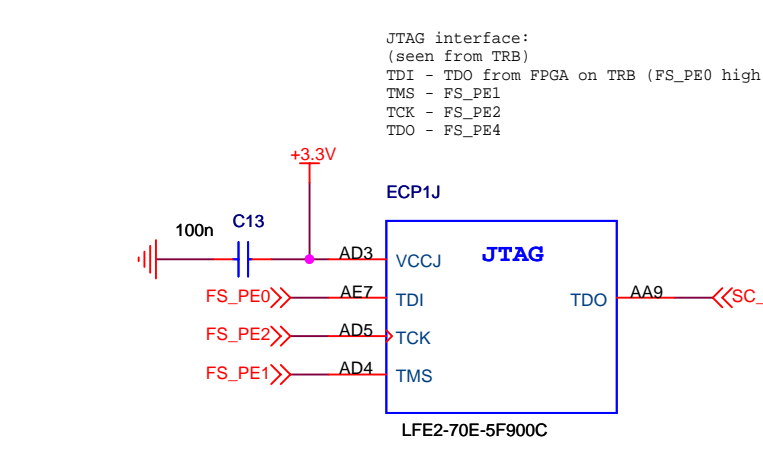
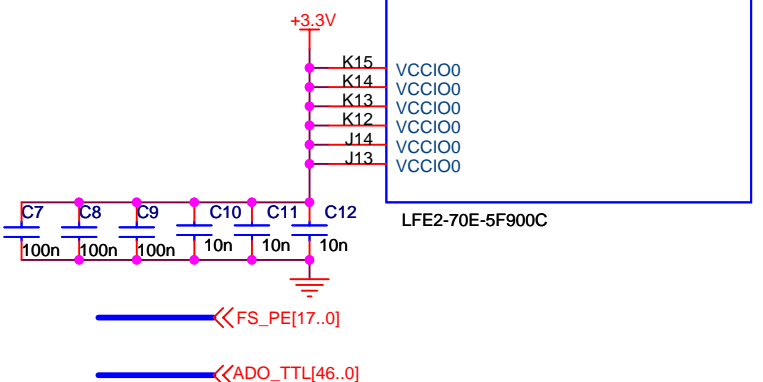
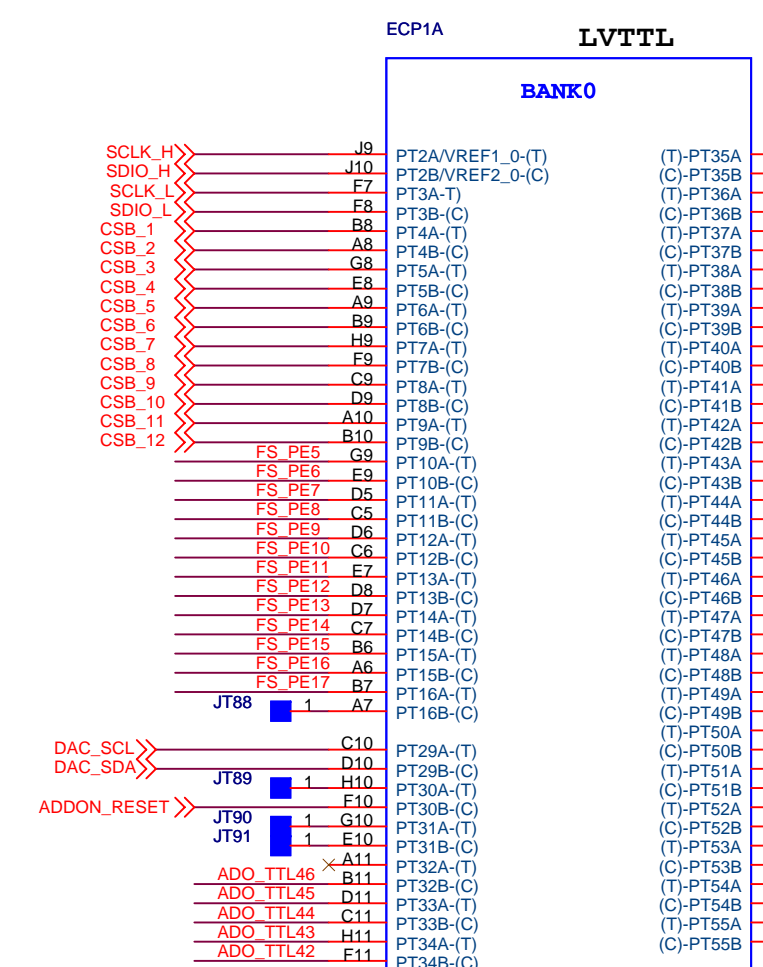
DET_HIGH1

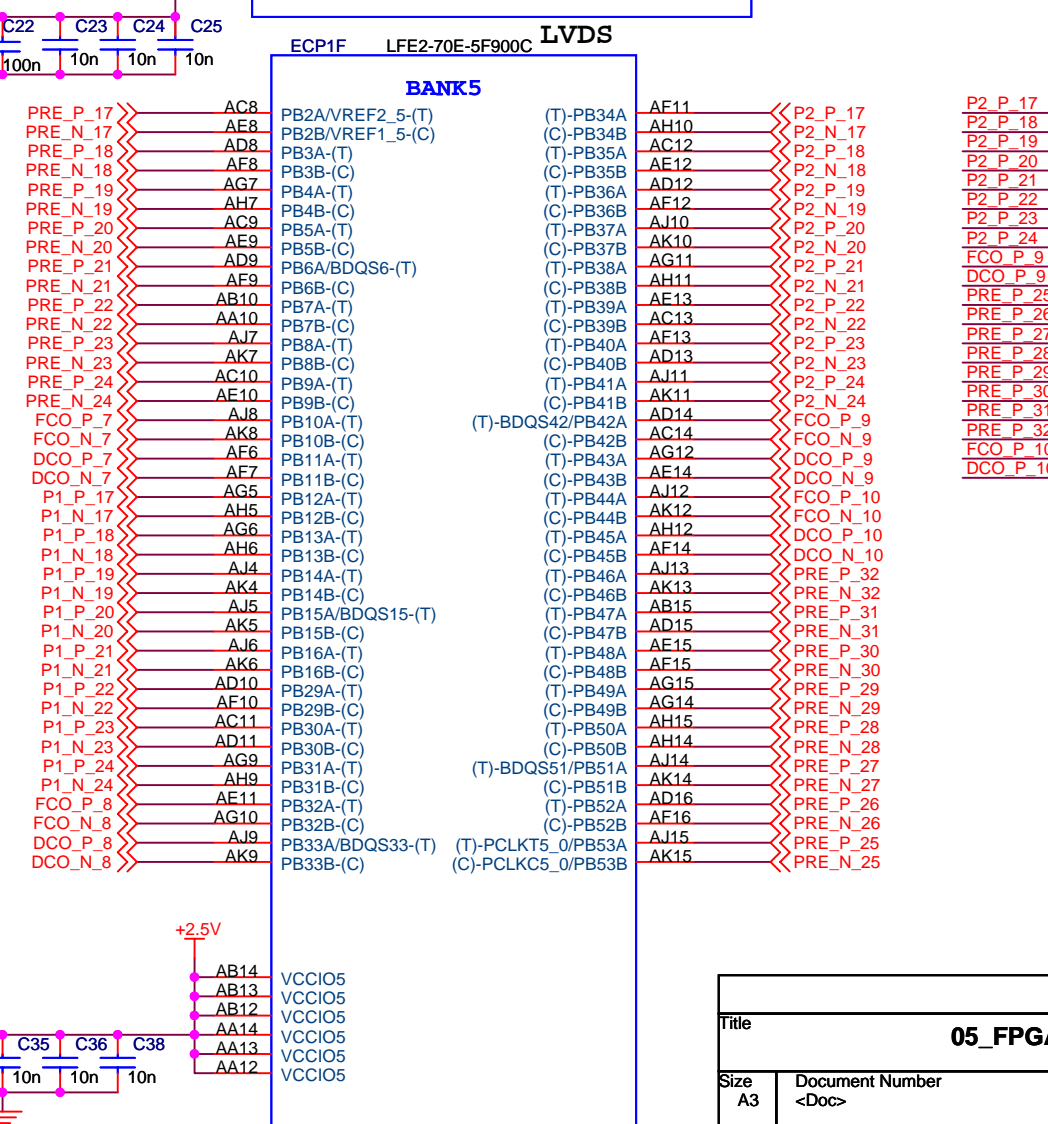
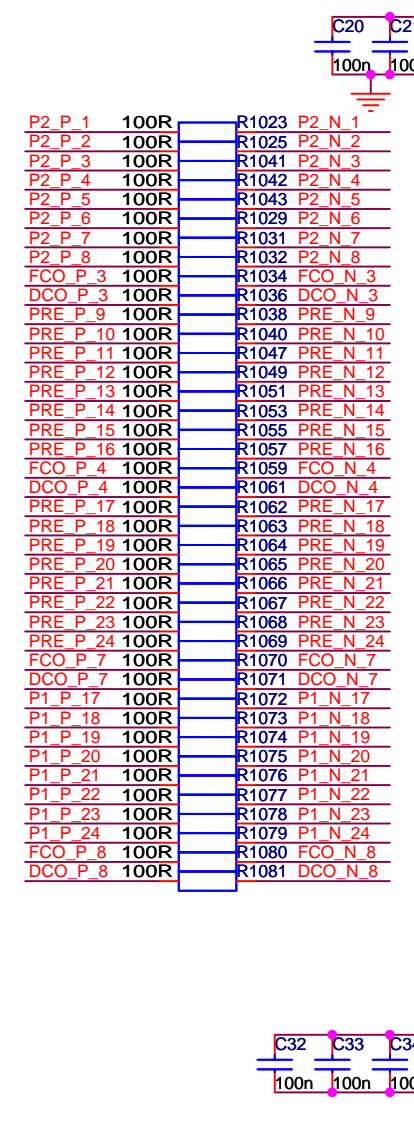
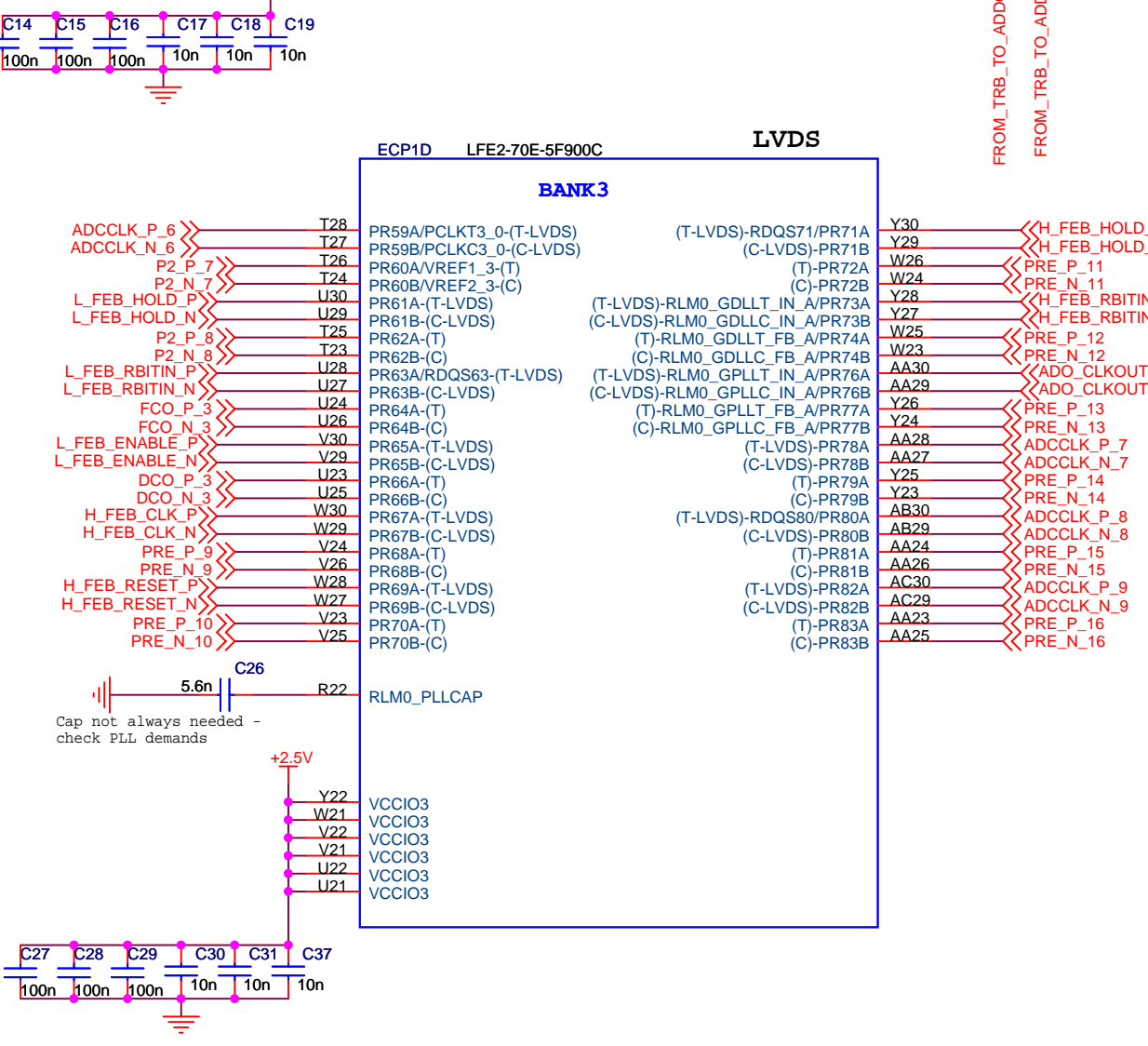
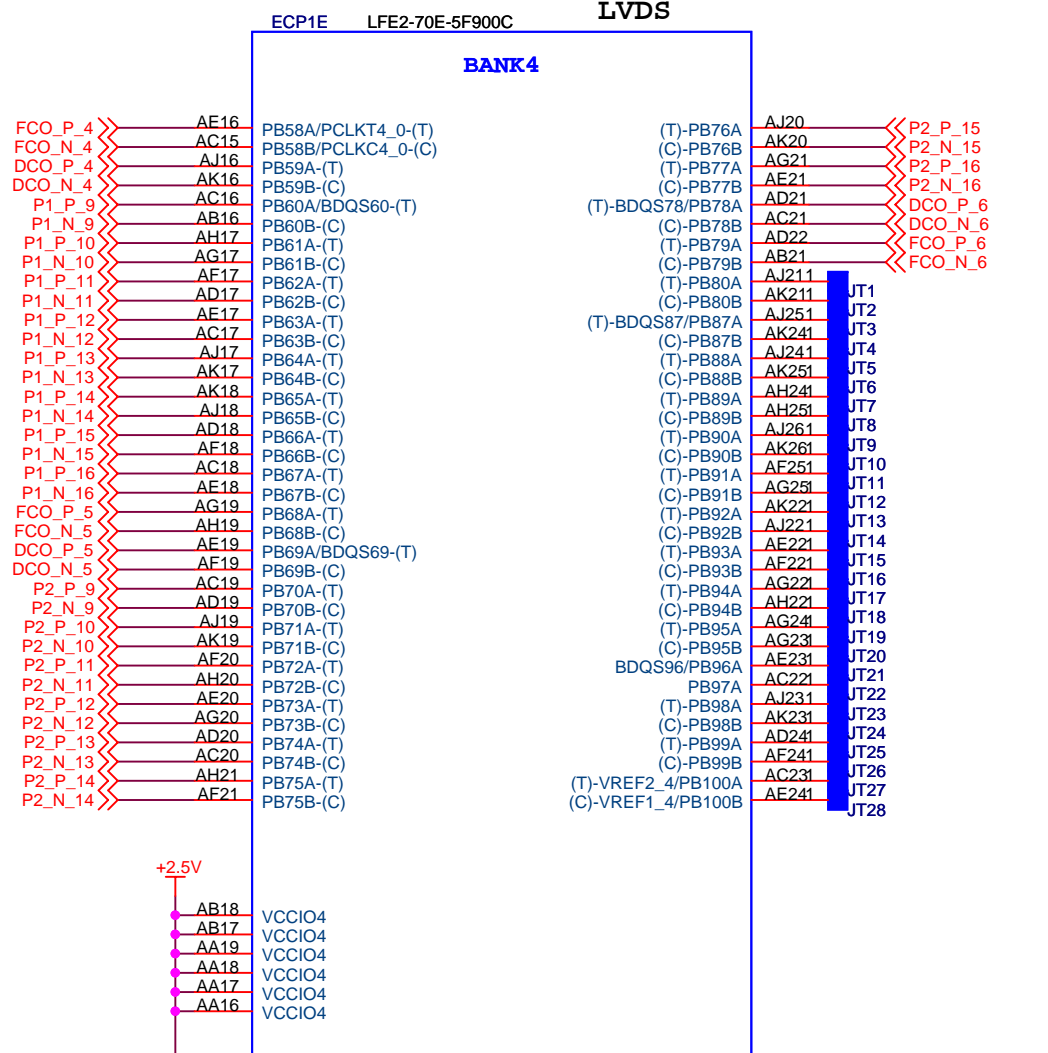
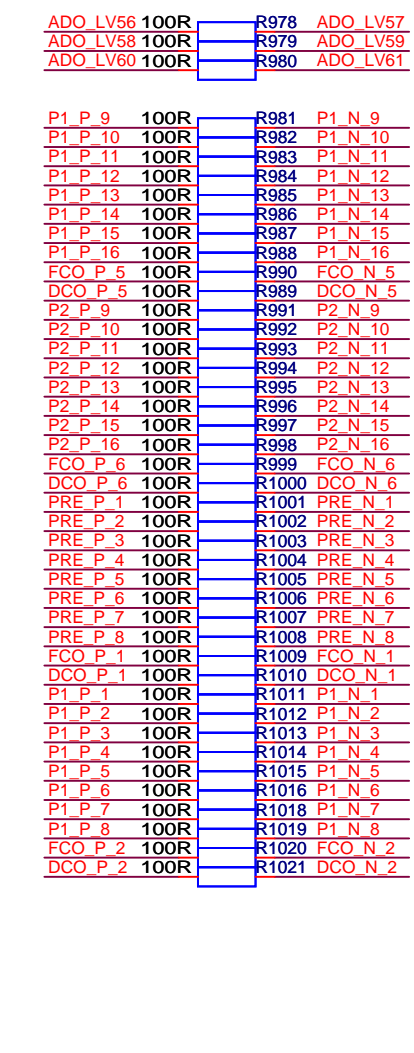
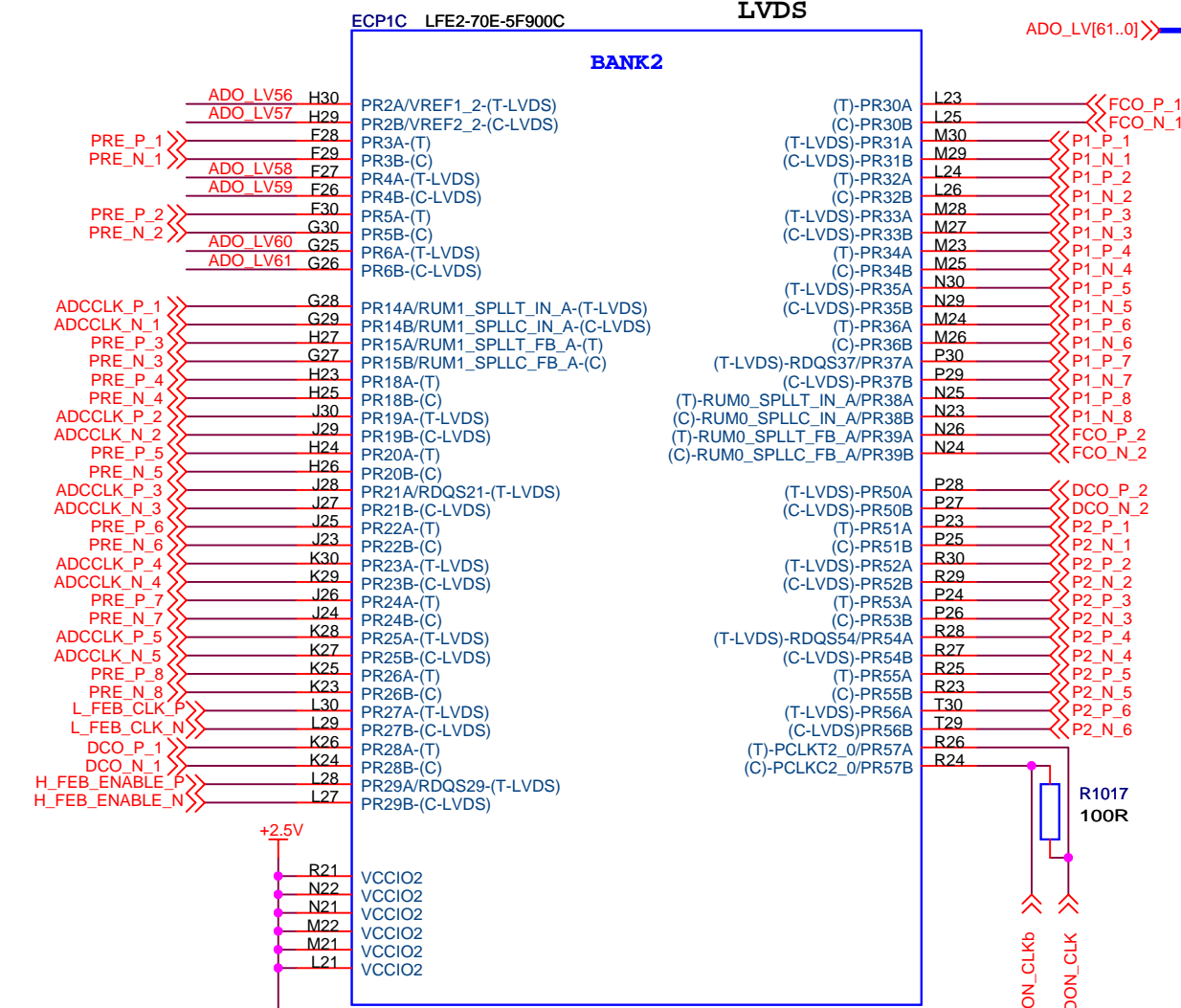


Title			02_DETECTOR_CONNECTORS		
Size	Document Number				Rev
A4	<Doc>				<RevCo
Date:	Tuesday, July 31, 2007		Sheet	2	of 21



Title			03_INPUT_CHANNELS		
Size	Document Number				Rev
A3	<Doc>				<RevC>
Date:	Friday, April 13, 2007	Sheet	3	of	21

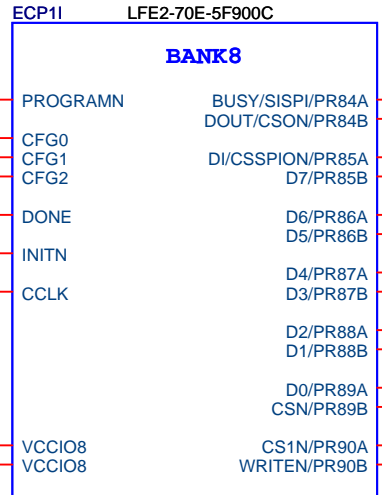
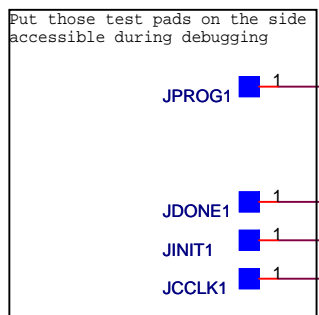
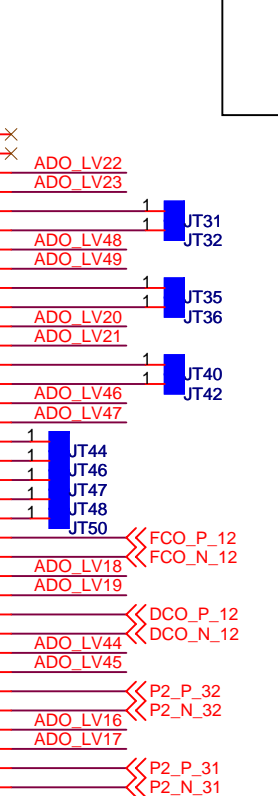
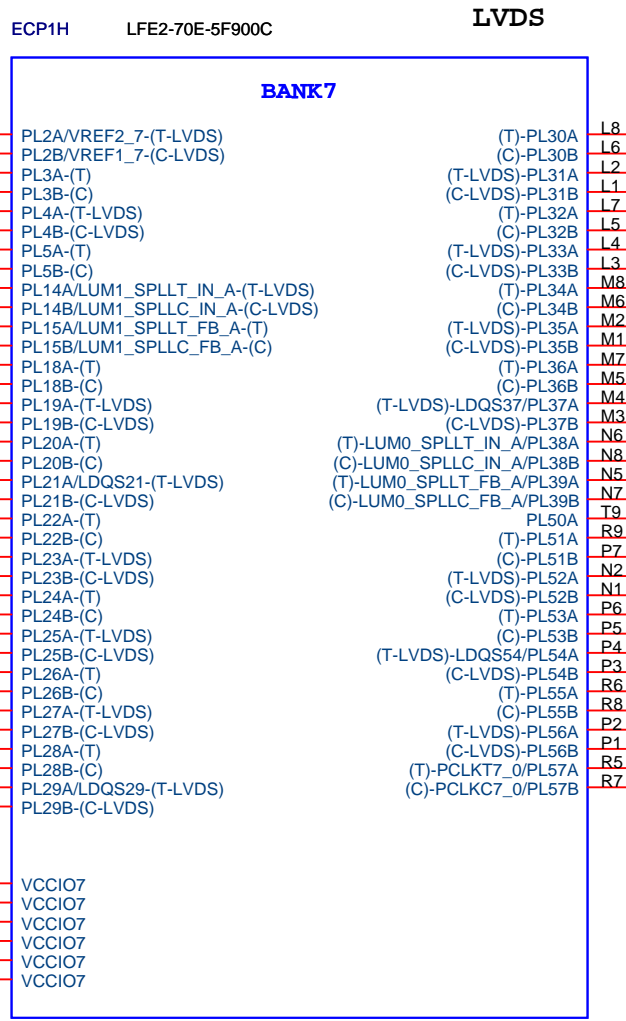
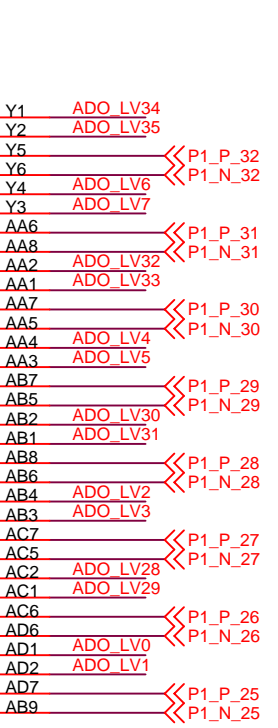
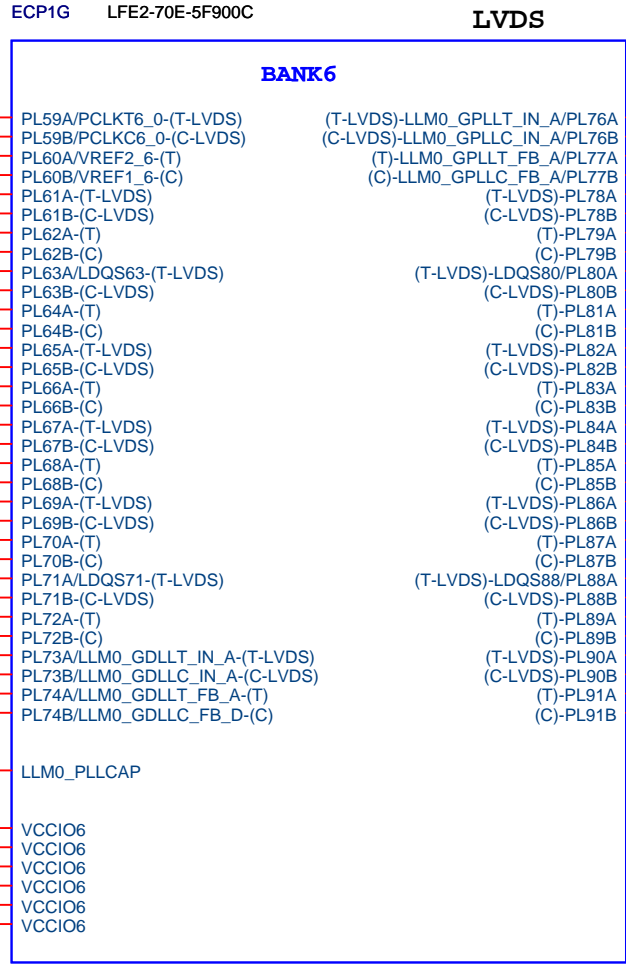
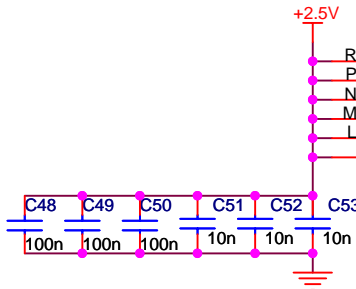
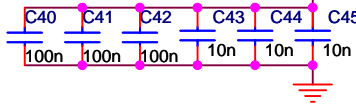
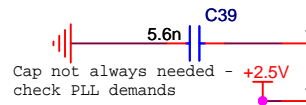




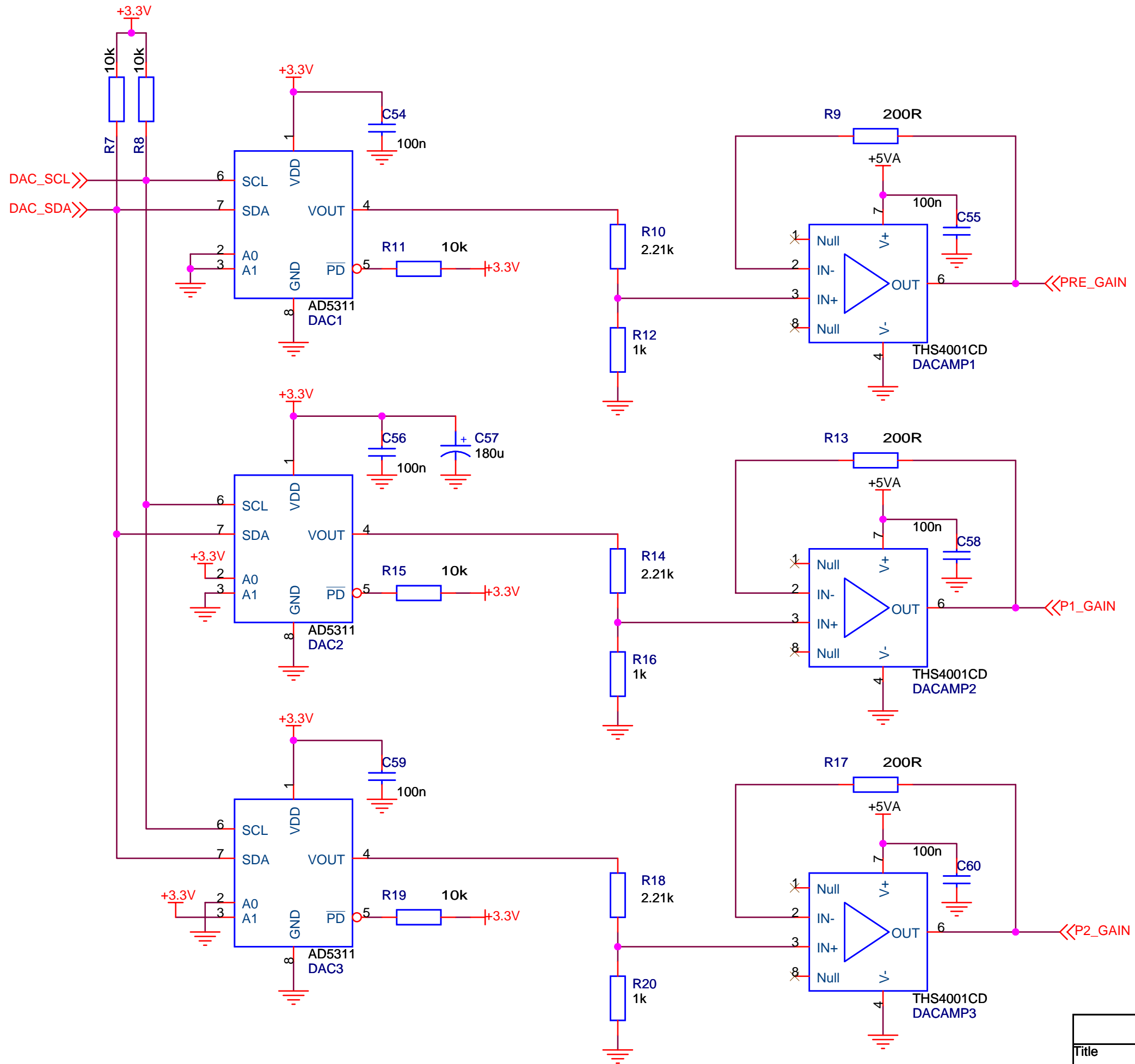
ADO_LV[61..0]

ADO LV0 100R	R1082	ADO LV1
ADO LV2 100R	R1083	ADO LV3
ADO LV4 100R	R1084	ADO LV5
ADO LV6 100R	R1085	ADO LV7
ADO LV8 100R	R1086	ADO LV9
ADO LV10 100R	R1087	ADO LV11
ADO LV12 100R	R1088	ADO LV13
ADO LV14 100R	R1089	ADO LV15
ADO LV16 100R	R1090	ADO LV17
ADO LV18 100R	R1091	ADO LV19
ADO LV20 100R	R1092	ADO LV21
ADO LV22 100R	R1093	ADO LV23
ADO LV24 100R	R1094	ADO LV25
ADO LV26 100R	R1095	ADO LV27
ADO LV28 100R	R1096	ADO LV29
ADO LV30 100R	R1097	ADO LV31
ADO LV32 100R	R1098	ADO LV33
ADO LV34 100R	R1099	ADO LV35
ADO LV36 100R	R1100	ADO LV37
ADO LV38 100R	R1101	ADO LV39
ADO LV40 100R	R1102	ADO LV41
ADO LV42 100R	R1103	ADO LV43
ADO LV44 100R	R1104	ADO LV45
ADO LV46 100R	R1105	ADO LV47
ADO LV48 100R	R1106	ADO LV49
ADO LV50 100R	R1107	ADO LV51
ADO LV52 100R	R1108	ADO LV53
ADO LV54 100R	R1109	ADO LV55

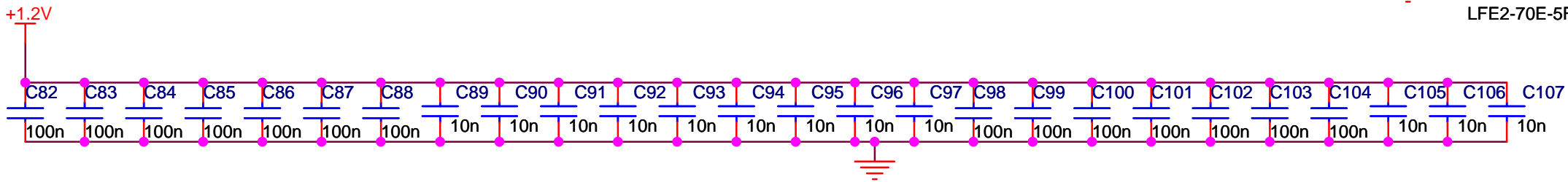
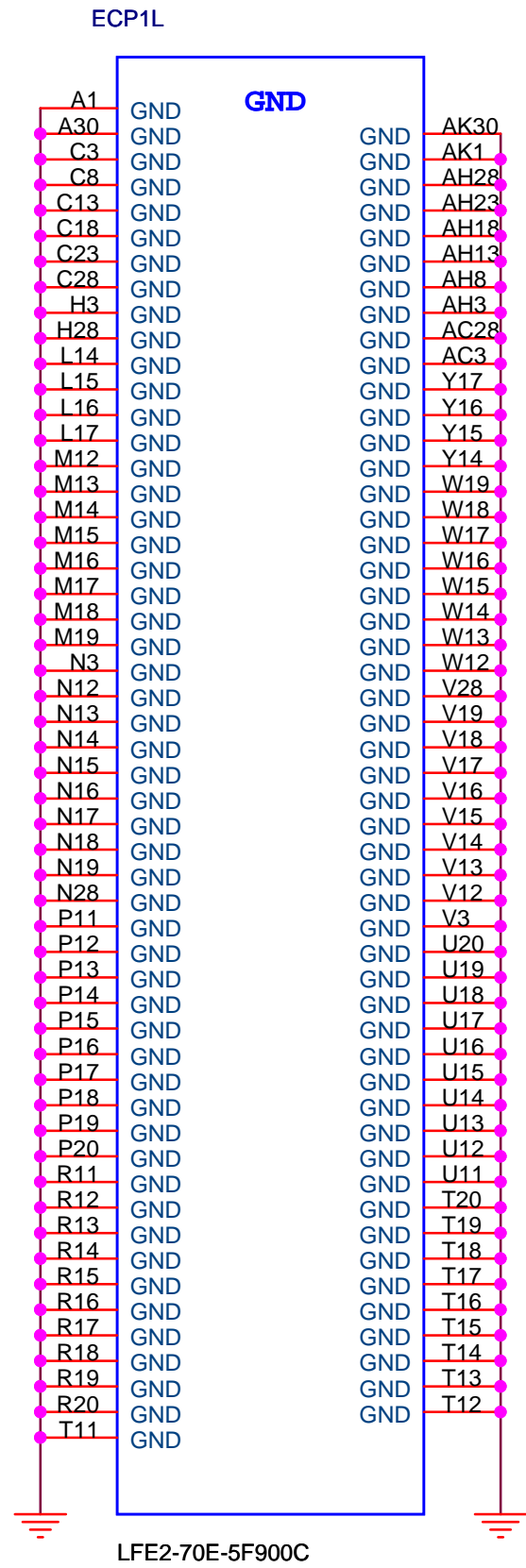
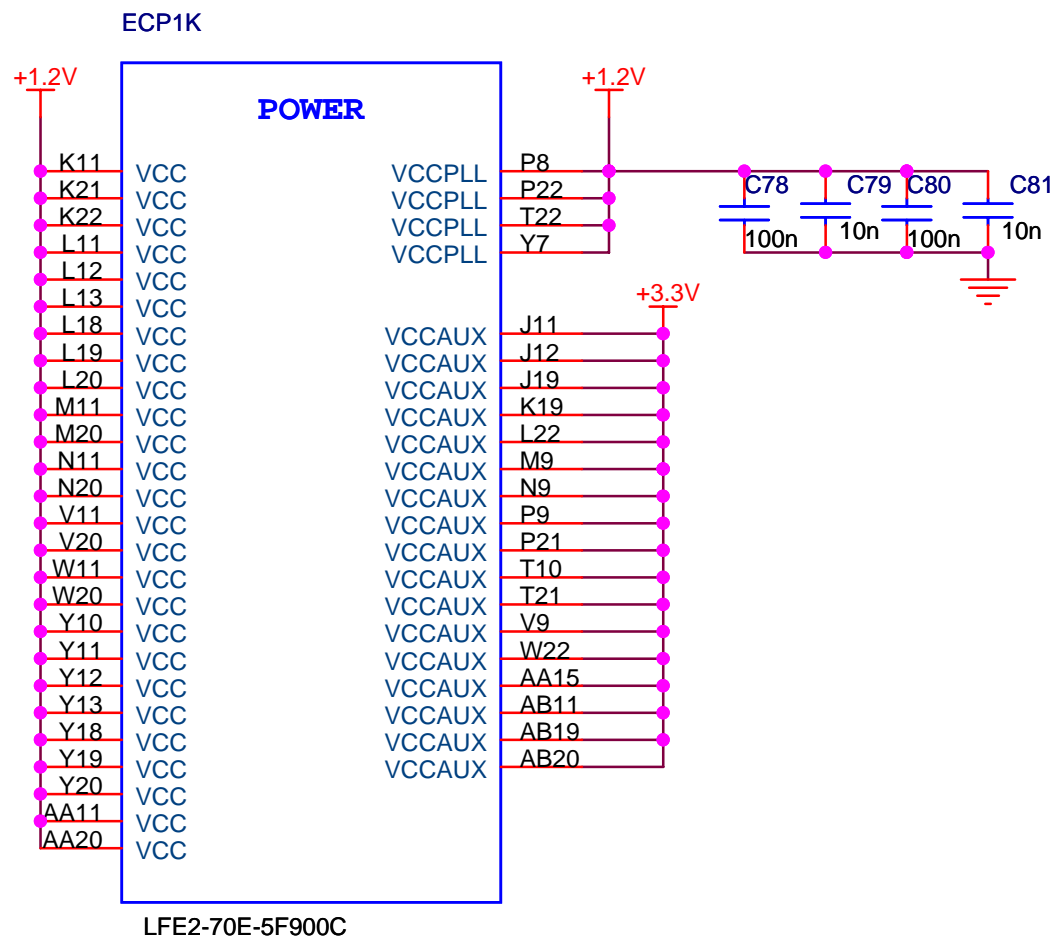
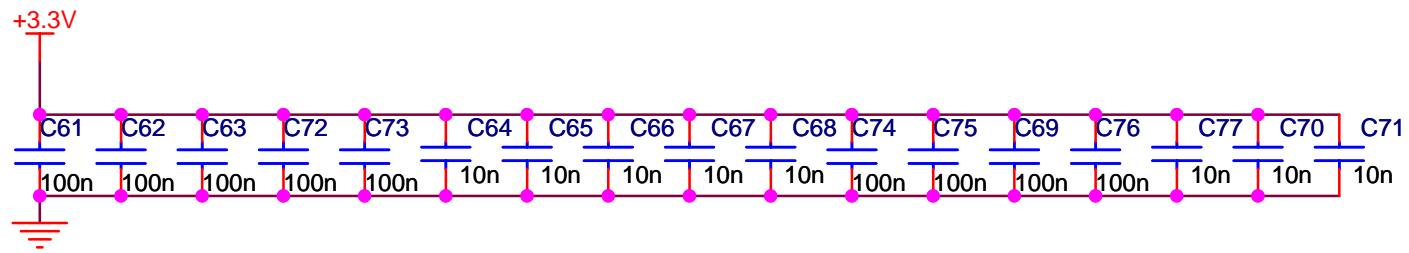
P1_P_25 100R	R1110	P1_N_25
P1_P_26 100R	R1111	P1_N_26
P1_P_27 100R	R1112	P1_N_27
P1_P_28 100R	R1113	P1_N_28
P1_P_29 100R	R1114	P1_N_29
P1_P_30 100R	R1115	P1_N_30
P1_P_31 100R	R1116	P1_N_31
P1_P_32 100R	R1117	P1_N_32
FCO_P_11 100R	R1118	FCO_N_11
DCO_P_11 100R	R1119	DCO_N_11
P2_P_25 100R	R1120	P2_N_25
P2_P_26 100R	R1121	P2_N_26
P2_P_27 100R	R1122	P2_N_27
P2_P_28 100R	R1124	P2_N_28
P2_P_29 100R	R1123	P2_N_29
P2_P_30 100R	R1125	P2_N_30
P2_P_31 100R	R1126	P2_N_31
P2_P_32 100R	R1127	P2_N_32
DCO_P_12 100R	R1129	DCO_N_12
FCO_P_12 100R	R1128	FCO_N_12



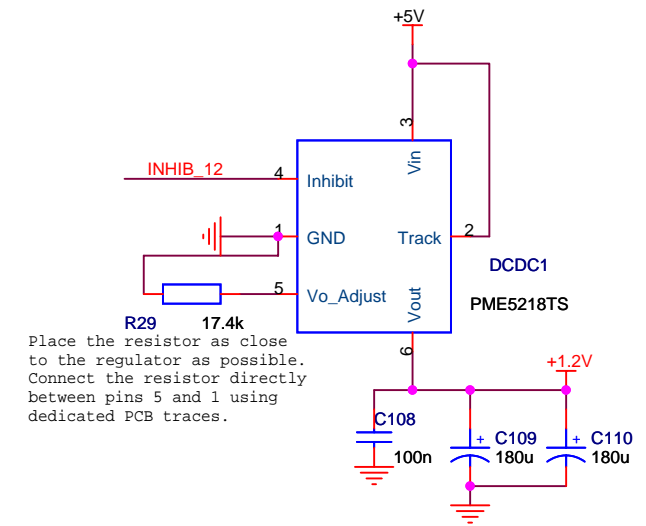
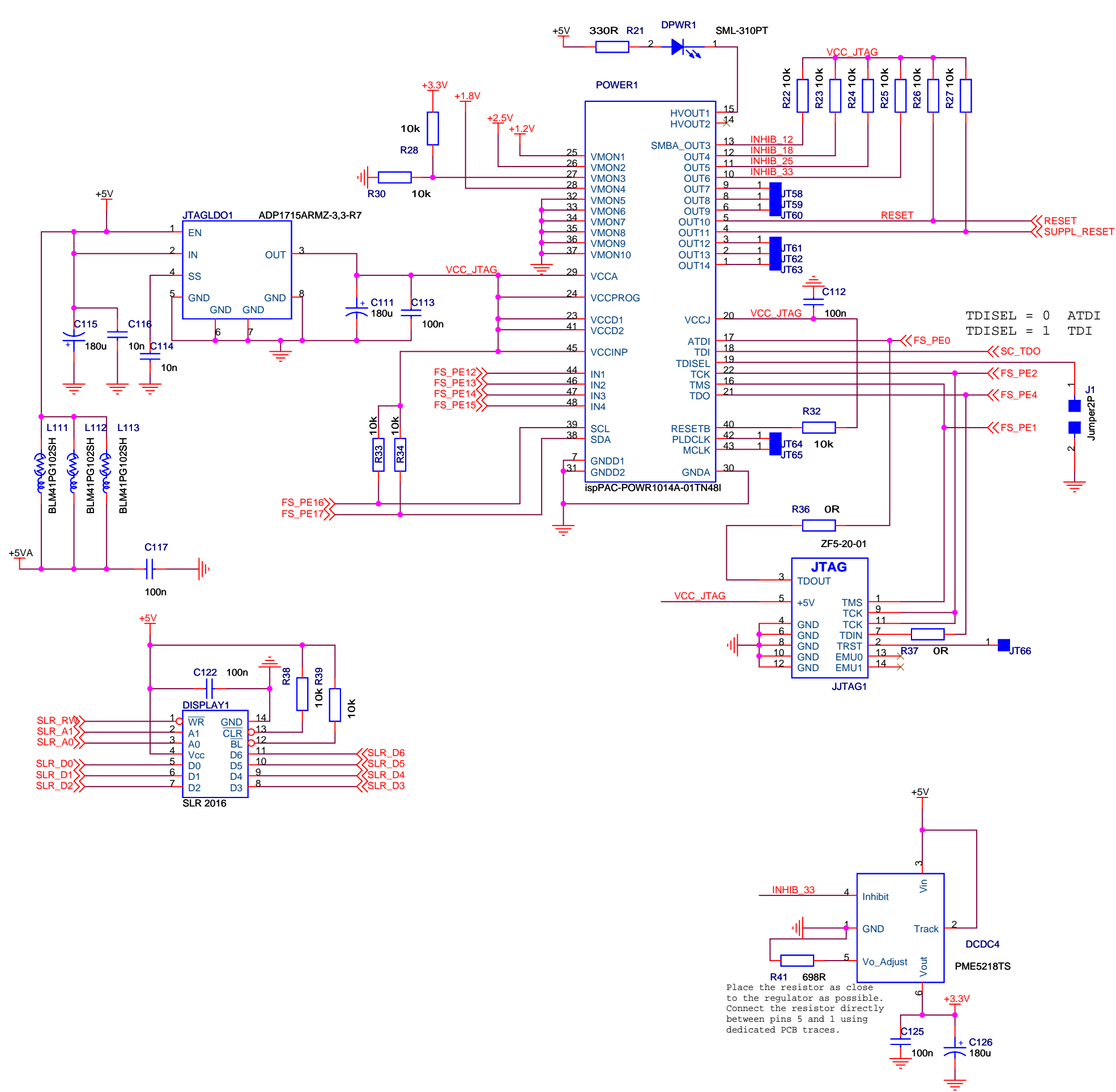
Title 06_FPGA_LVDS_B6_B7_B8		
Size A3	Document Number <Doc>	Rev <RevC>
Date: Wednesday, January 09, 2008	Sheet 6	of 21



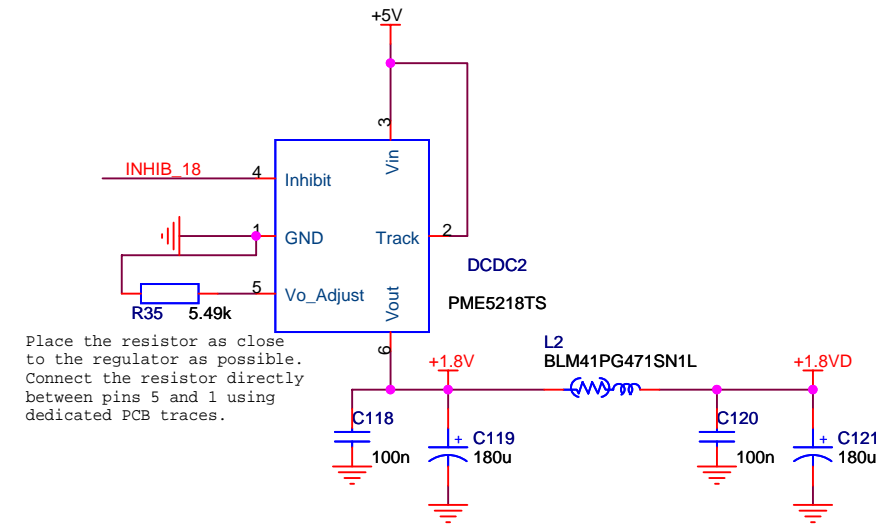
Title			07_DACS		
Size	Document Number				Rev
A4	<Doc>				<RevCo
Date:	Wednesday, November 28, 2007	Sheet	7	of	21



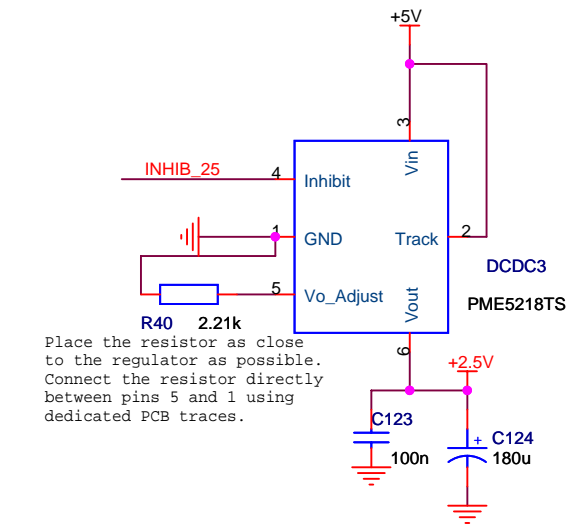
Title			08_FPGA_POWER_CAPS		
Size	Document Number				Rev
A4	<Doc>				<RevCo
Date:	Wednesday, December 19, 2007	Sheet	8	of	21



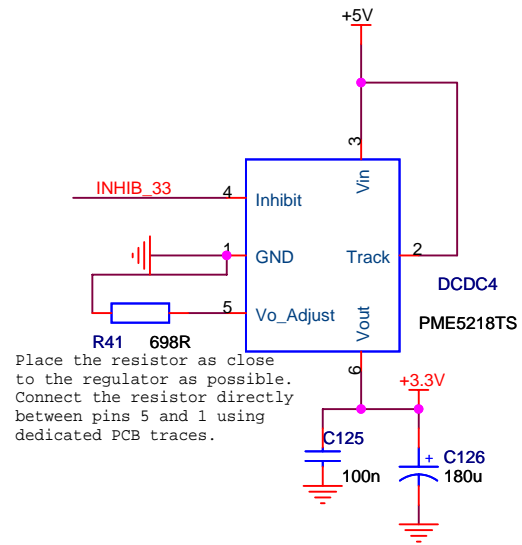
Place the resistor as close to the regulator as possible. Connect the resistor directly between pins 5 and 1 using dedicated PCB traces.



Place the resistor as close to the regulator as possible. Connect the resistor directly between pins 5 and 1 using dedicated PCB traces.

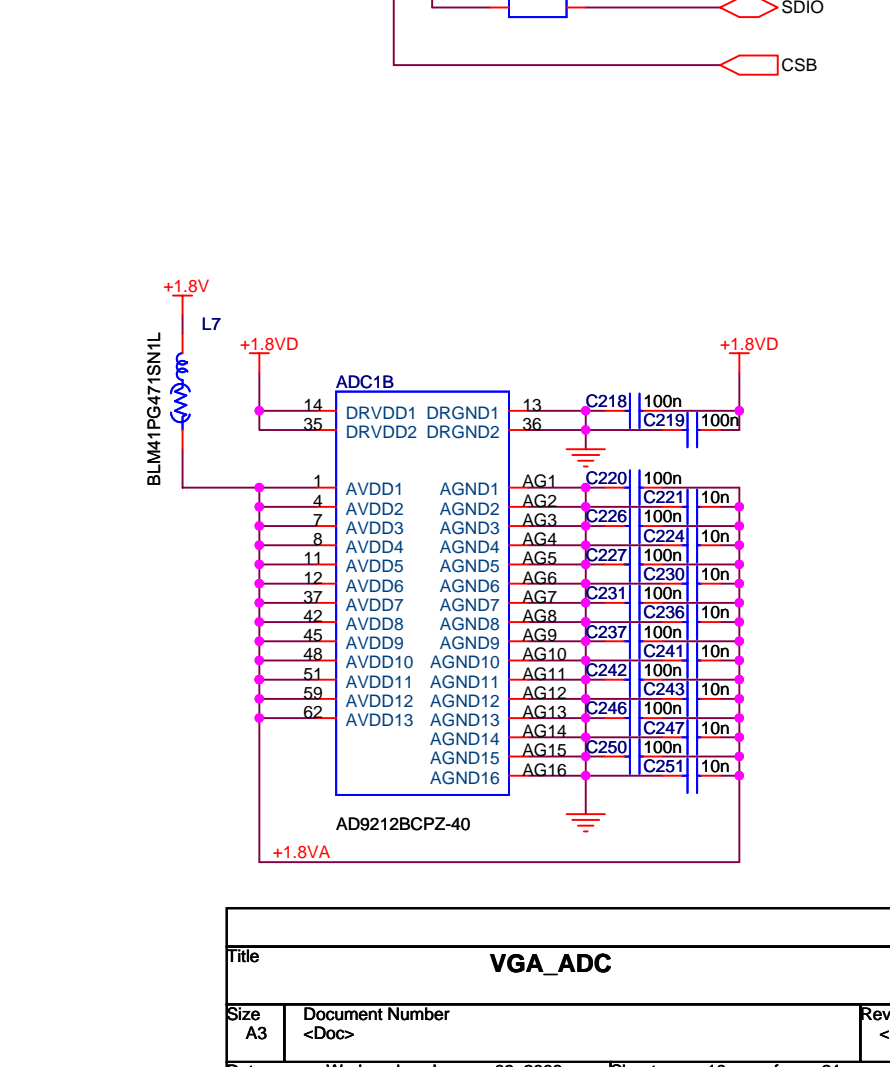
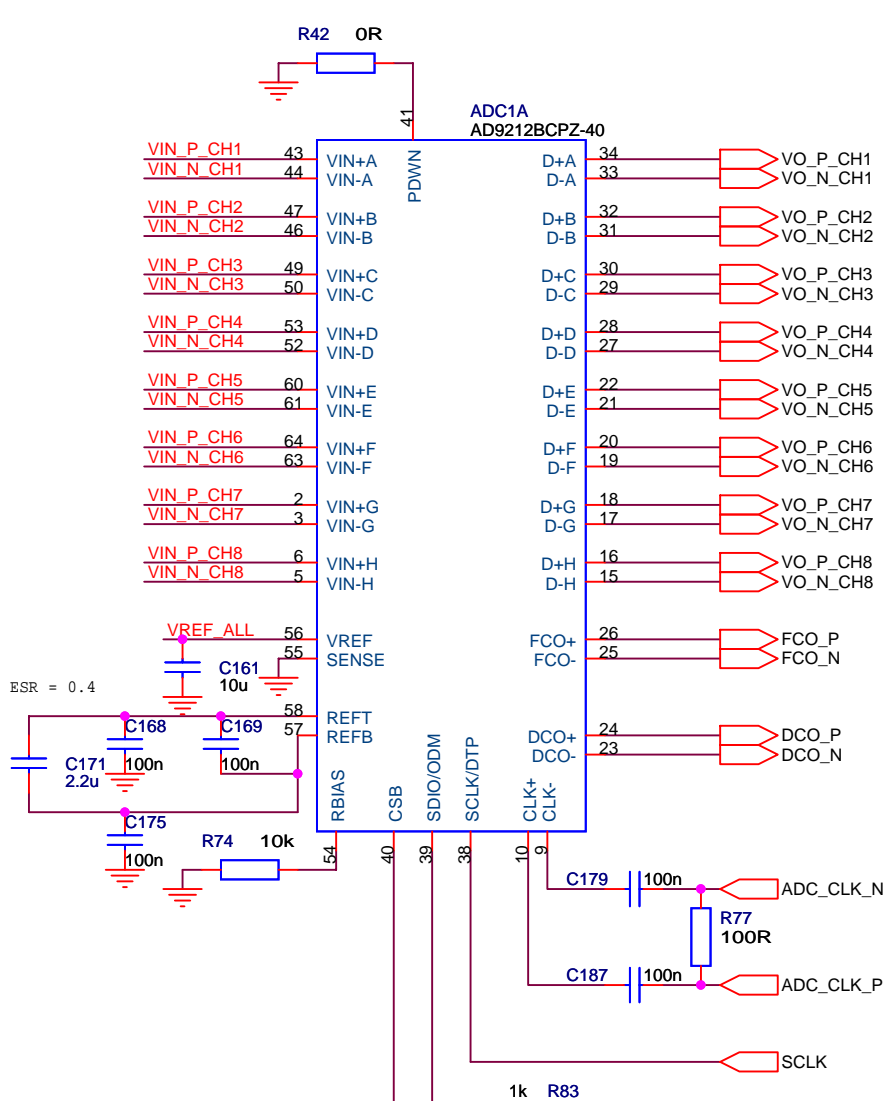
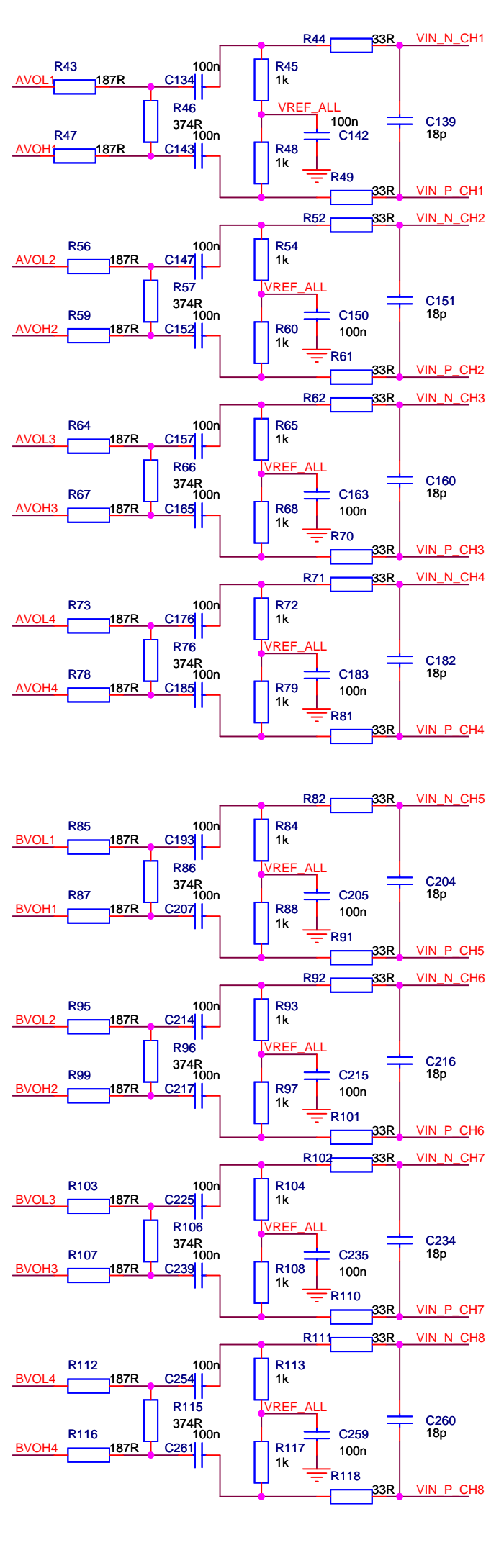
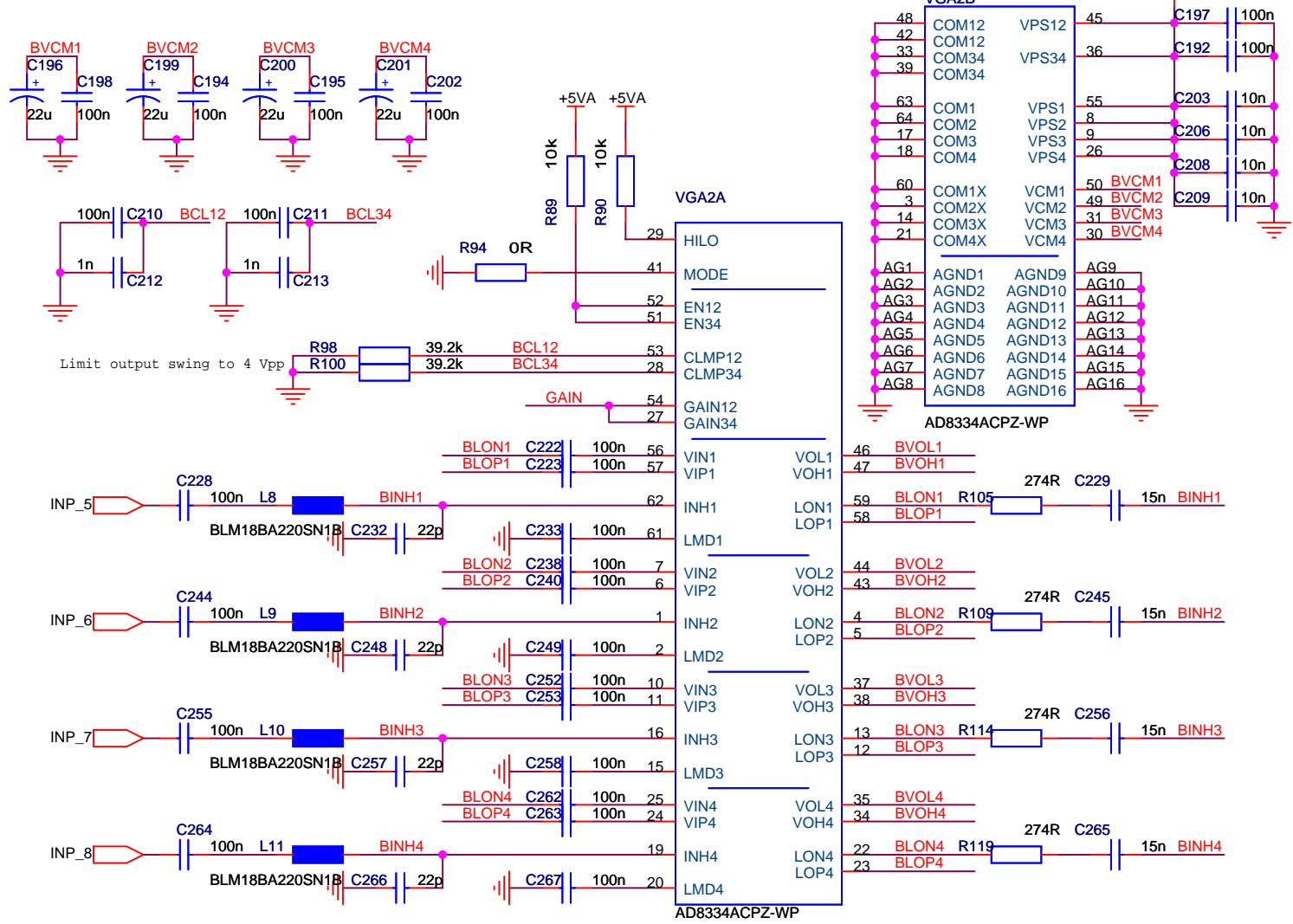
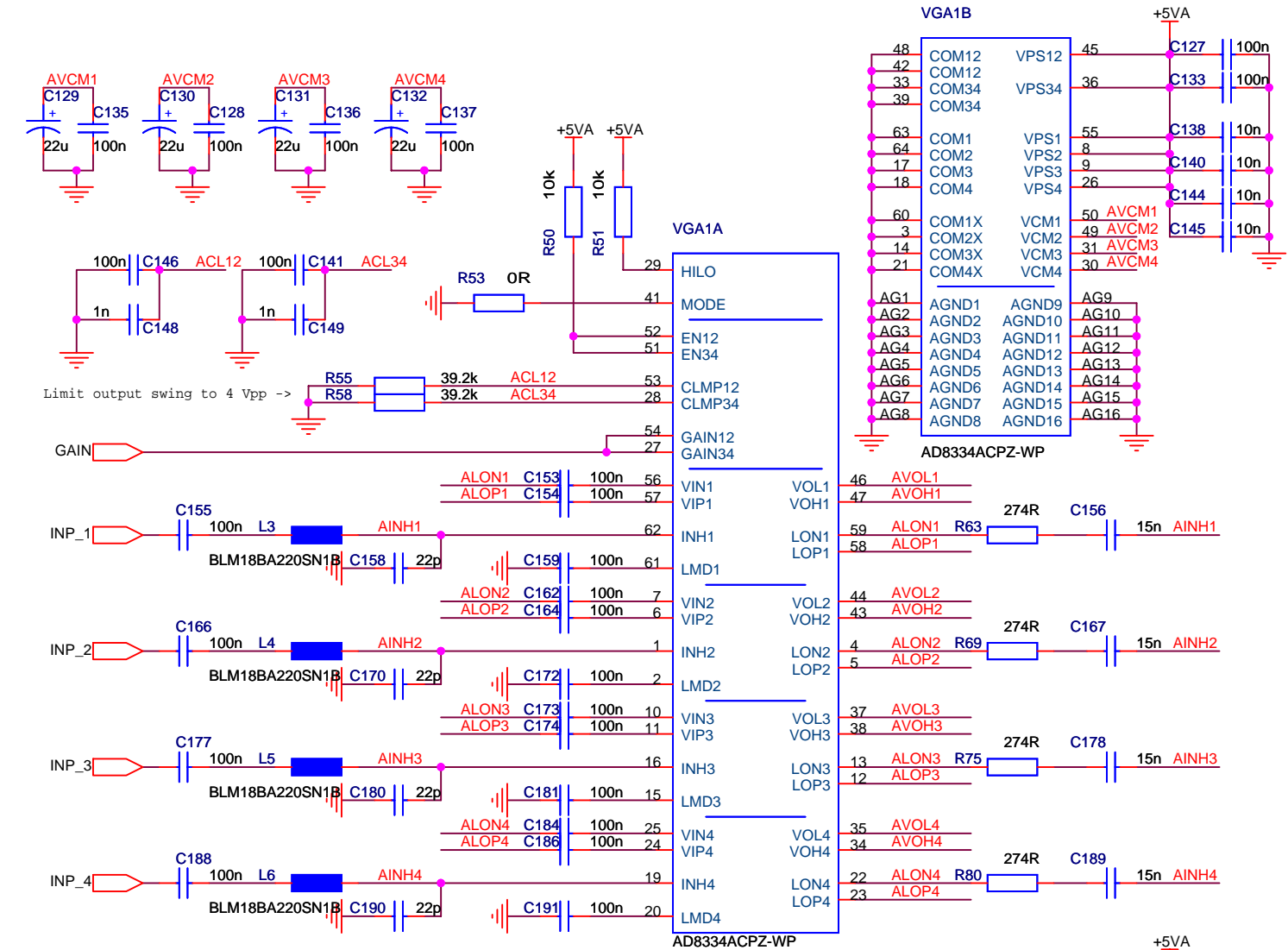


Place the resistor as close to the regulator as possible. Connect the resistor directly between pins 5 and 1 using dedicated PCB traces.

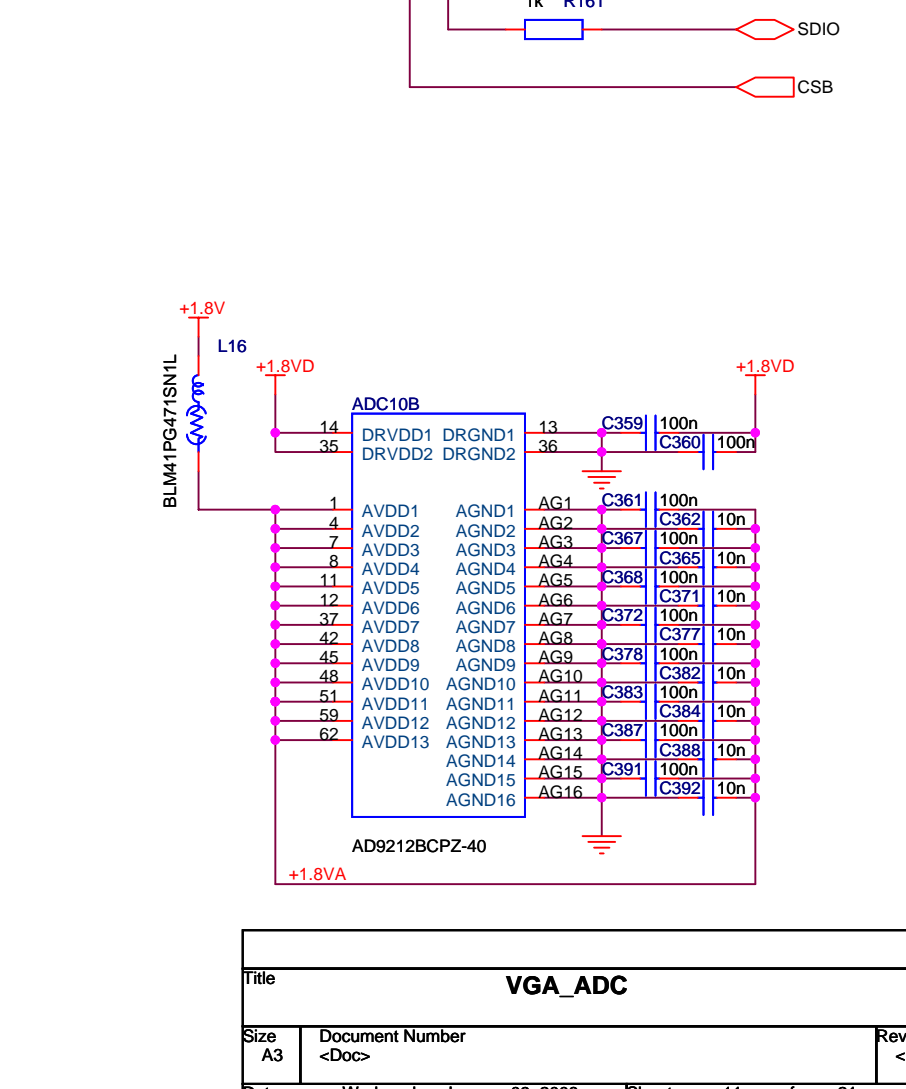
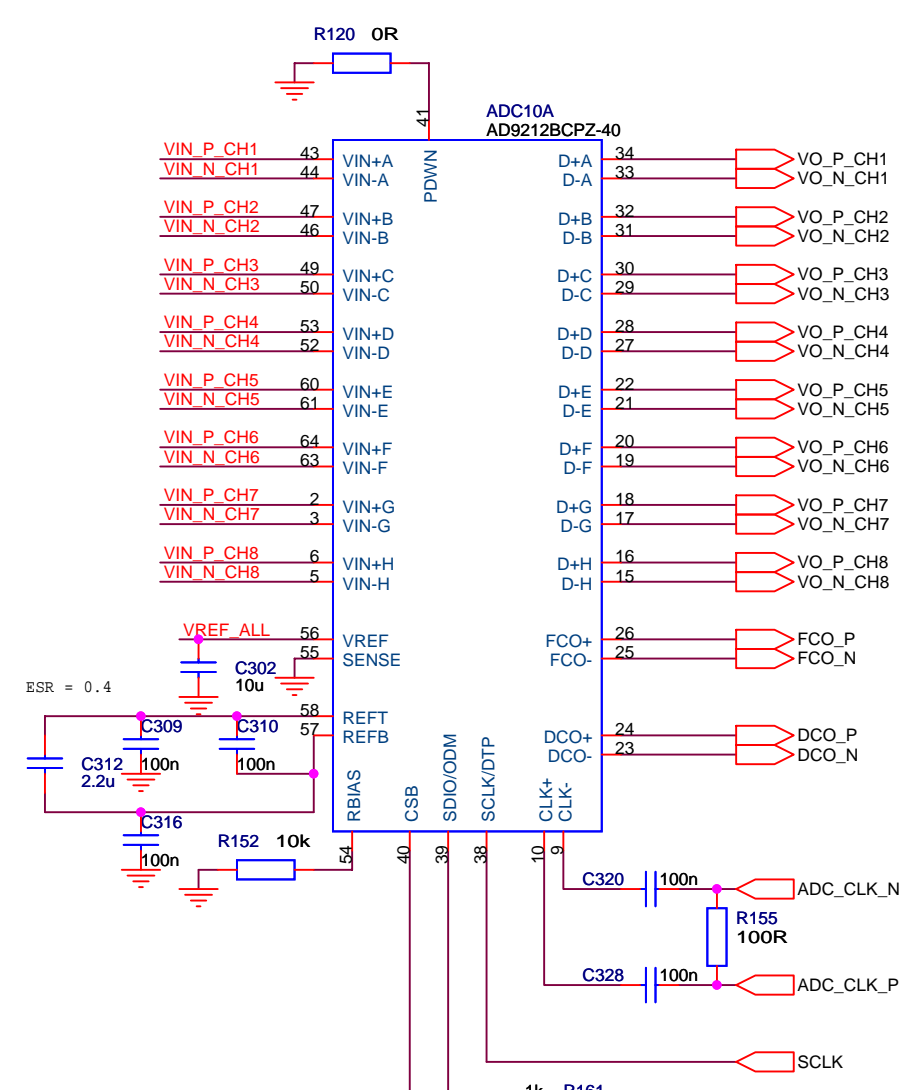
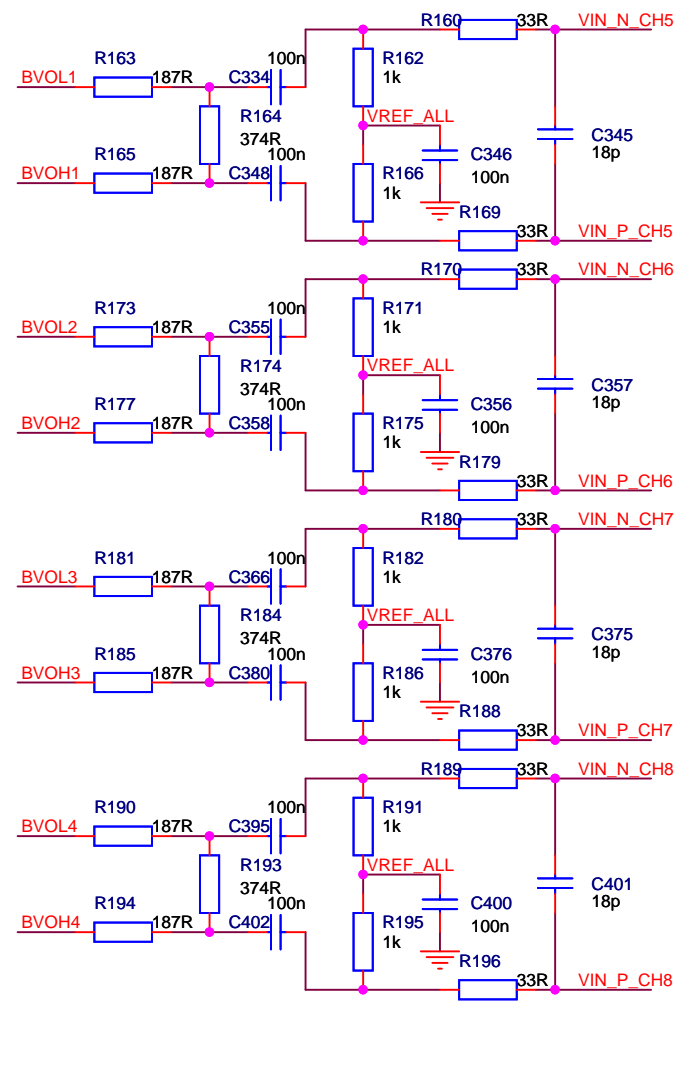
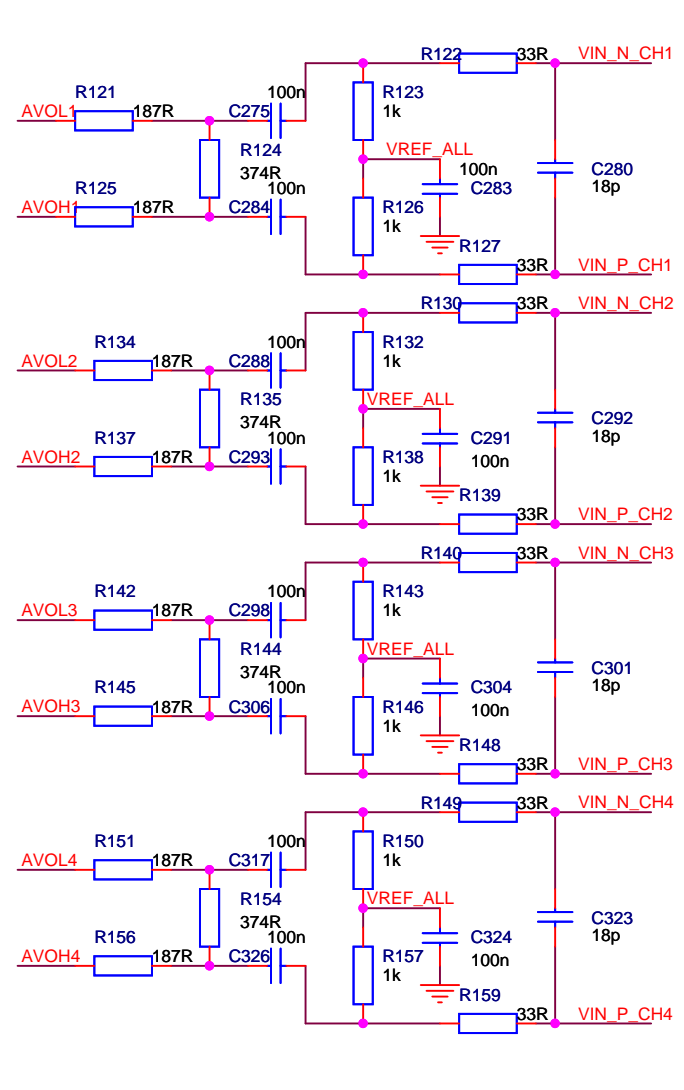
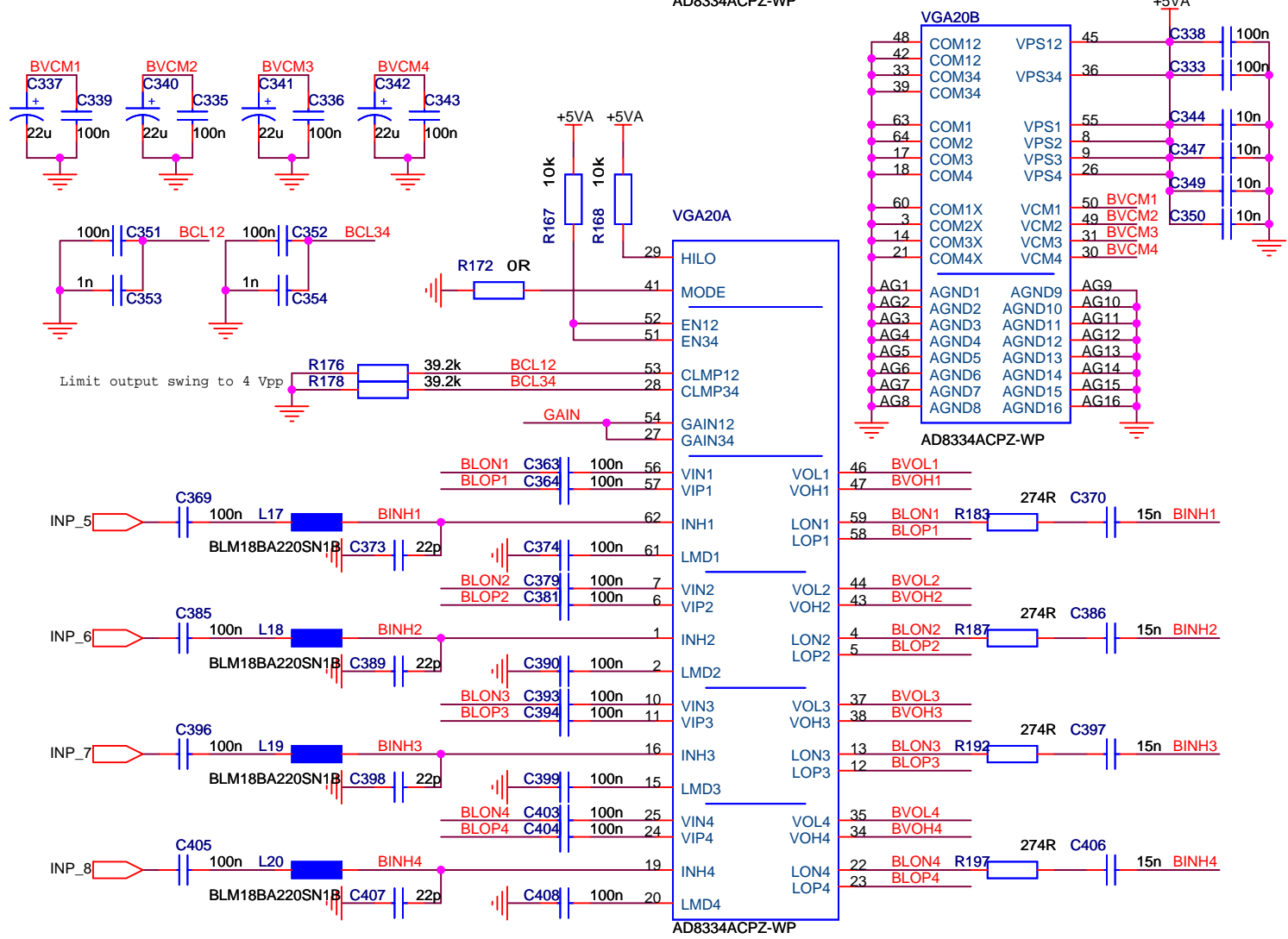
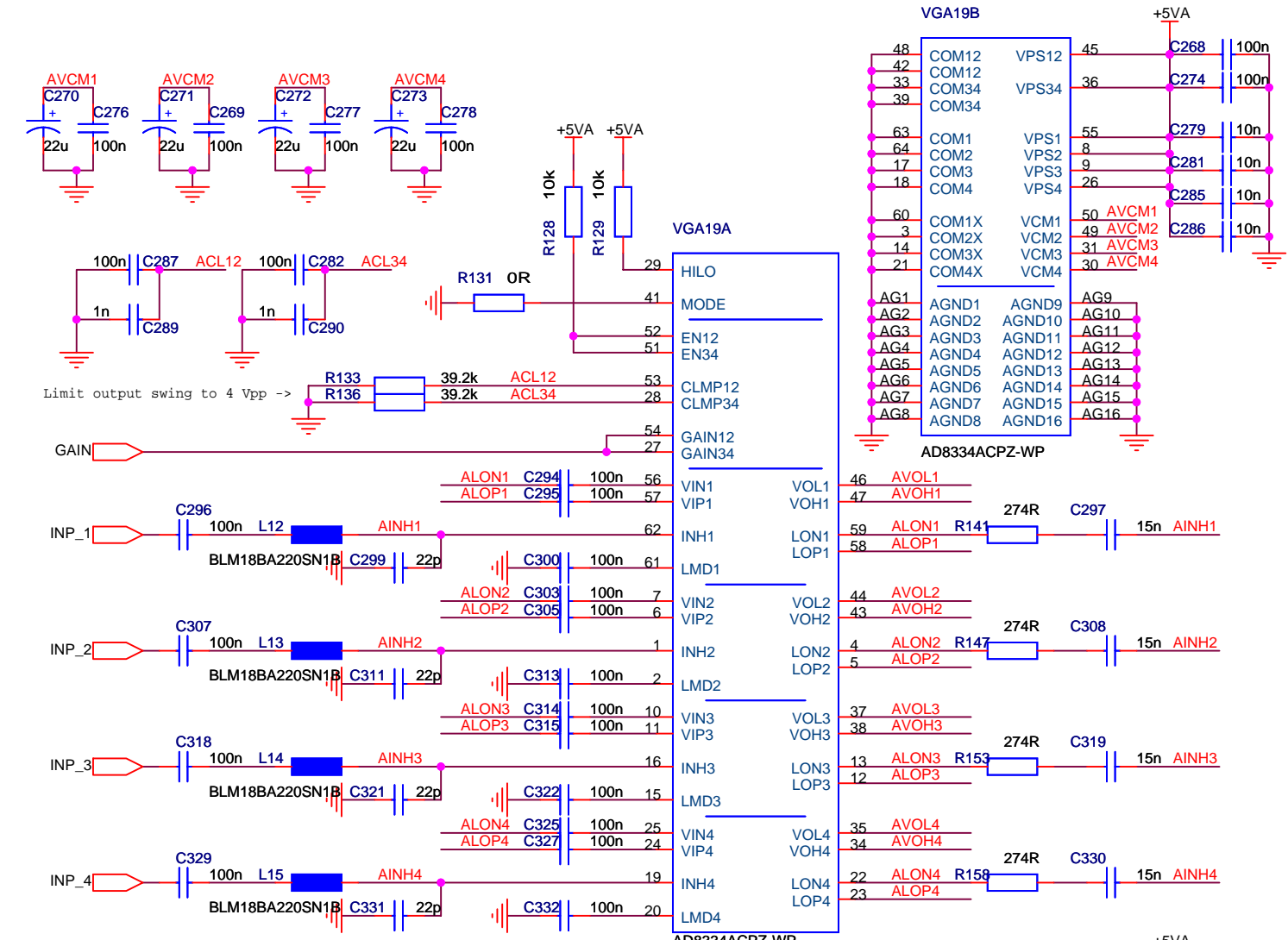


Place the resistor as close to the regulator as possible. Connect the resistor directly between pins 5 and 1 using dedicated PCB traces.

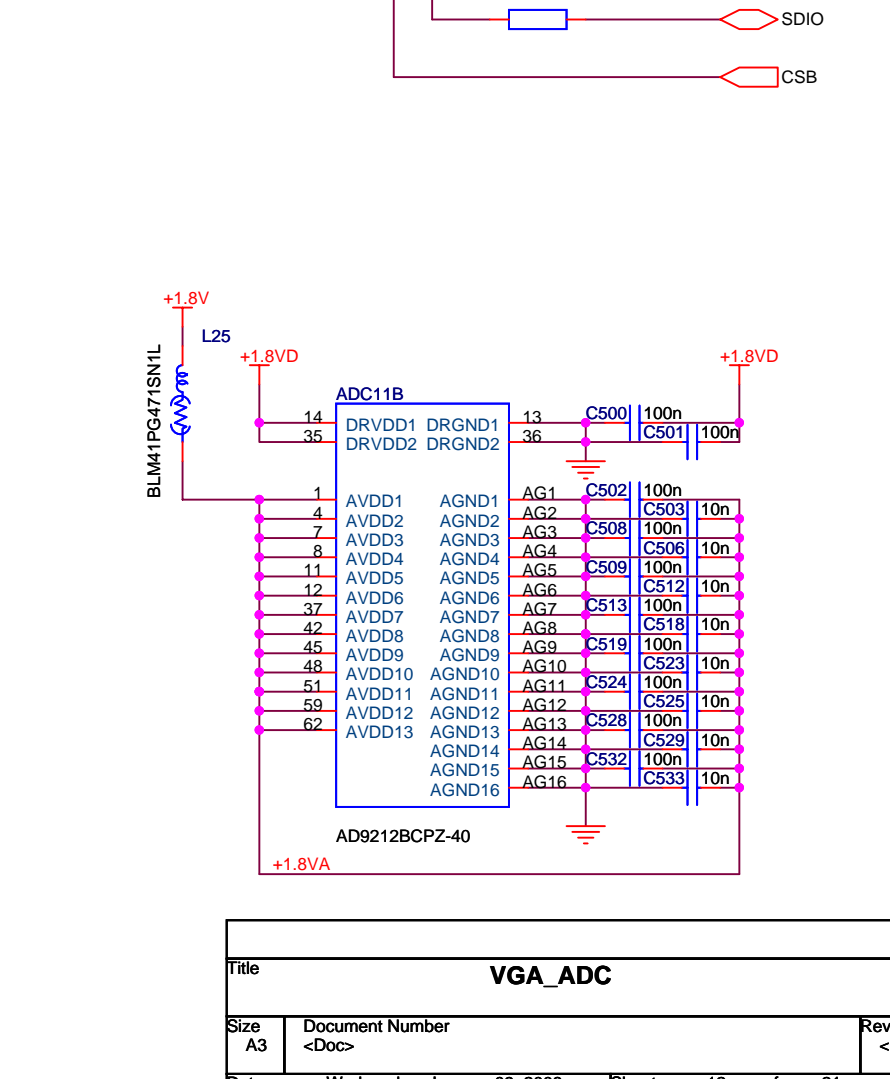
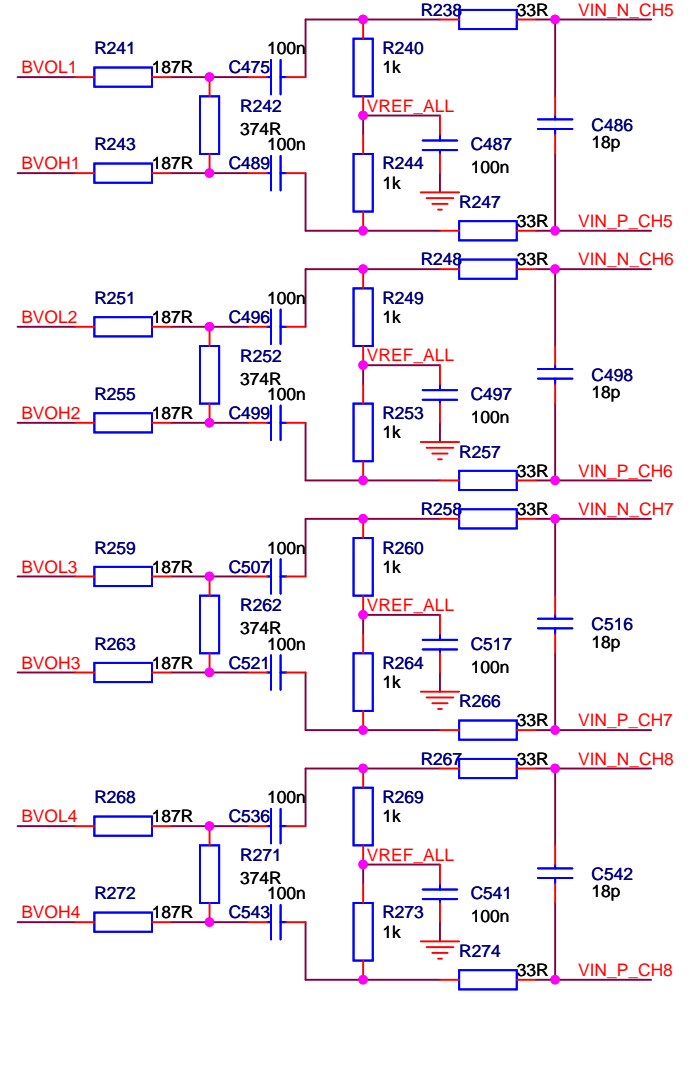
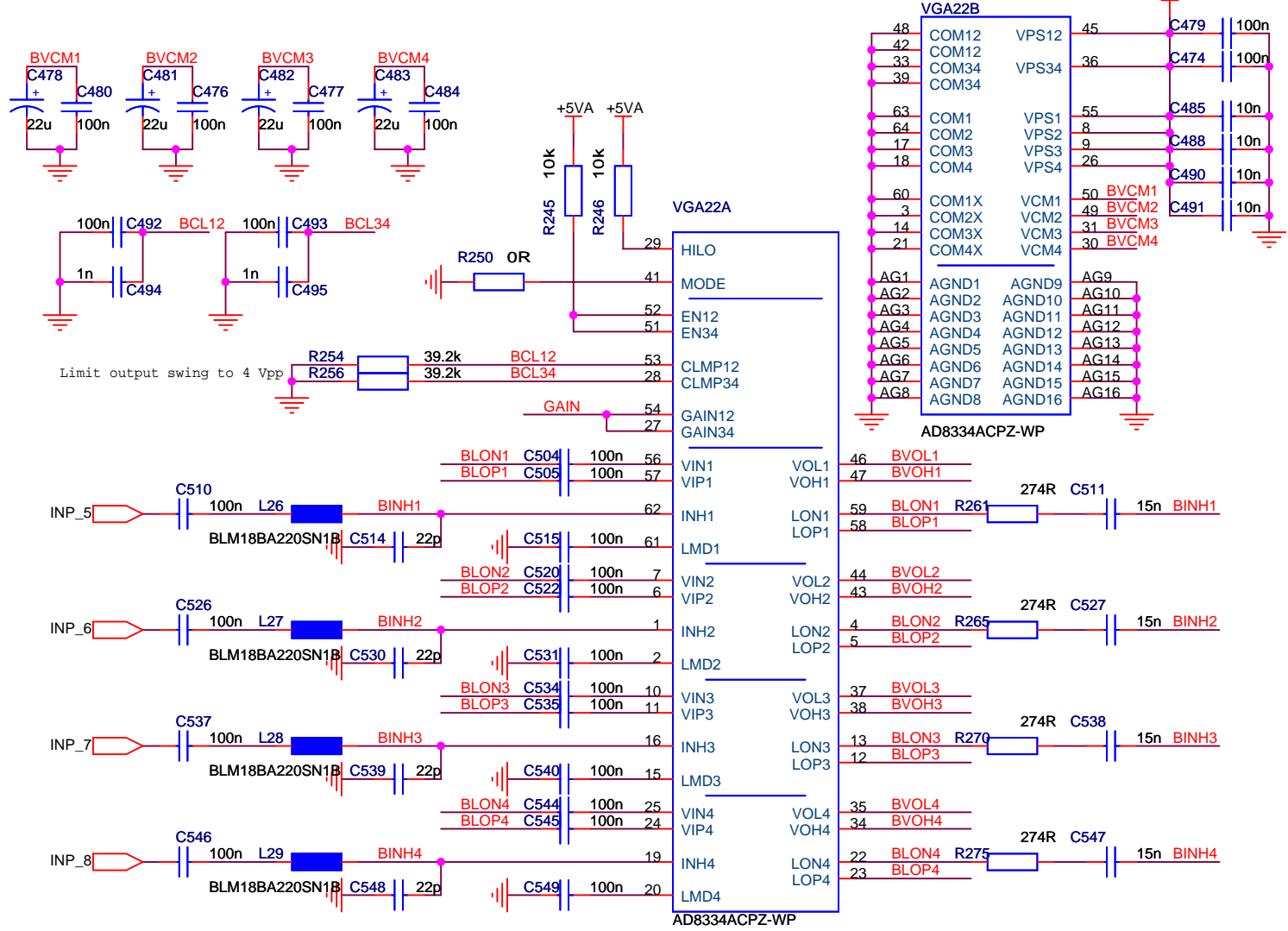
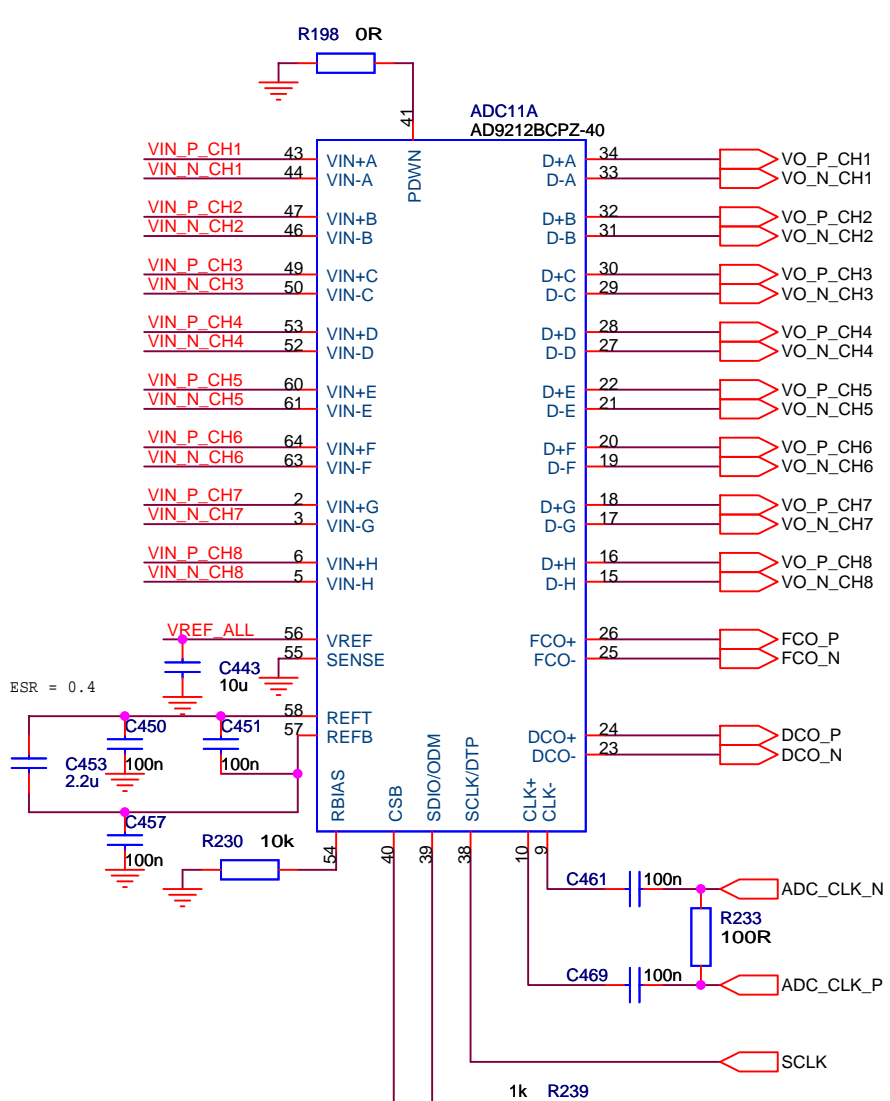
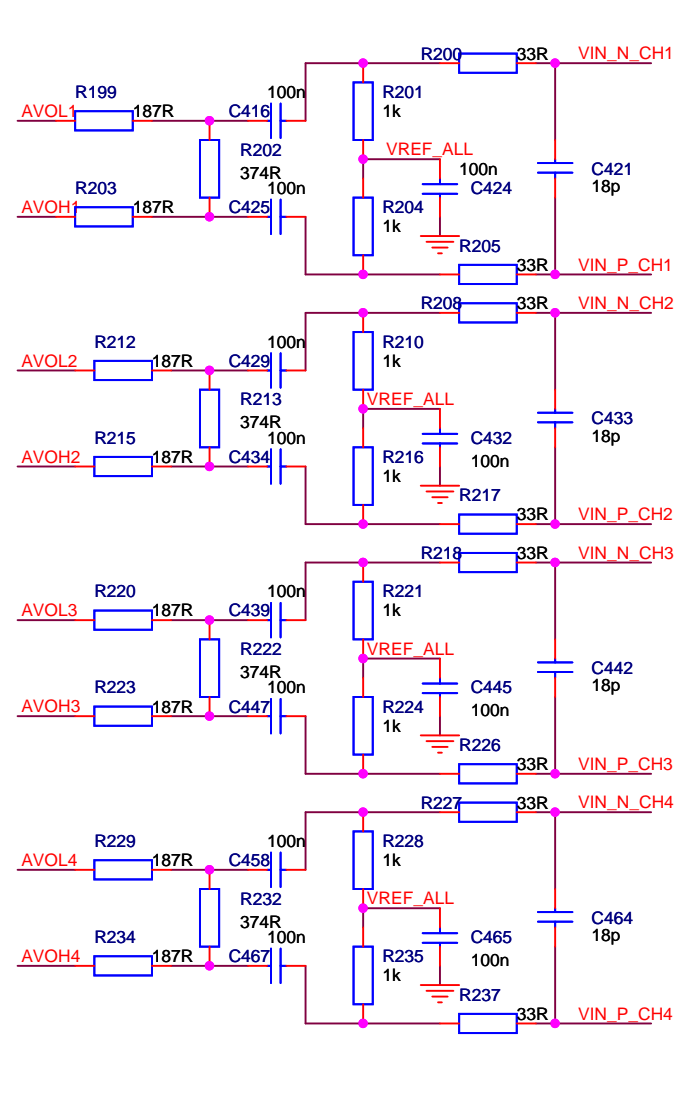
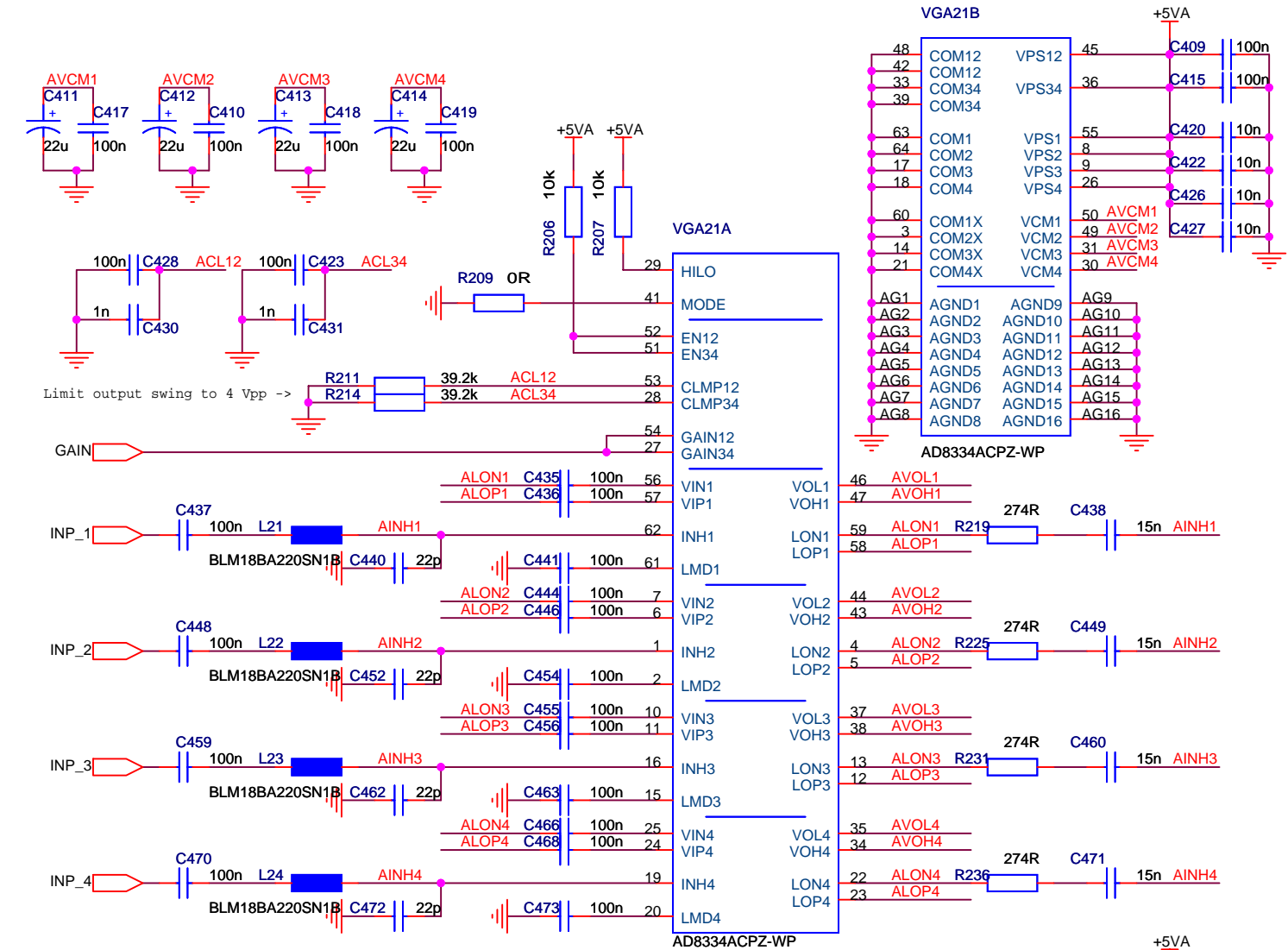
Title			09_POWER_SOURCE		
Size	Document Number	Rev			
A3	<Doc>	<RevC			
Date:	Tuesday, January 29, 2008	Sheet	9	of	21



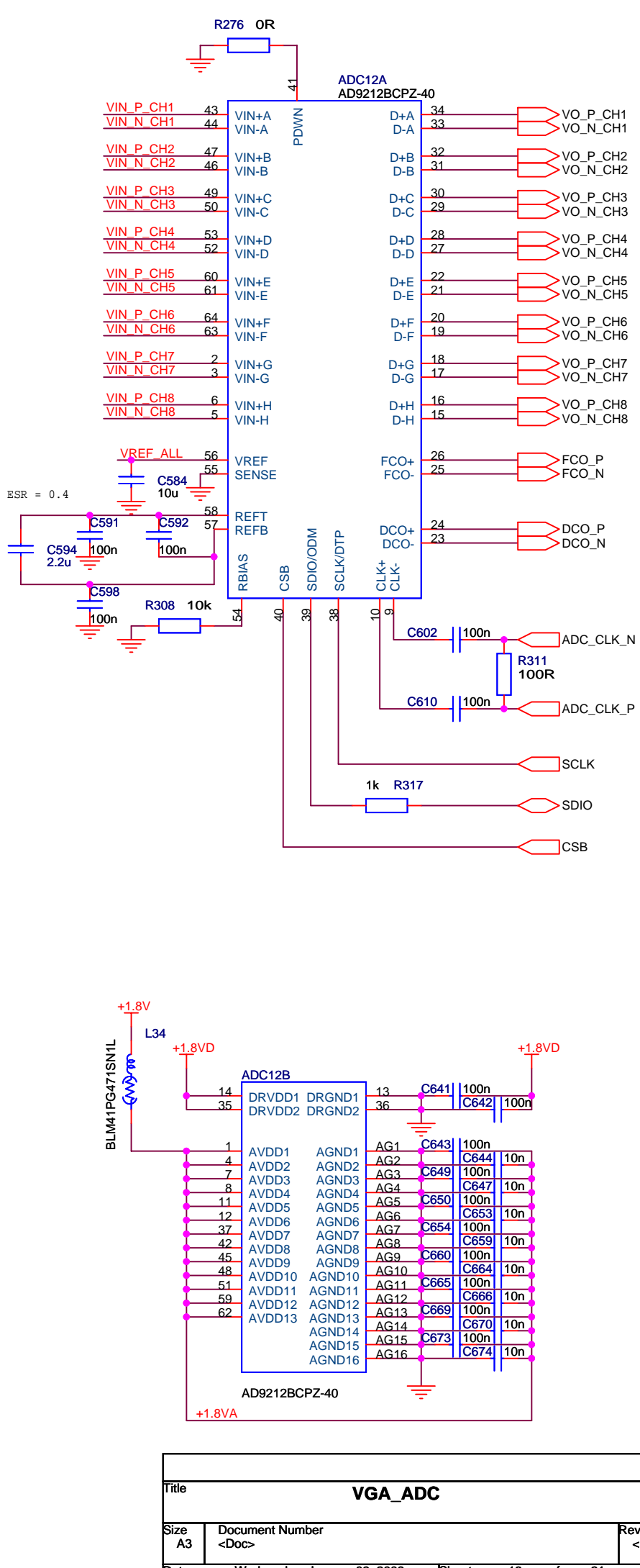
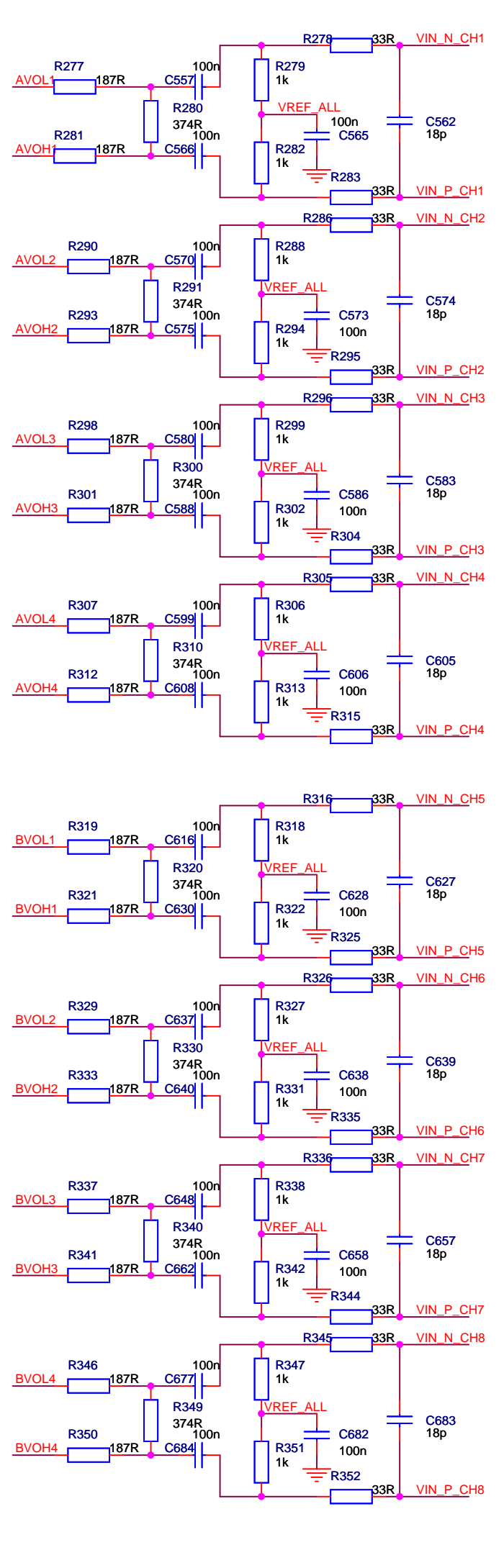
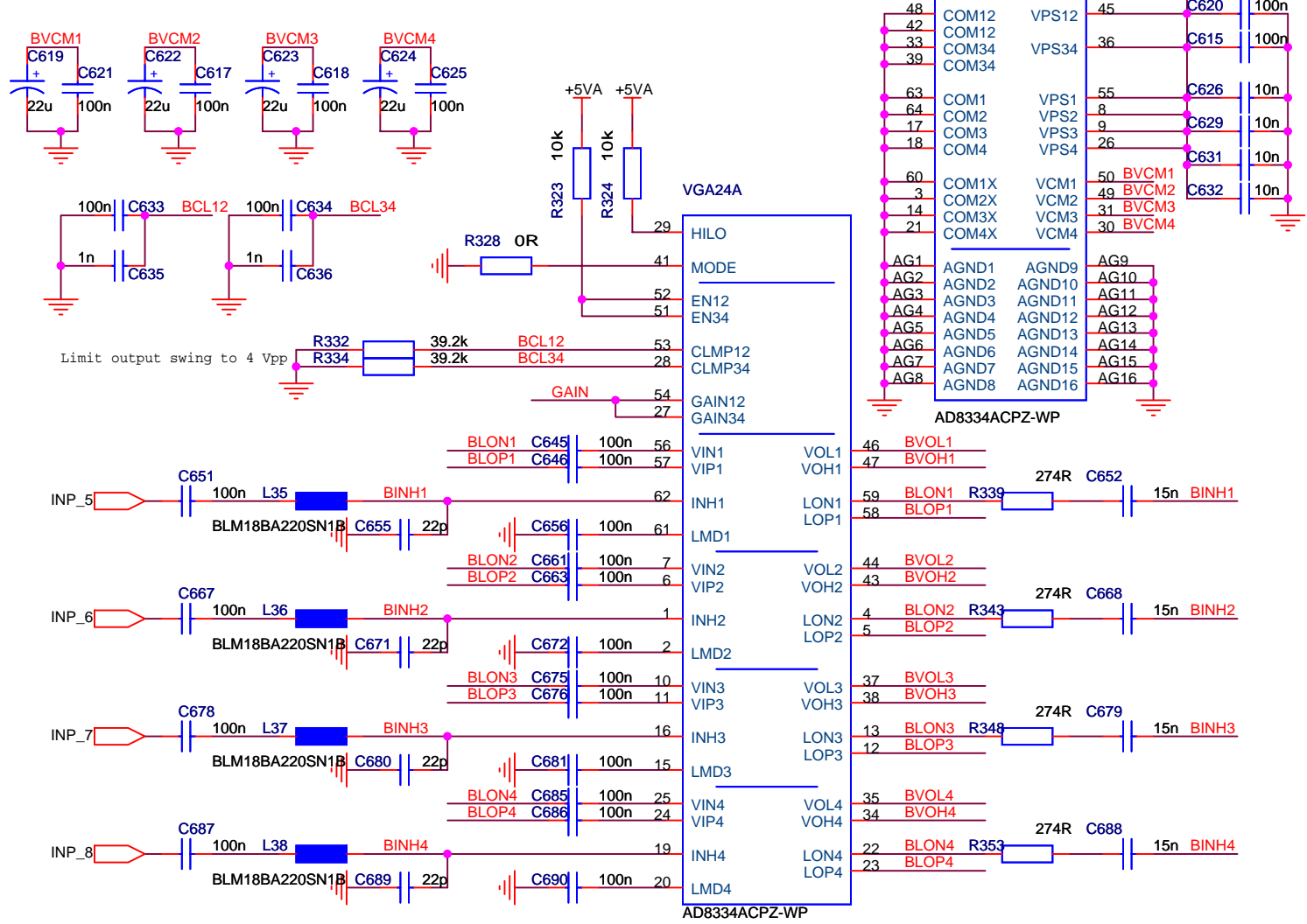
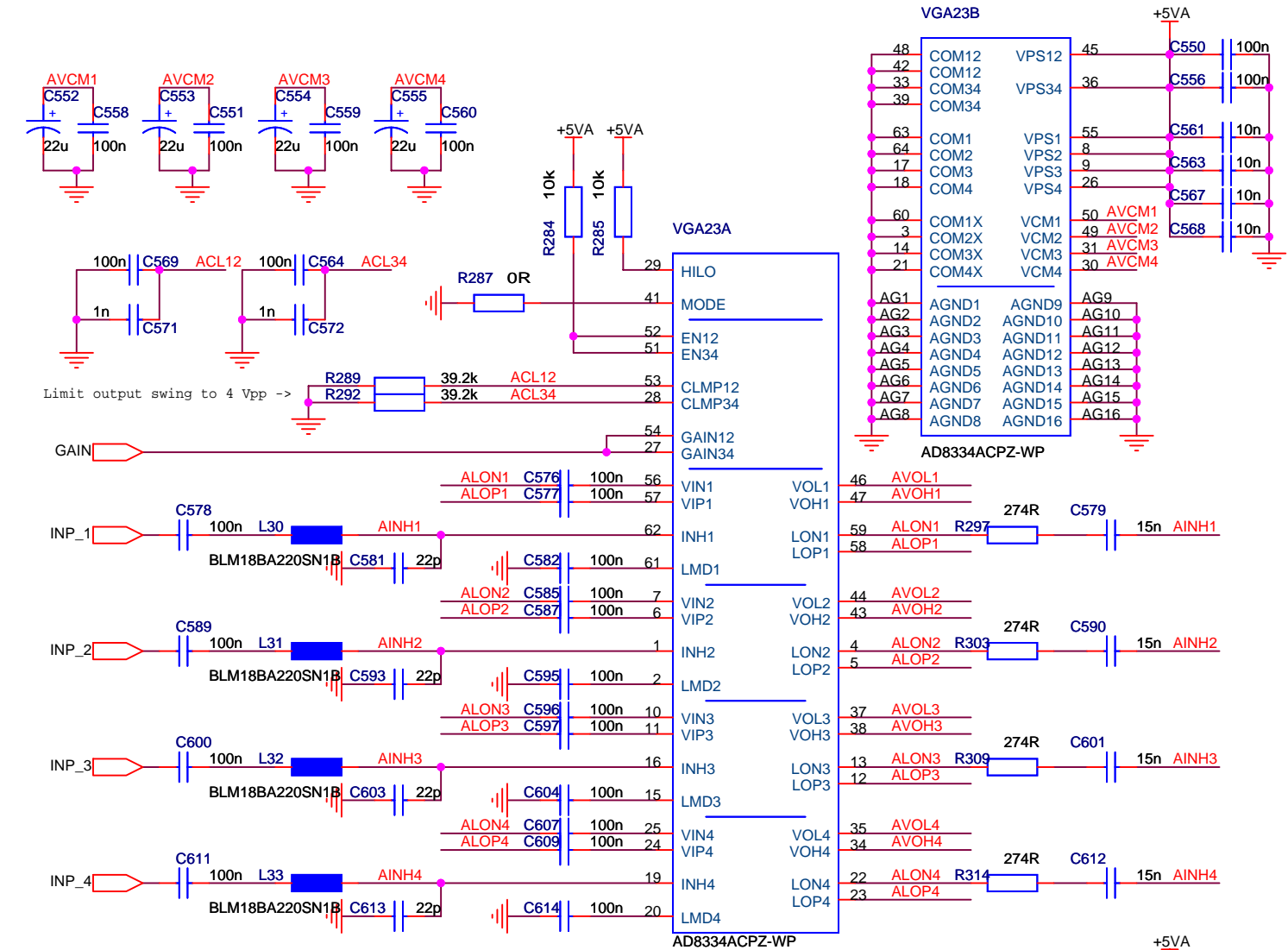
Title			VGA_ADC		
Size	A3	Document Number	<Doc>		Rev
Date:	Wednesday, January 09, 2008	Sheet	10	of	21

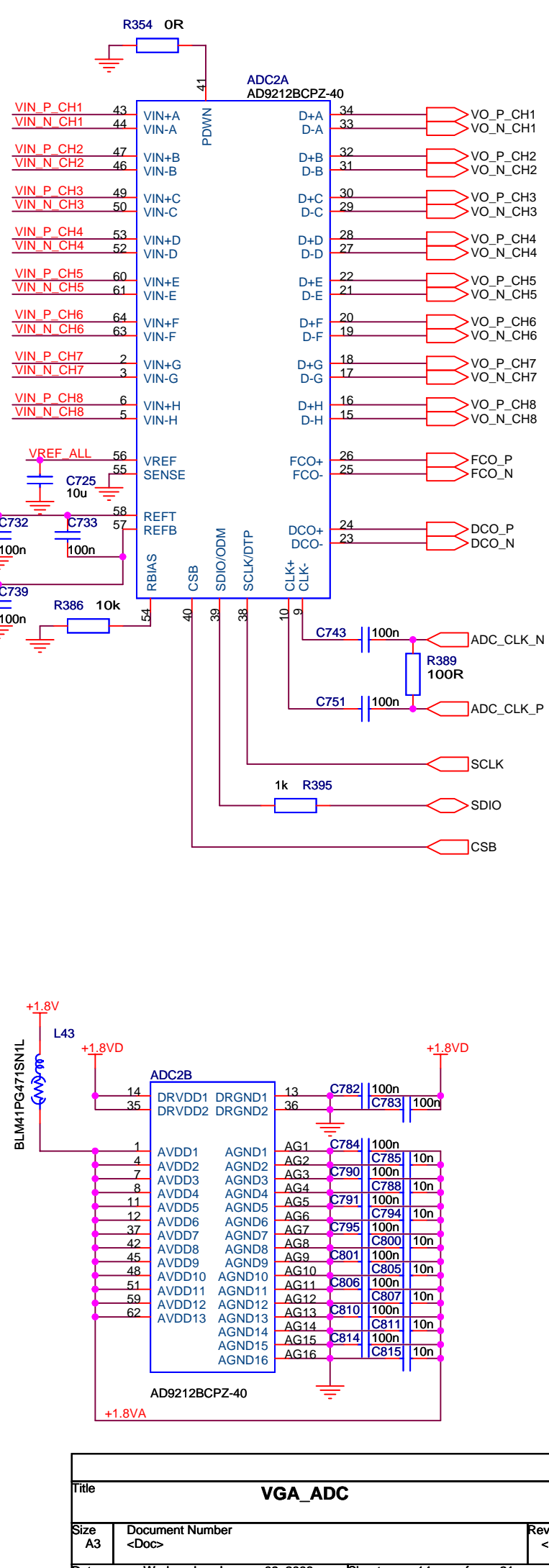
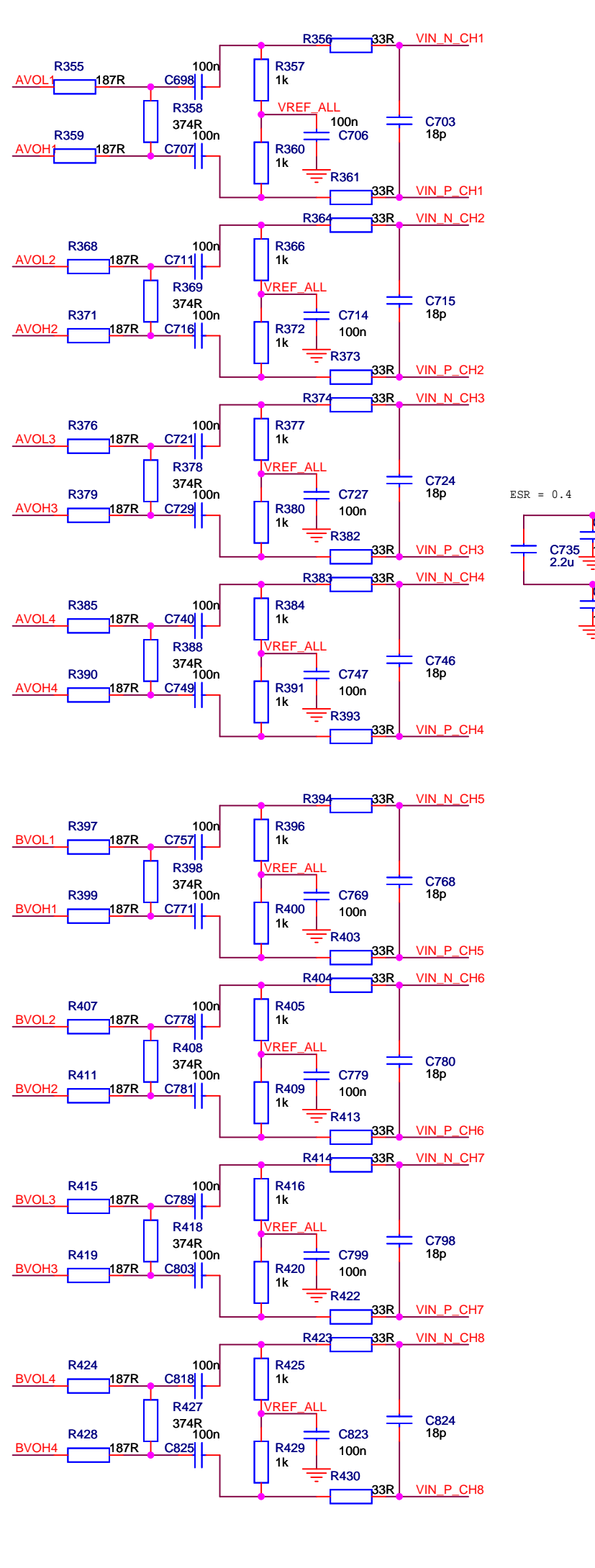
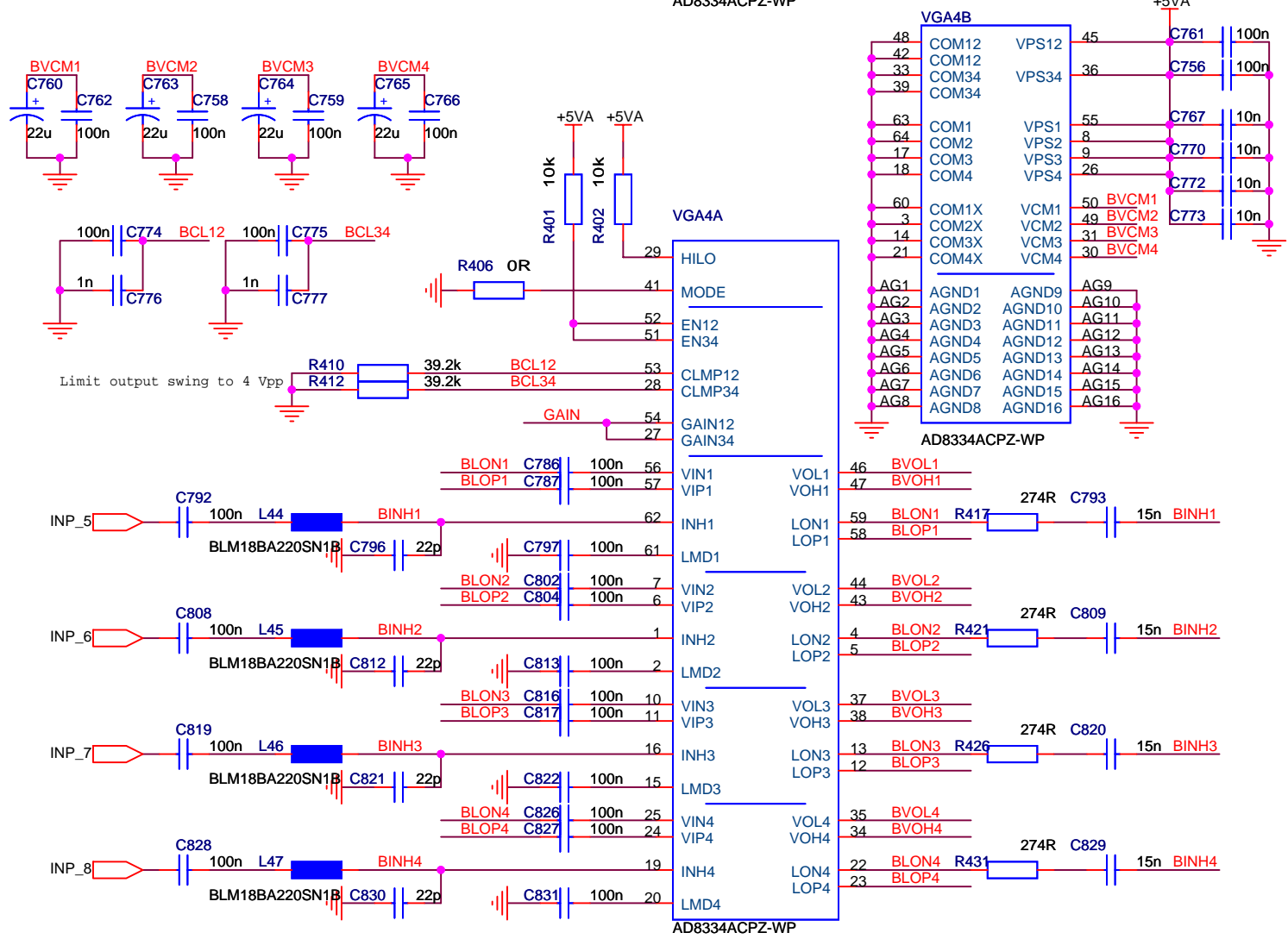
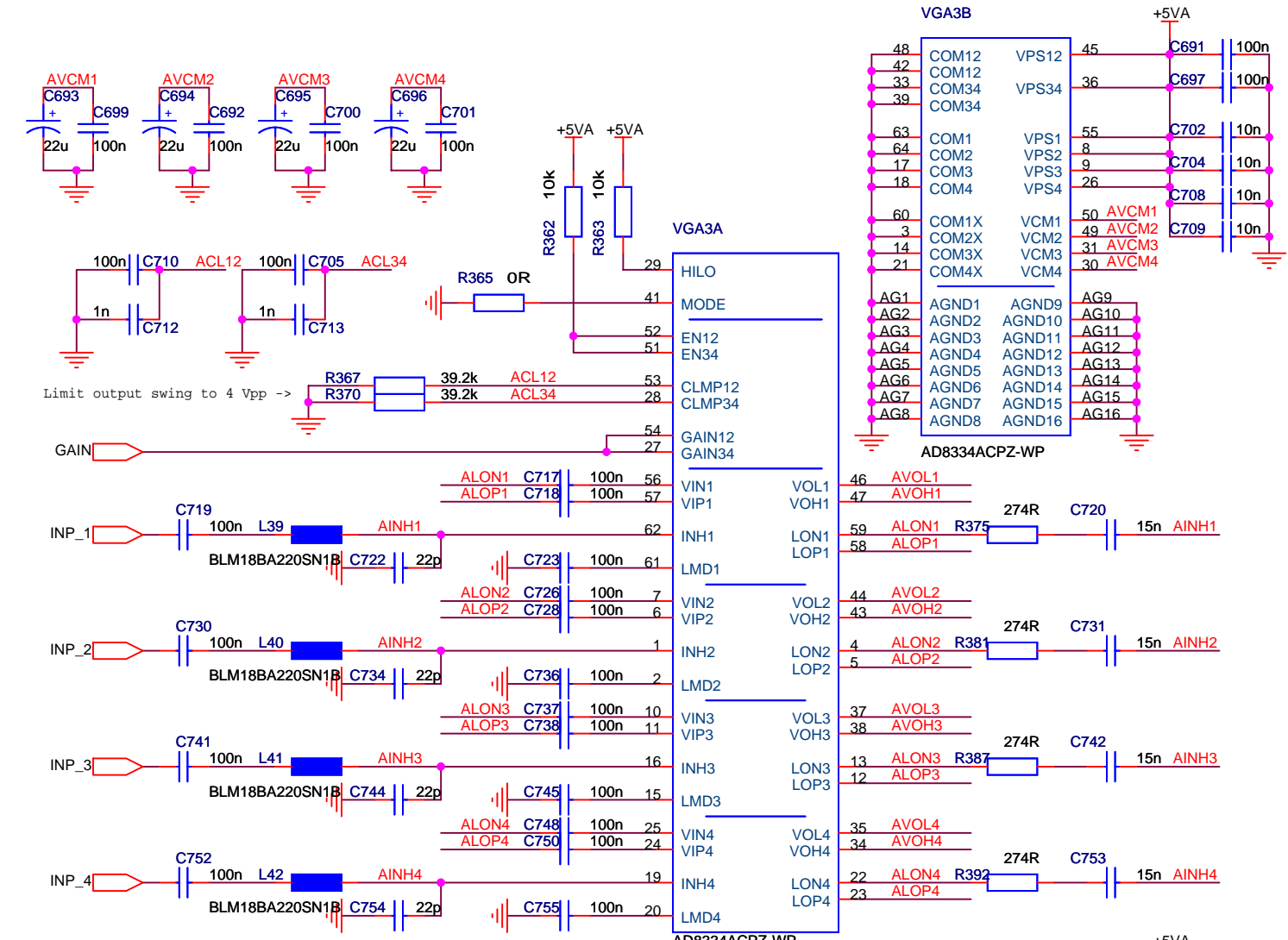


Title			VGA_ADC		
Size	Document Number				Rev
A3	<Doc>				<RevC>
Date:	Wednesday, January 09, 2008	Sheet	11	of	21

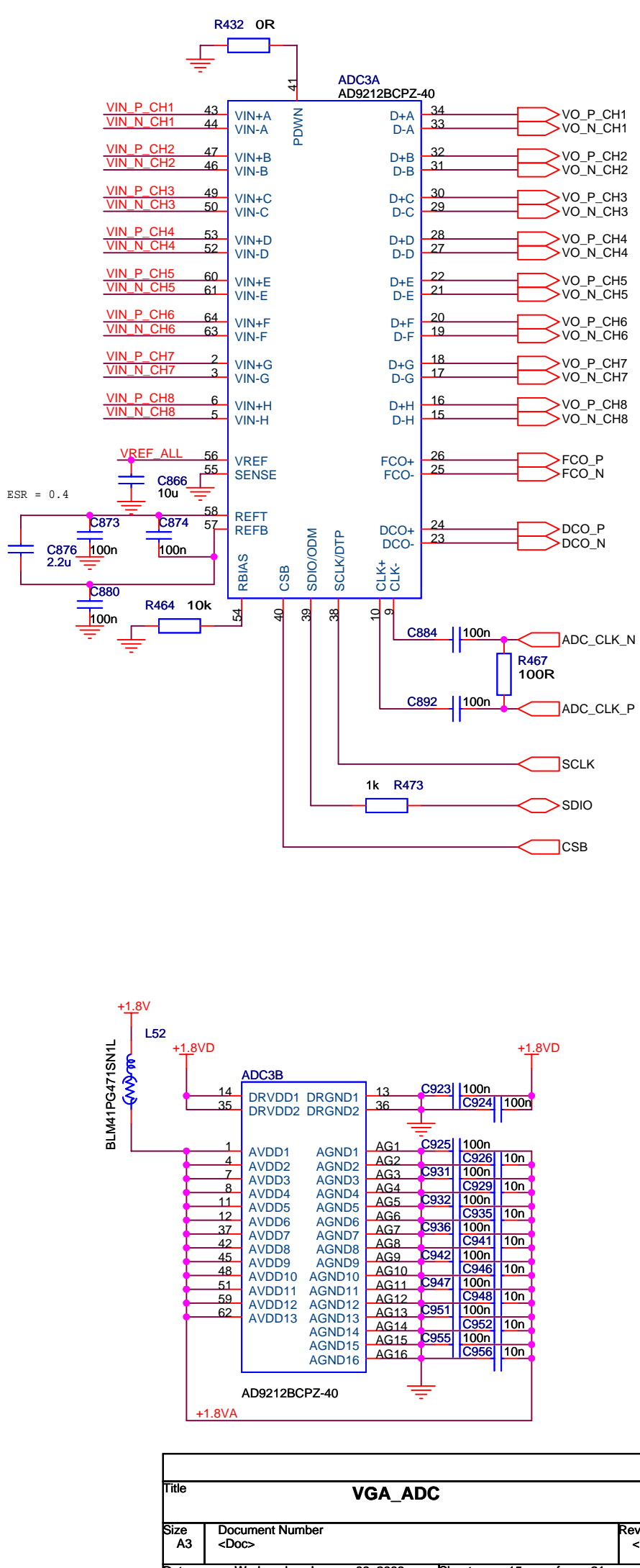
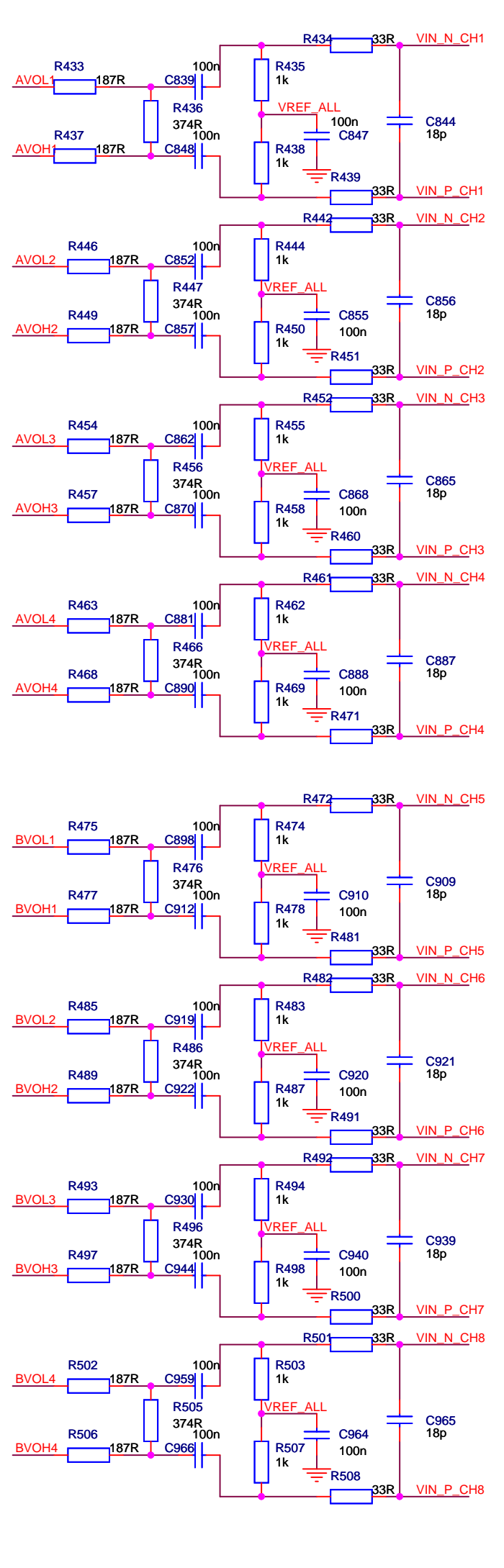
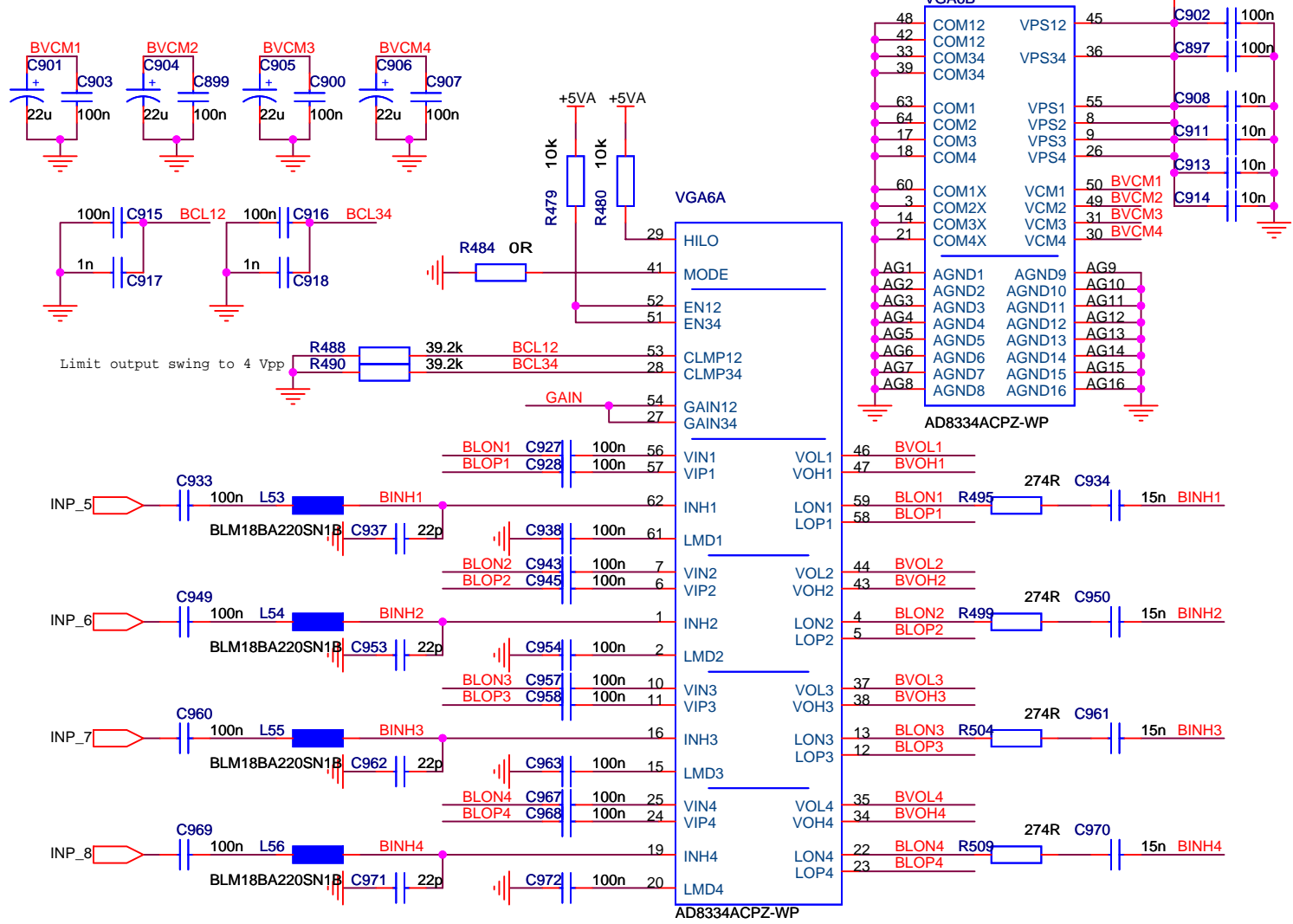
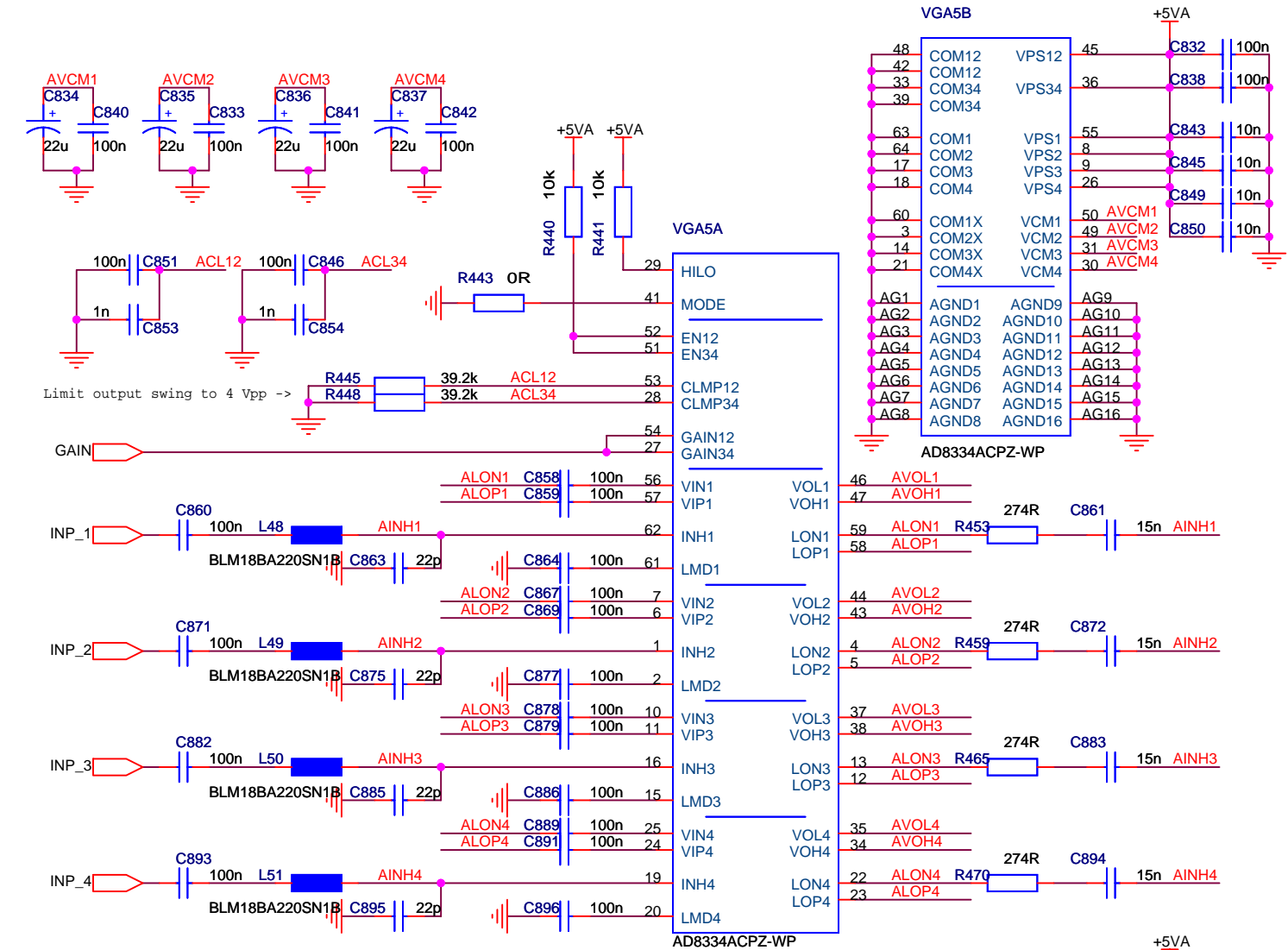


Title			VGA_ADC		
Size	Document Number				Rev
A3	<Doc>				<RevC>
Date:	Wednesday, January 09, 2008	Sheet	12	of	21

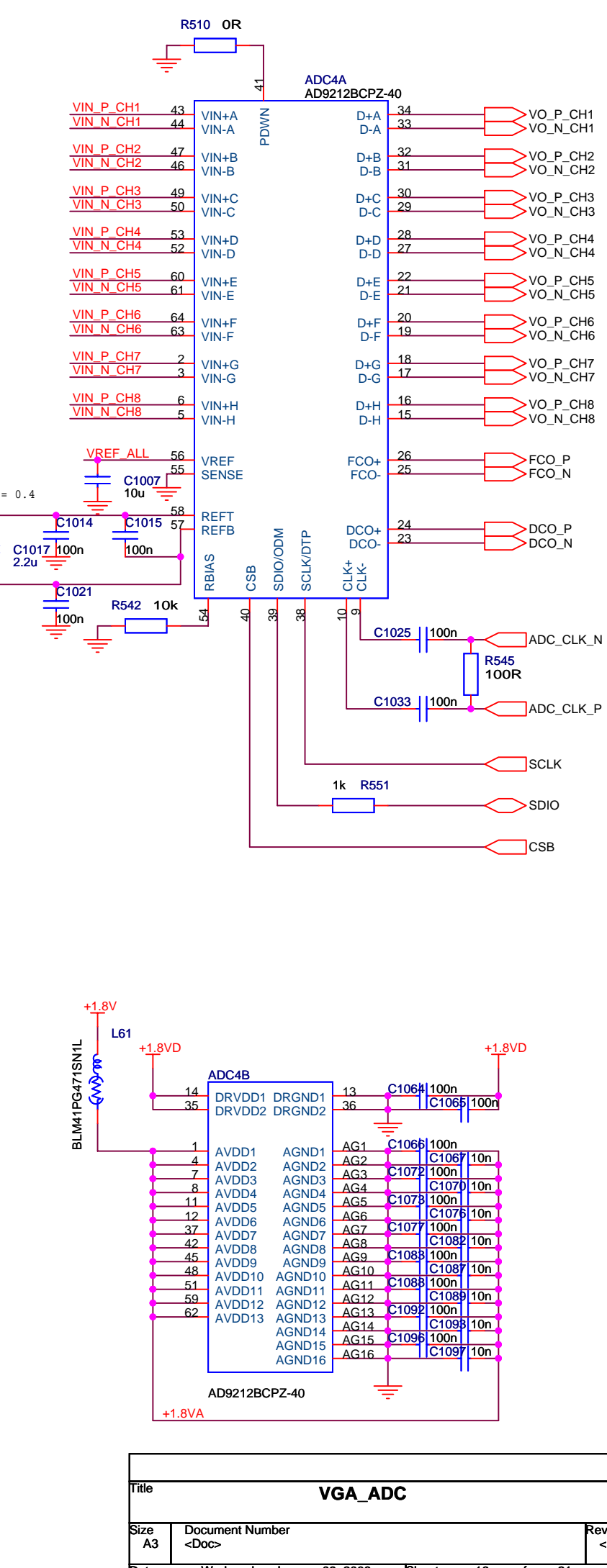
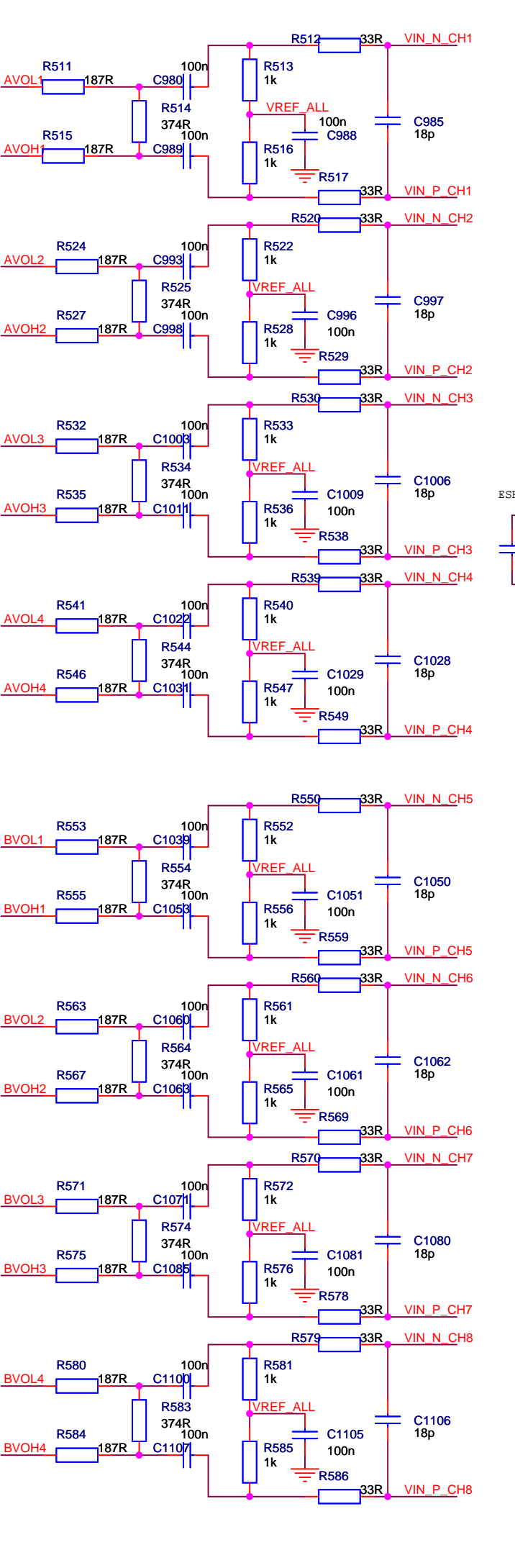
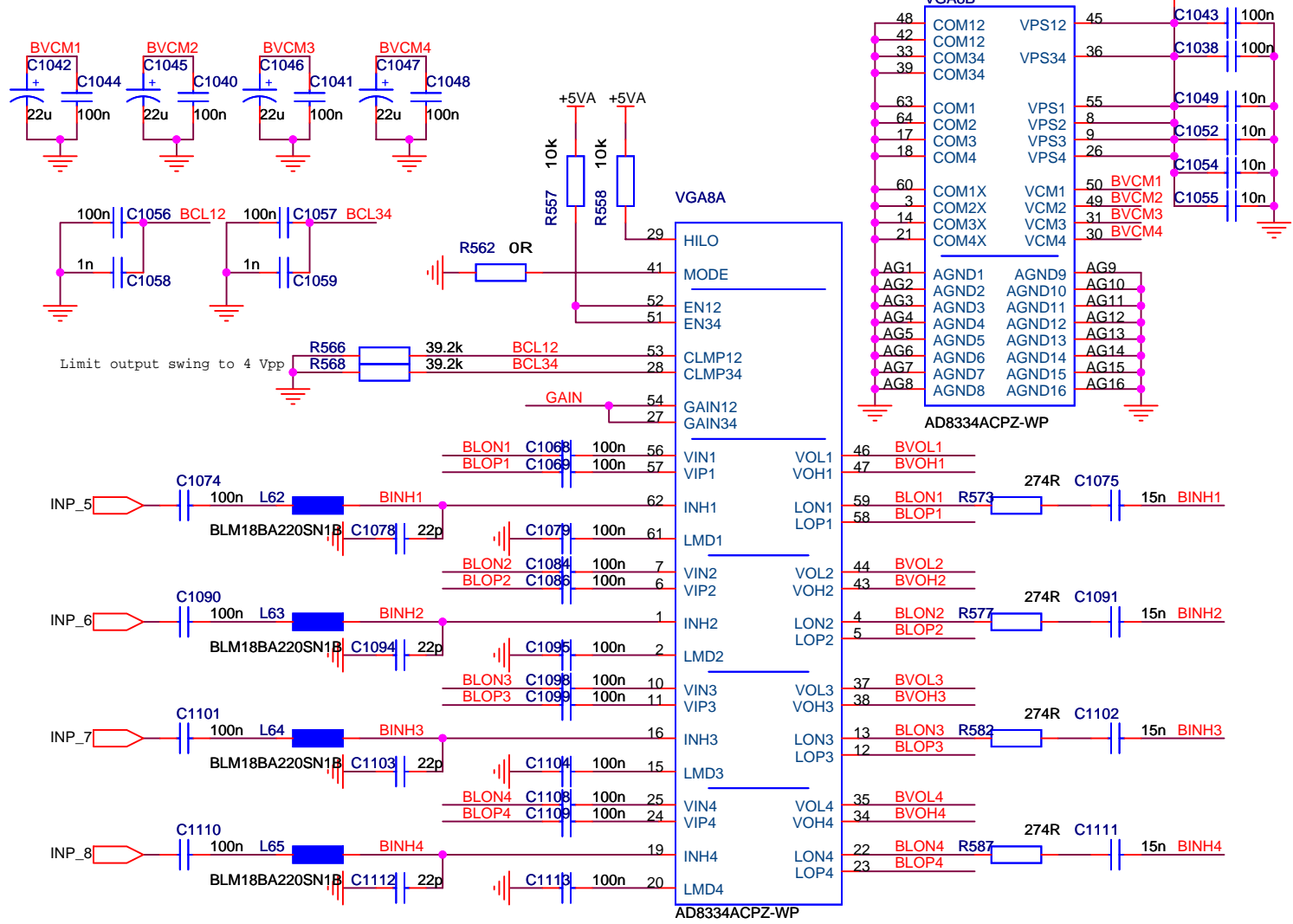
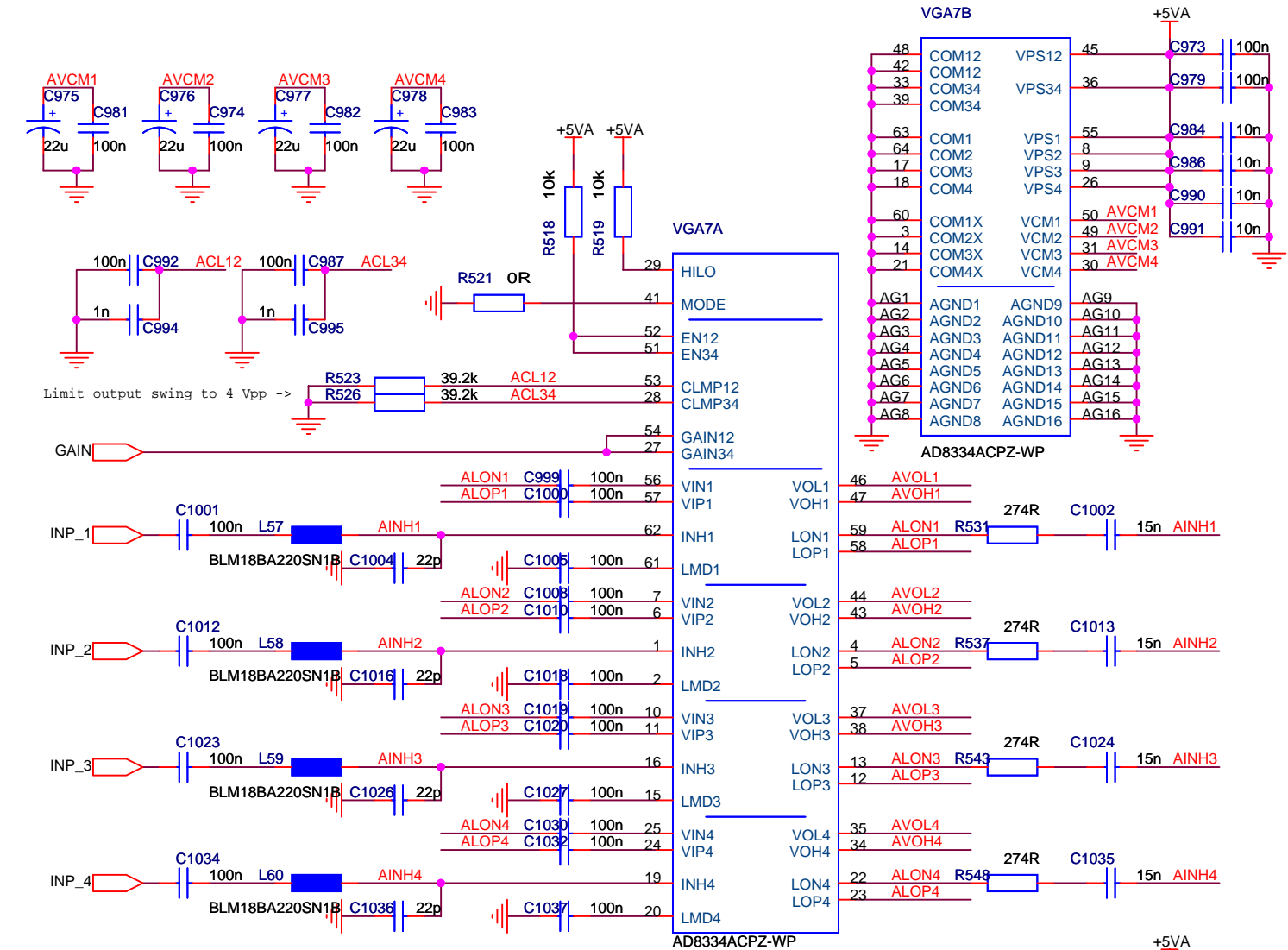




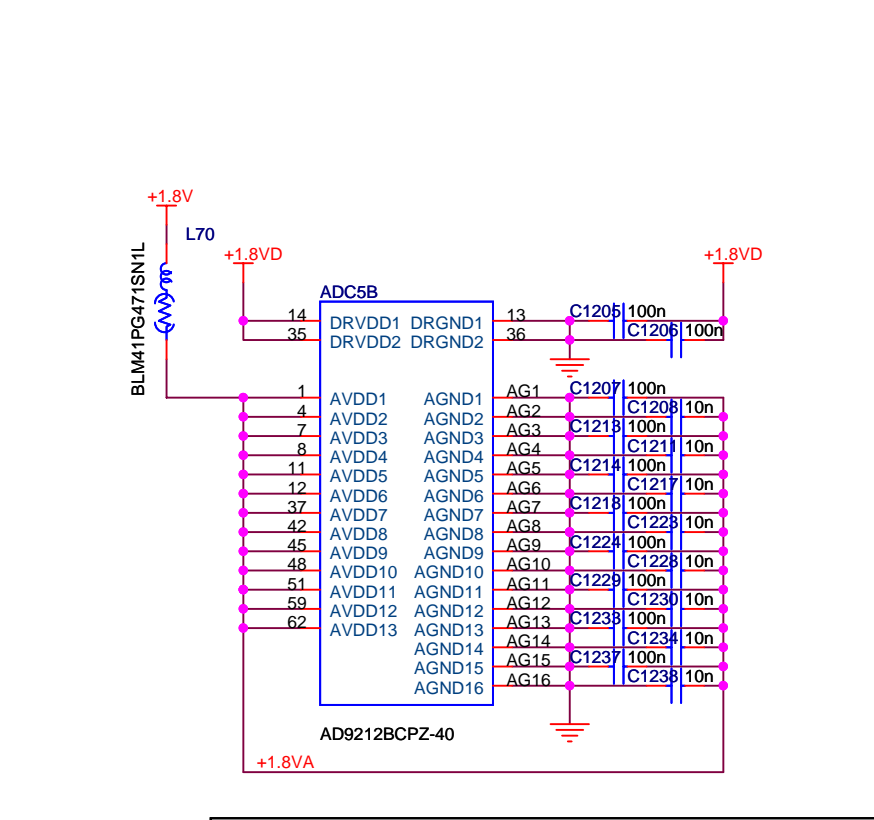
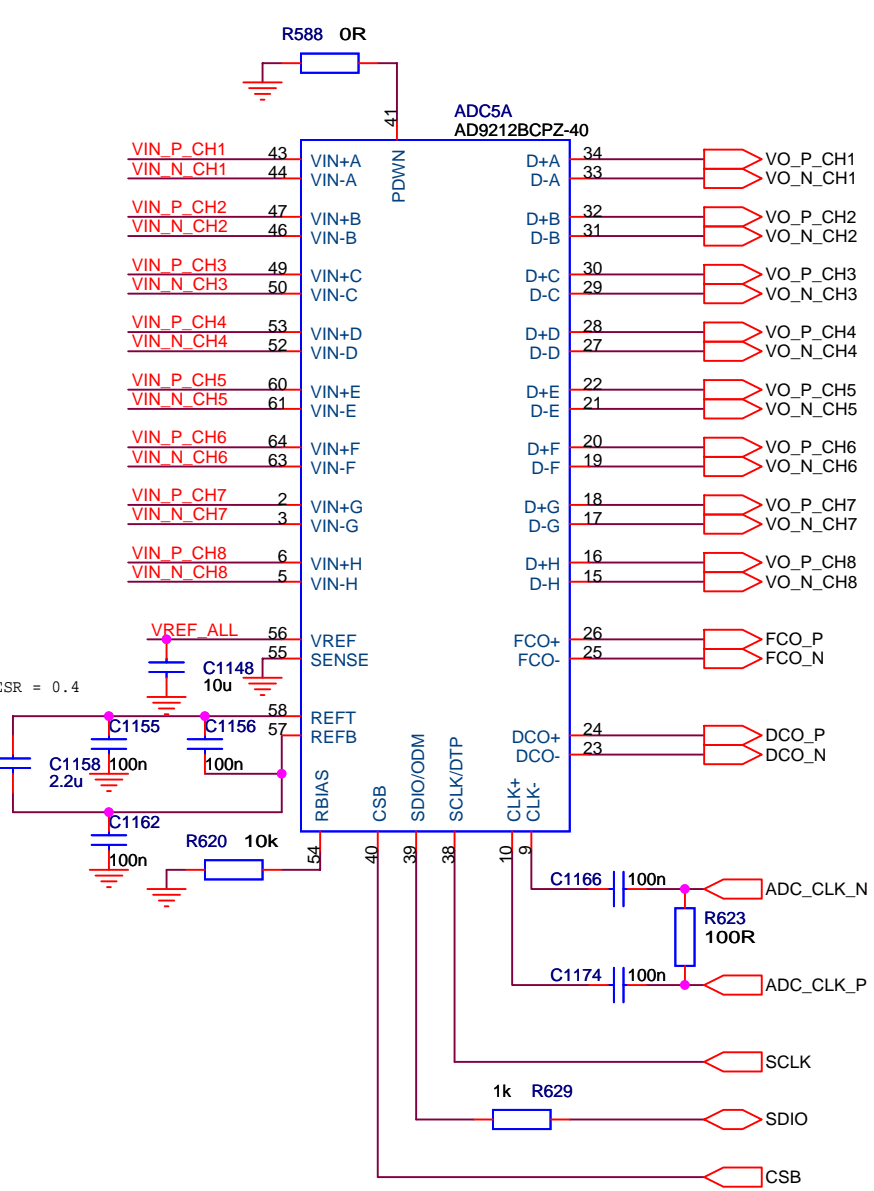
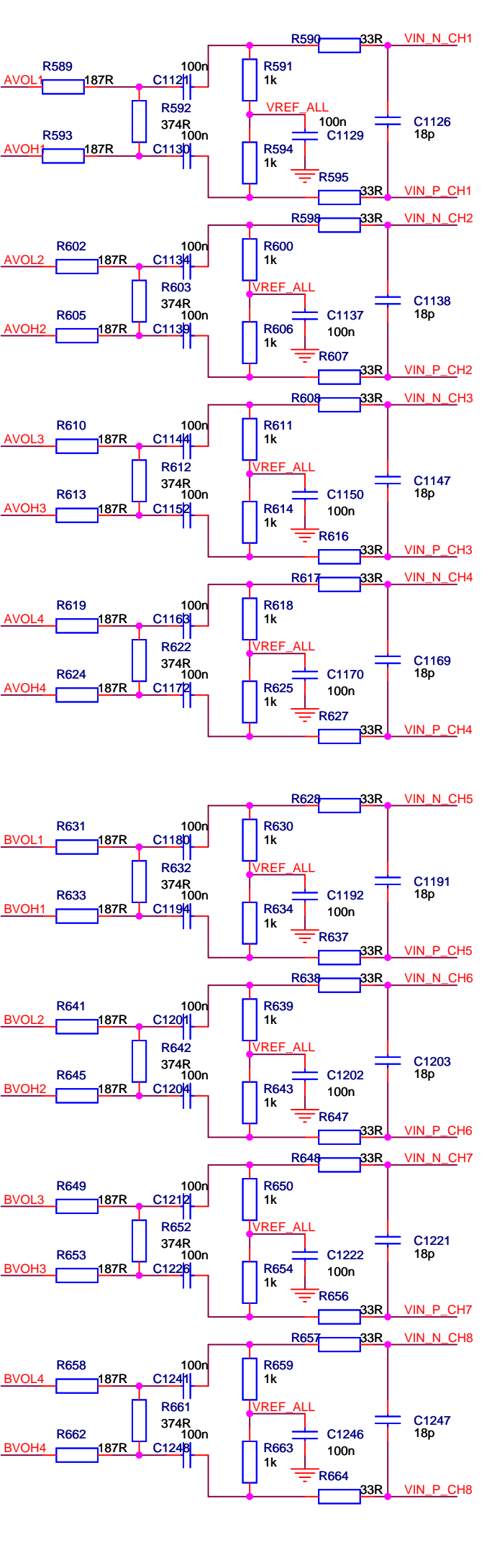
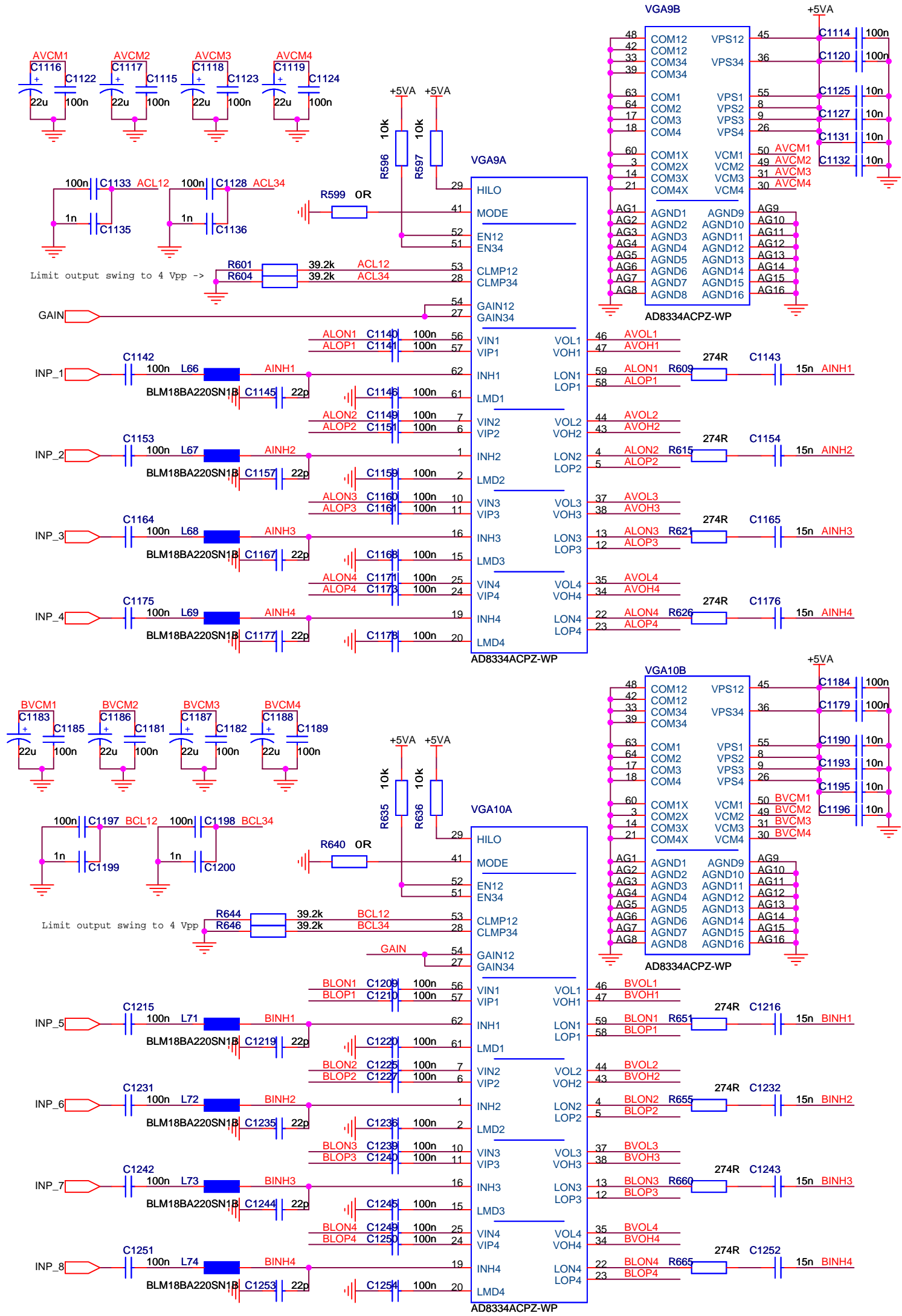
Title			VGA_ADC		
Size	A3	Document Number	<Doc>		
Date:	Wednesday, January 09, 2008		Sheet	14	of 21



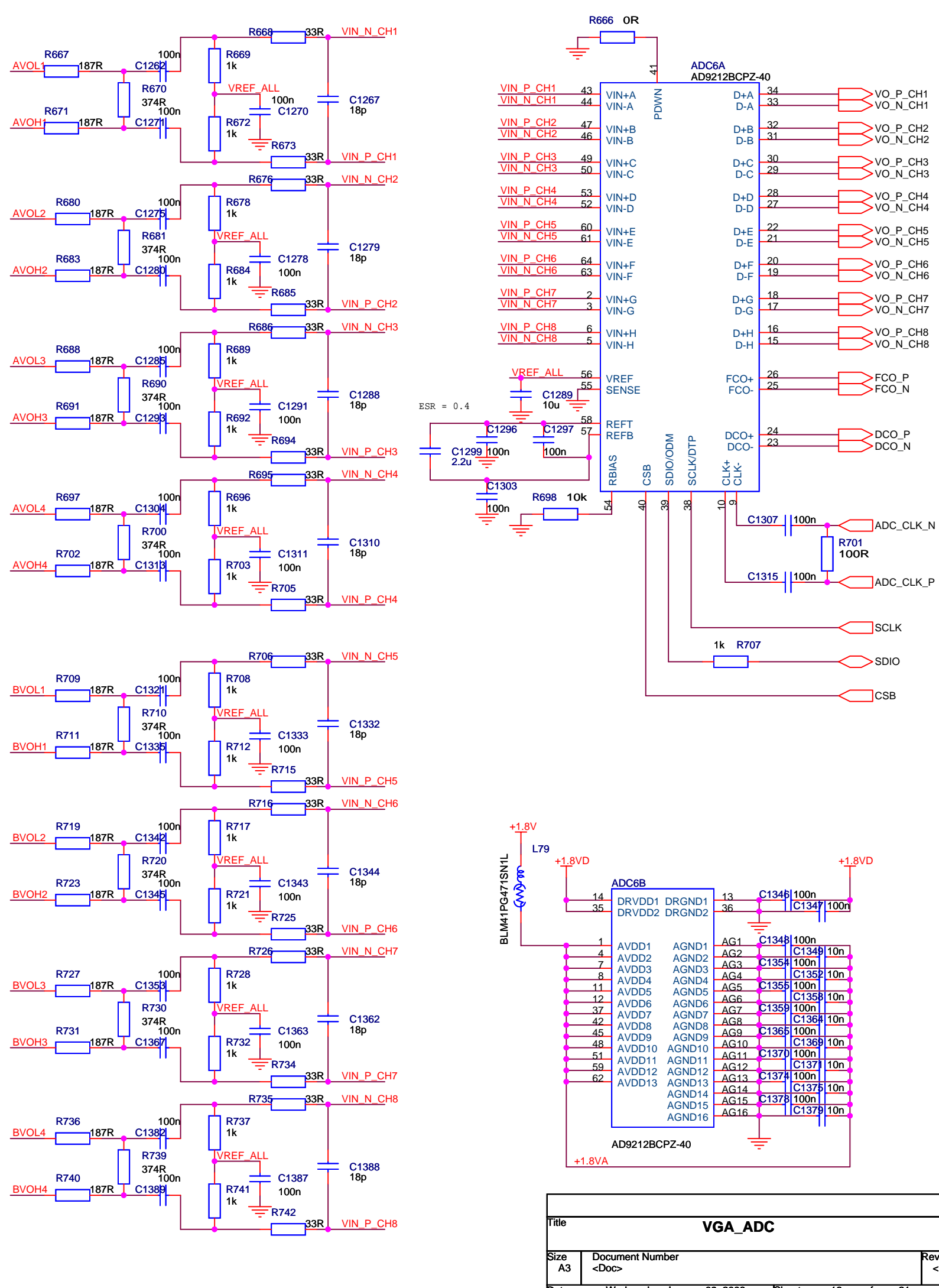
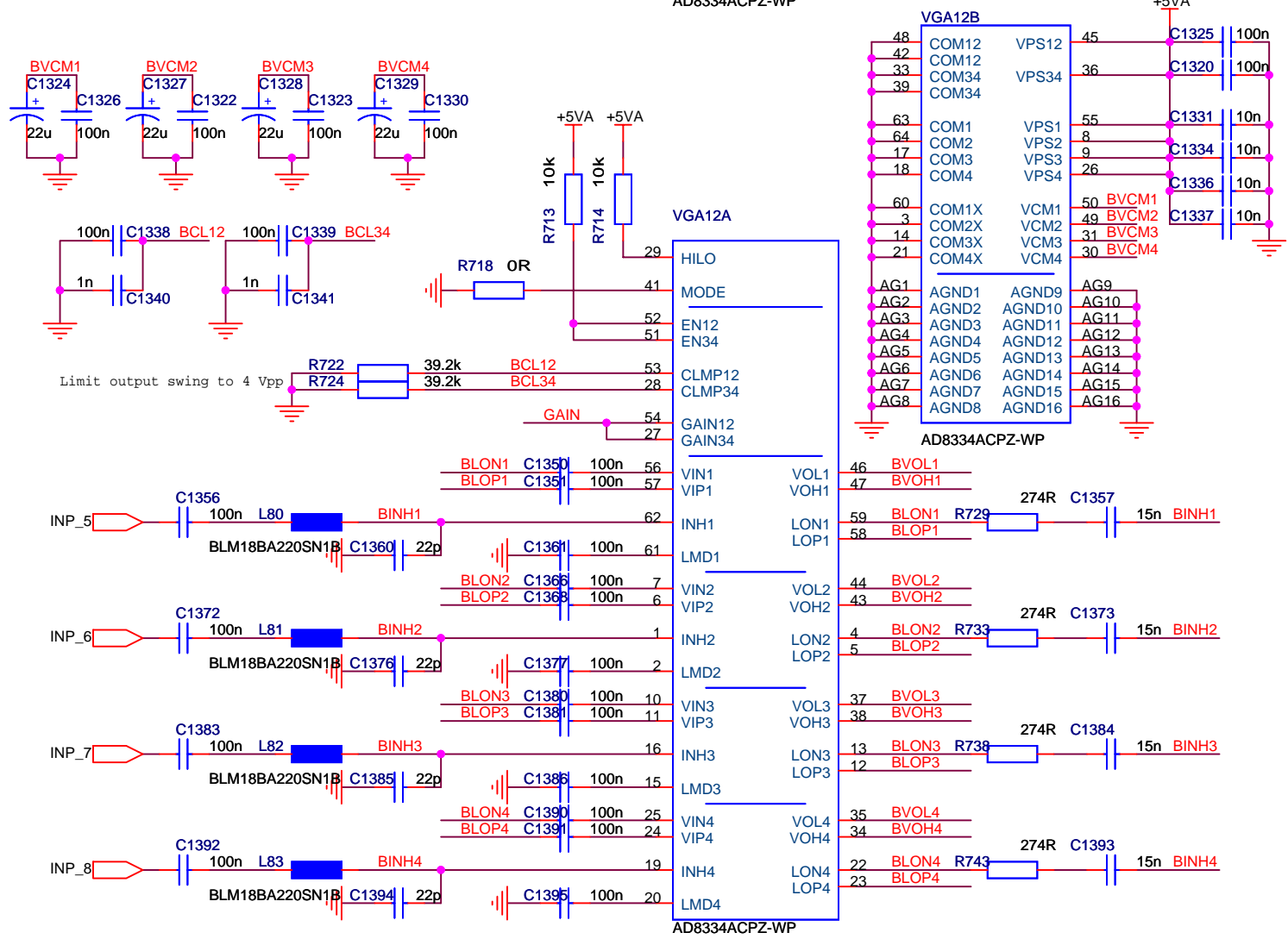
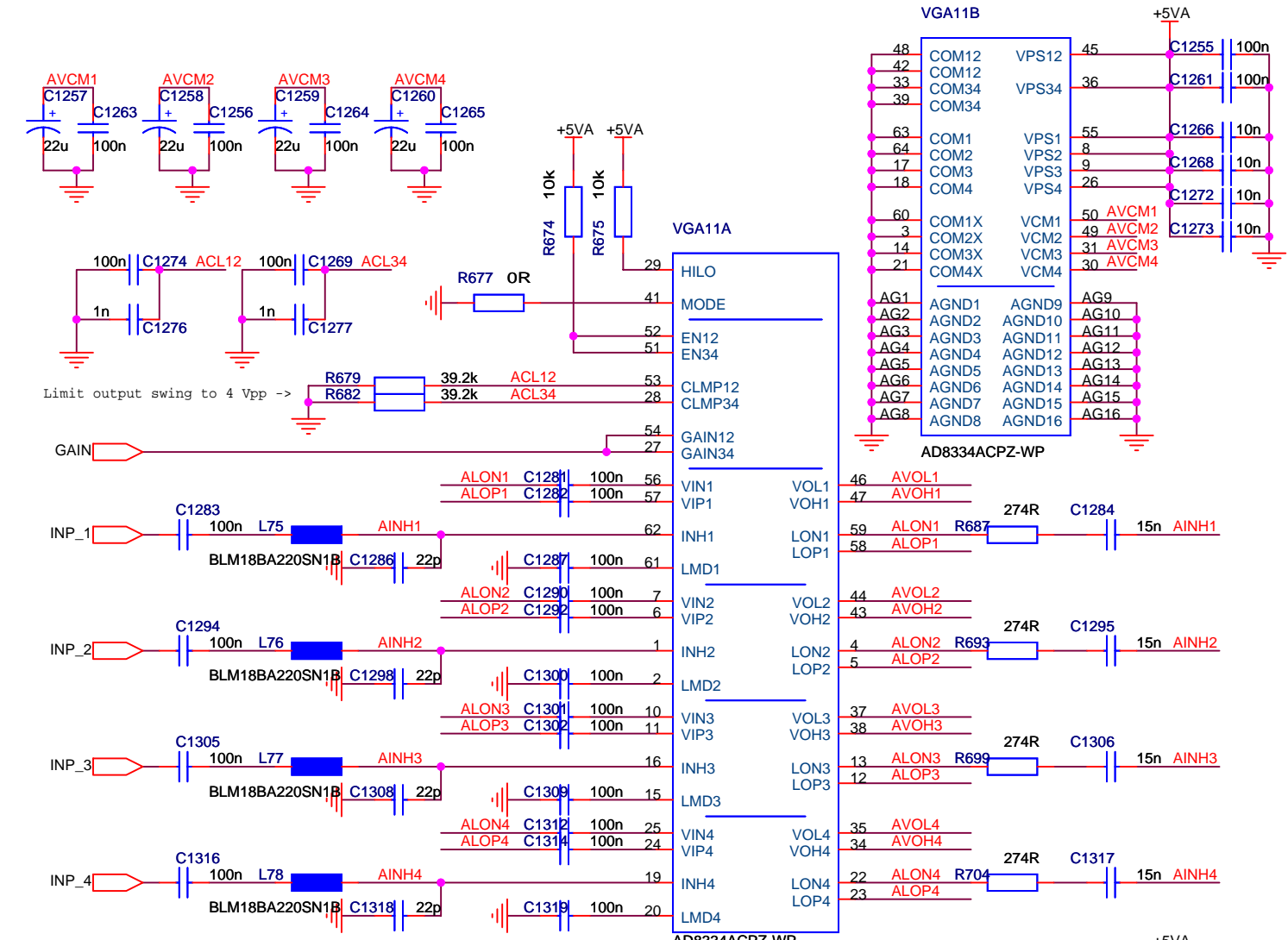
Title			VGA_ADC		
Size	A3	Document Number	<Doc>		Rev
Date:	Wednesday, January 09, 2008	Sheet	15	of	21



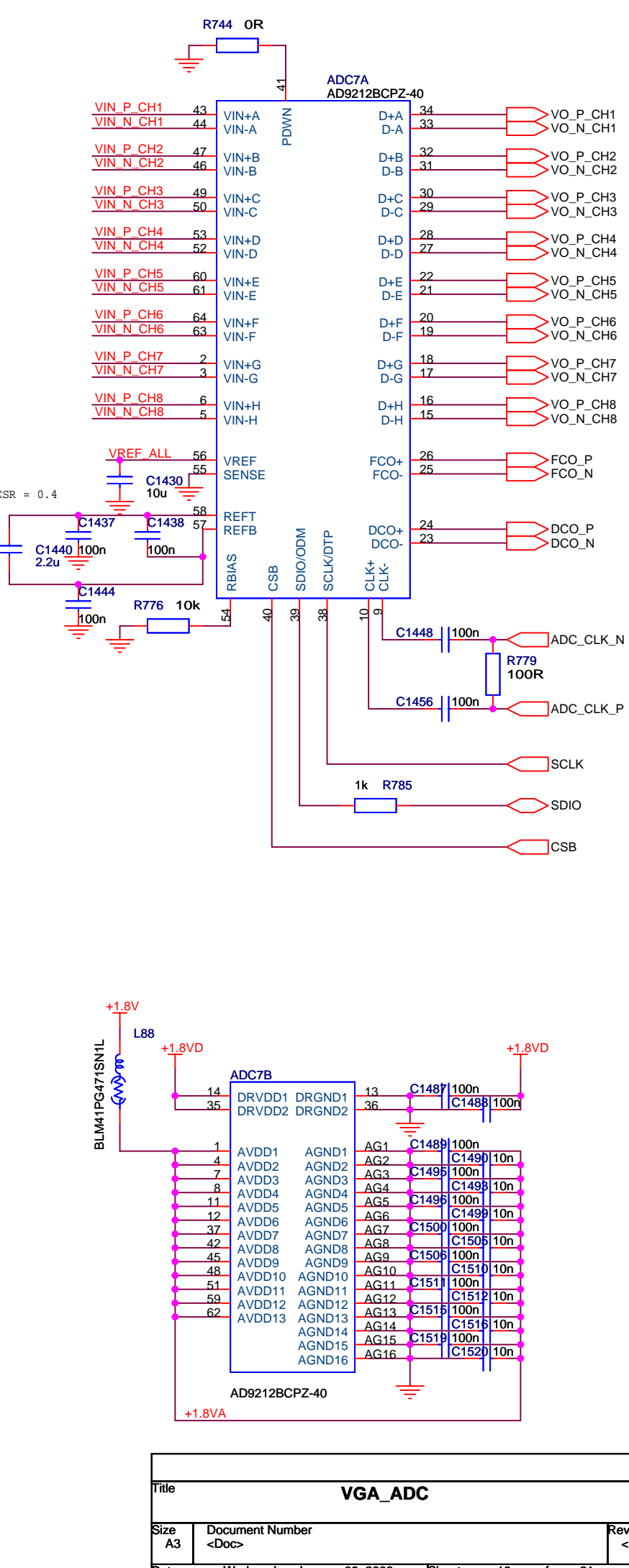
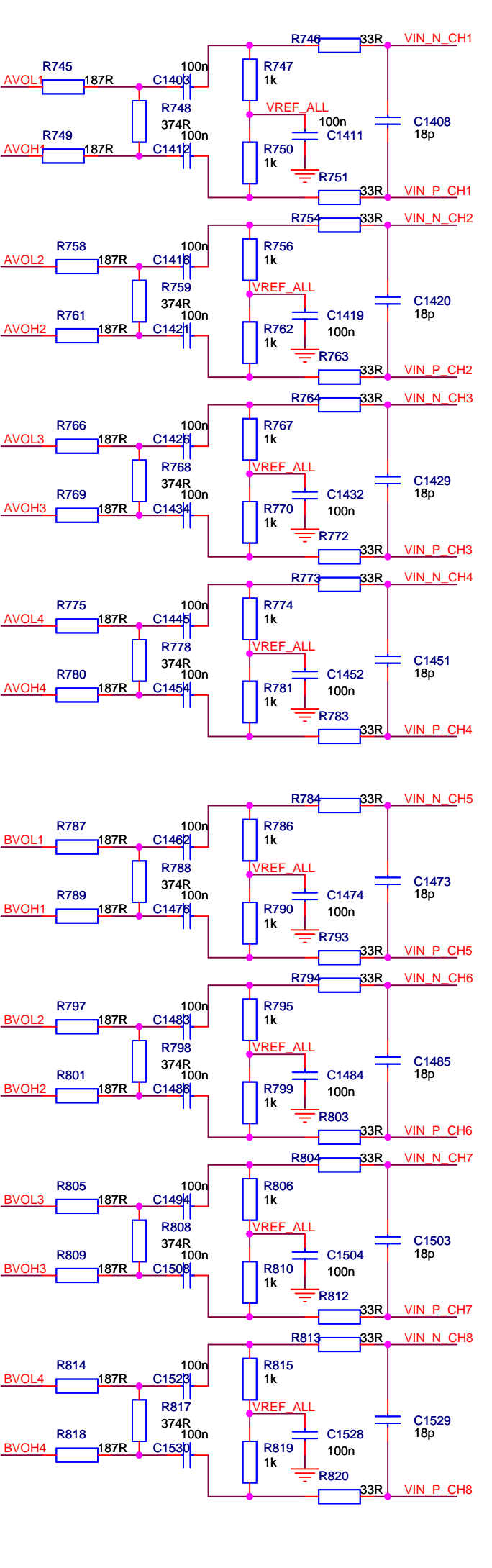
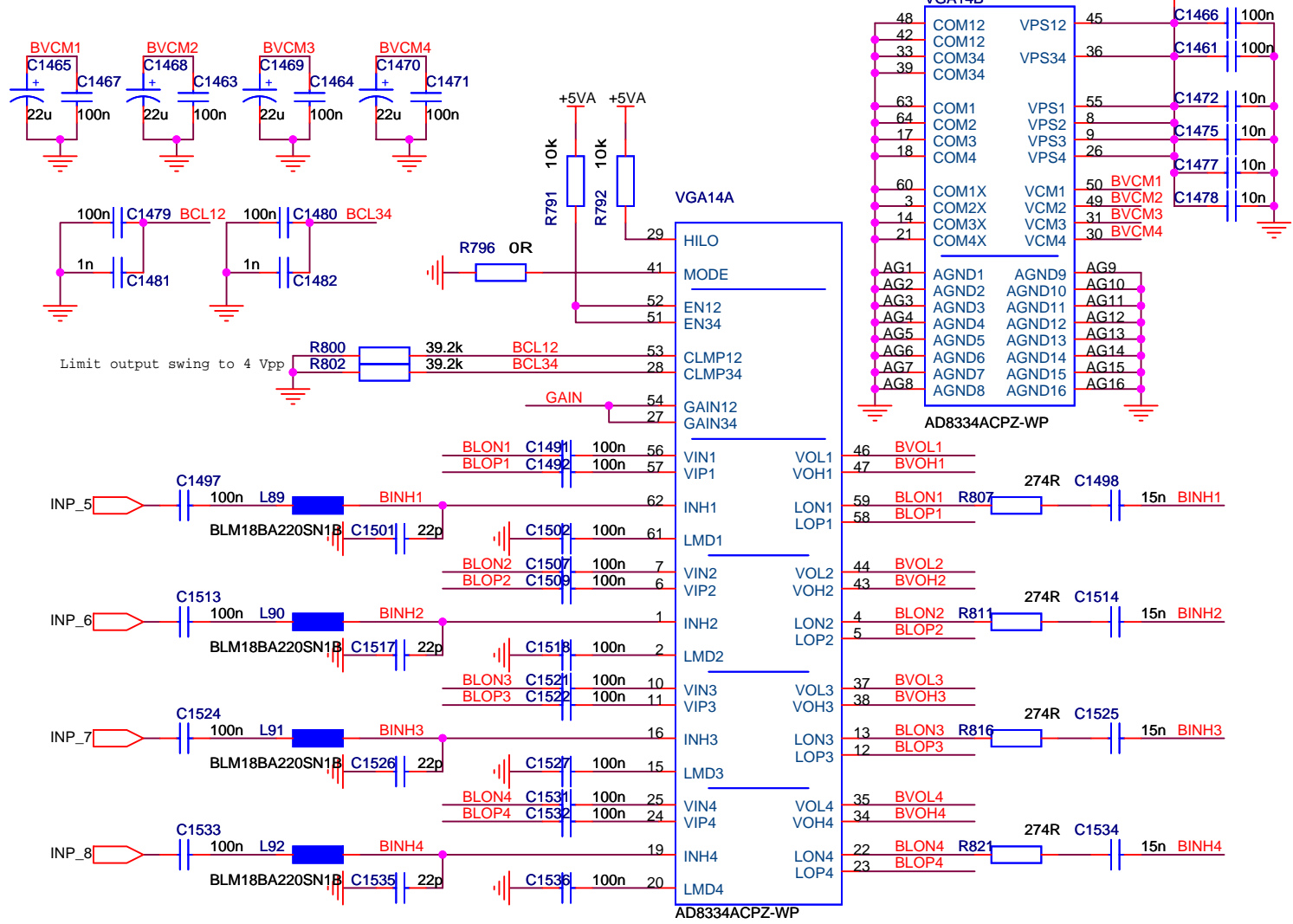
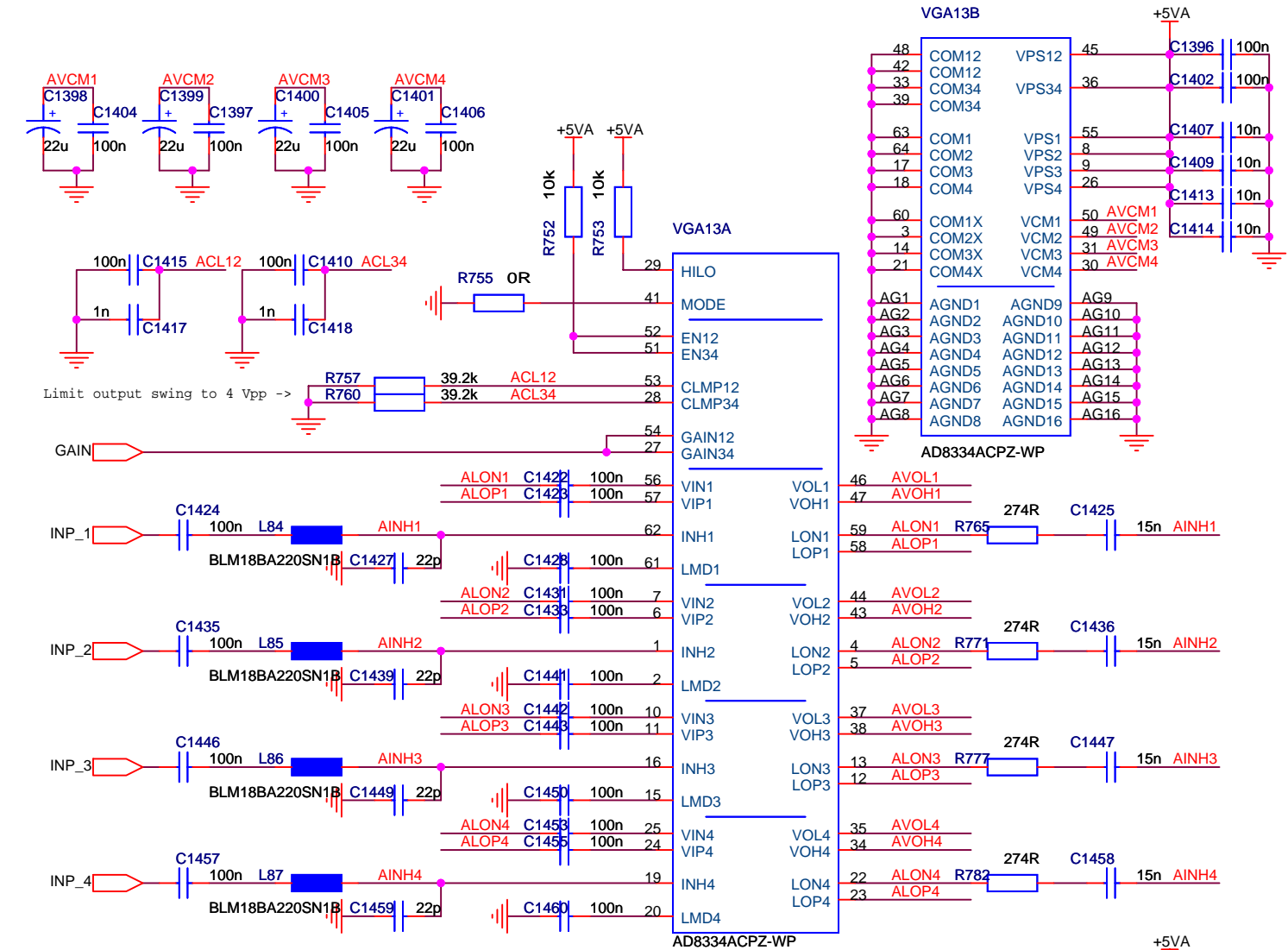
Title			VGA_ADC		
Size	A3	Document Number	<Doc>		
Date:	Wednesday, January 09, 2008	Sheet	16	of	21



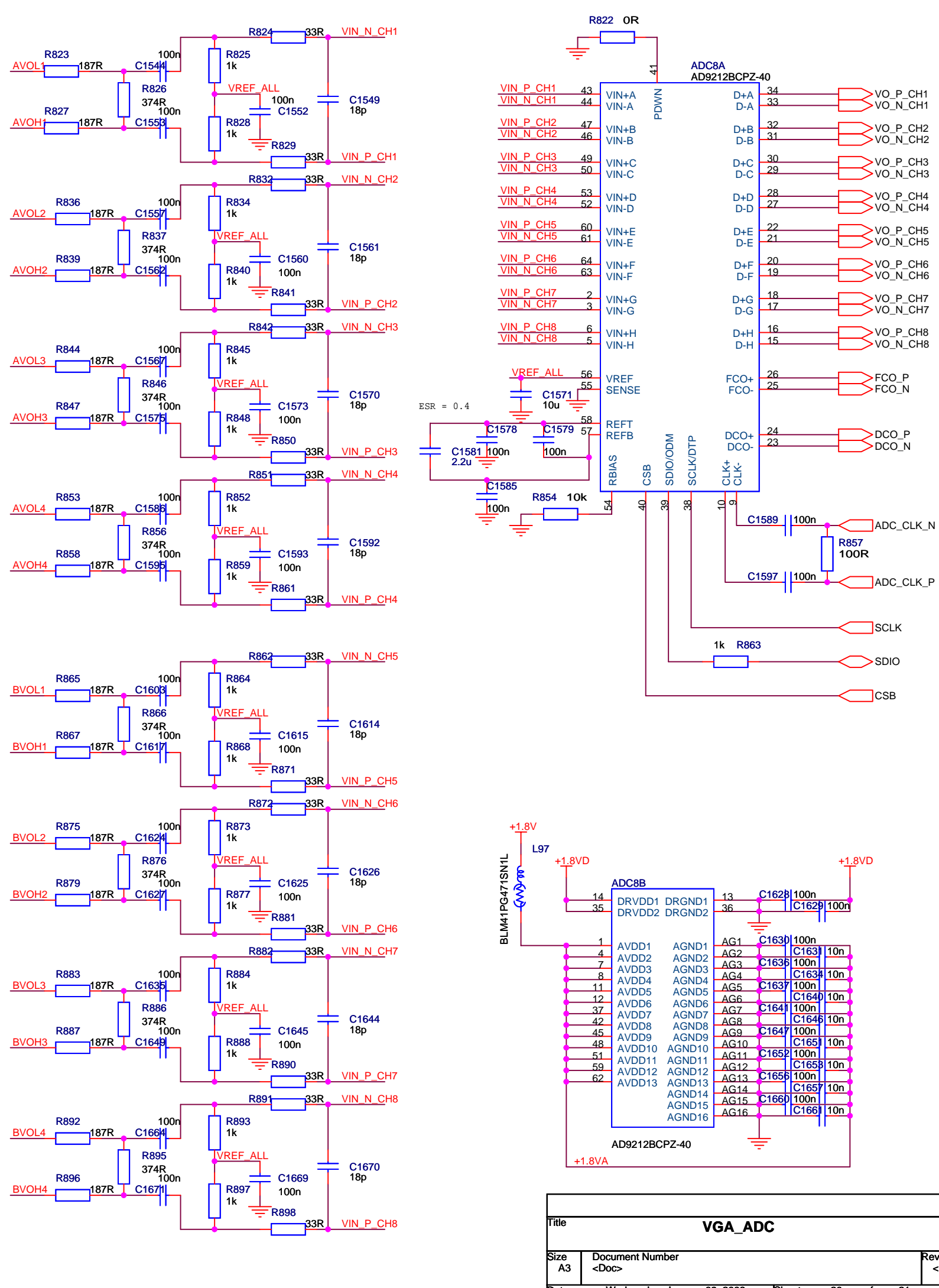
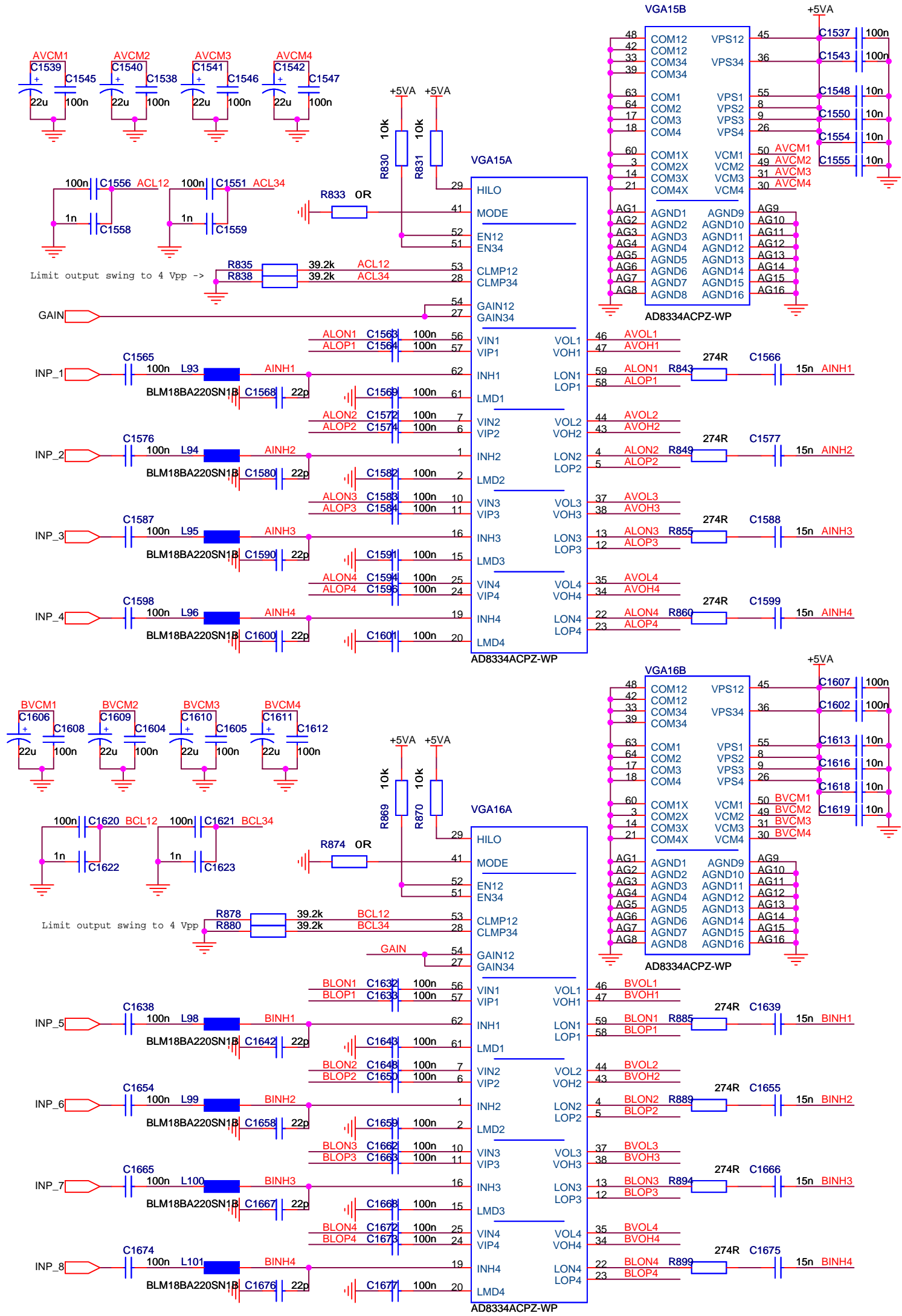
Title			VGA_ADC		
Size	Document Number				Rev
A3	<Doc>				<RevC>
Date:	Wednesday, January 09, 2008	Sheet	17	of	21

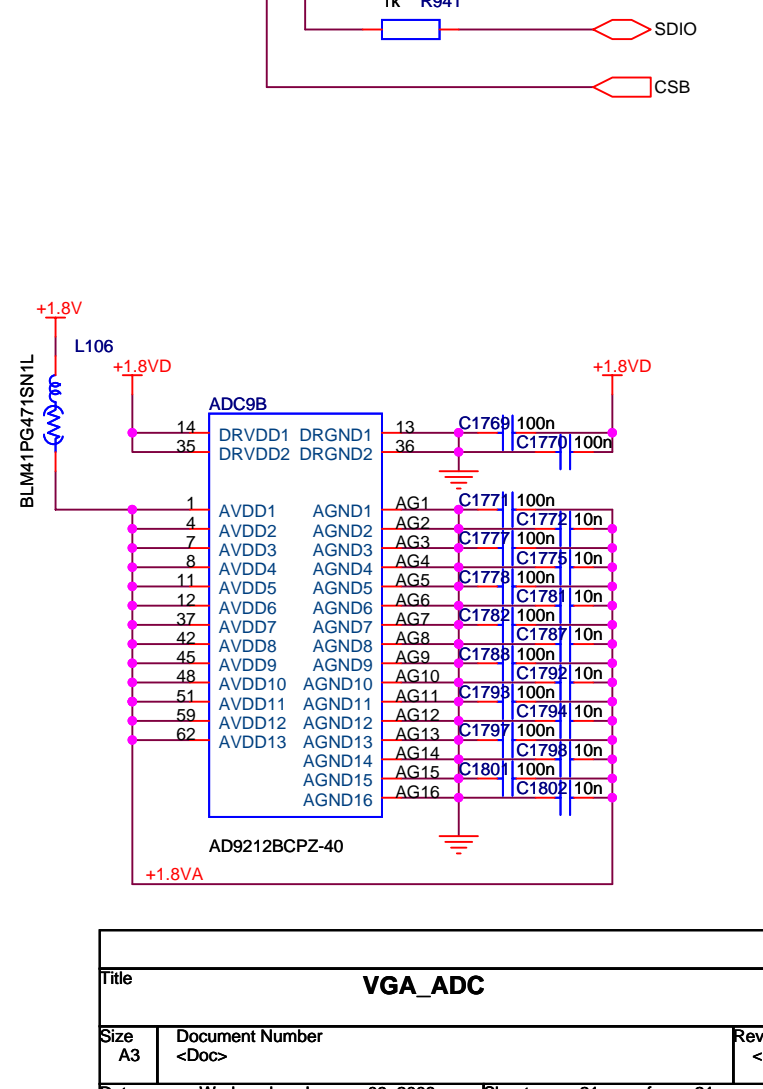
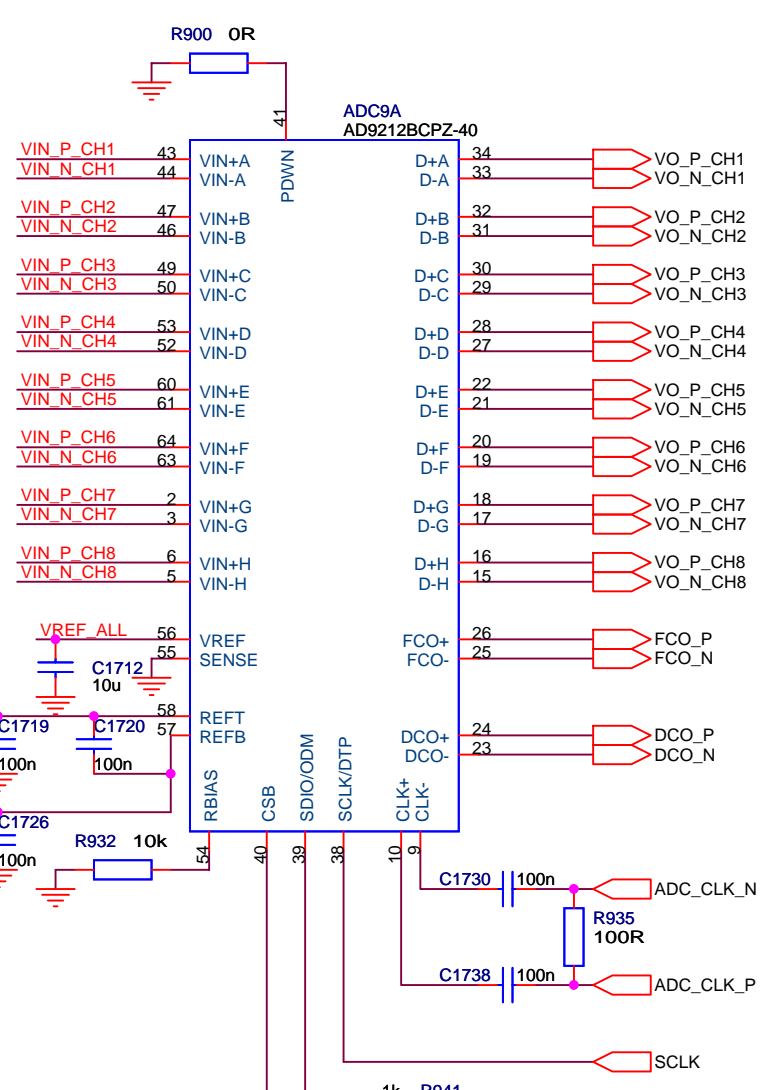
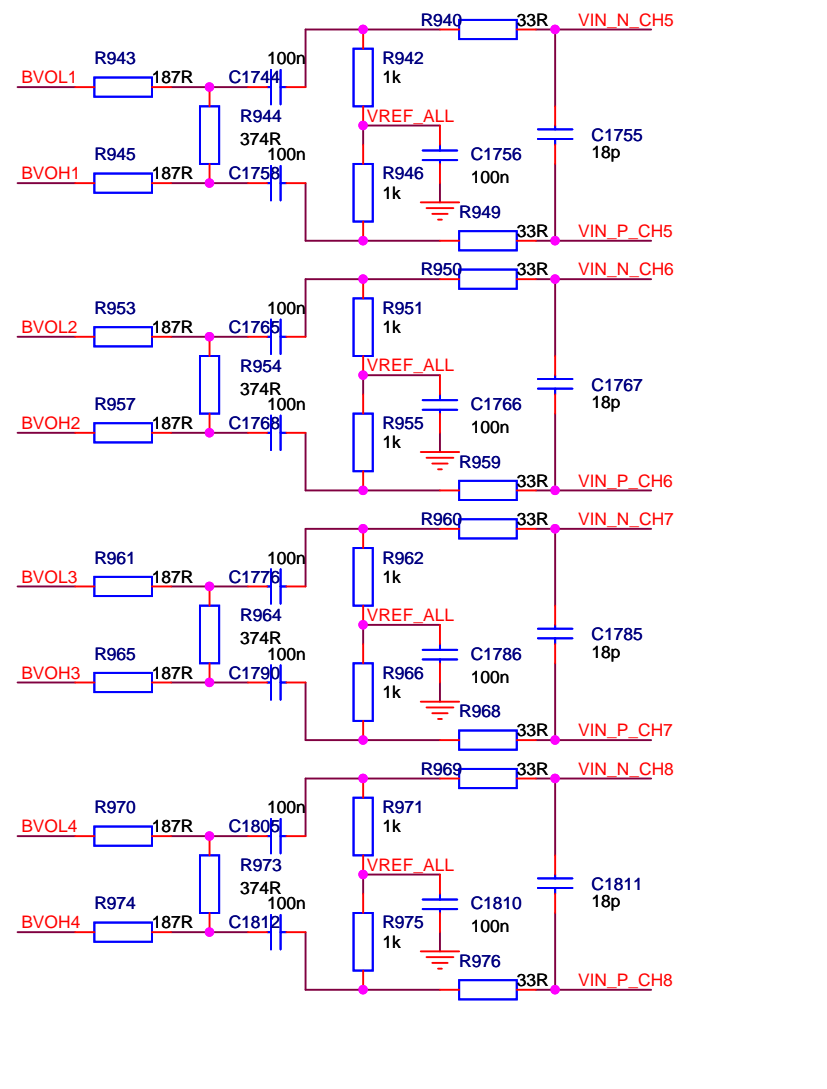
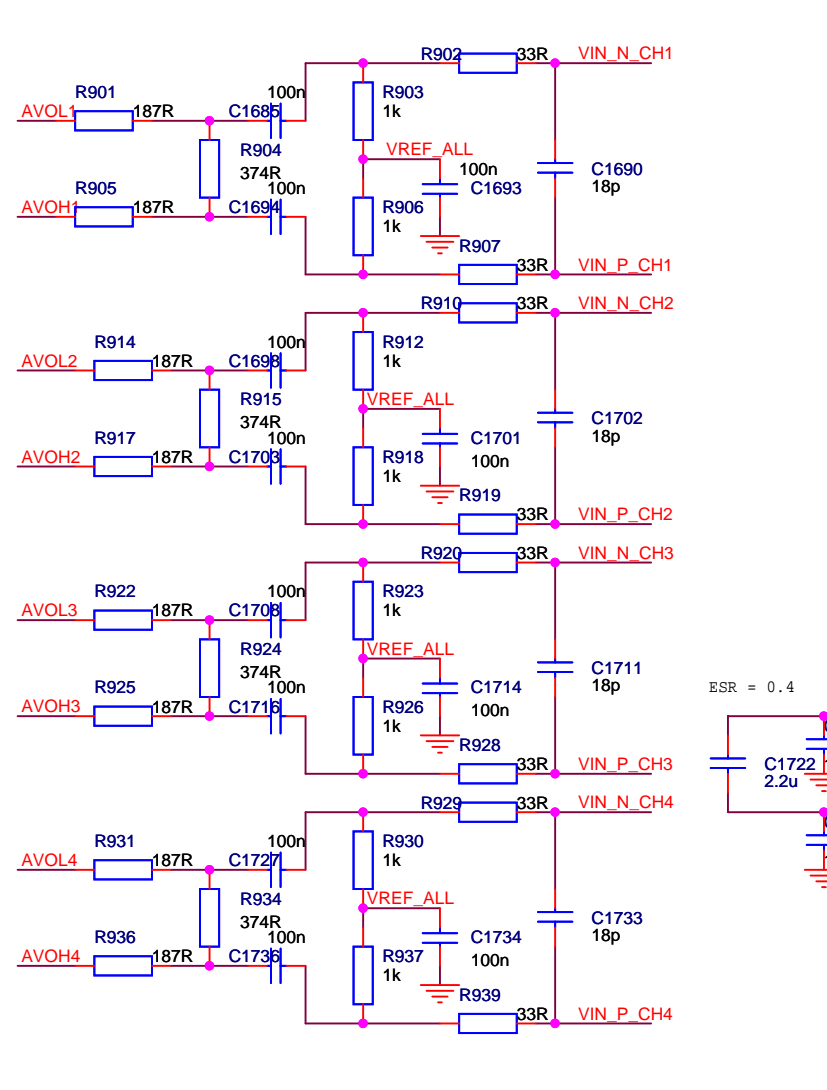
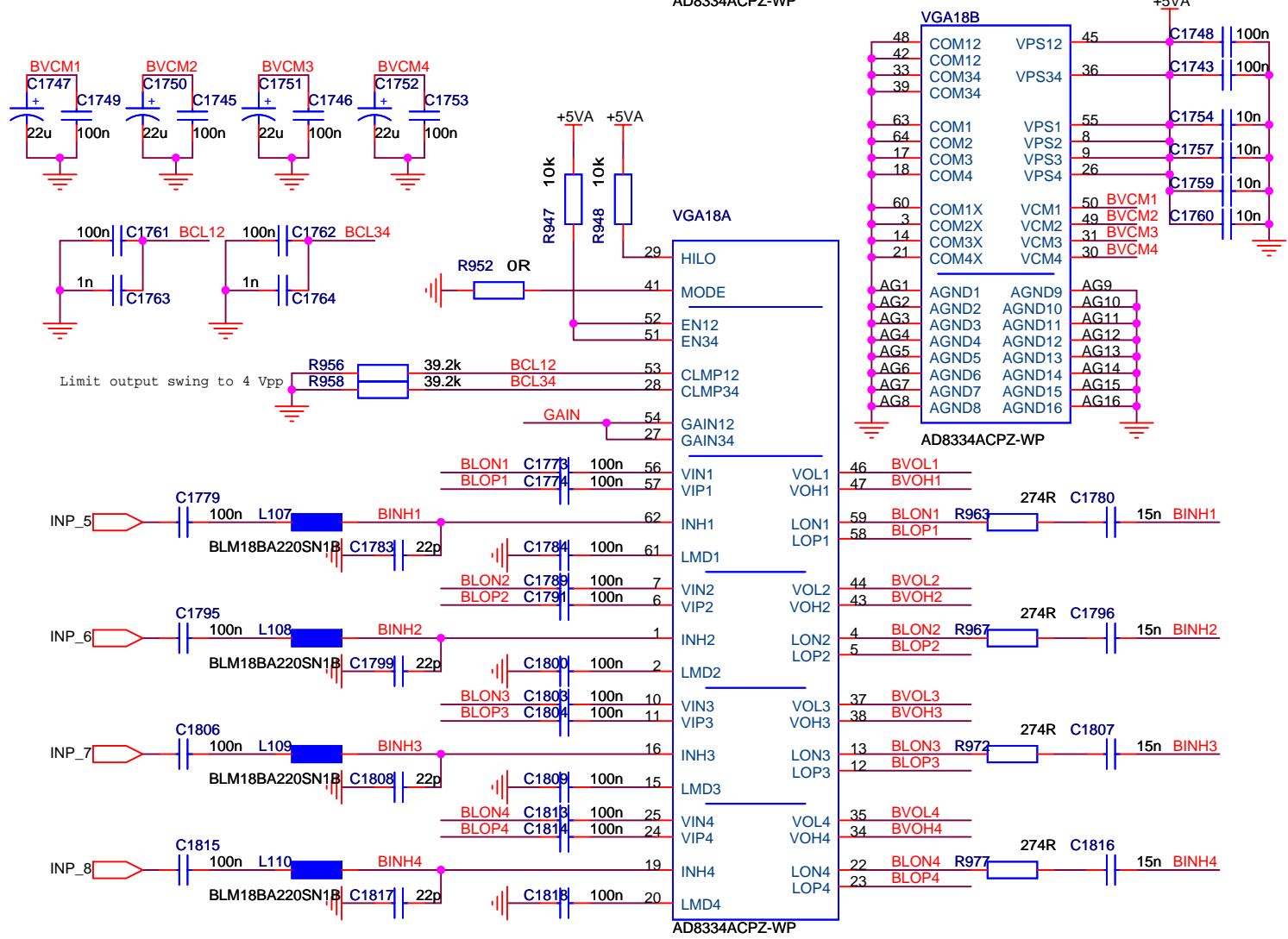
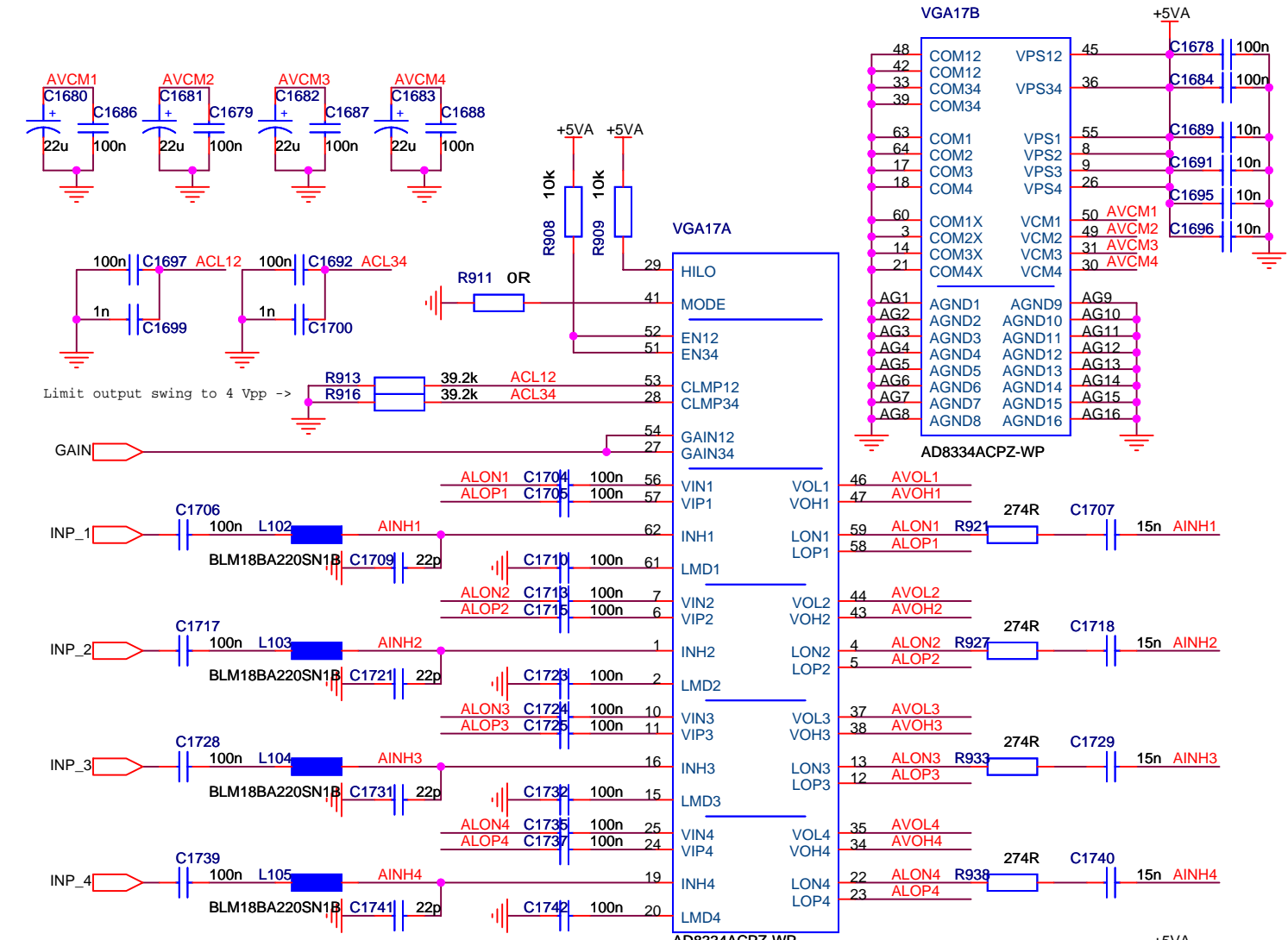


Title			VGA_ADC		
Size	Document Number		Rev		
A3	<Doc>		<RevC>		
Date:	Wednesday, January 09, 2008	Sheet	18	of	21



Title			VGA_ADC		
Size	Document Number				Rev
A3	<Doc>				<RevC>
Date:	Wednesday, January 09, 2008		Sheet	19	of 21





Title			VGA_ADC		
Size	Document Number				Rev
A3	<Doc>				<RevC>
Date:	Wednesday, January 09, 2008	Sheet	21	of	21