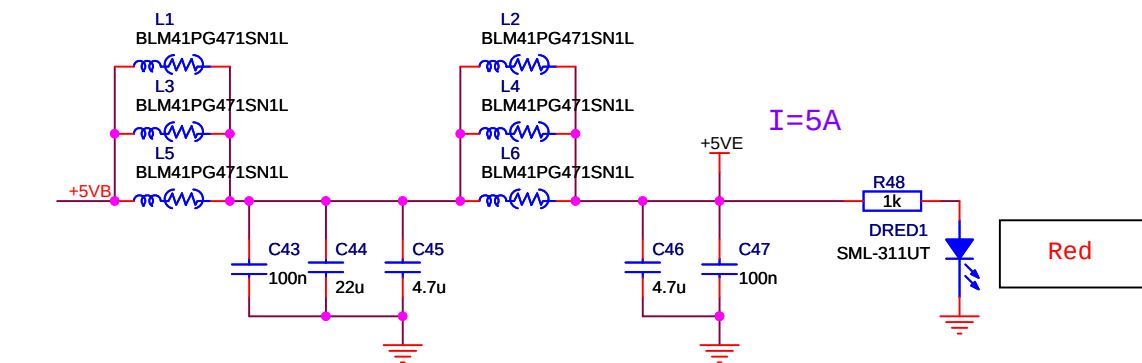
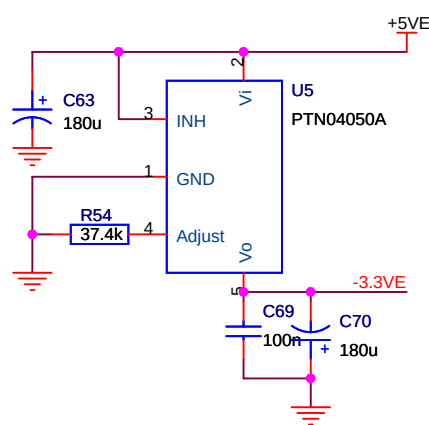
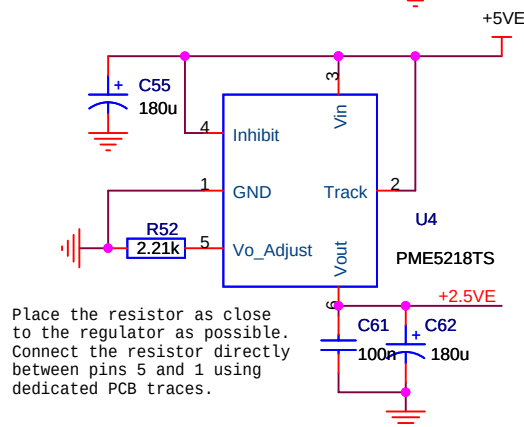
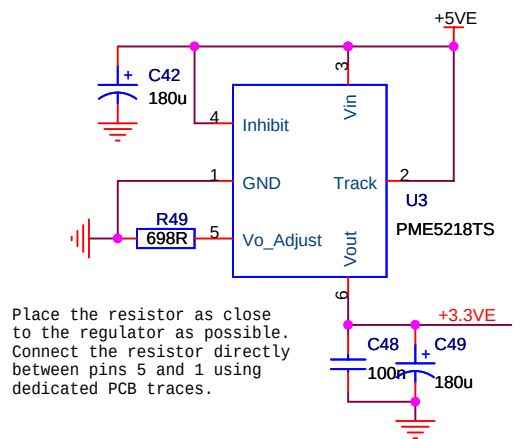
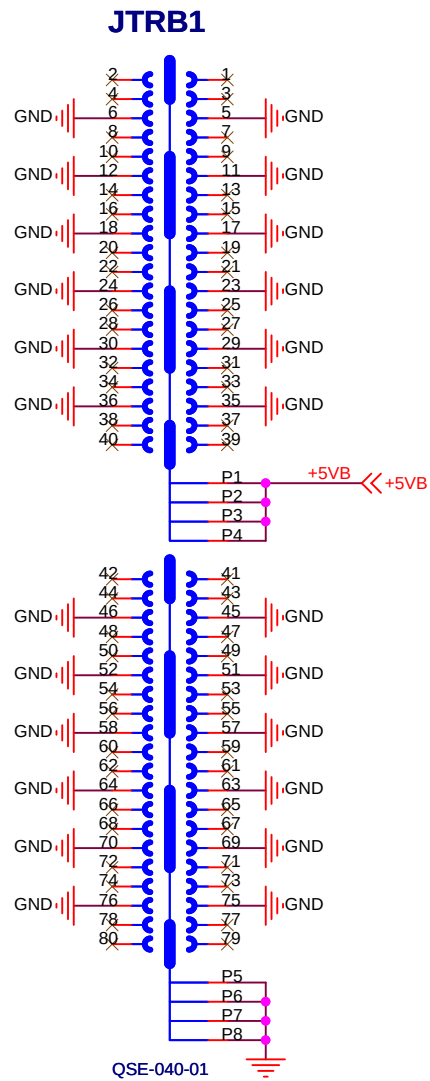
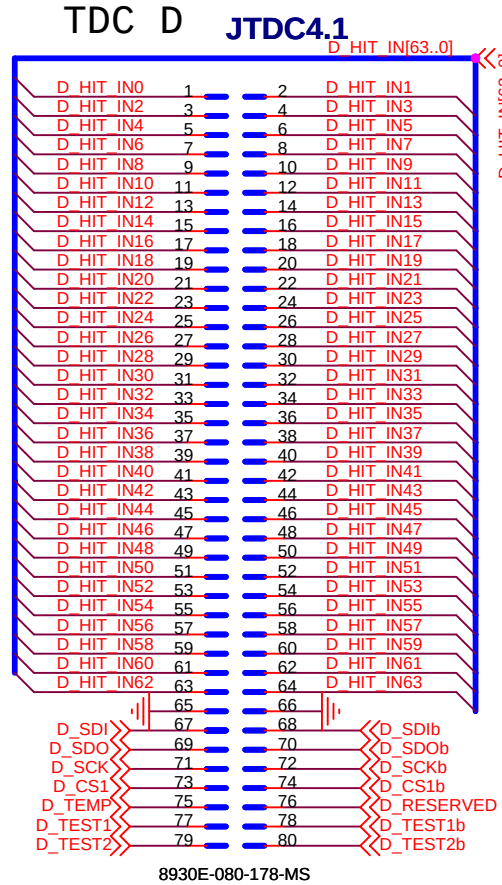
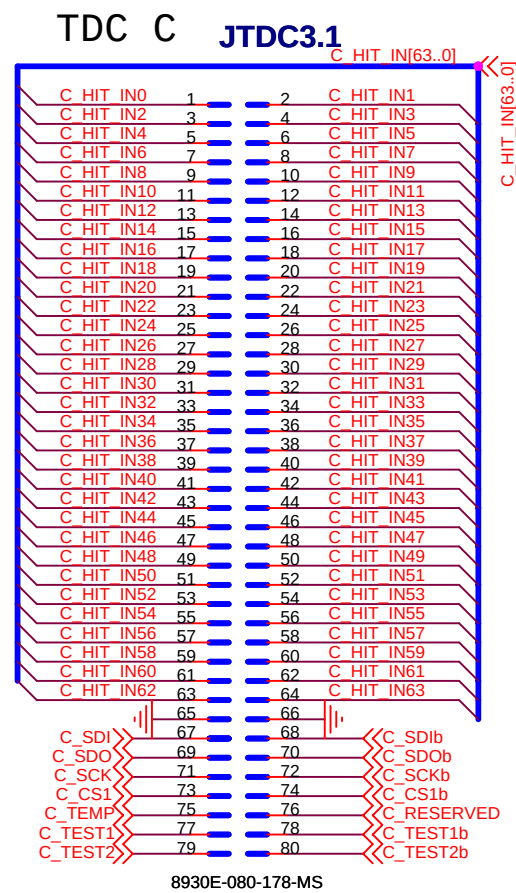
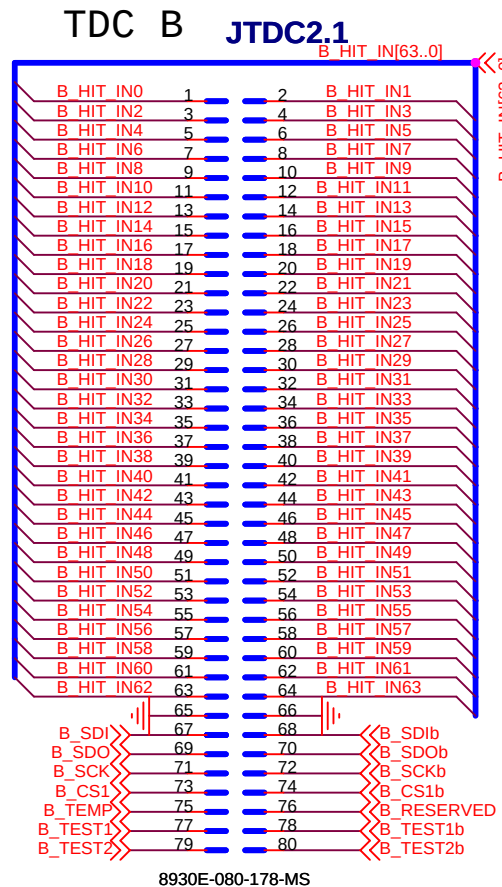
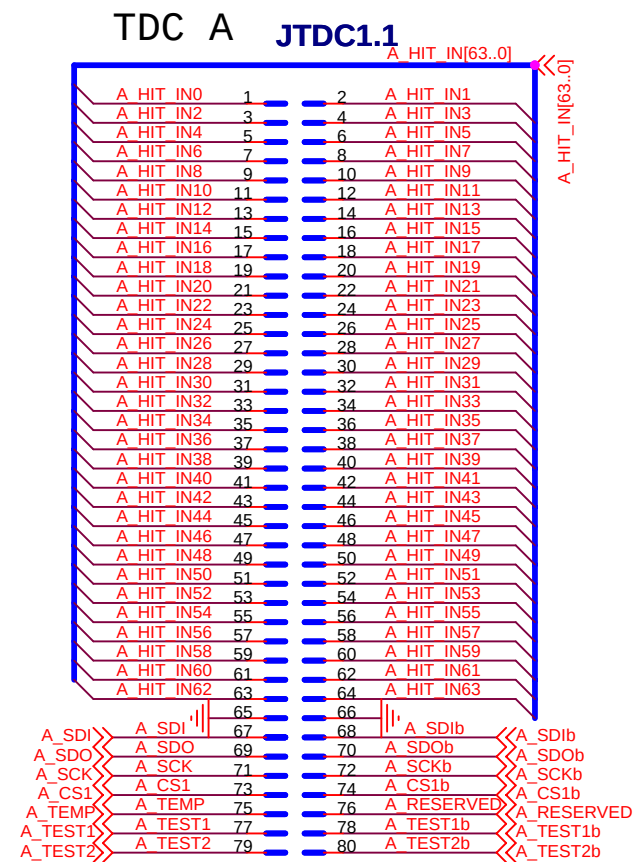
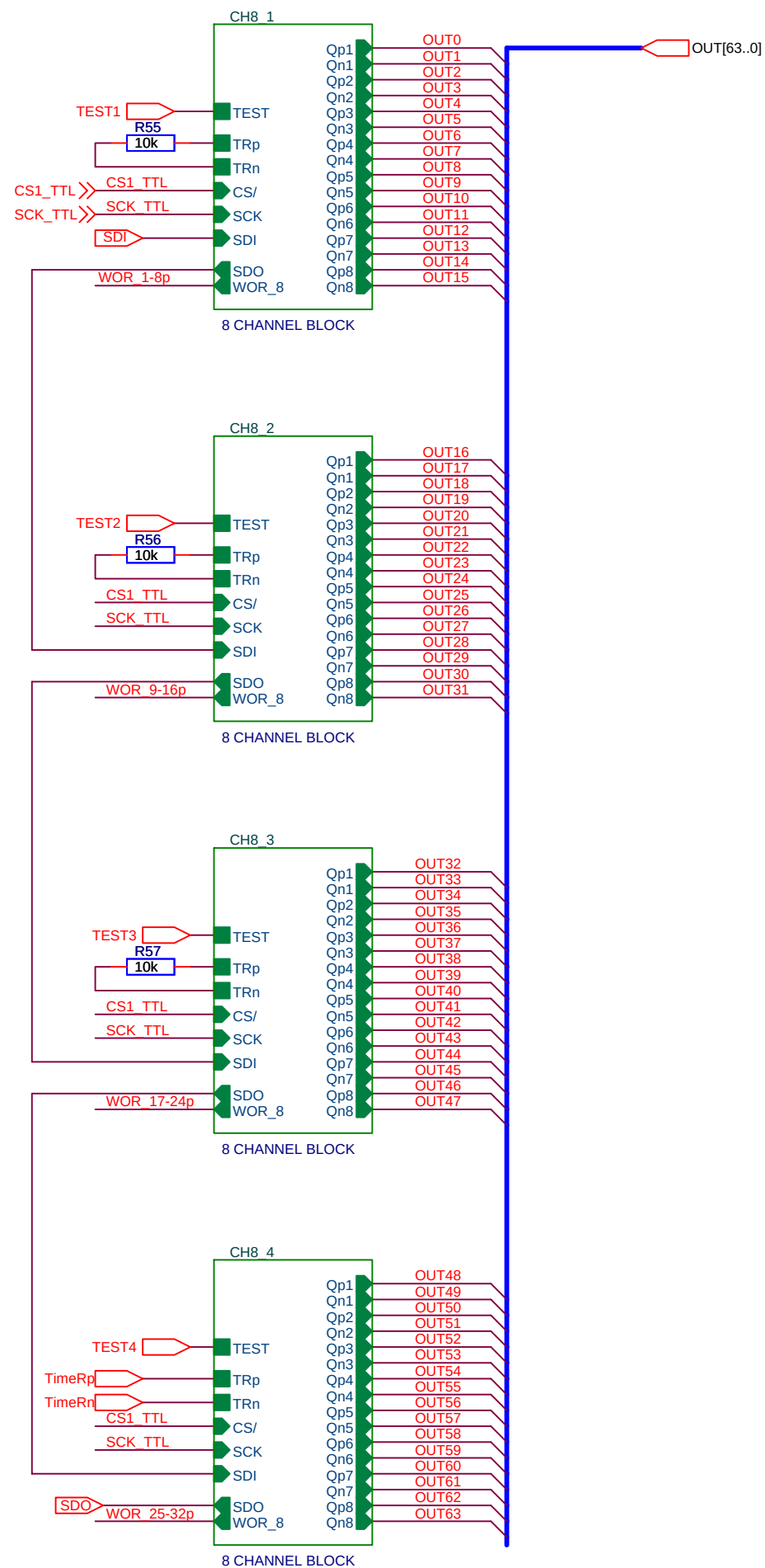
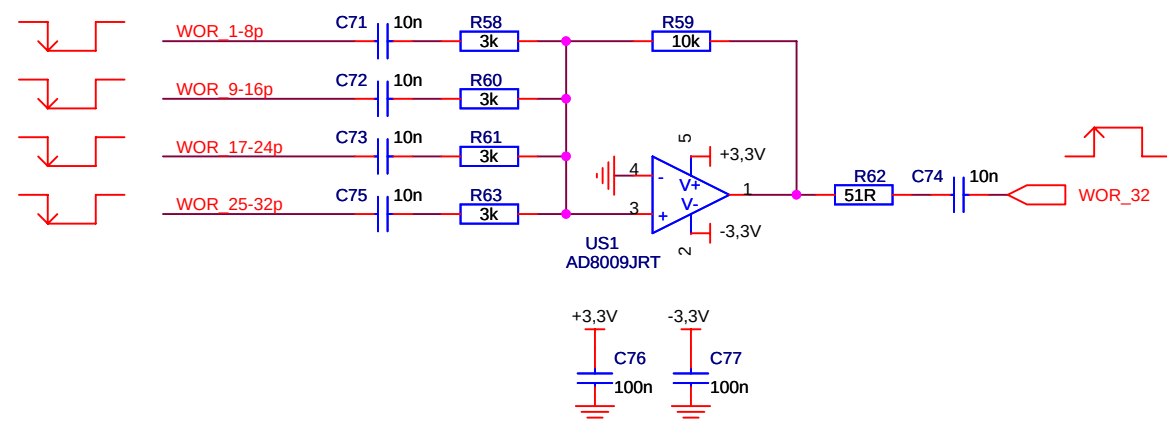


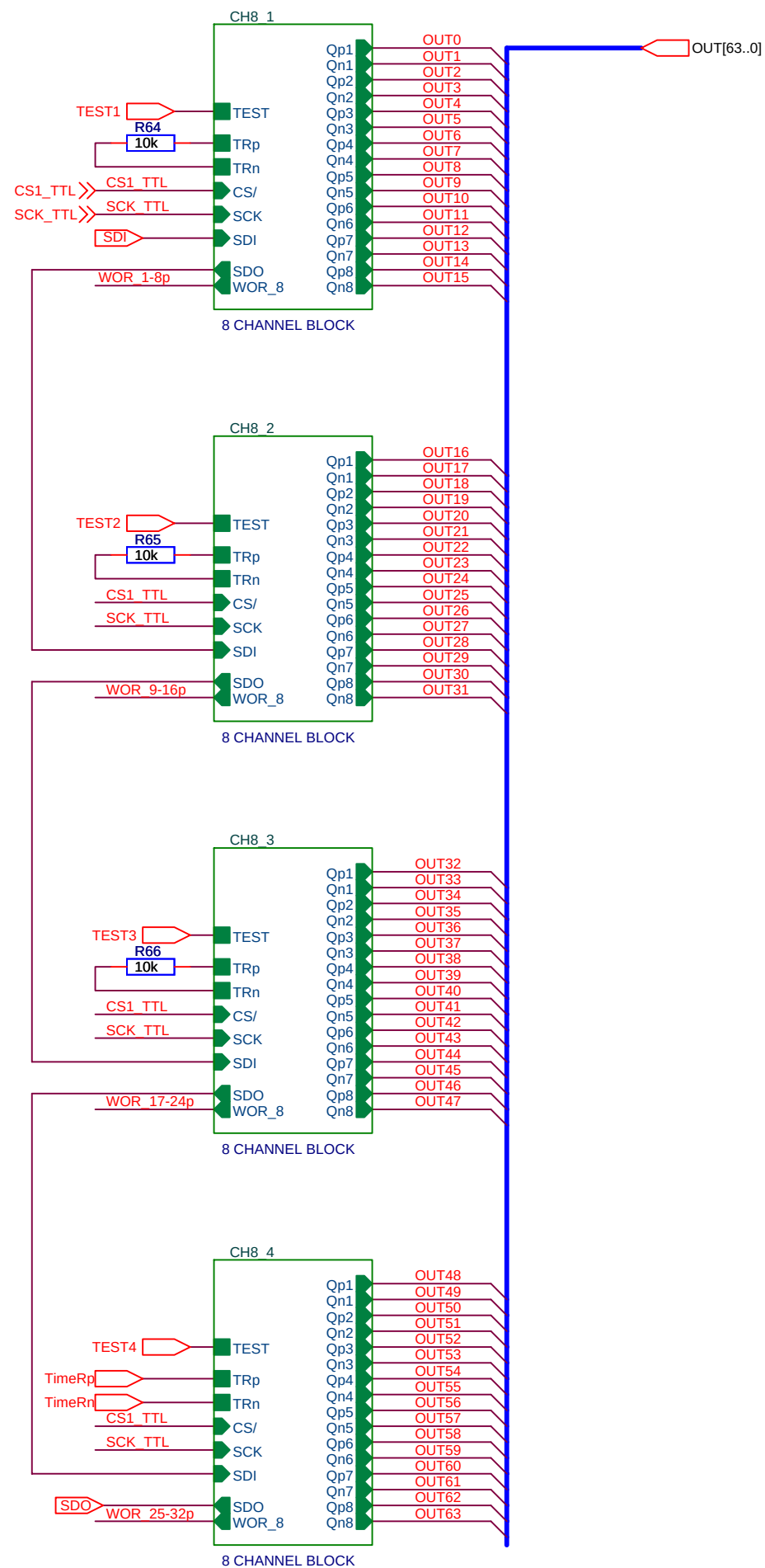




OR 32 SUMMING SCHEMATIC

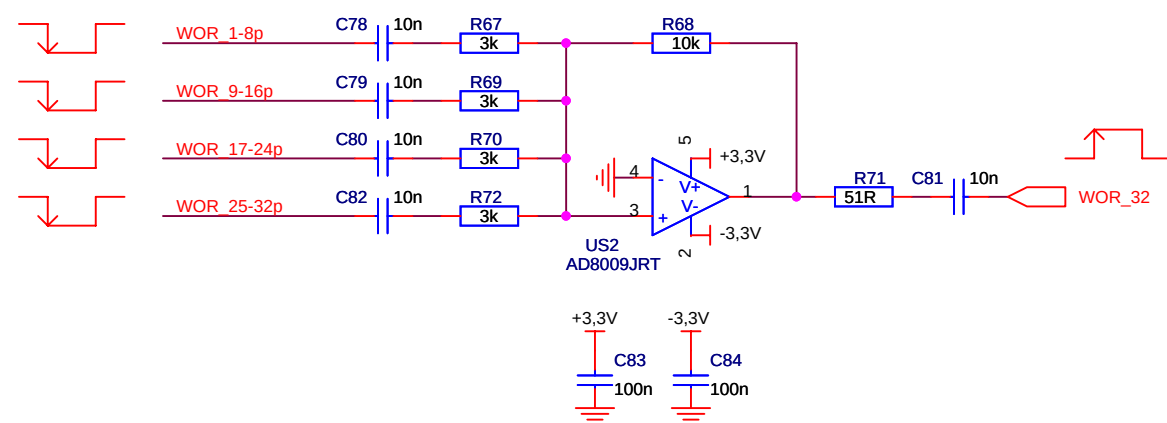
1. Nets WOR_... should be equal length and $Z_0=60\ \Omega$.
2. Summing point (n.4 of AD8009) must be minimum length, therefore all sum resistors must be placed as close as possible to summing point.

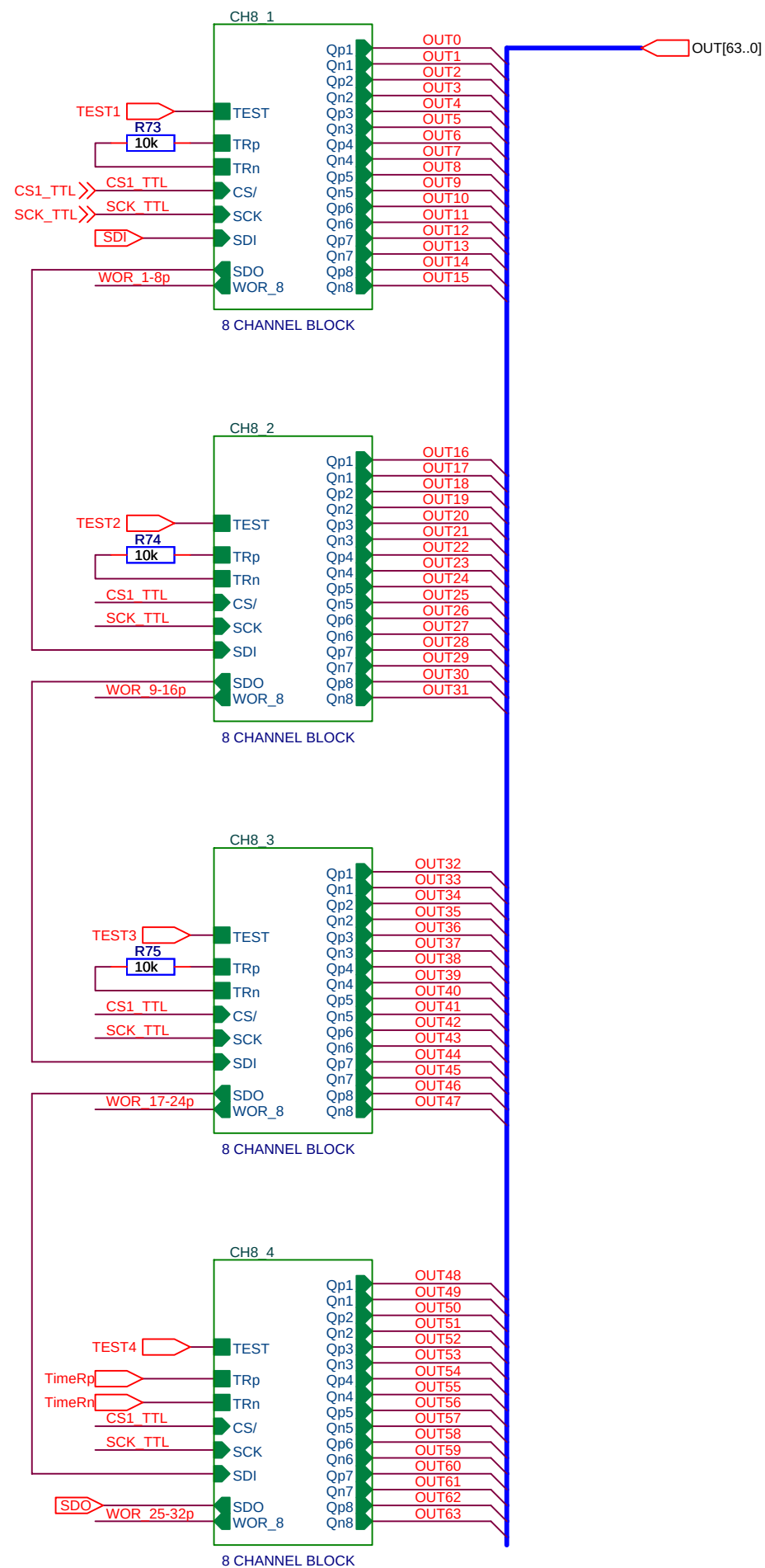




OR 32 SUMMING SCHEMATIC

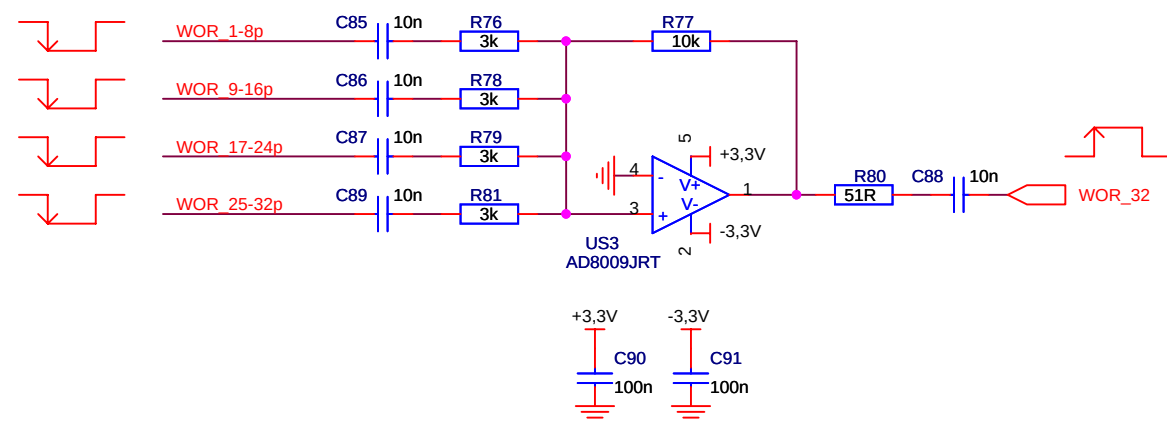
1. Nets WOR_... should be equal length and $Z_0=60\ \Omega$.
2. Summing point (n.4 of AD8009) must be minimum length, therefore all sum resistors must be placed as close as possible to summing point.

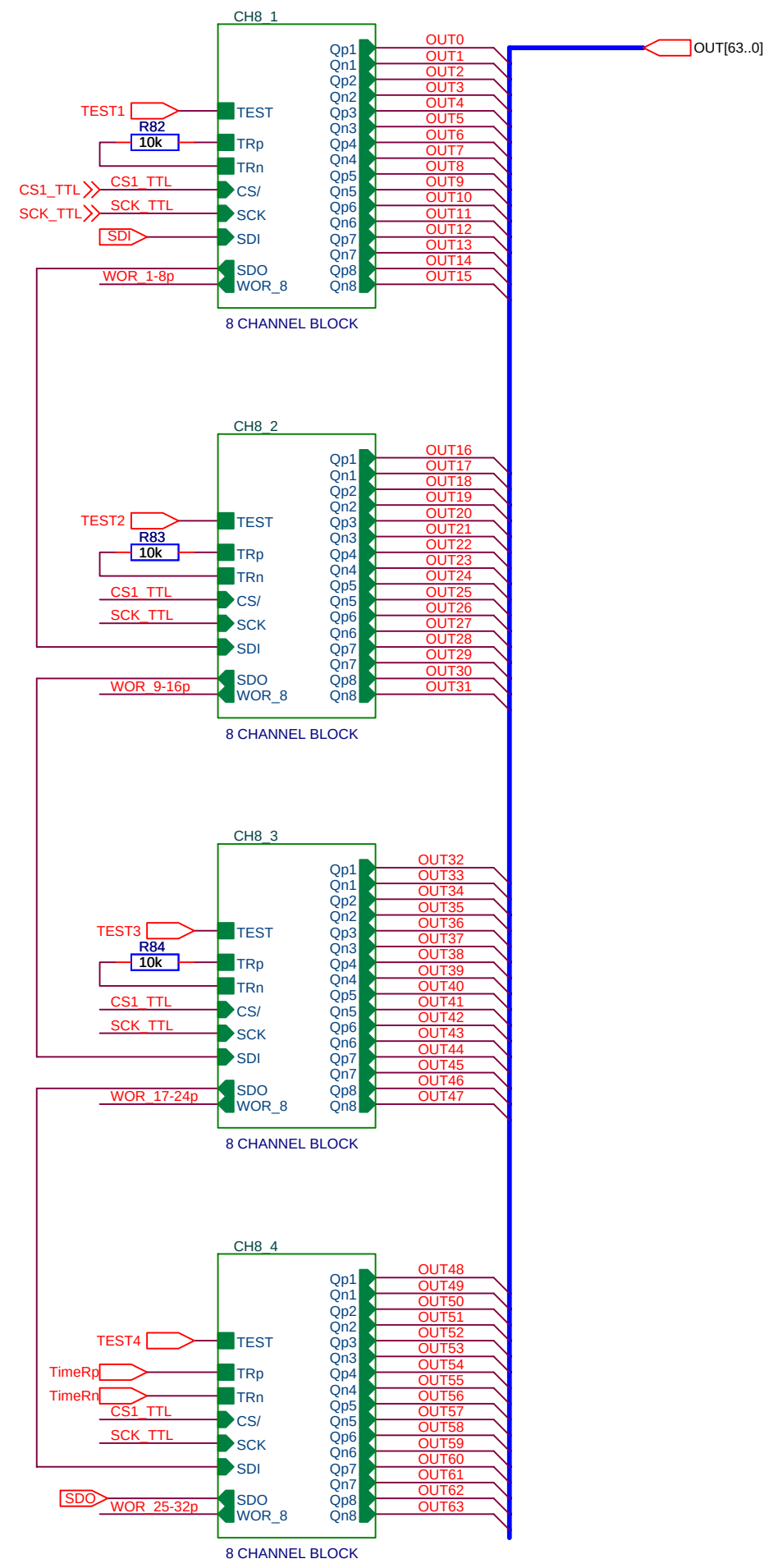




OR 32 SUMMING SCHEMATIC

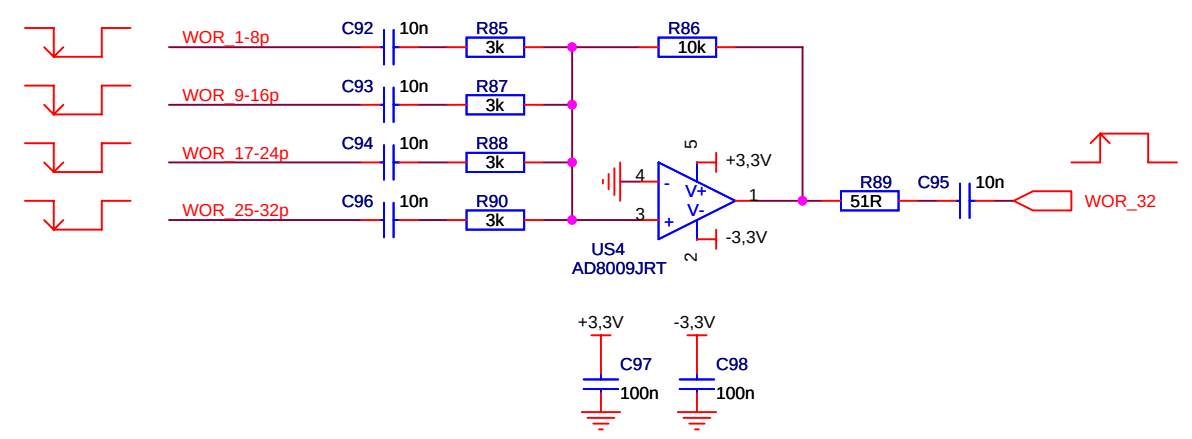
1. Nets WOR_... should be equal length and $Z_0=60\ \Omega$.
2. Summing point (n.4 of AD8009) must be minimum length, therefore all sum resistors must be placed as close as possible to summing point.

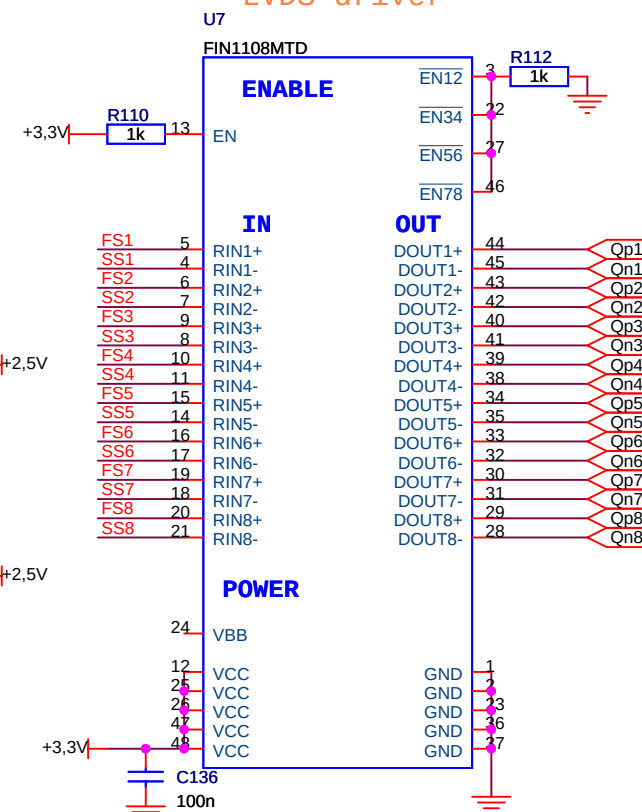
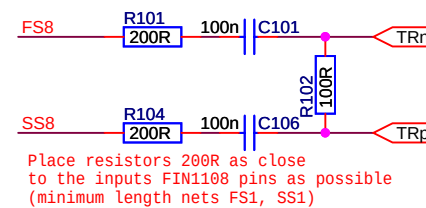
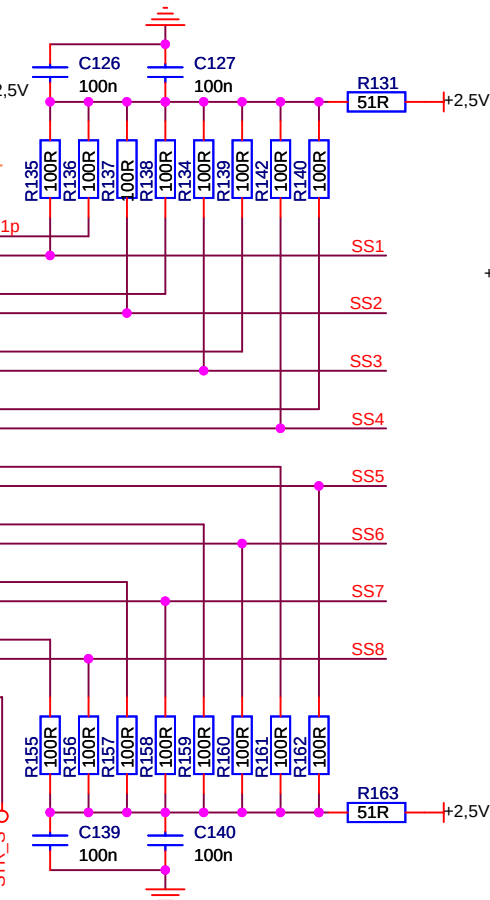
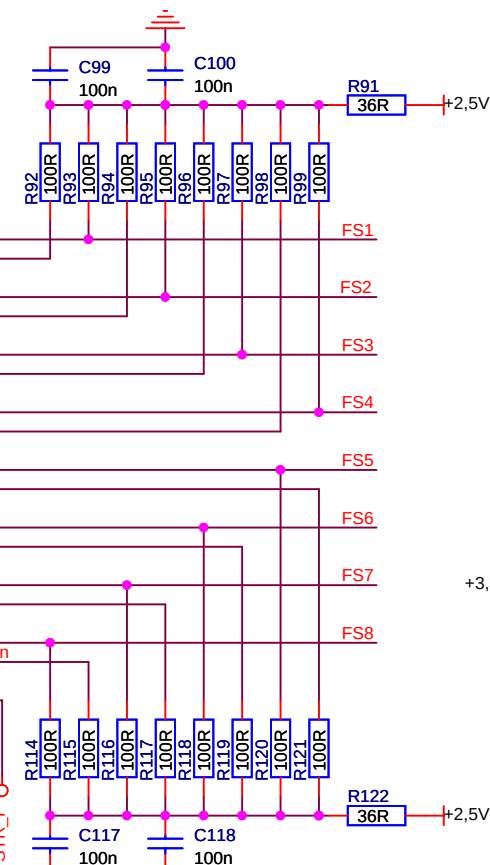
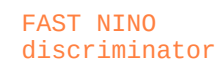
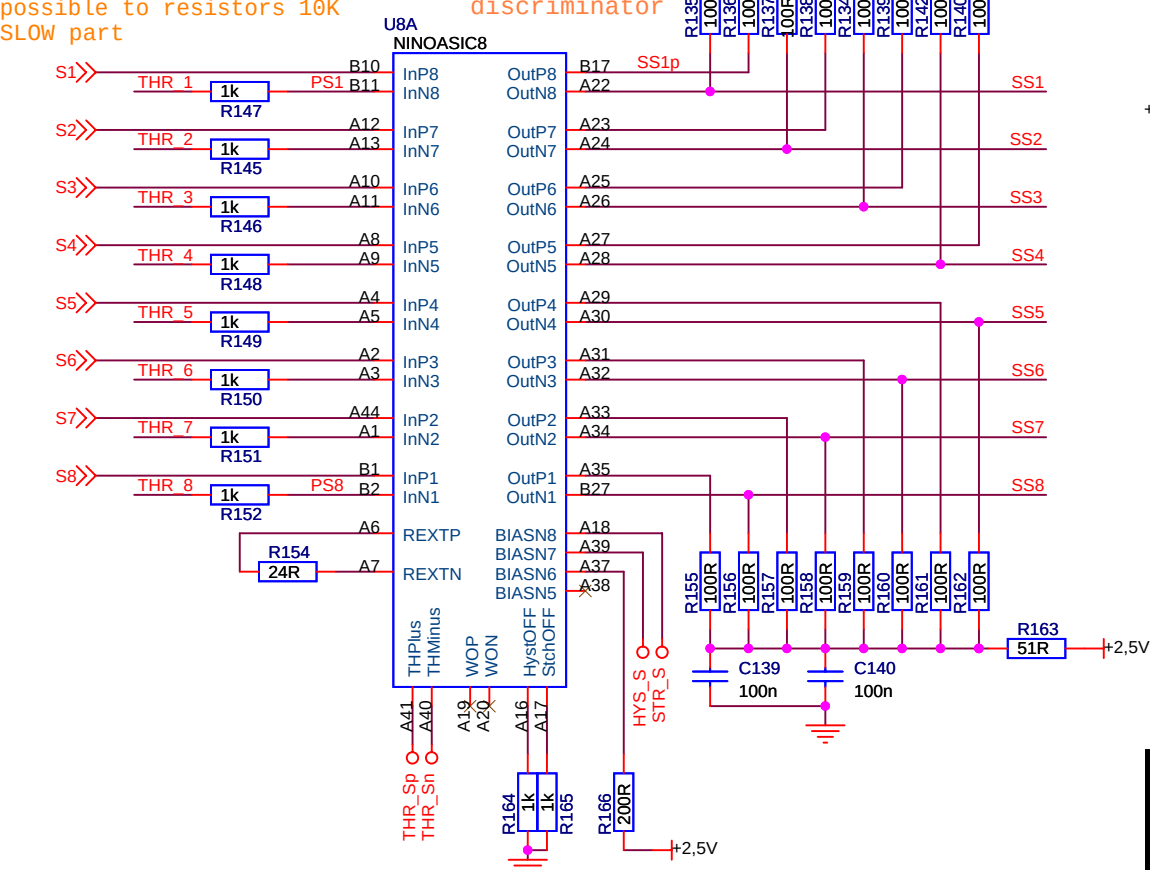
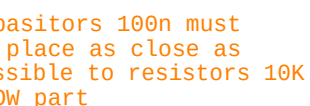
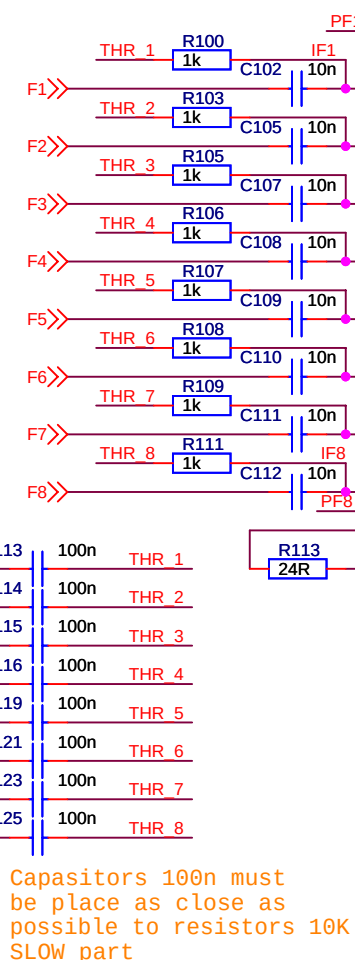
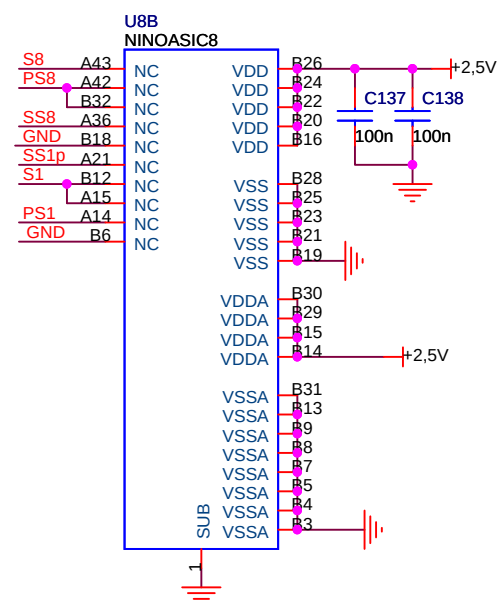
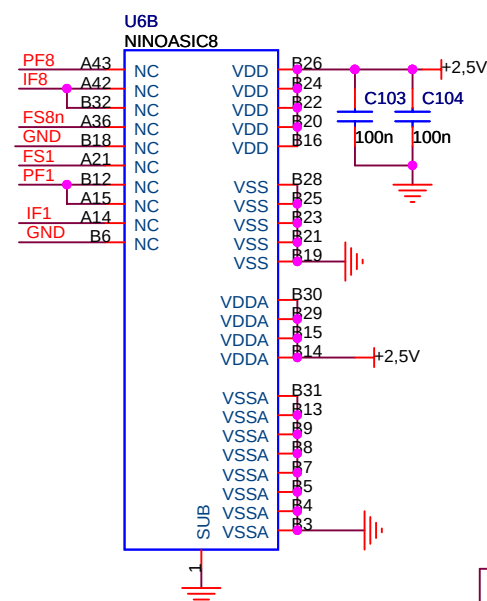
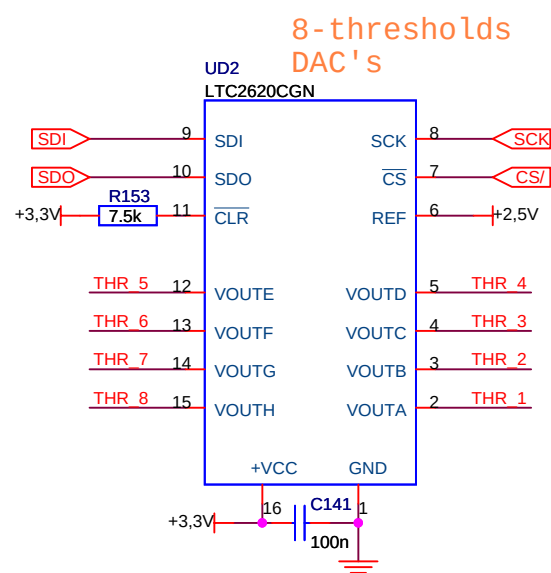
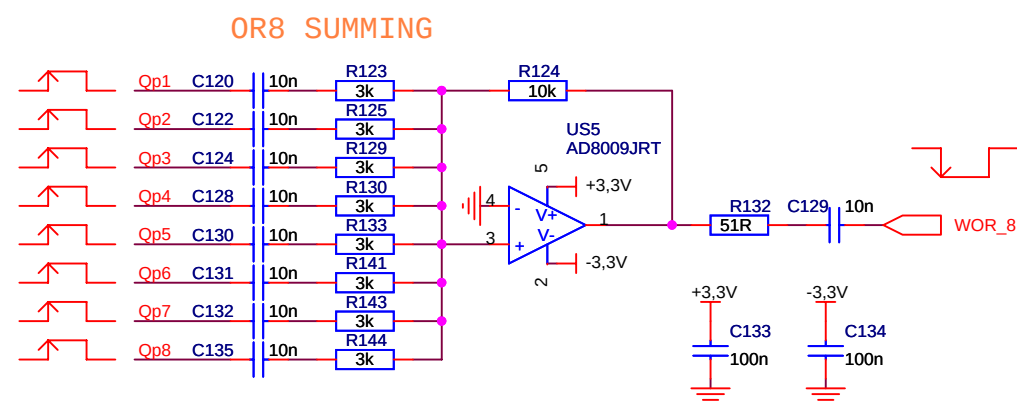


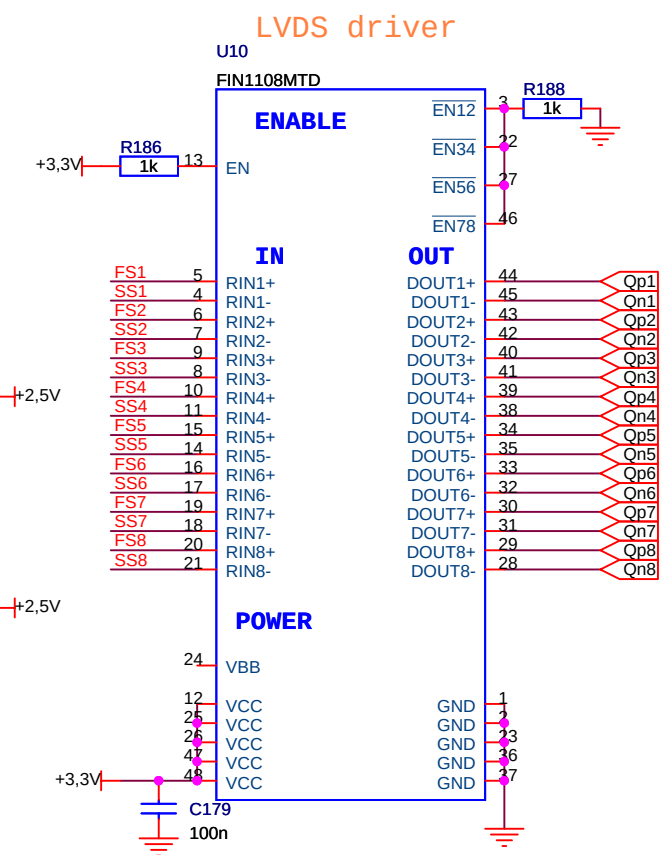
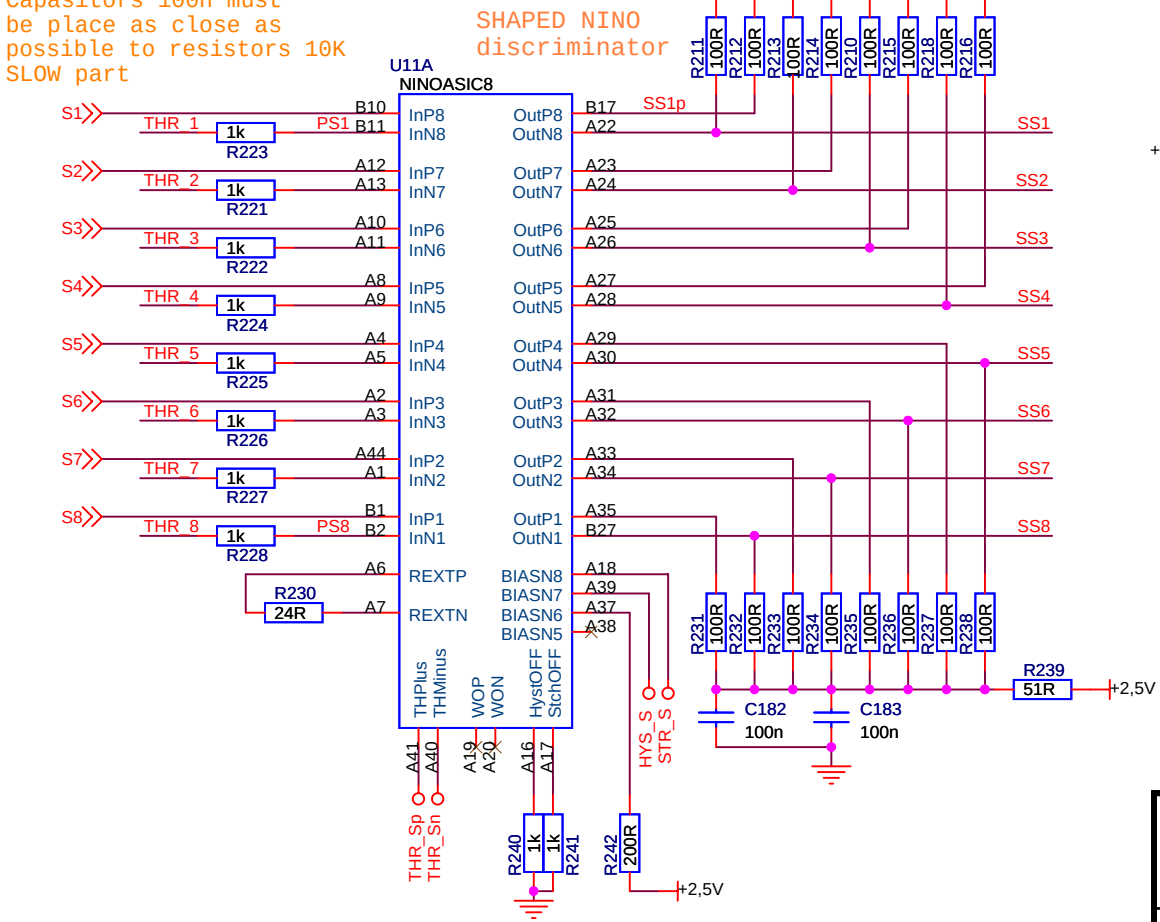
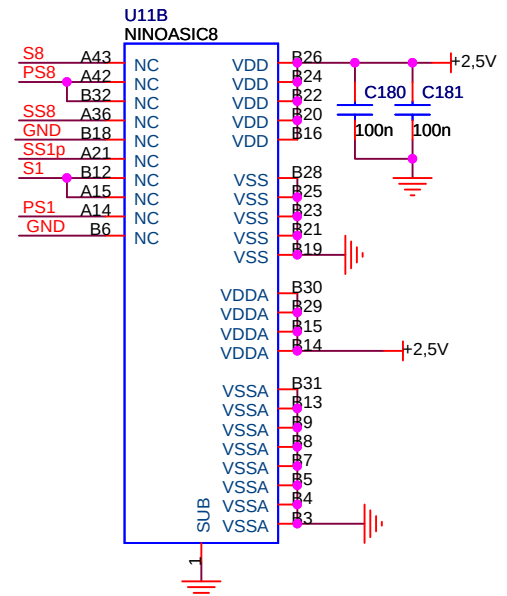
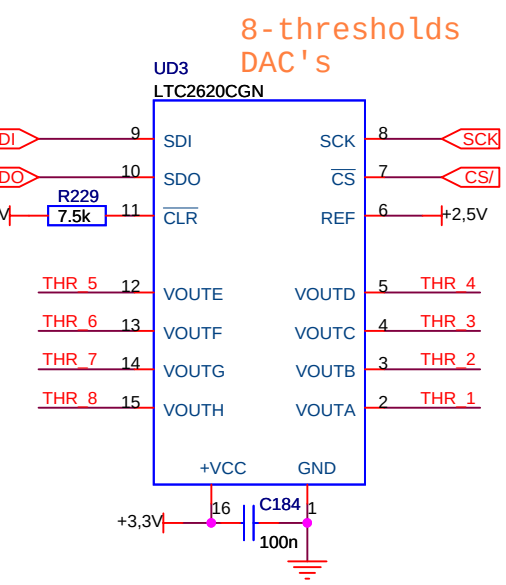


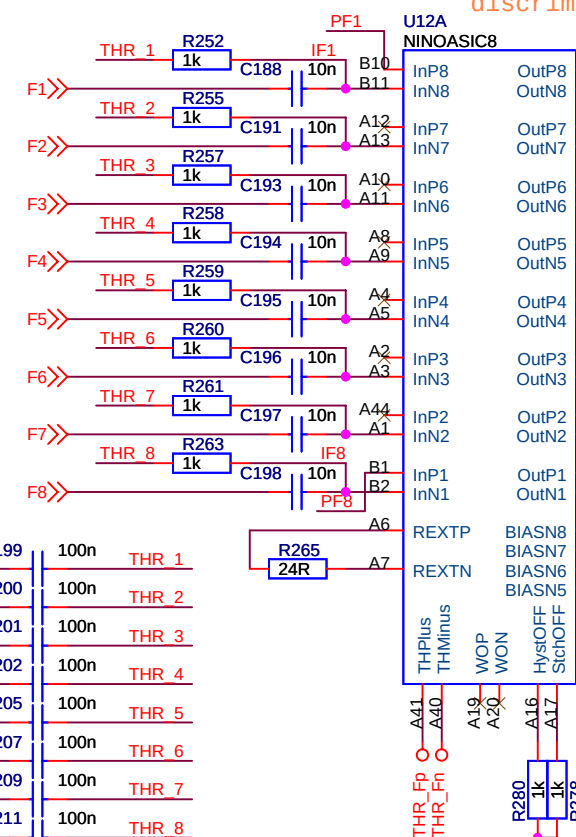
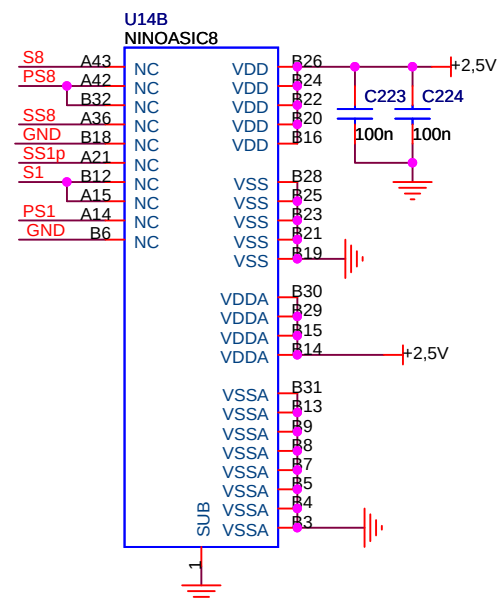
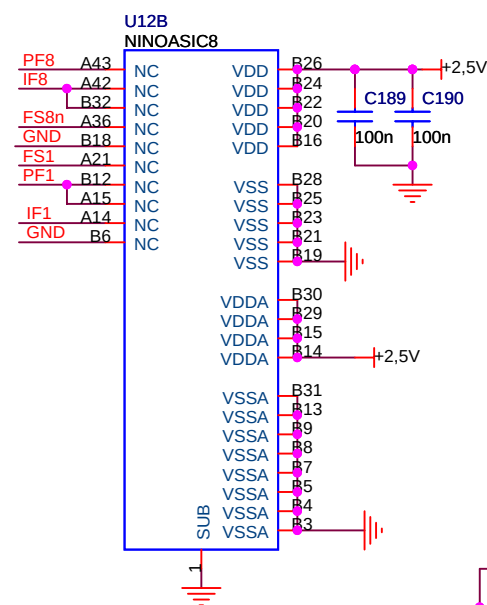
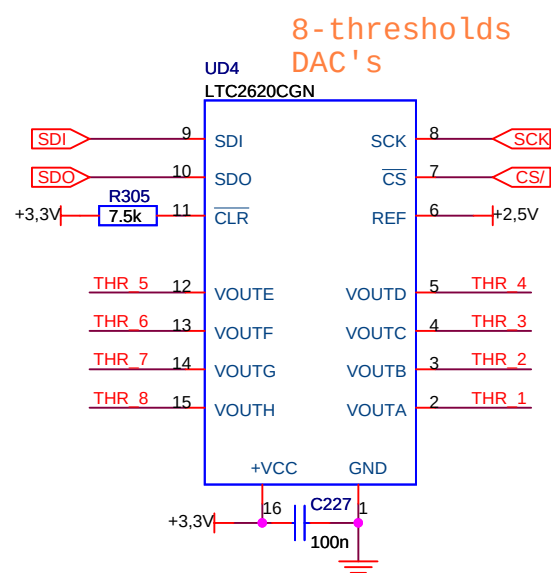
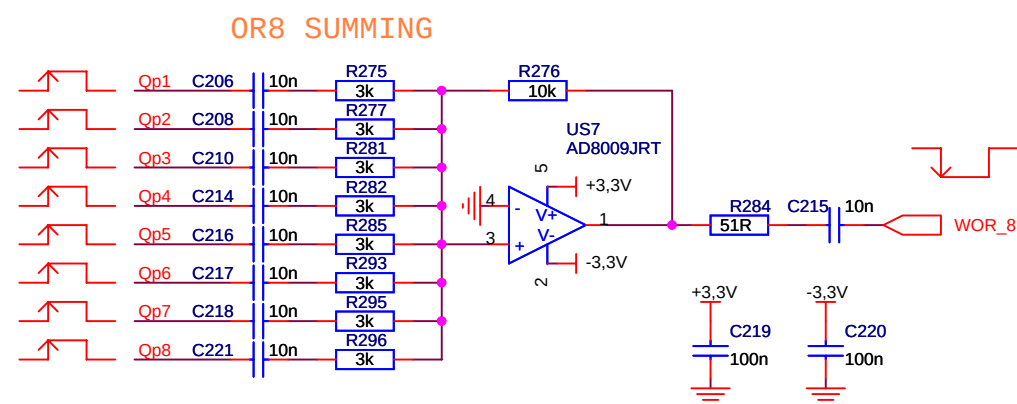
OR 32 SUMMING SCHEMATIC

1. Nets WOR_... should be equal length and $Z_0=60\ \Omega$.
2. Summing point (n.4 of AD8009) must be minimum length, therefore all sum resistors must be placed as close as possible to summing point.

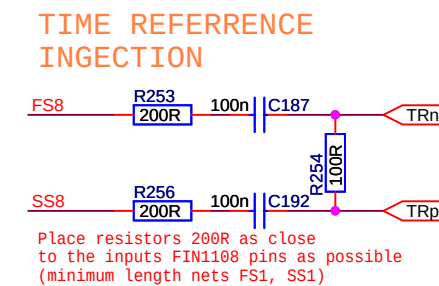
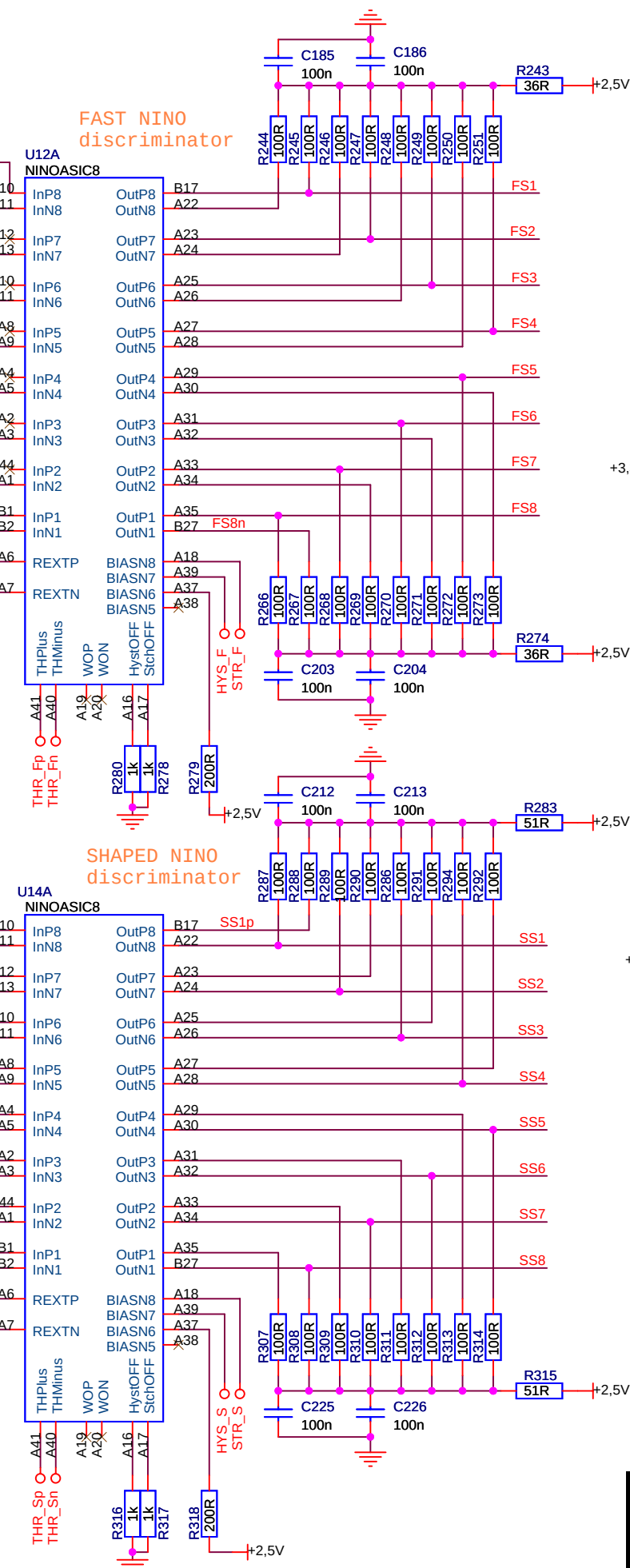




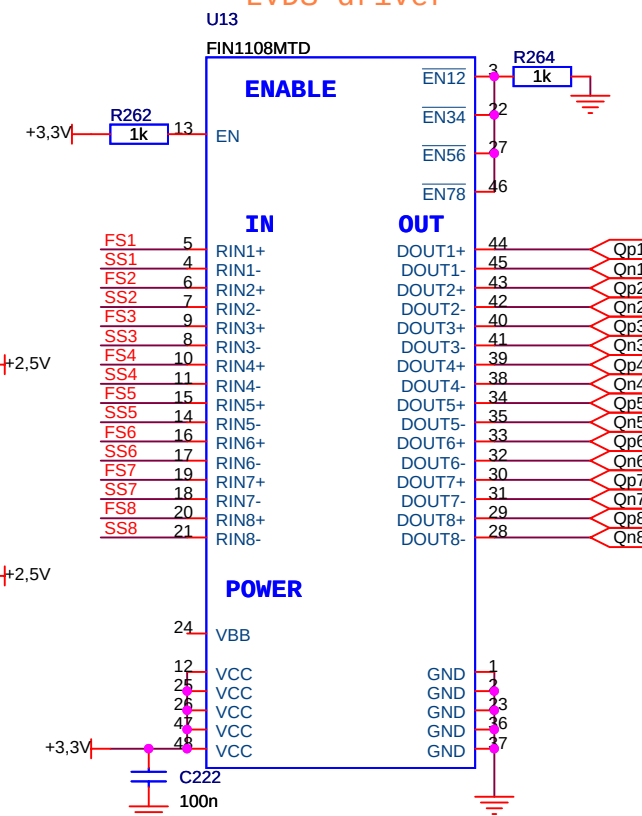


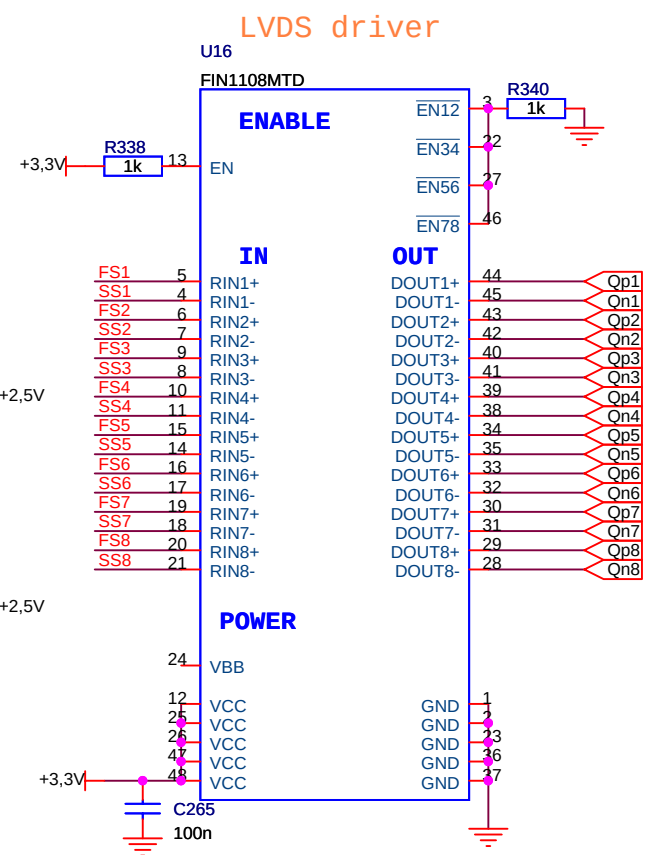
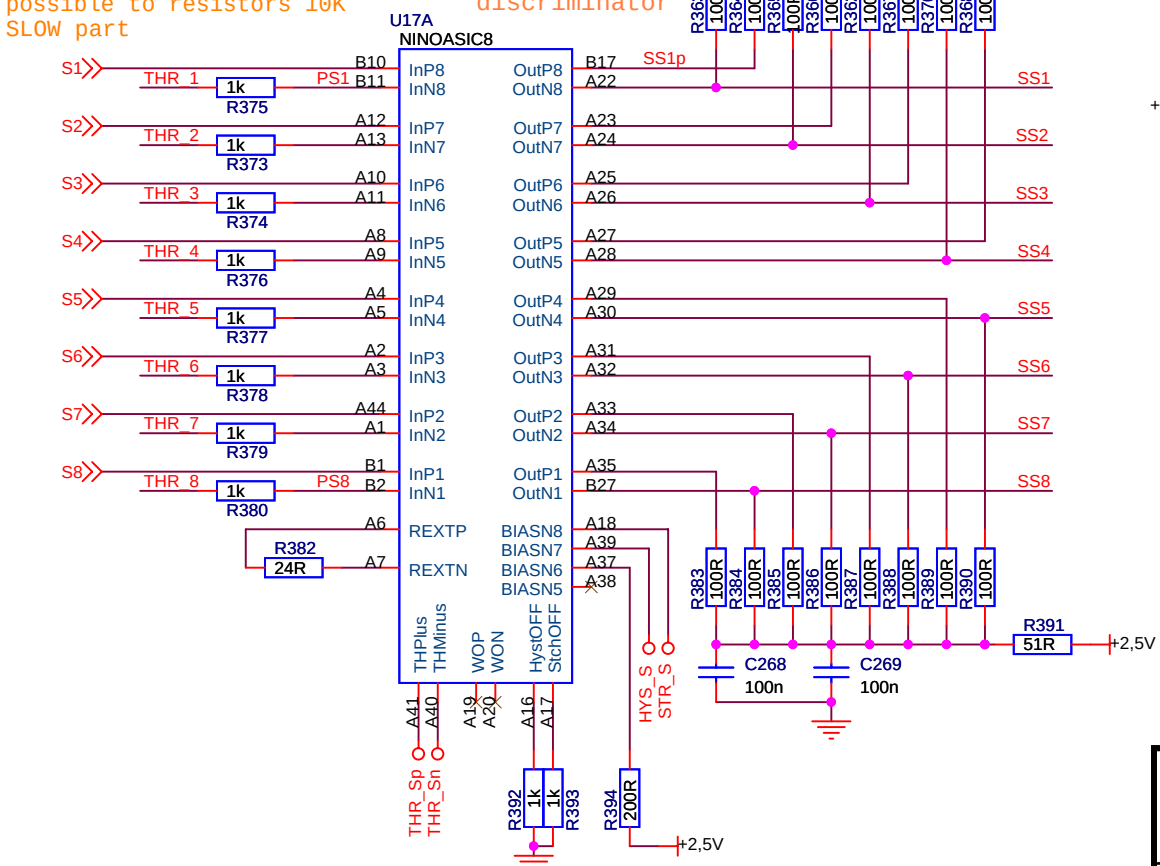
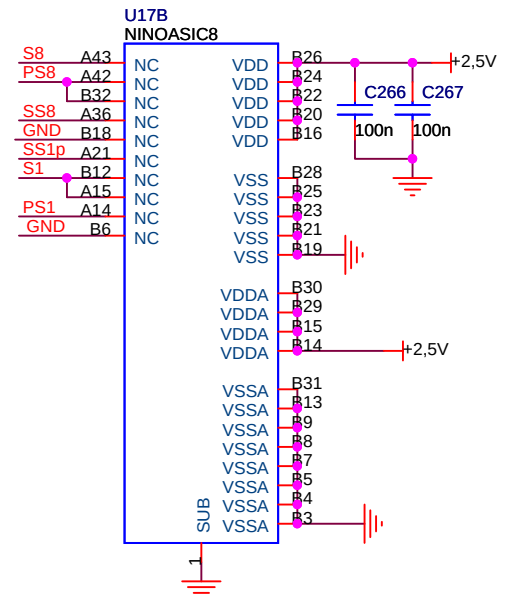
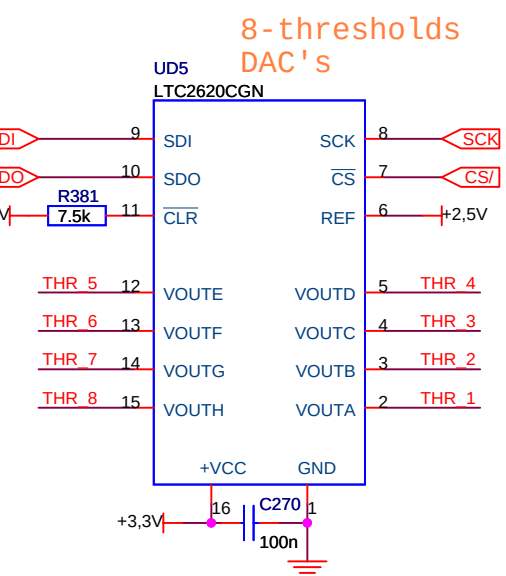


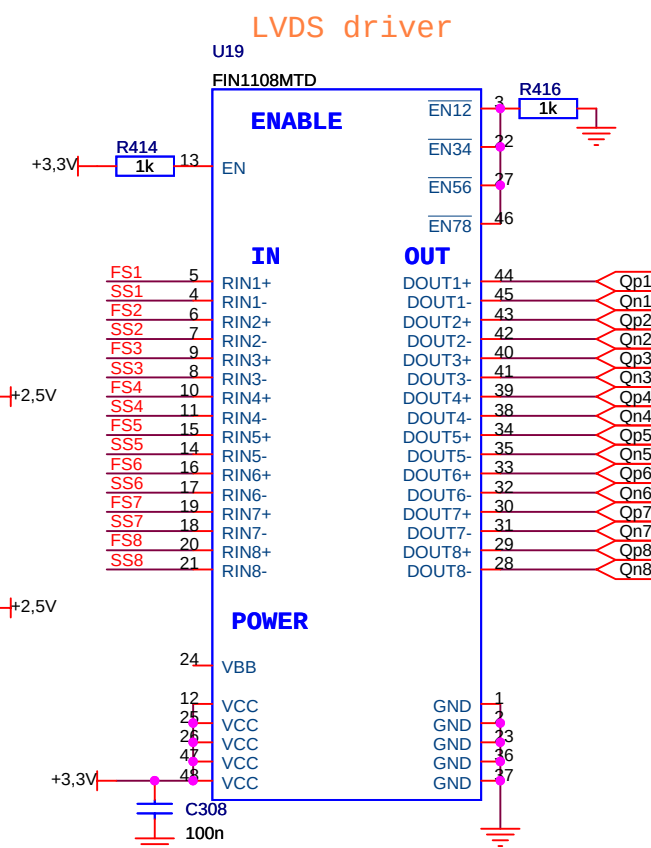
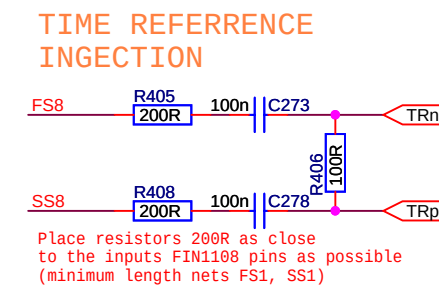
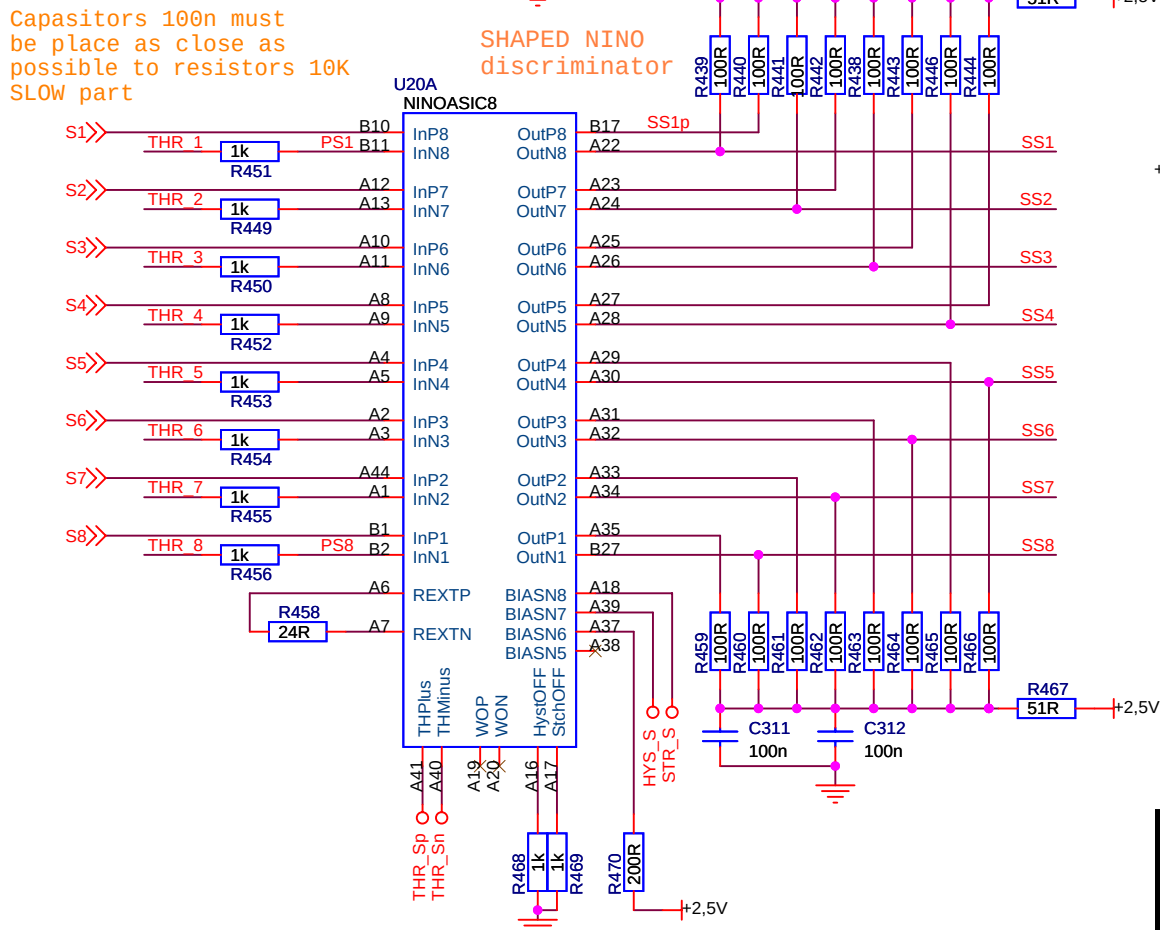
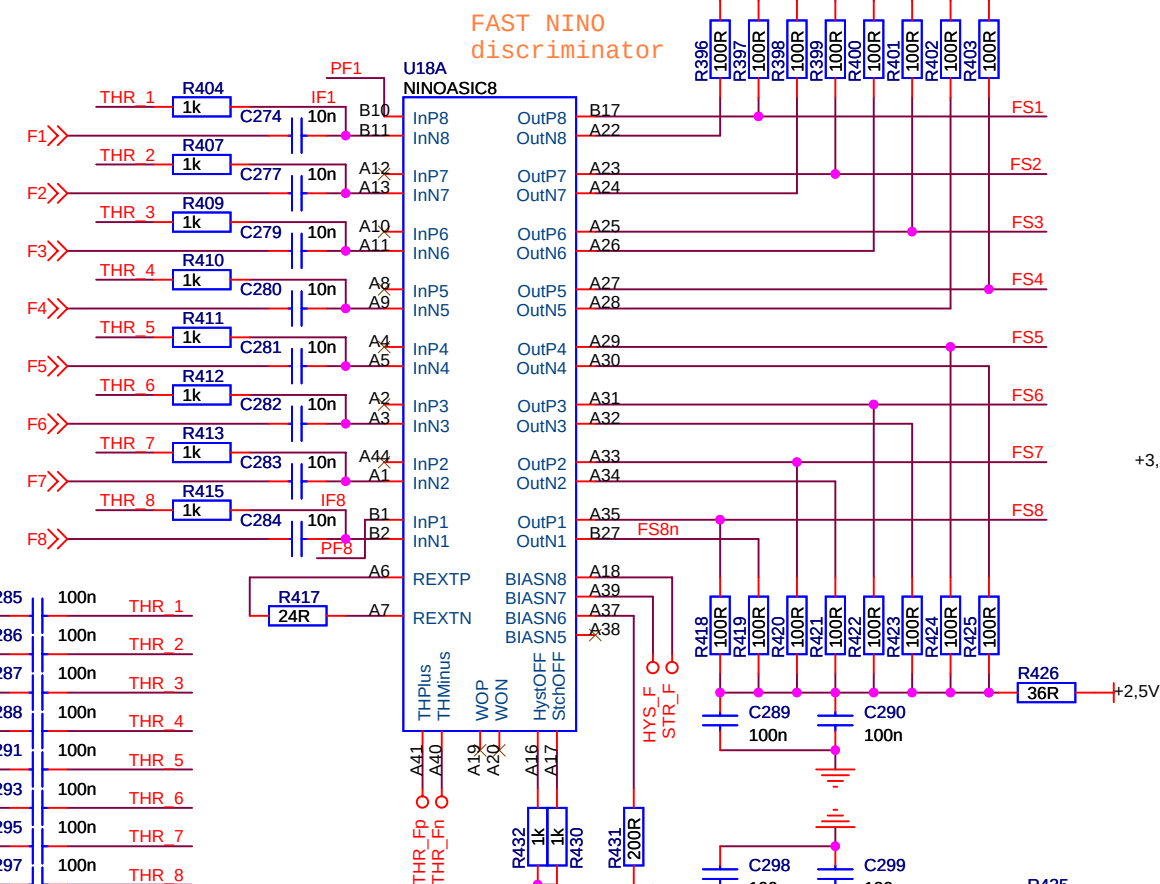
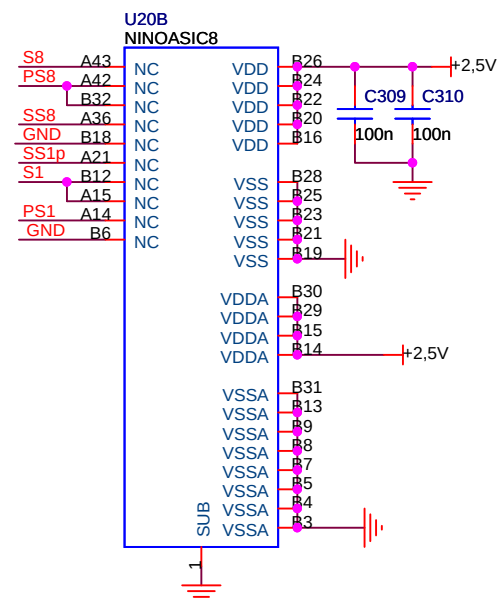
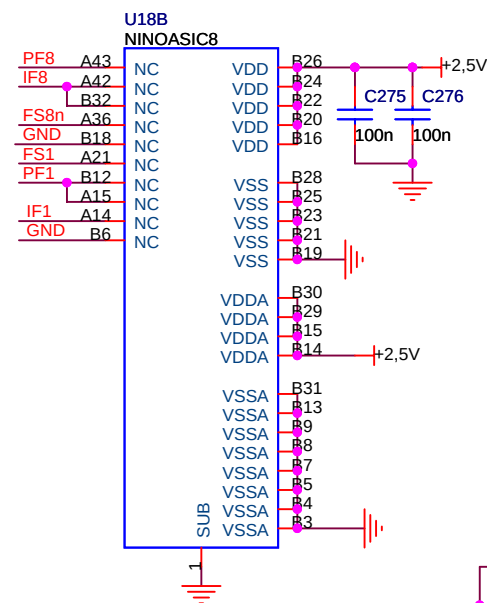
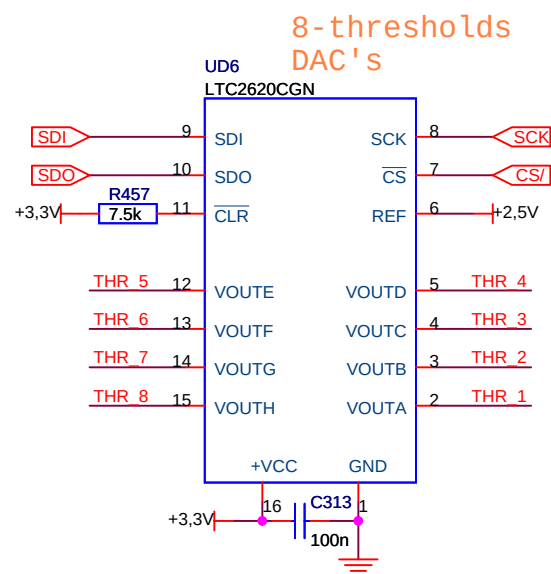
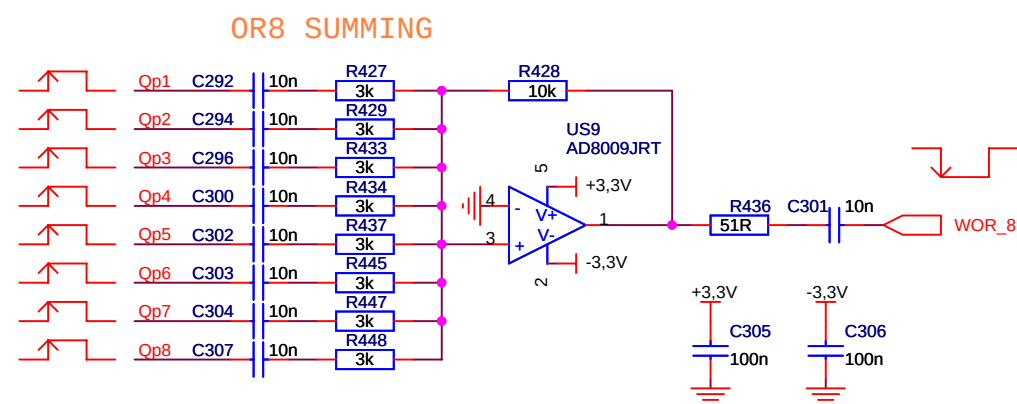
Capacitors 100n must be place as close as possible to resistors 10K SLOW part

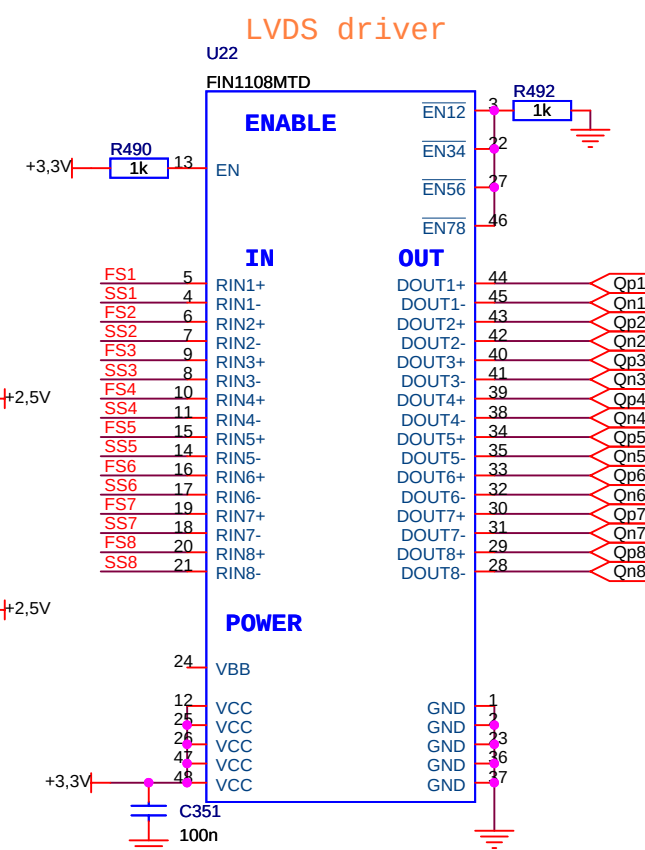
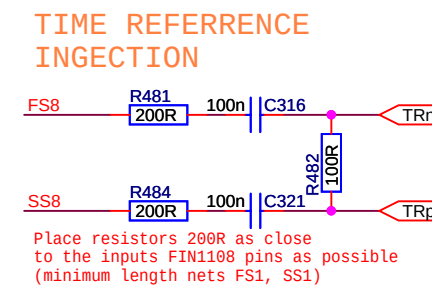
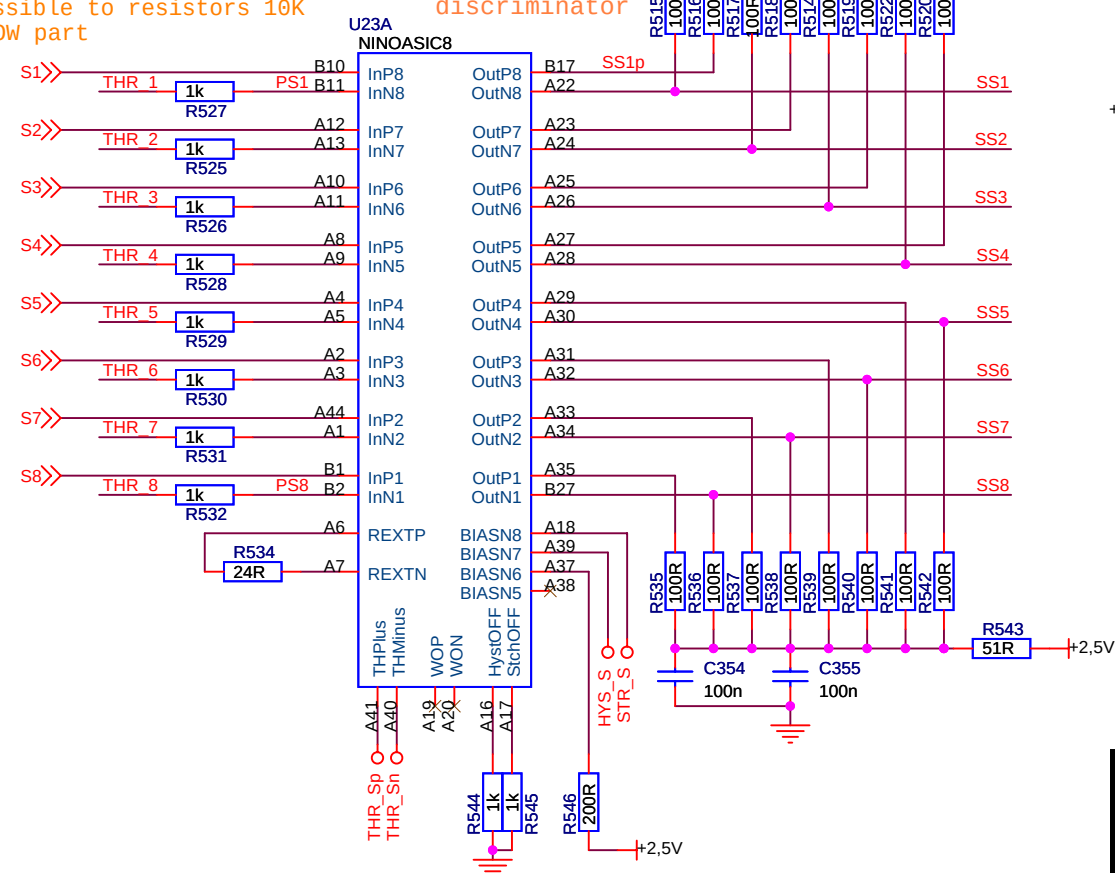
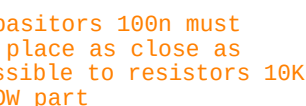
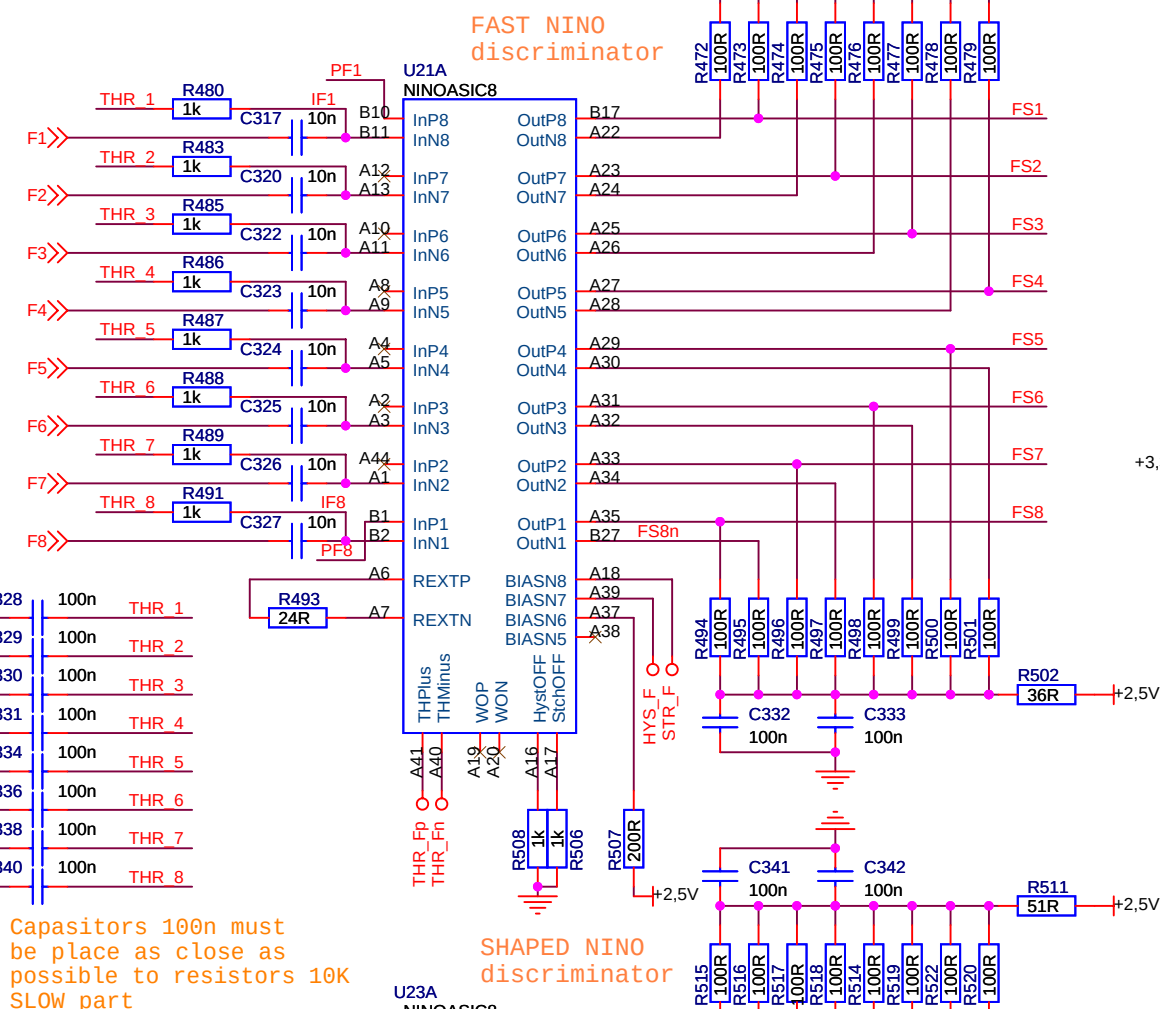
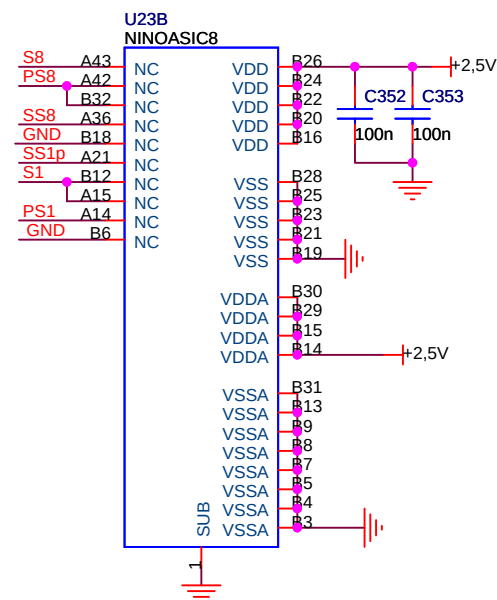
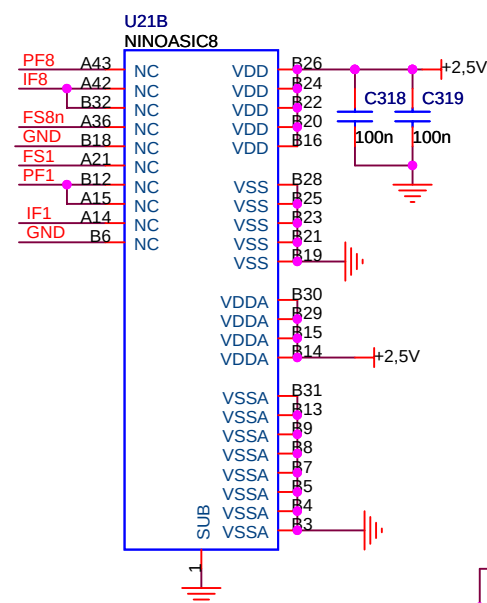
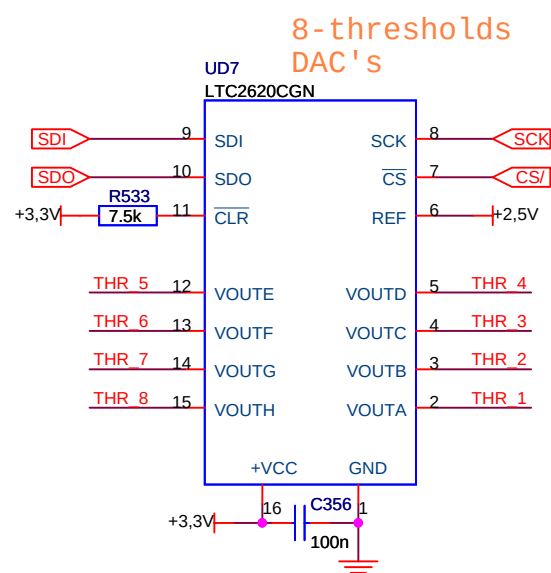
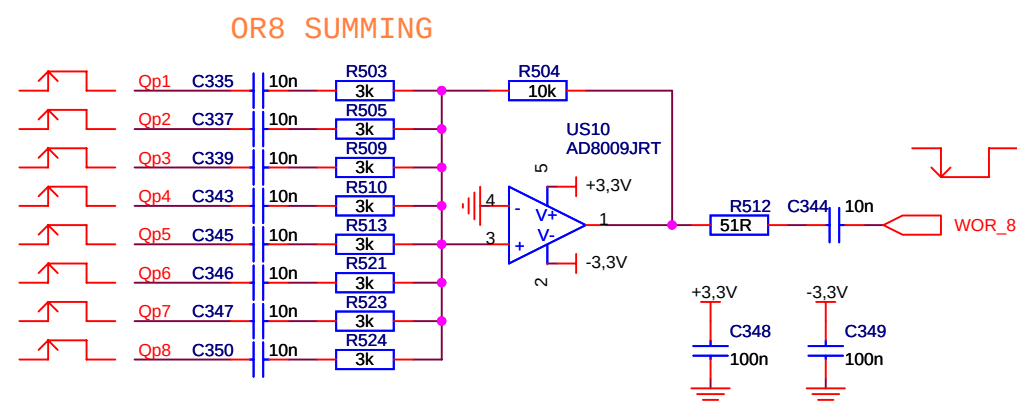


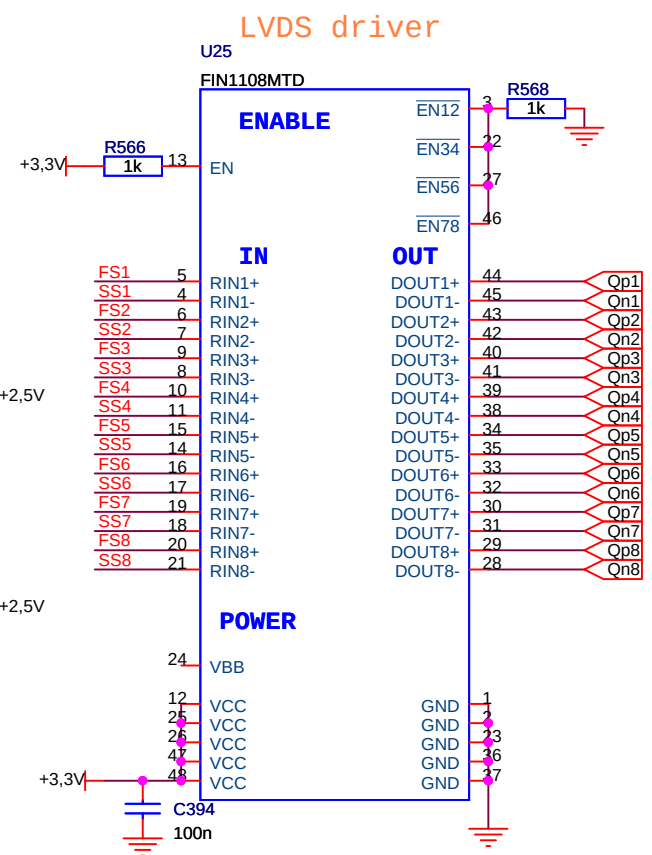
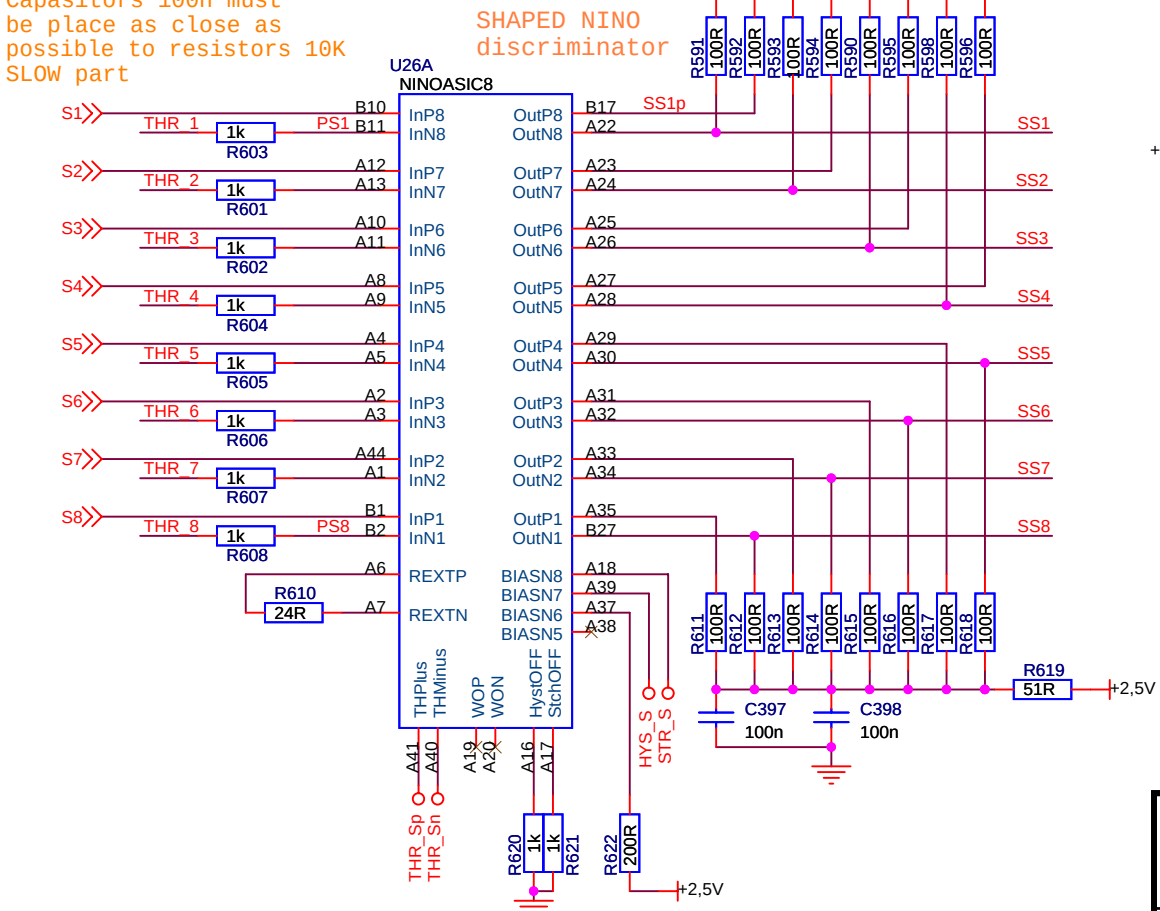
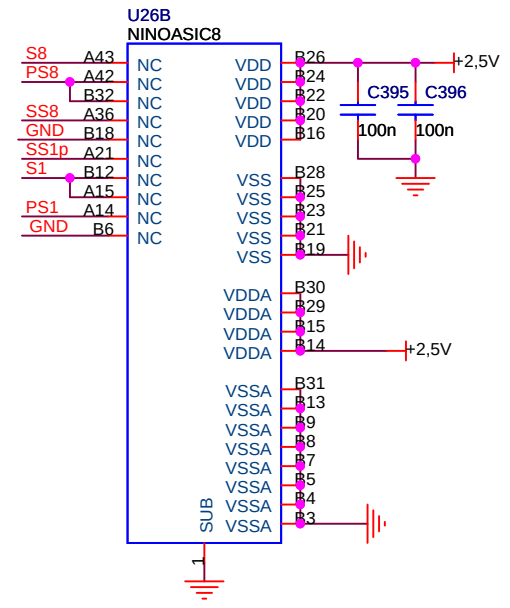
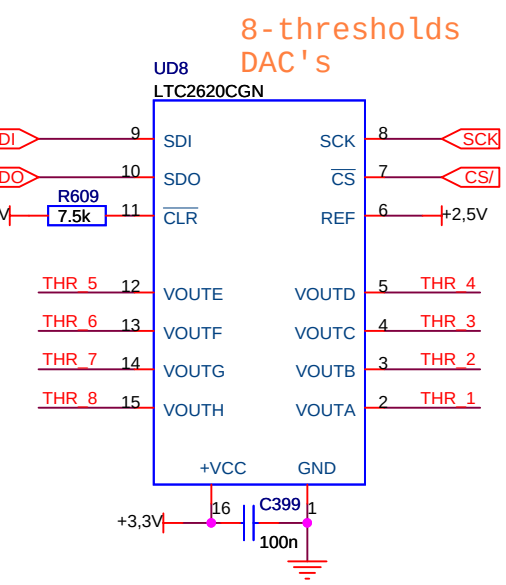
LVDS driver



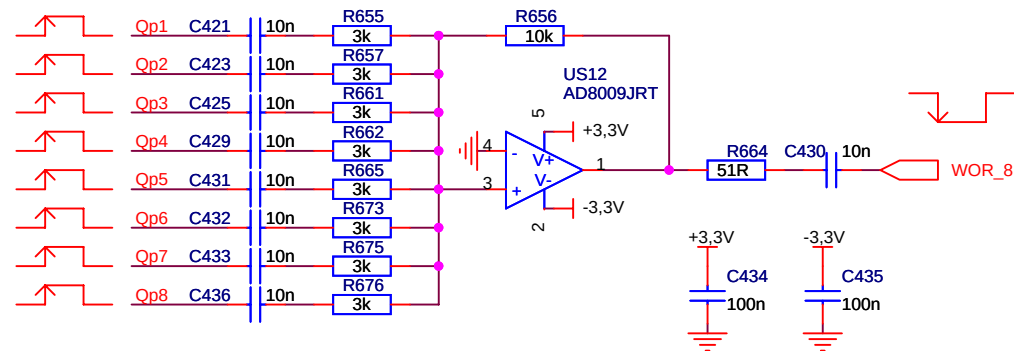




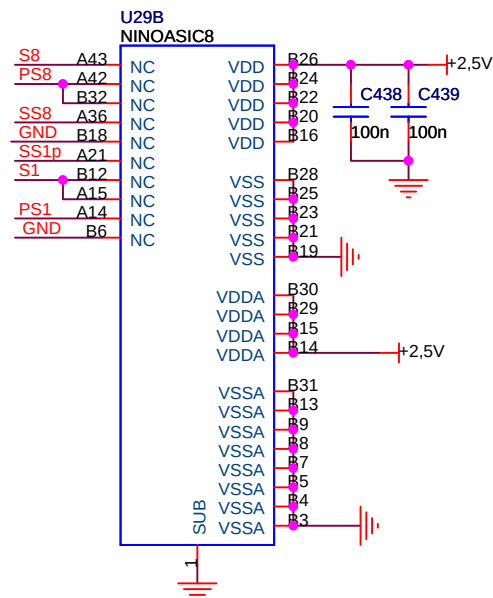
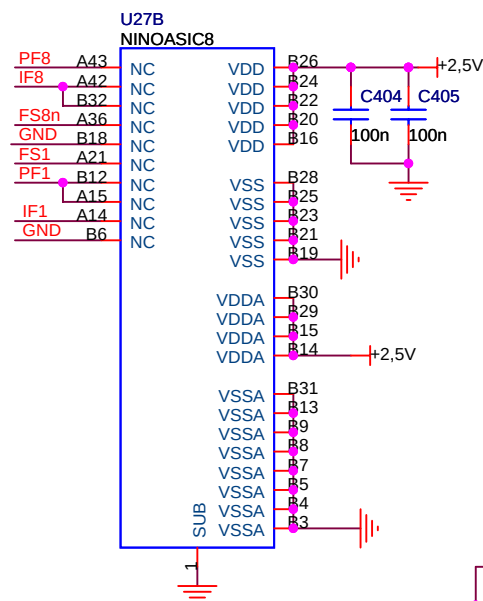
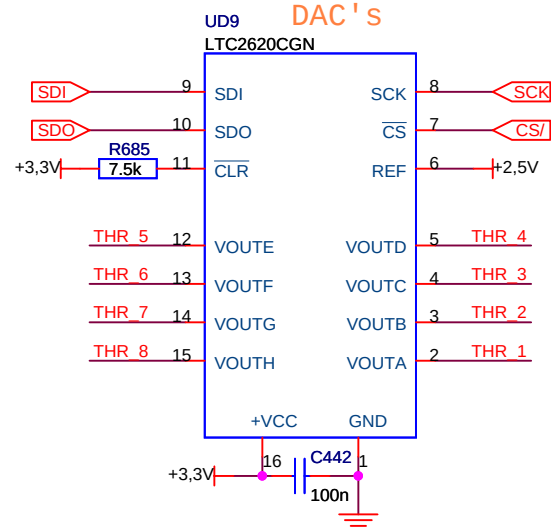




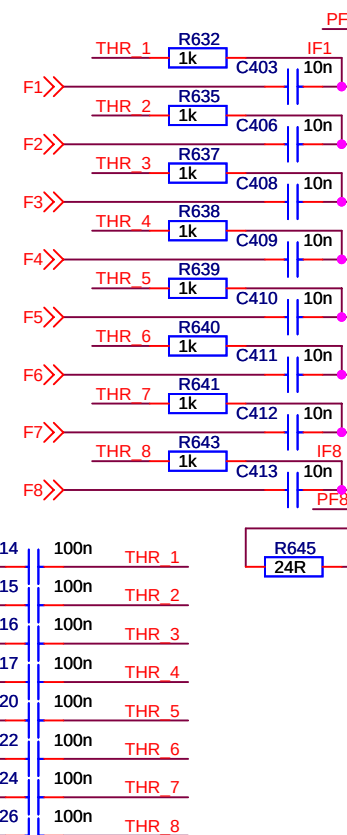
OR8 SUMMING



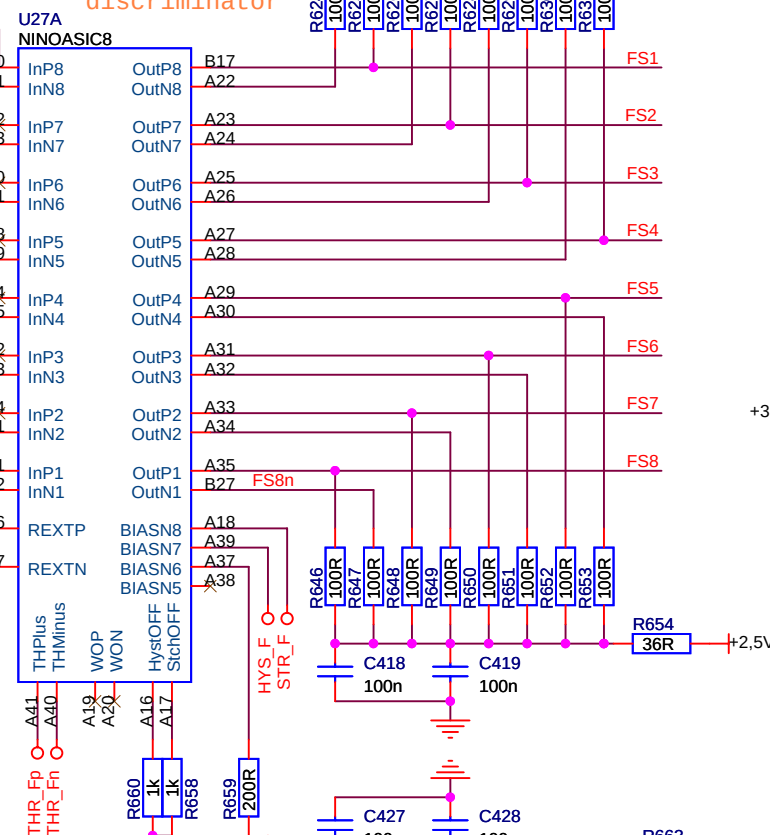
8-thresholds DAC's



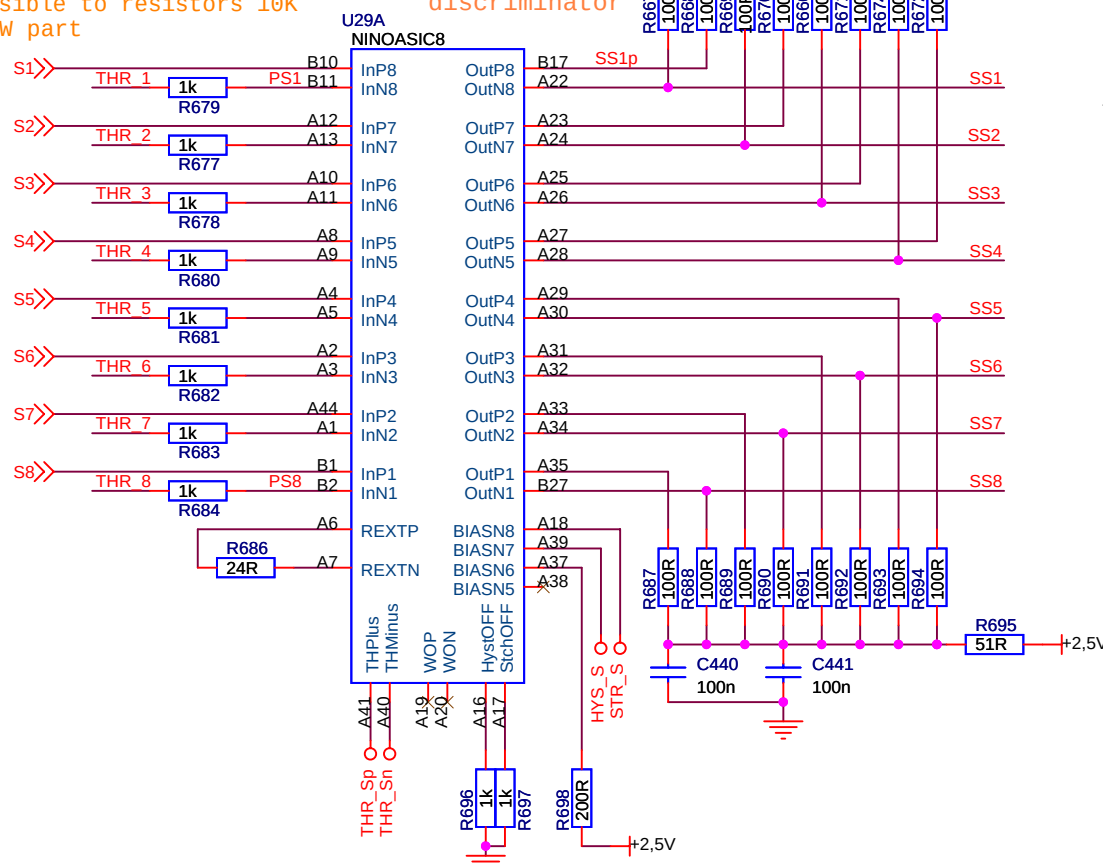
Capacitors 100n must be place as close as possible to resistors 10K SLOW part



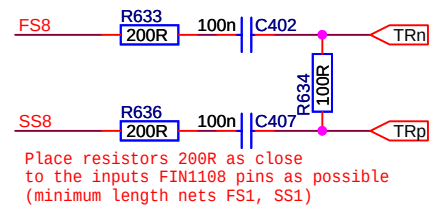
FAST NINO discriminator



SHAPED NINO discriminator

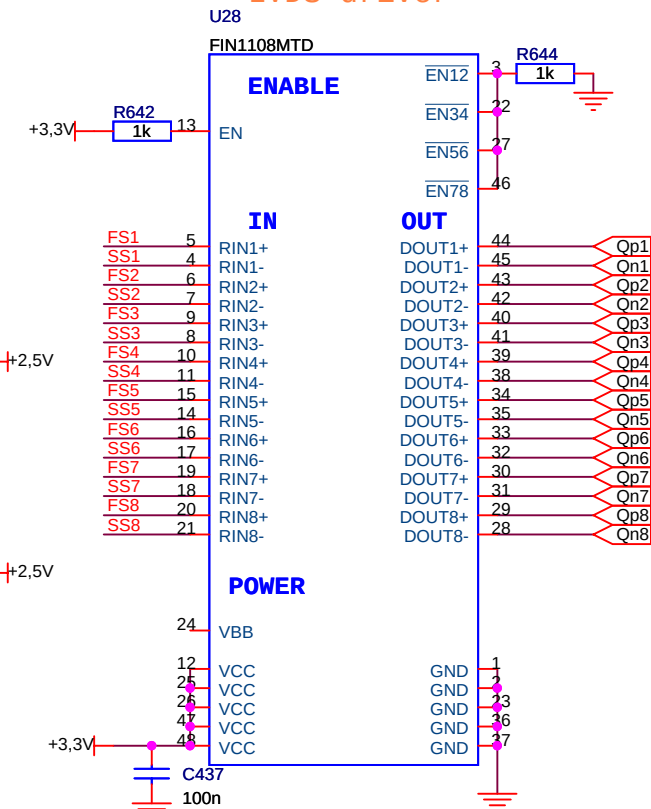


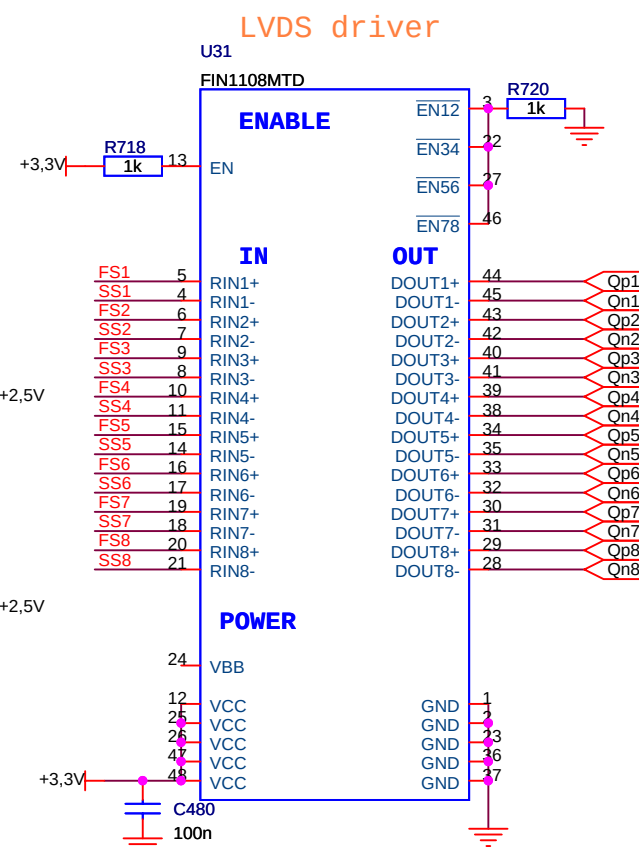
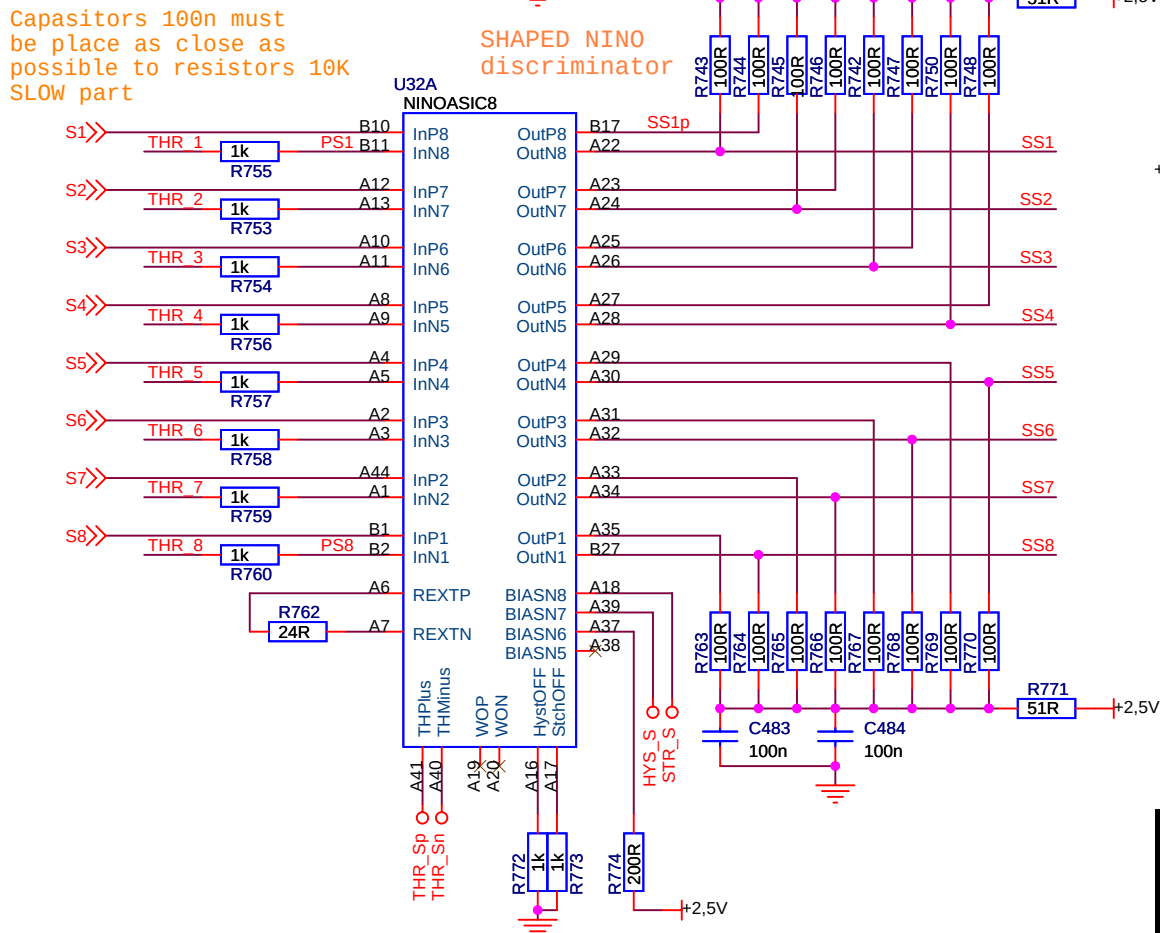
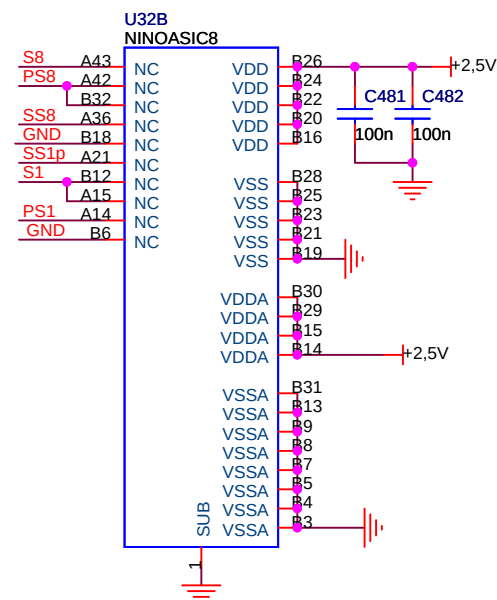
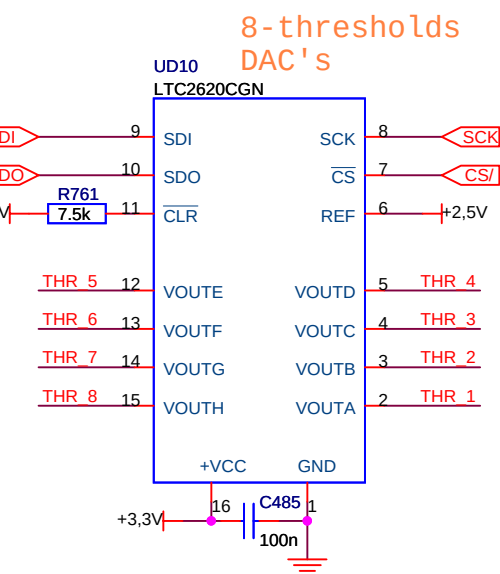
TIME REFERENCE INJECTION

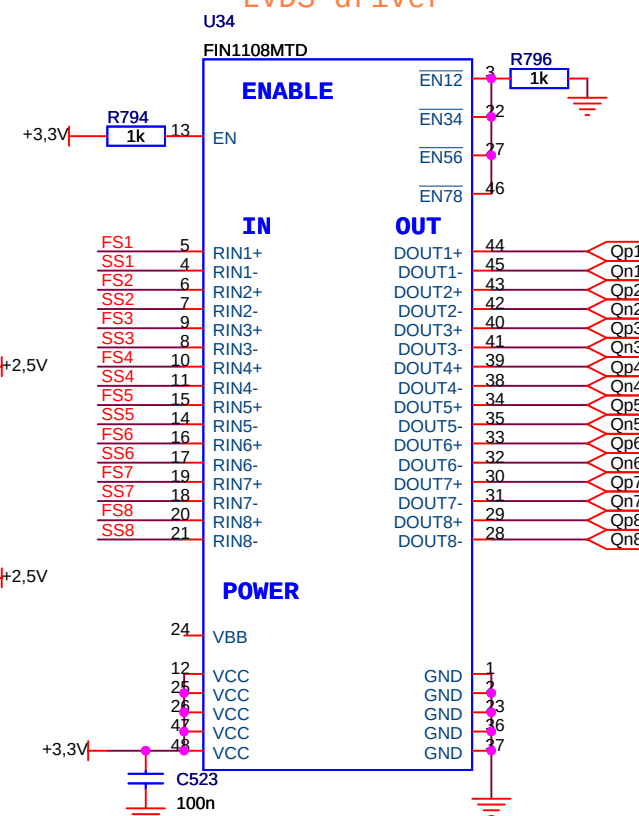
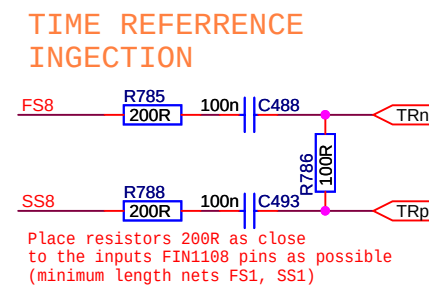
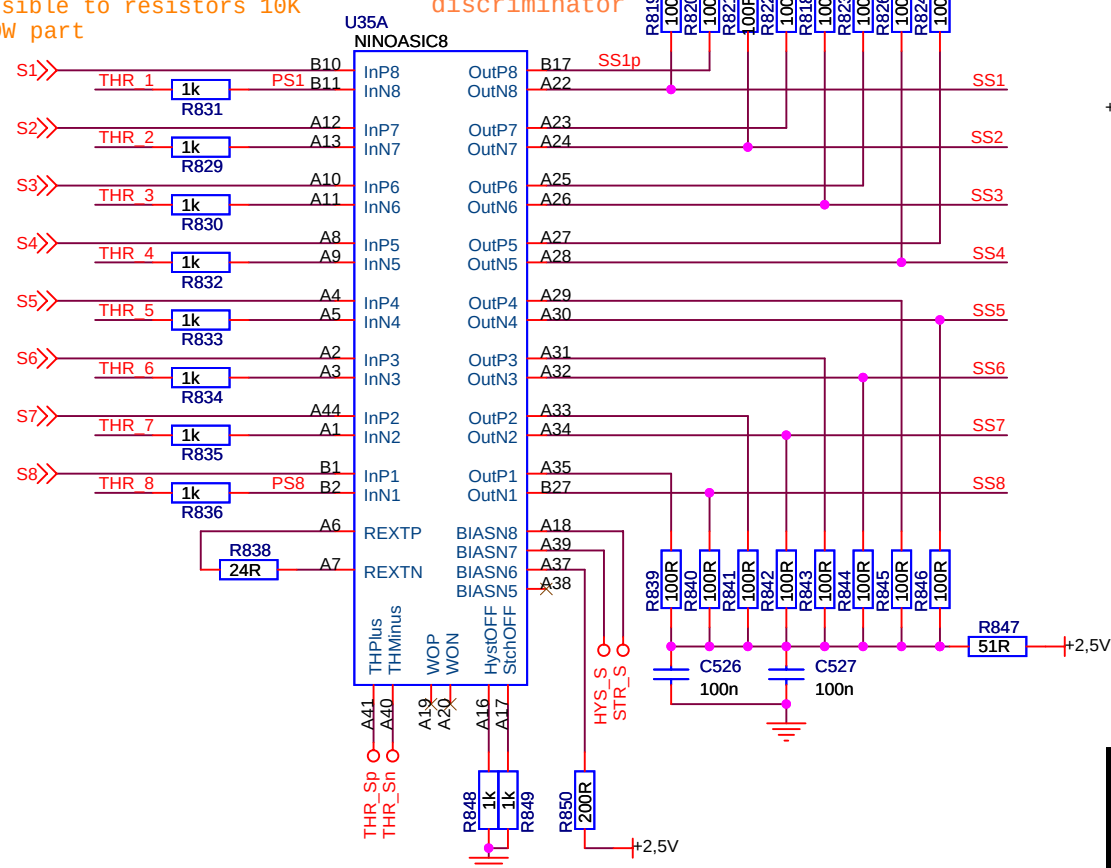
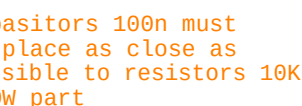
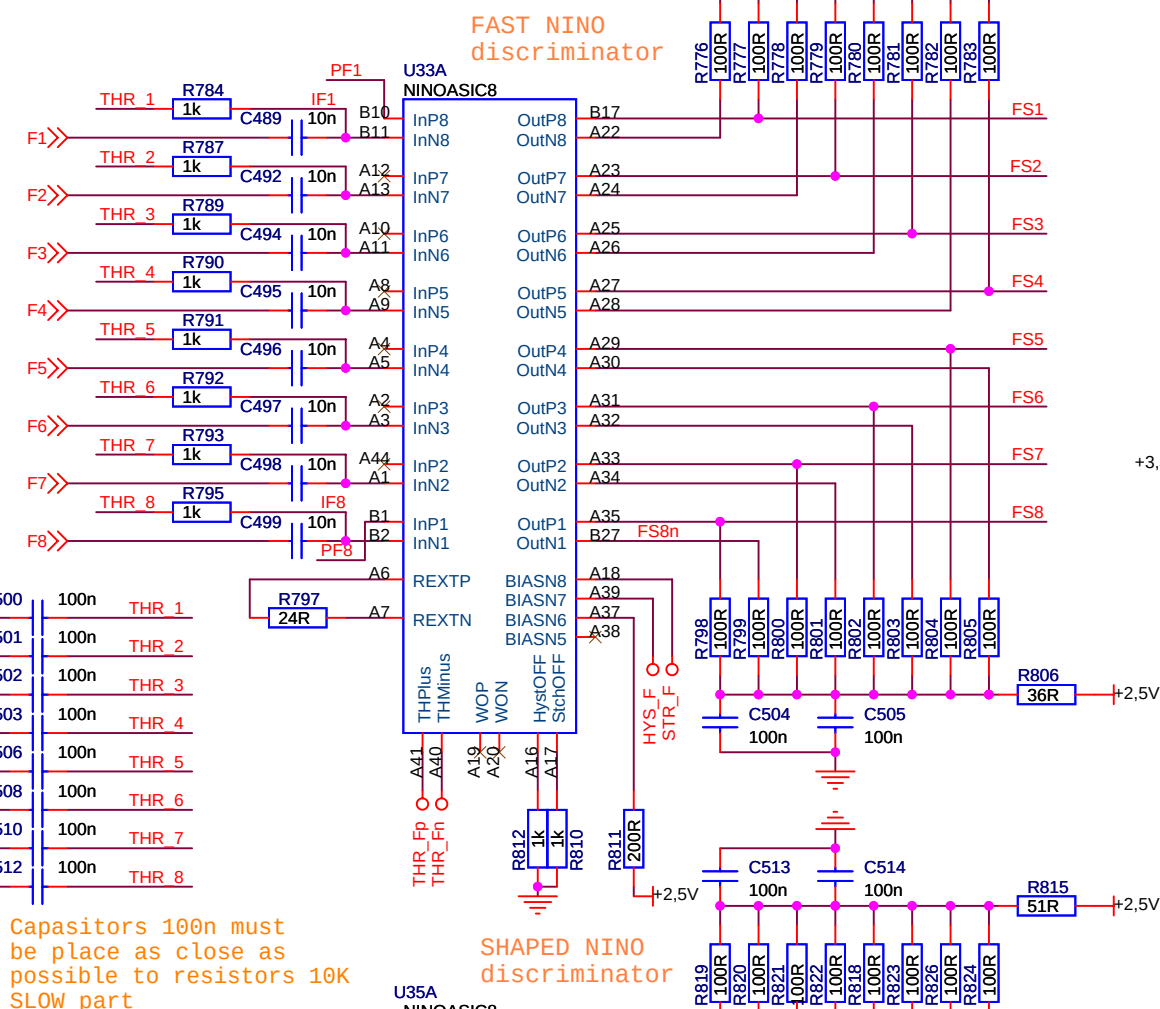
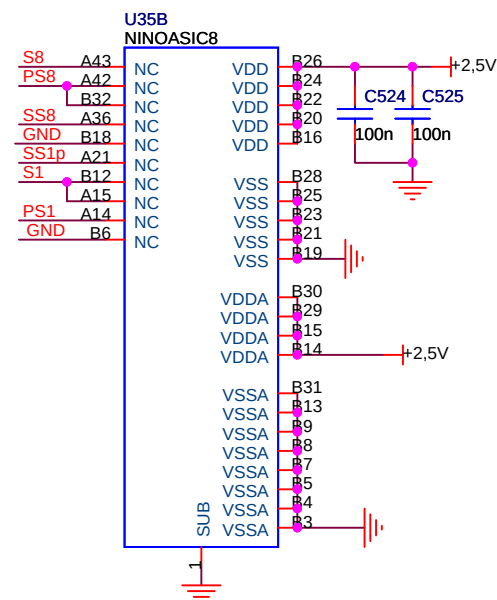
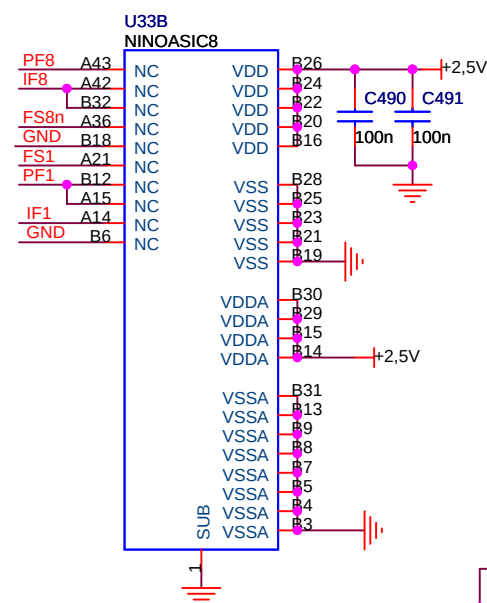
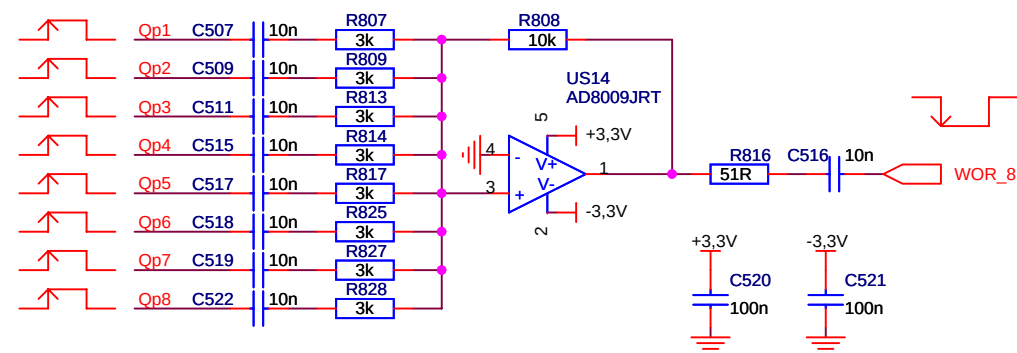


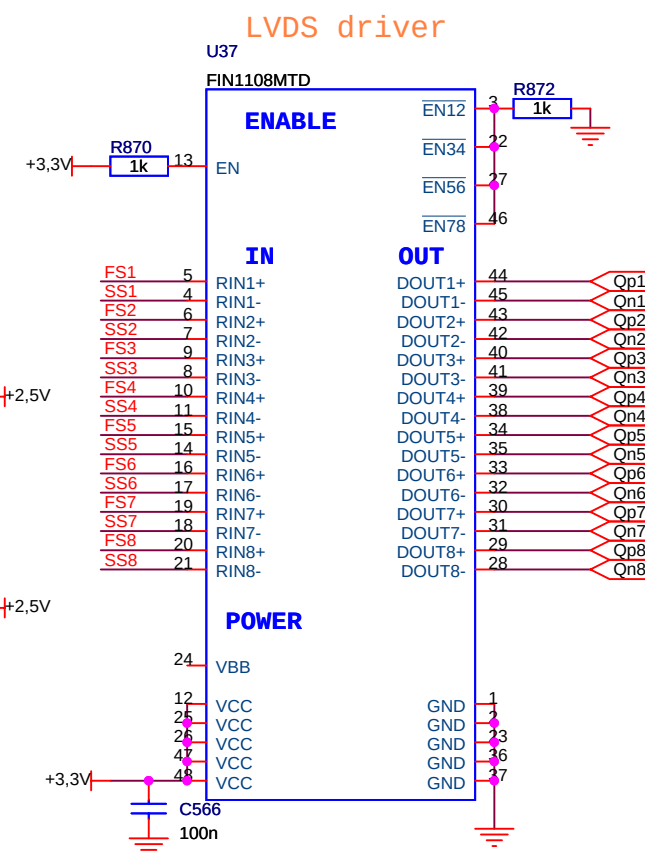
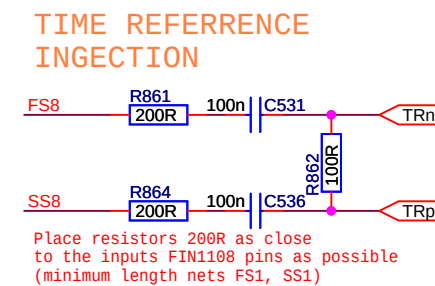
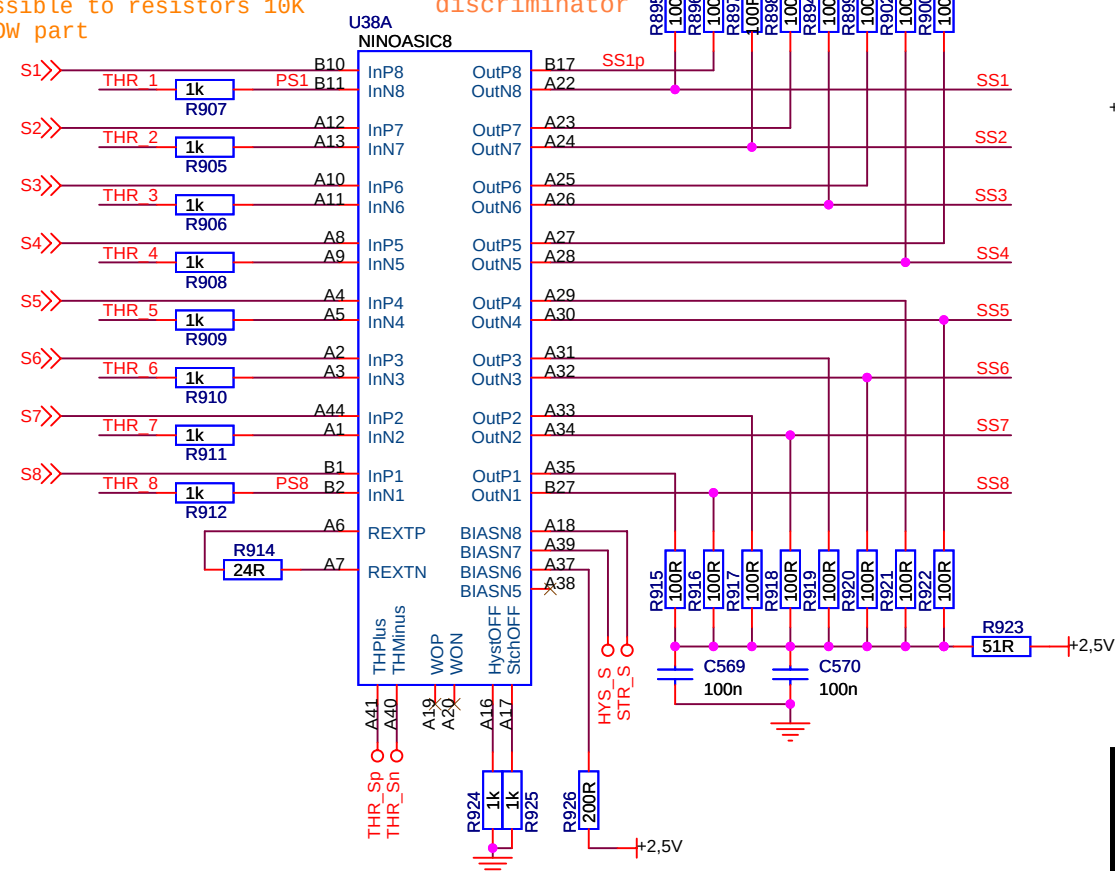
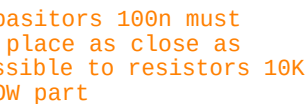
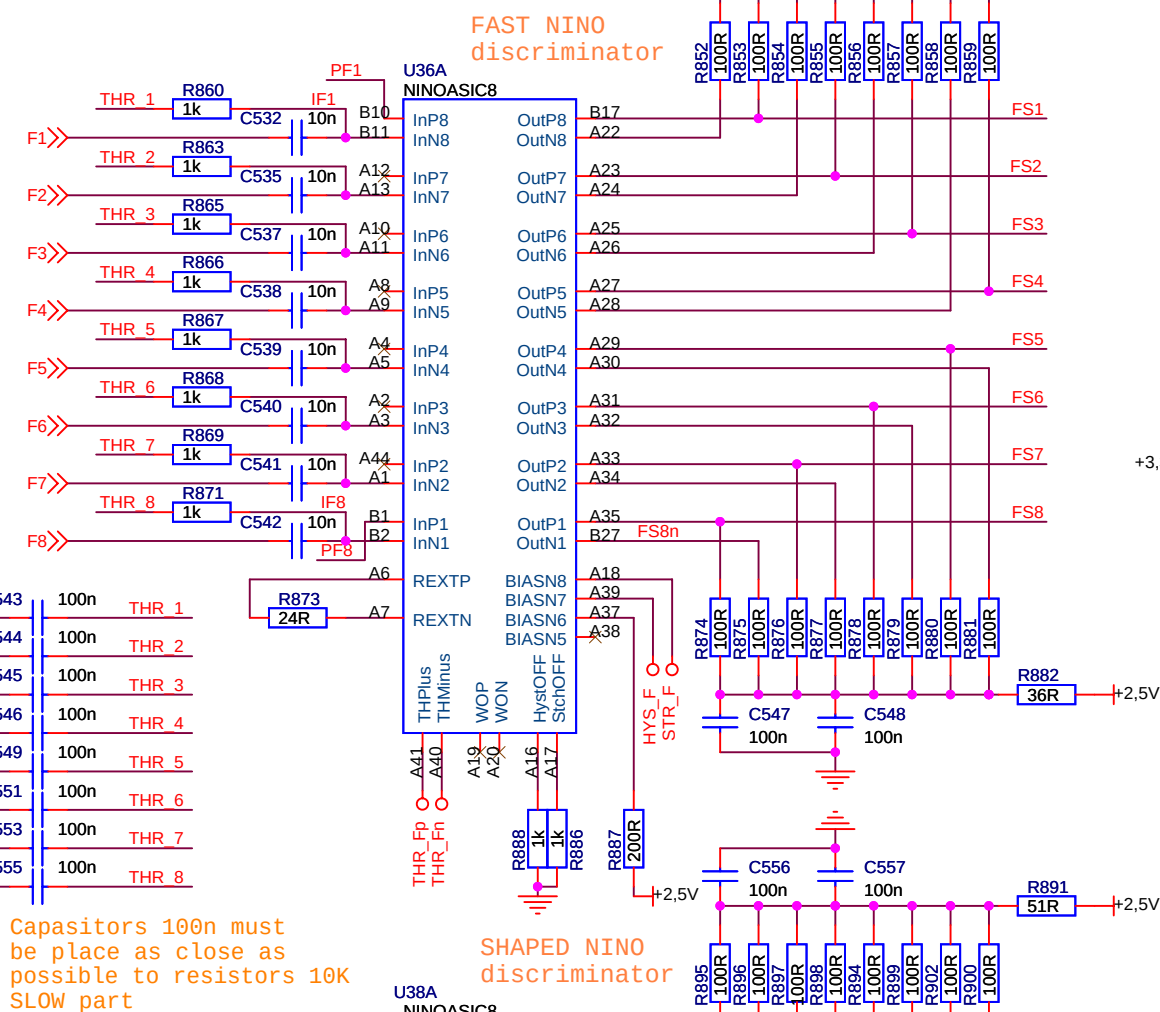
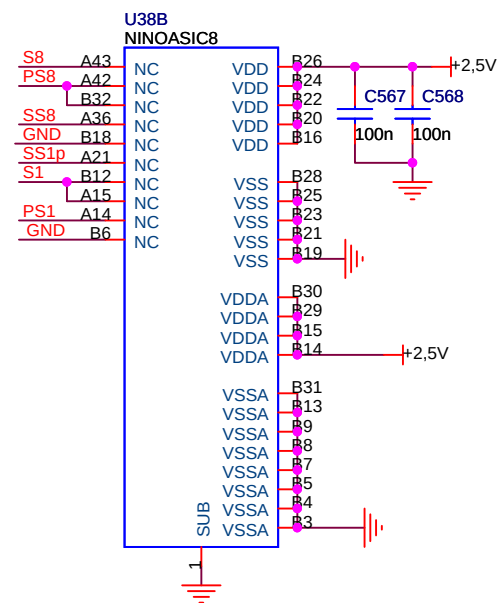
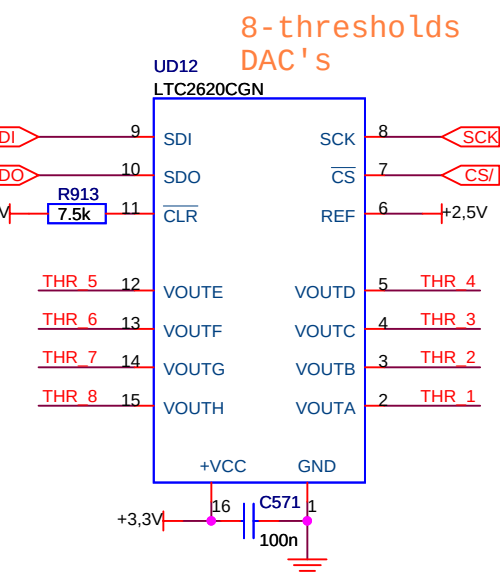
Place resistors 200R as close to the inputs FIN1108 pins as possible (minimum length nets FS1, SS1)

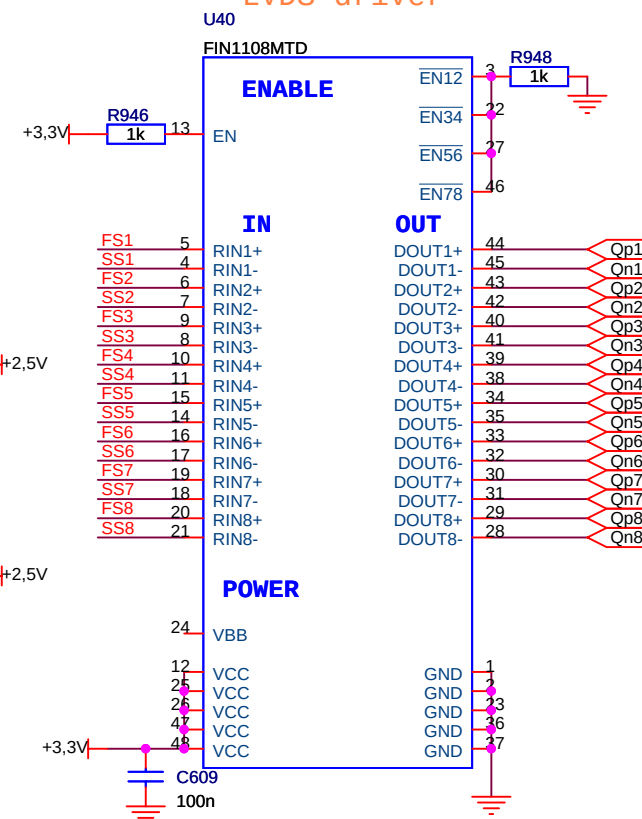
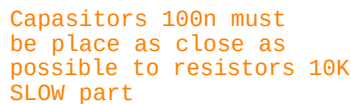
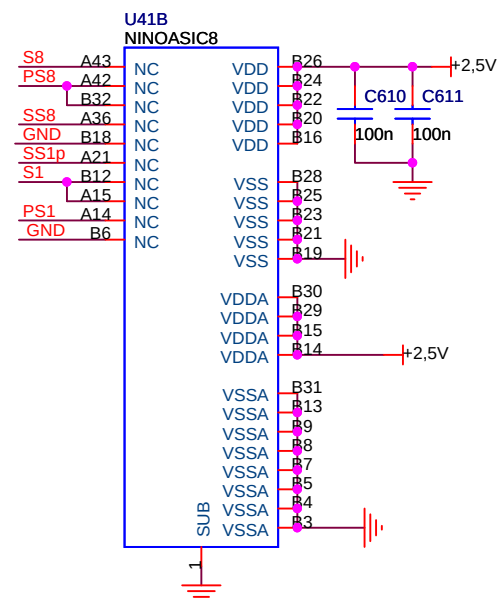
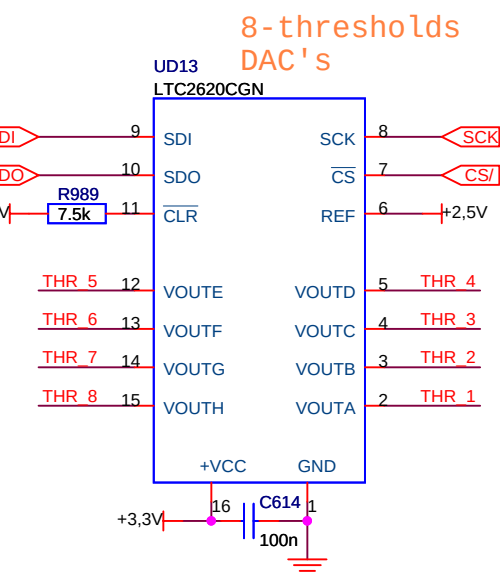
LVDS driver

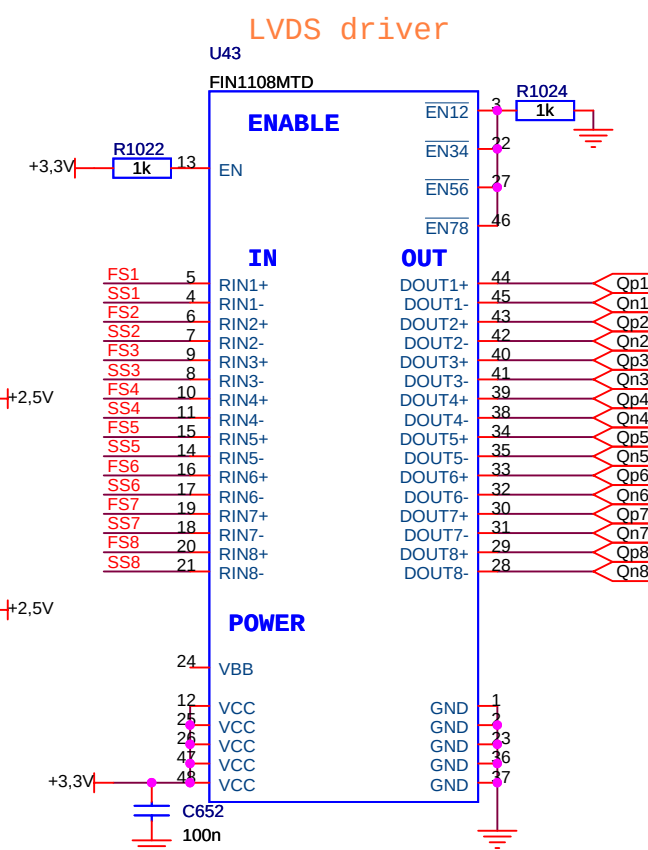
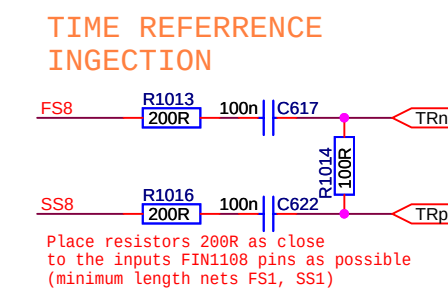
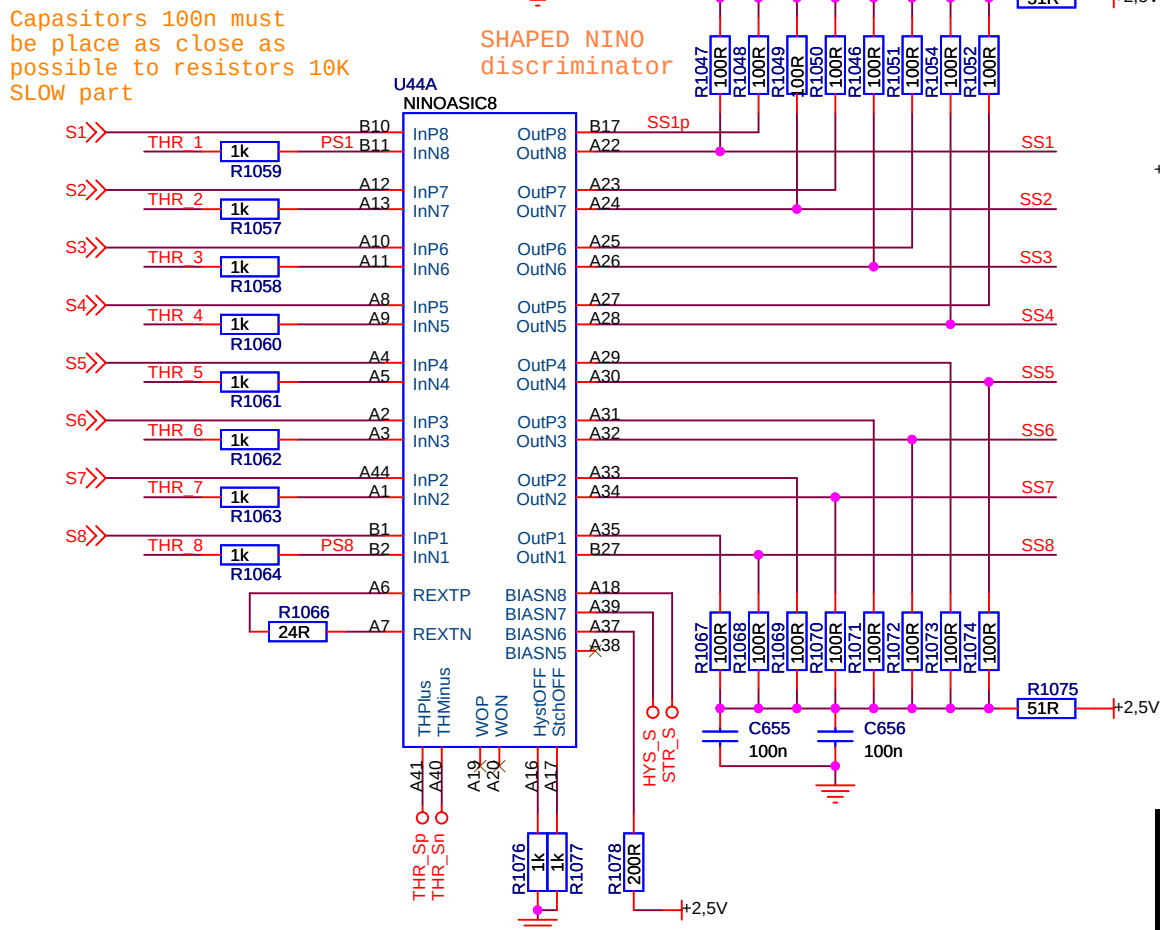
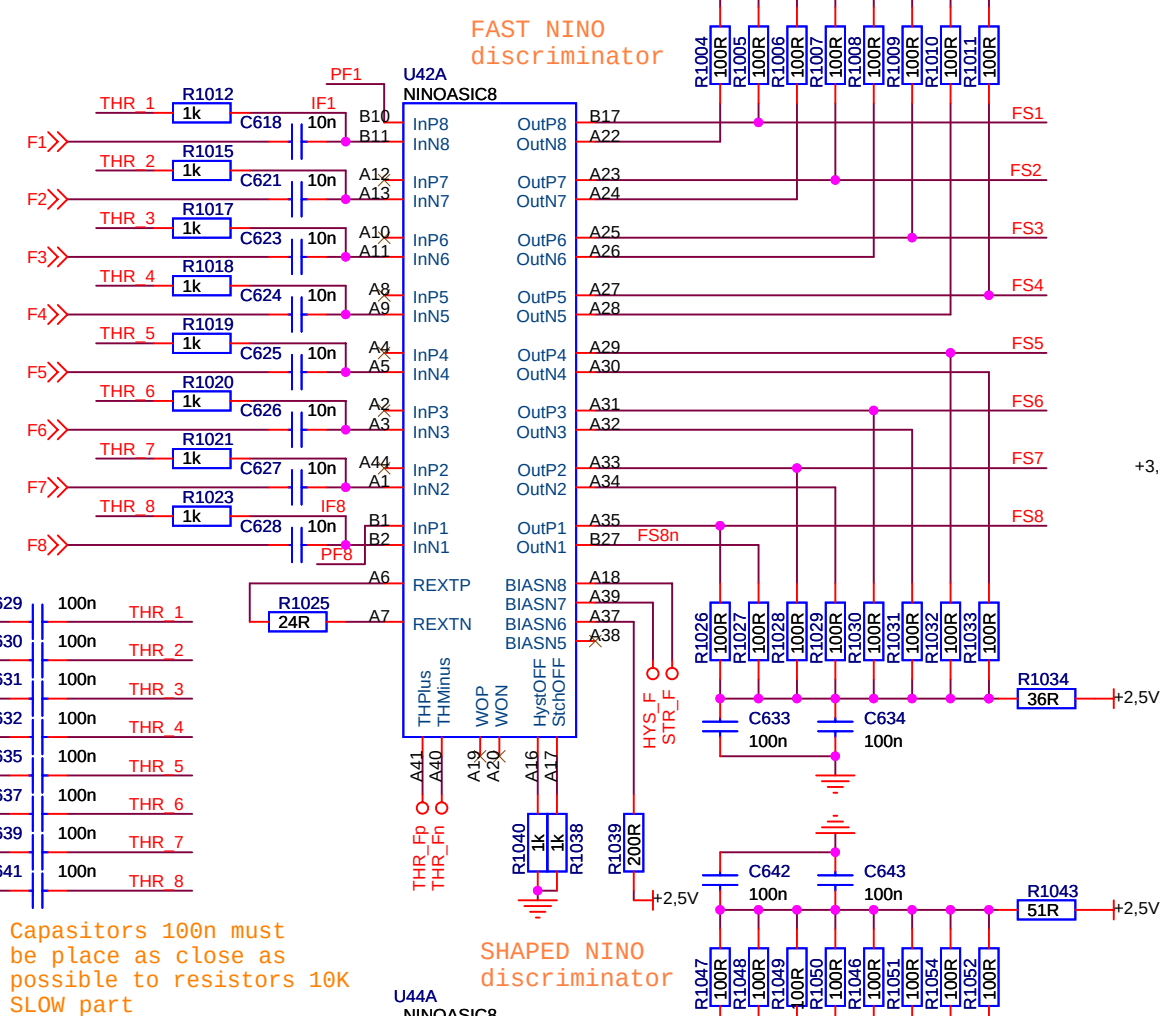
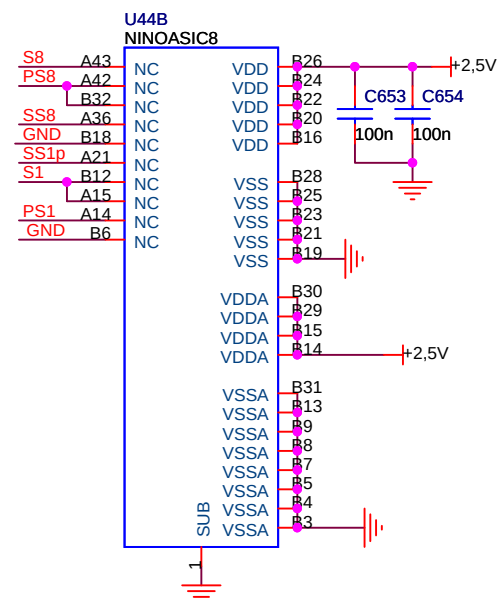
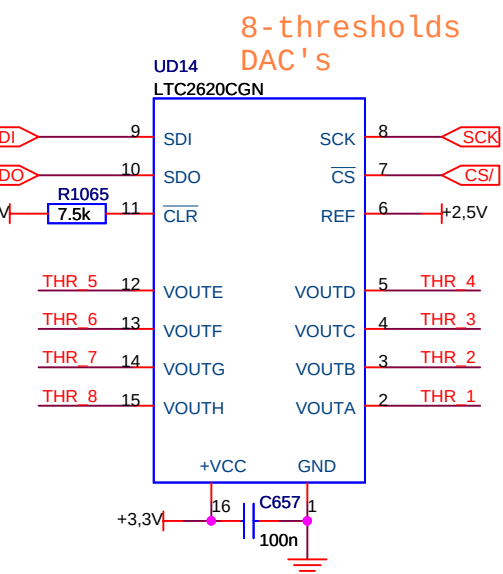


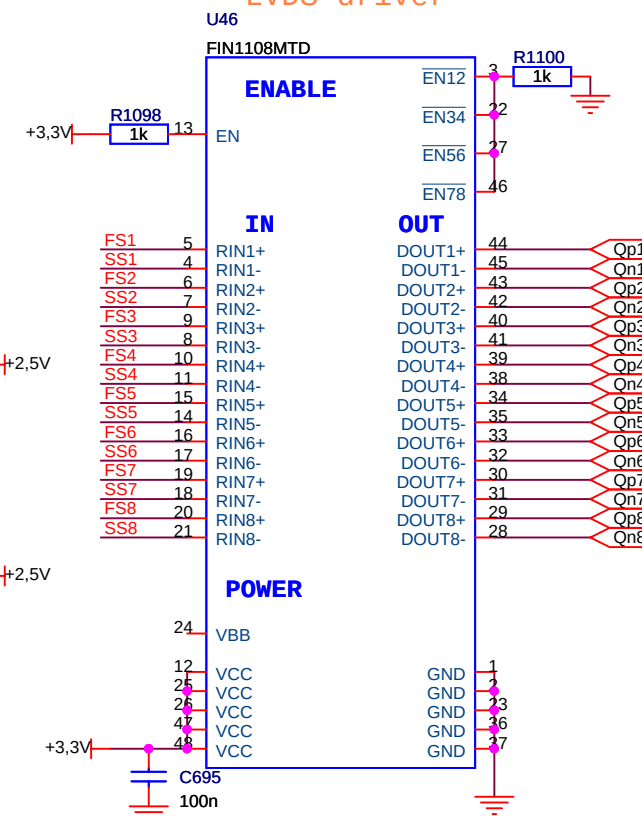
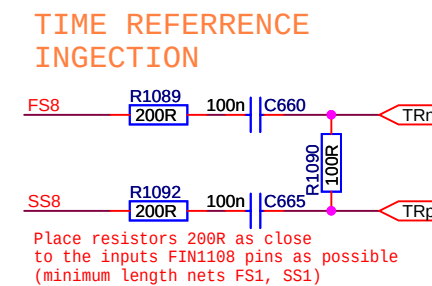
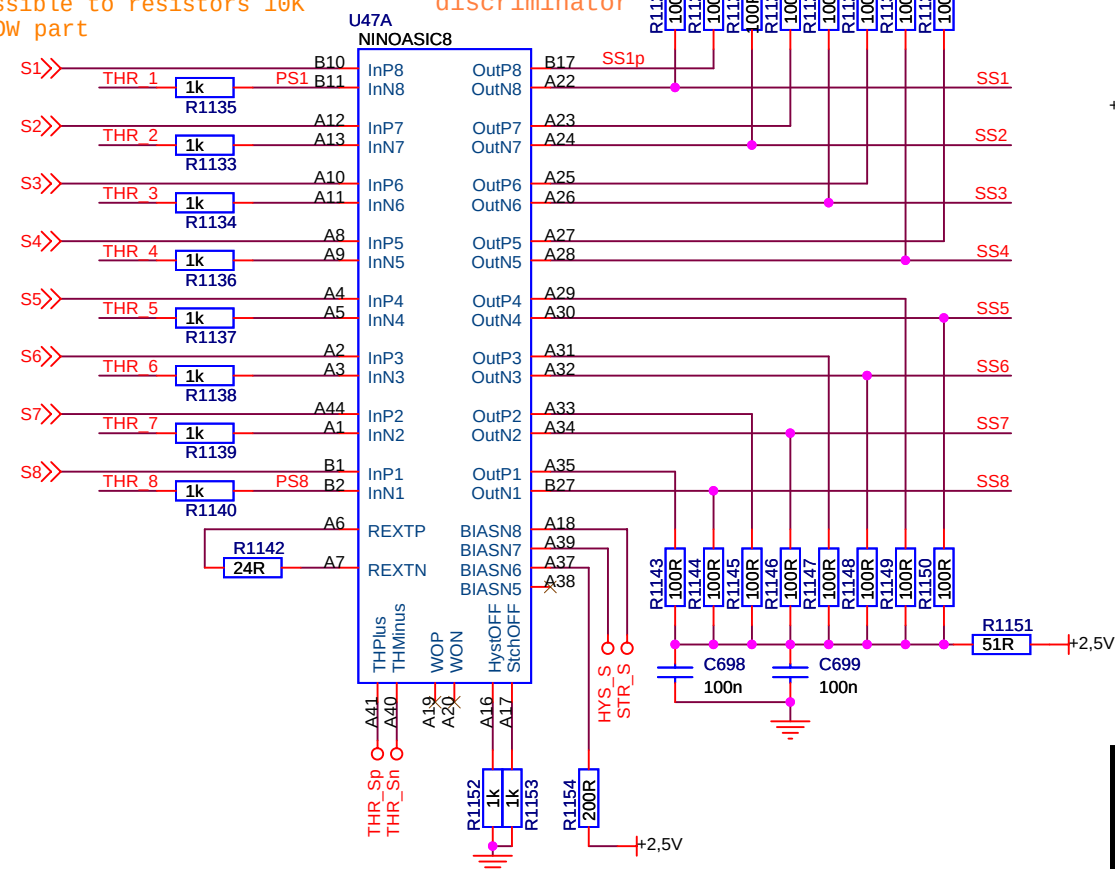
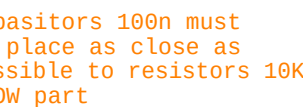
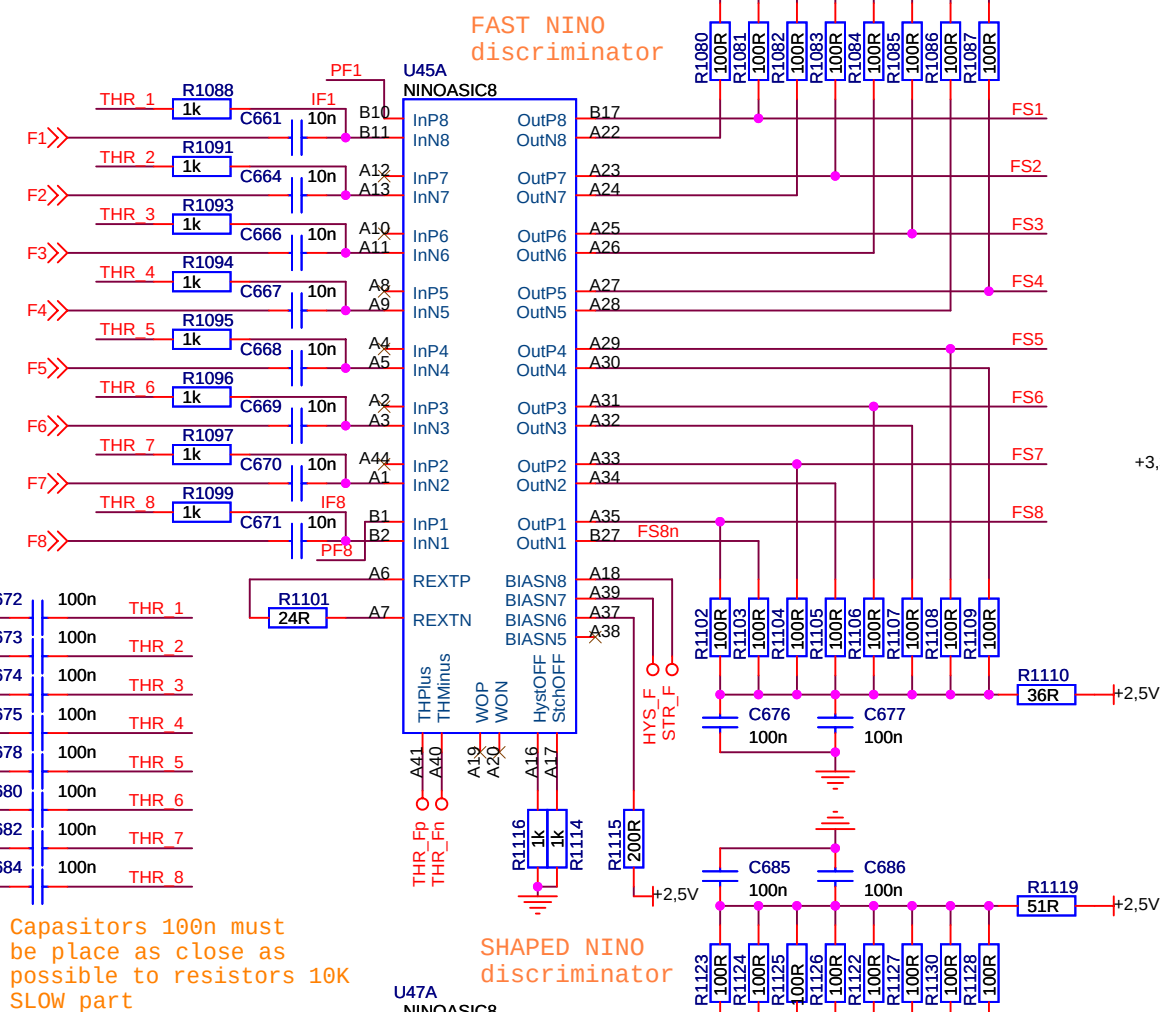
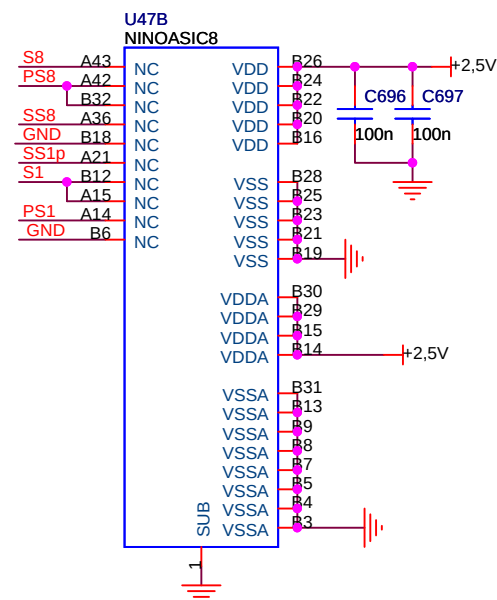
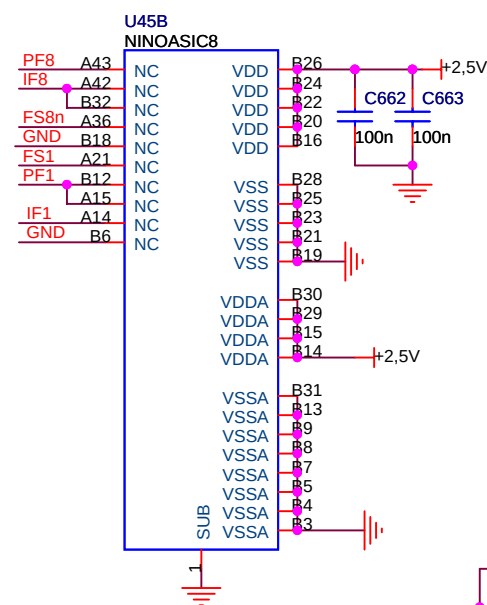
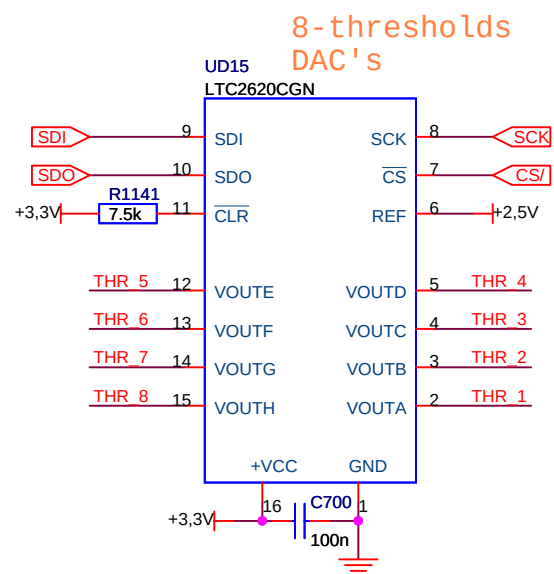
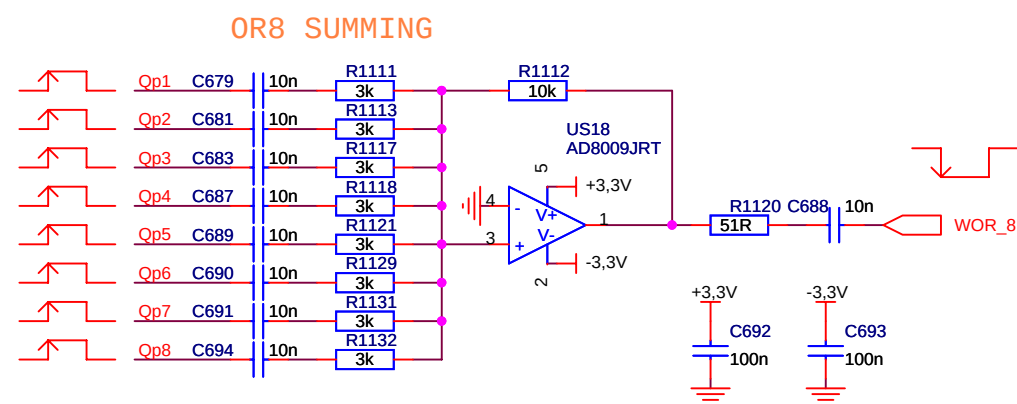


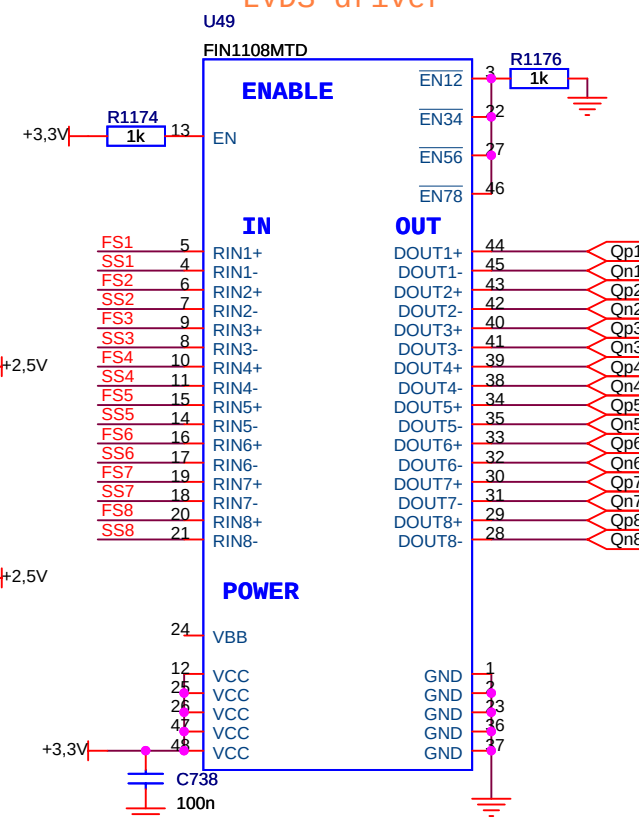
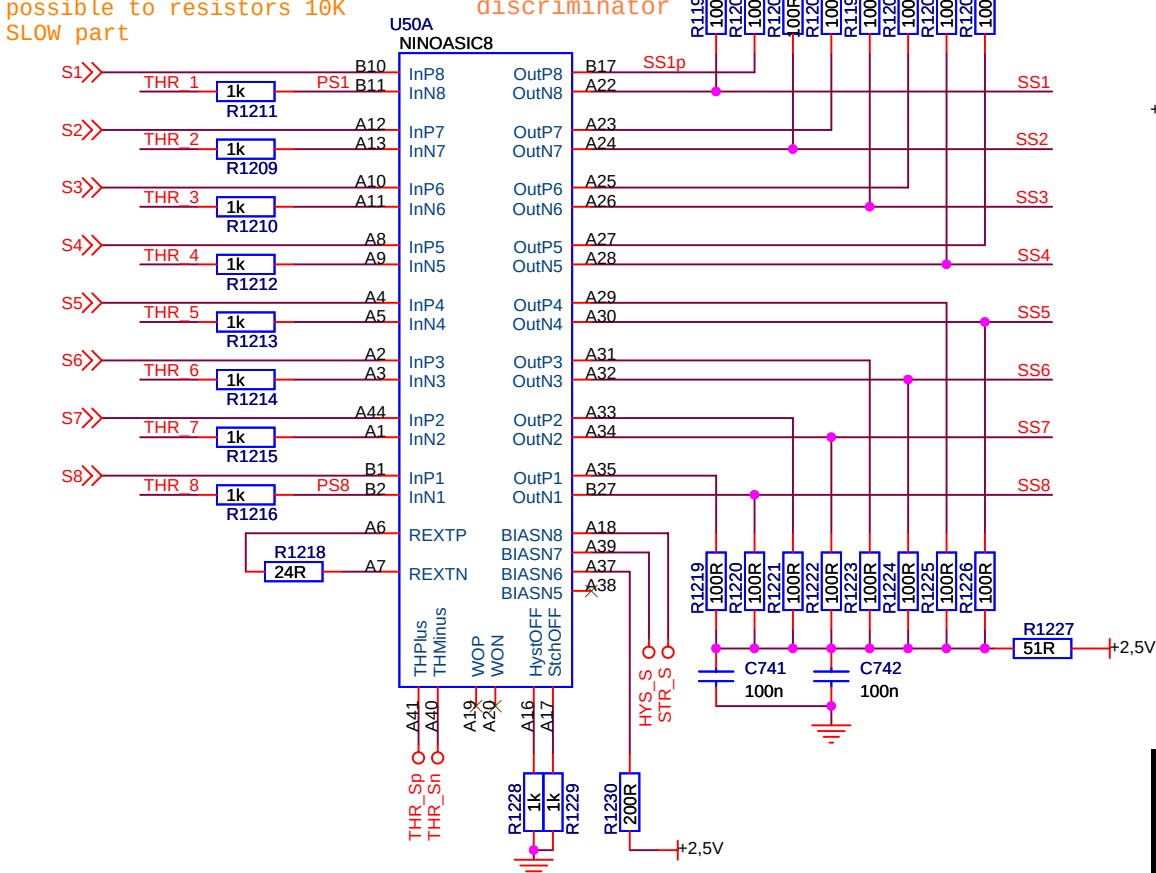
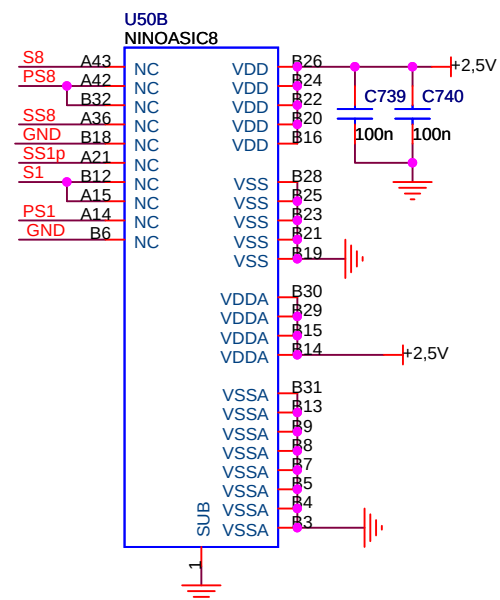
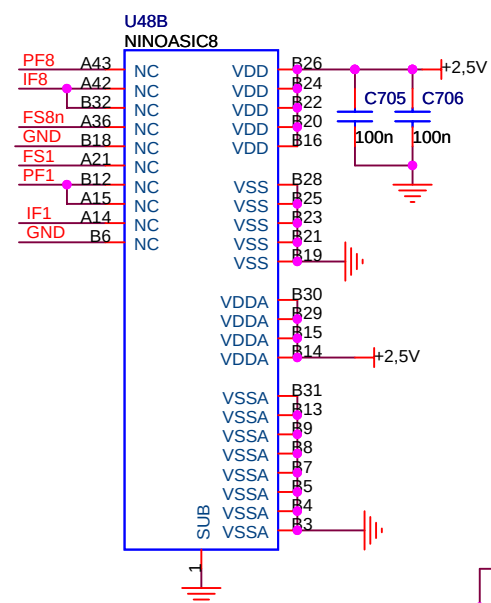
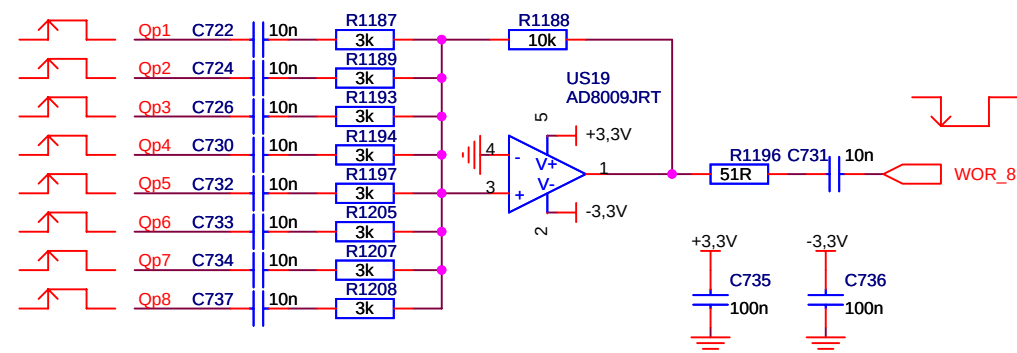


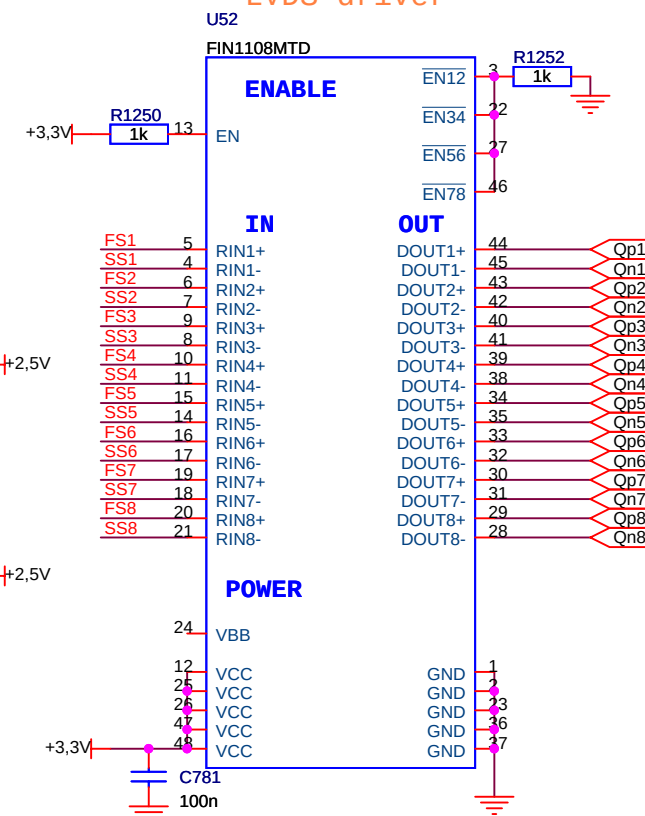
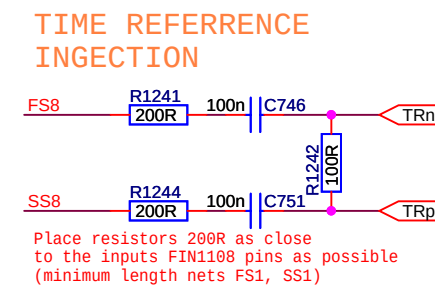
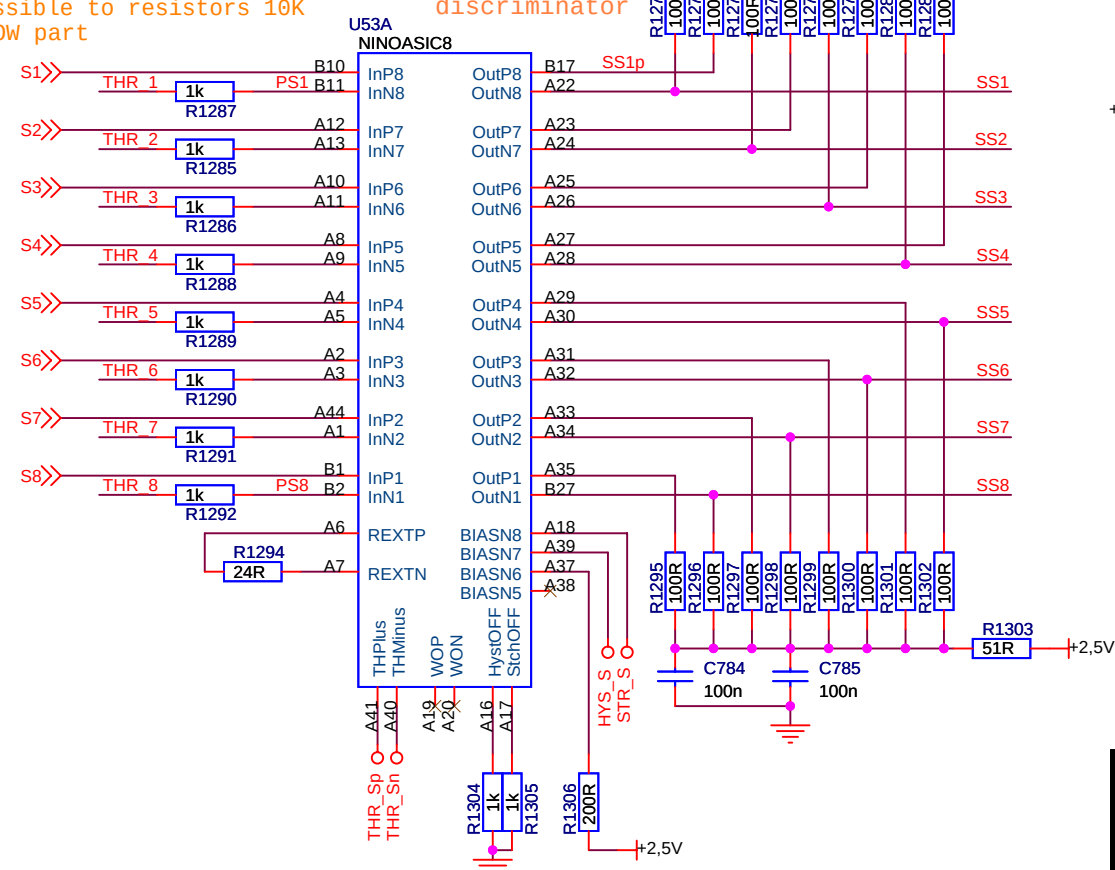
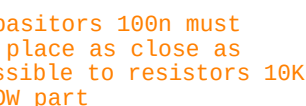
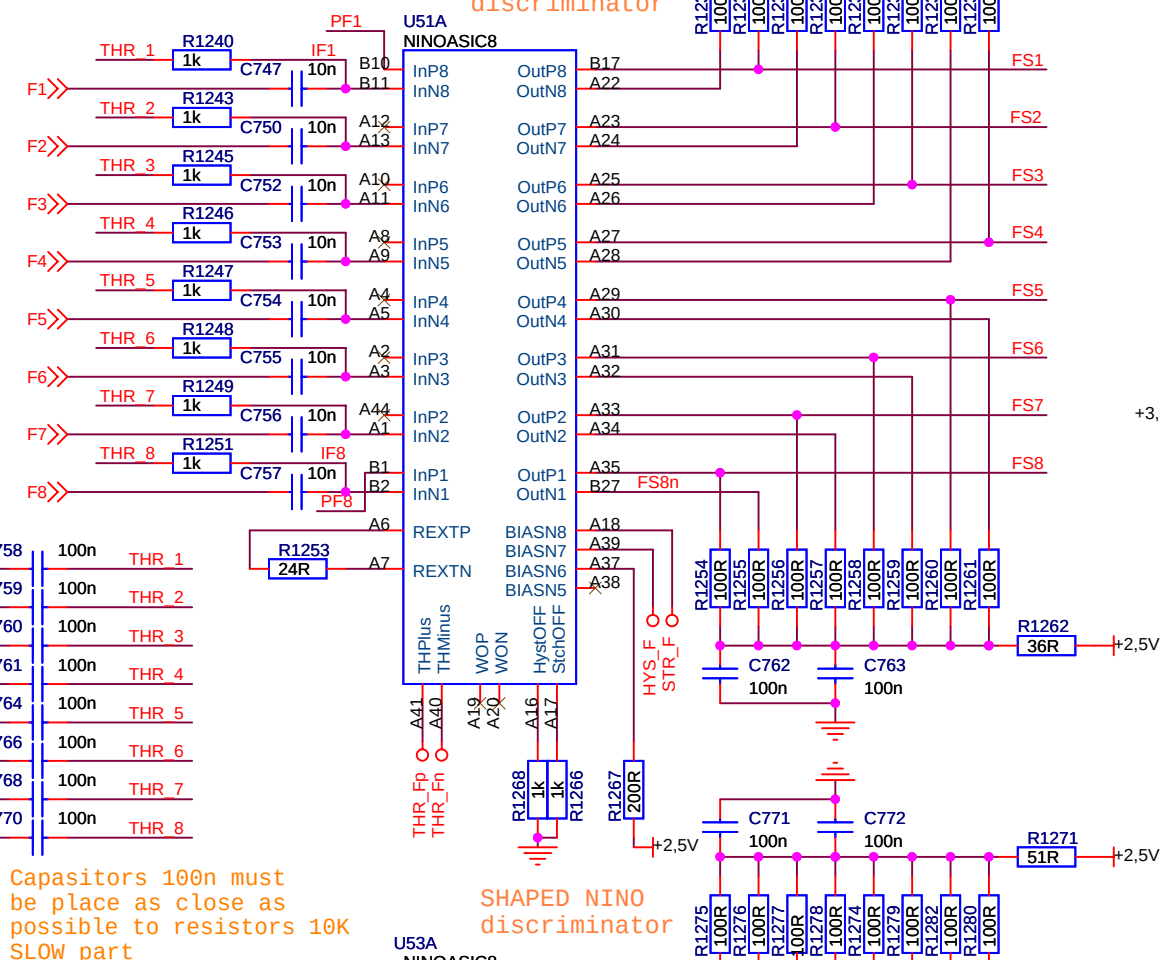
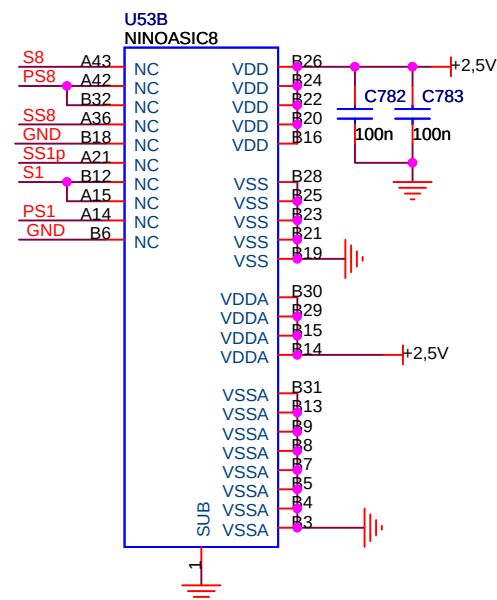
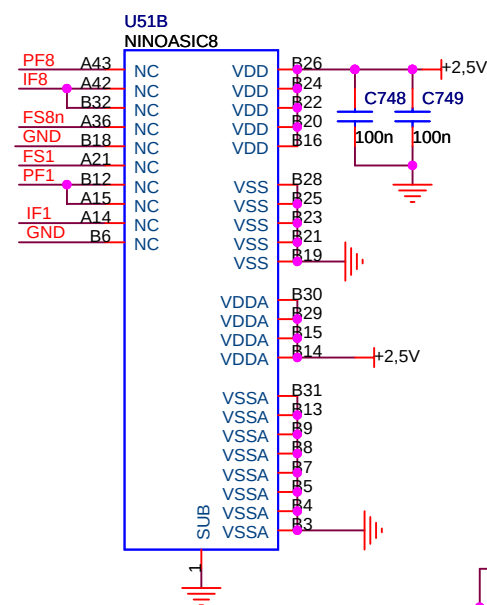
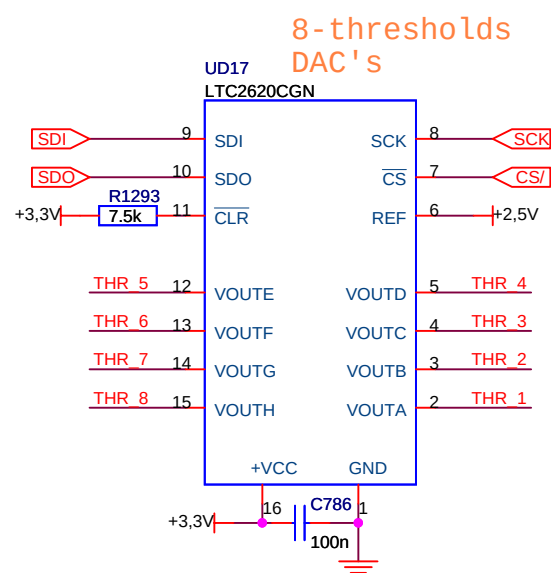
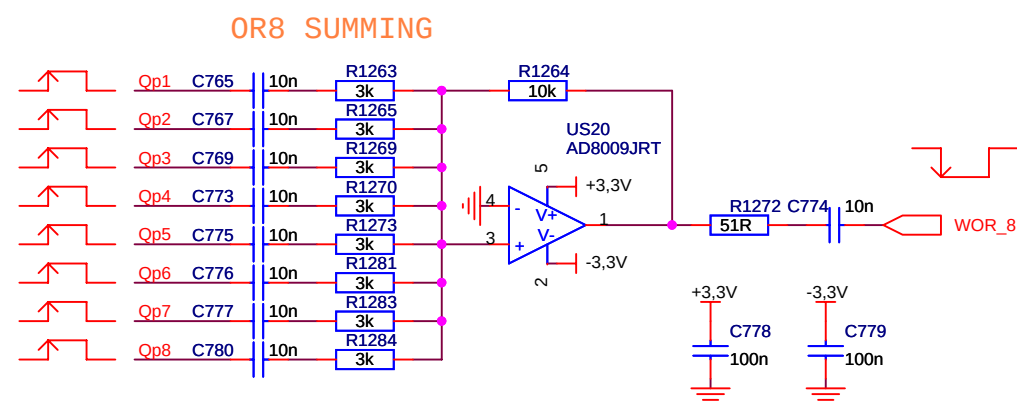


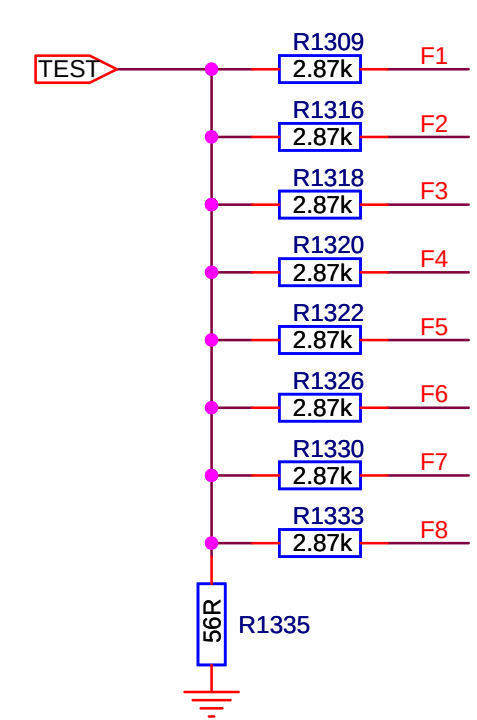
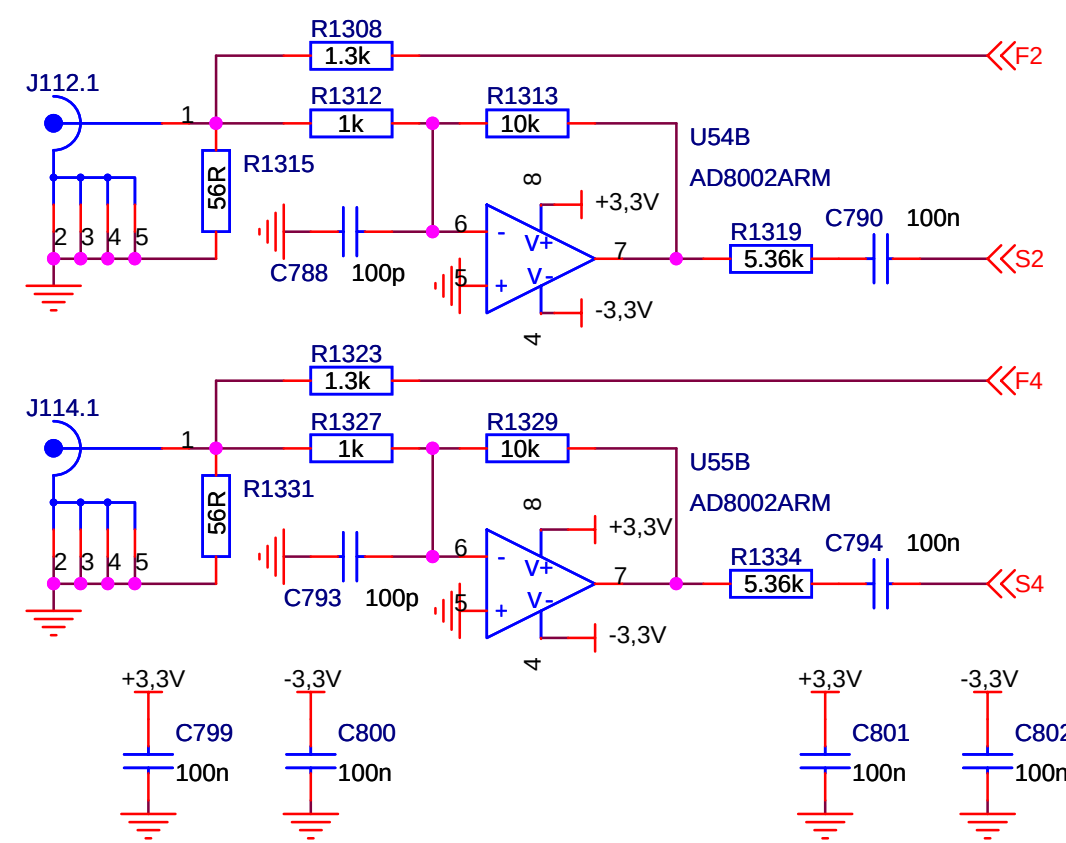
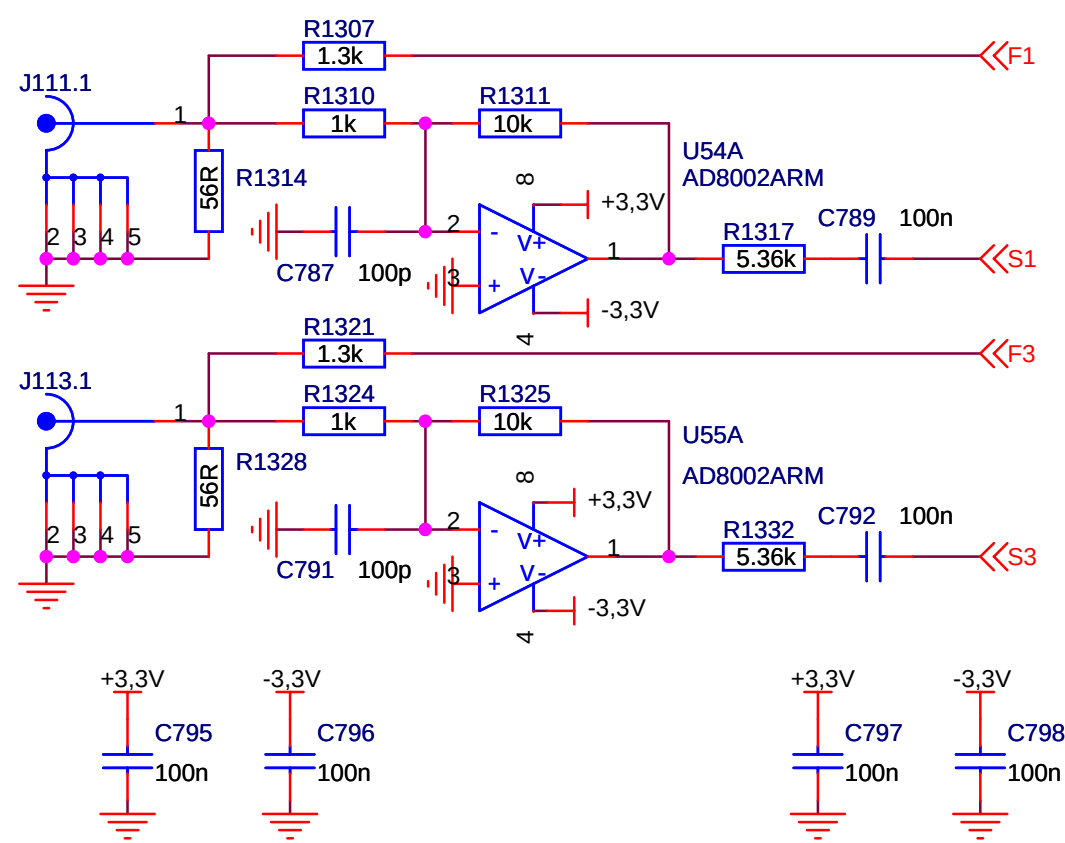










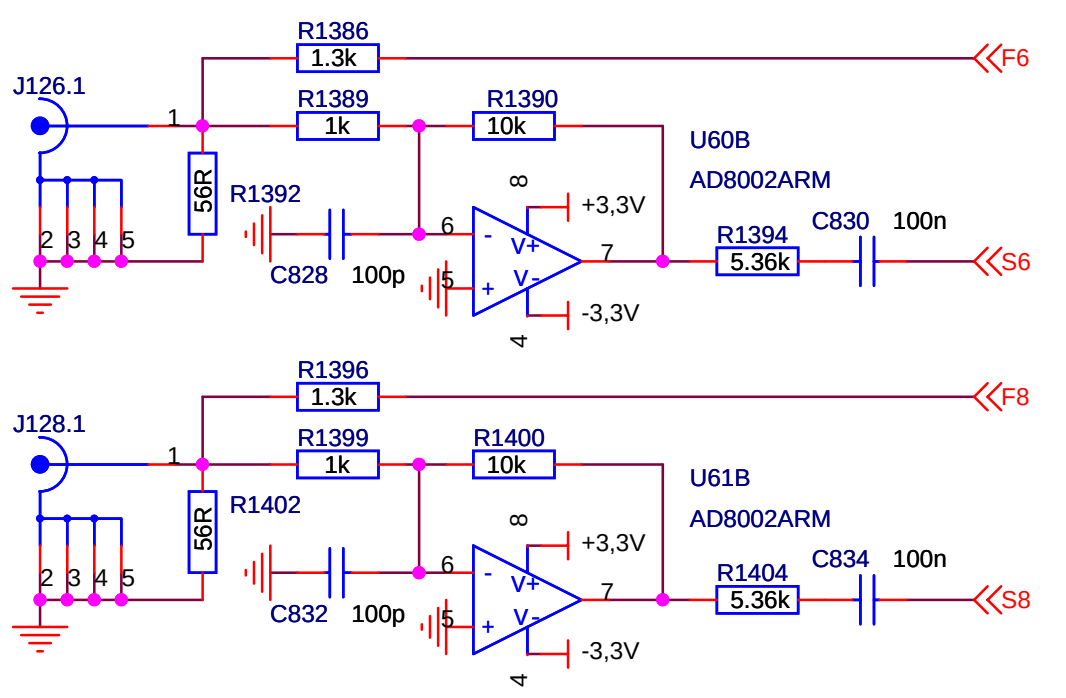
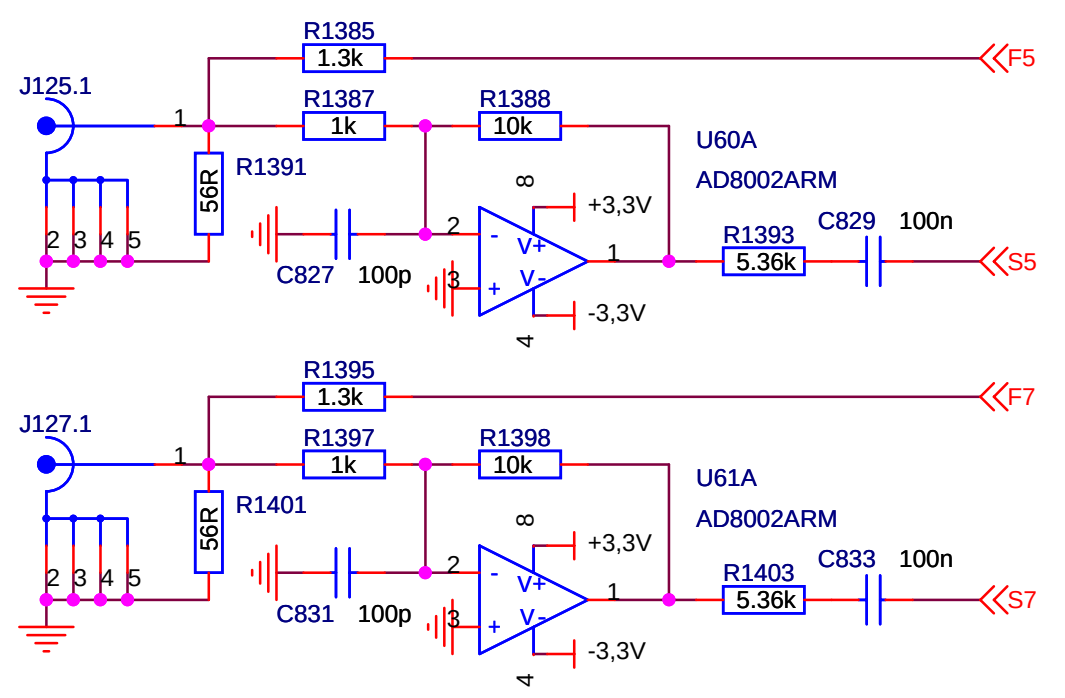
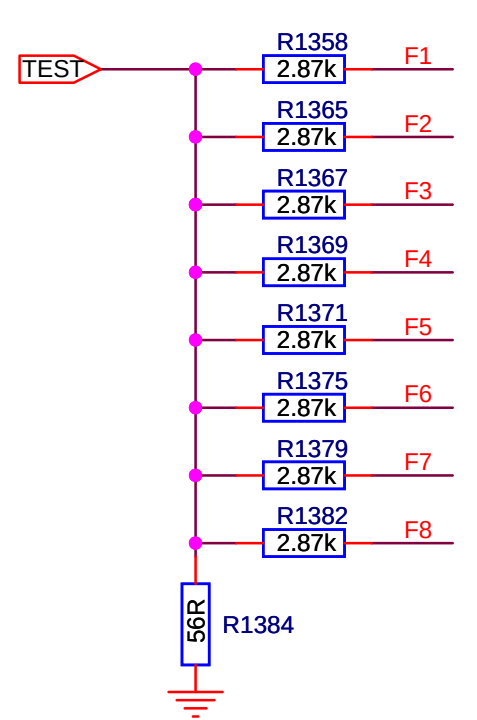
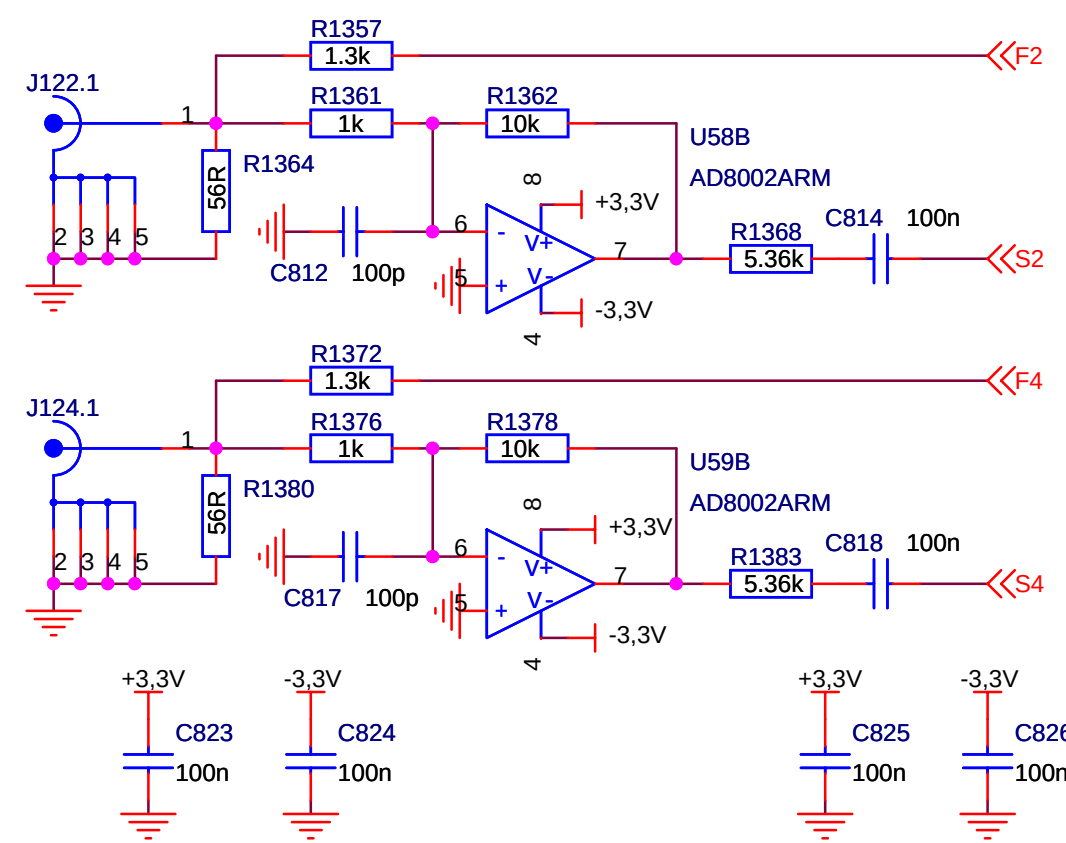
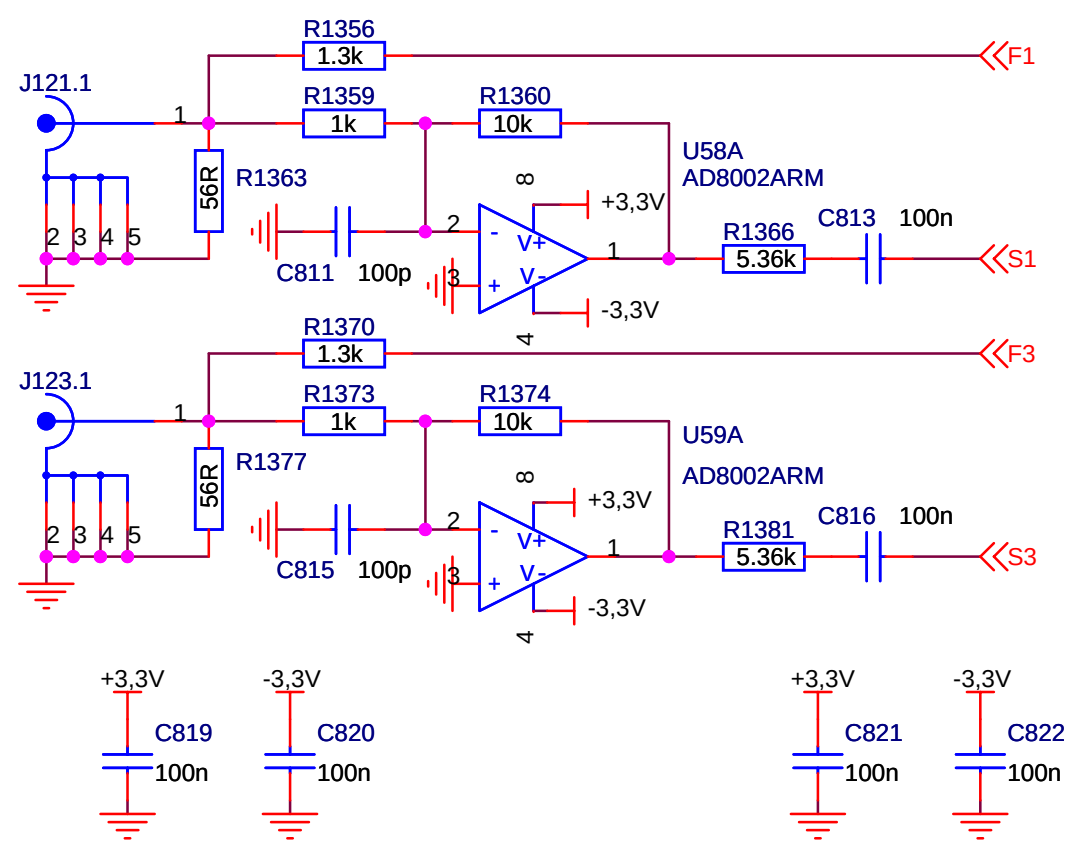




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Designer: <Designer>	Layouter: <Layouter>

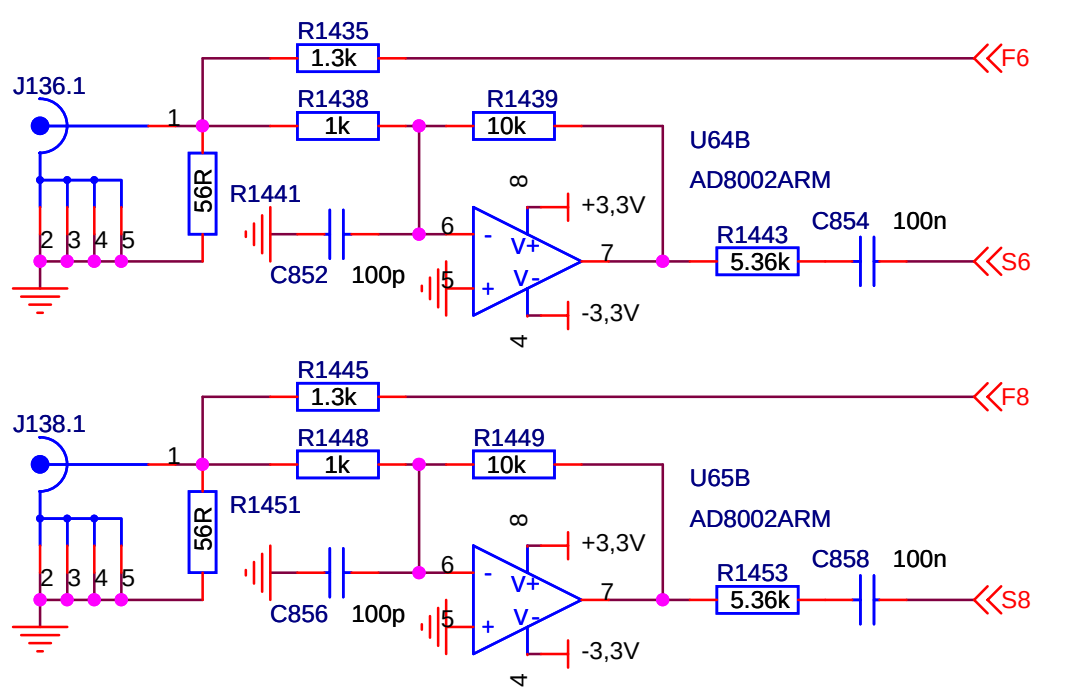
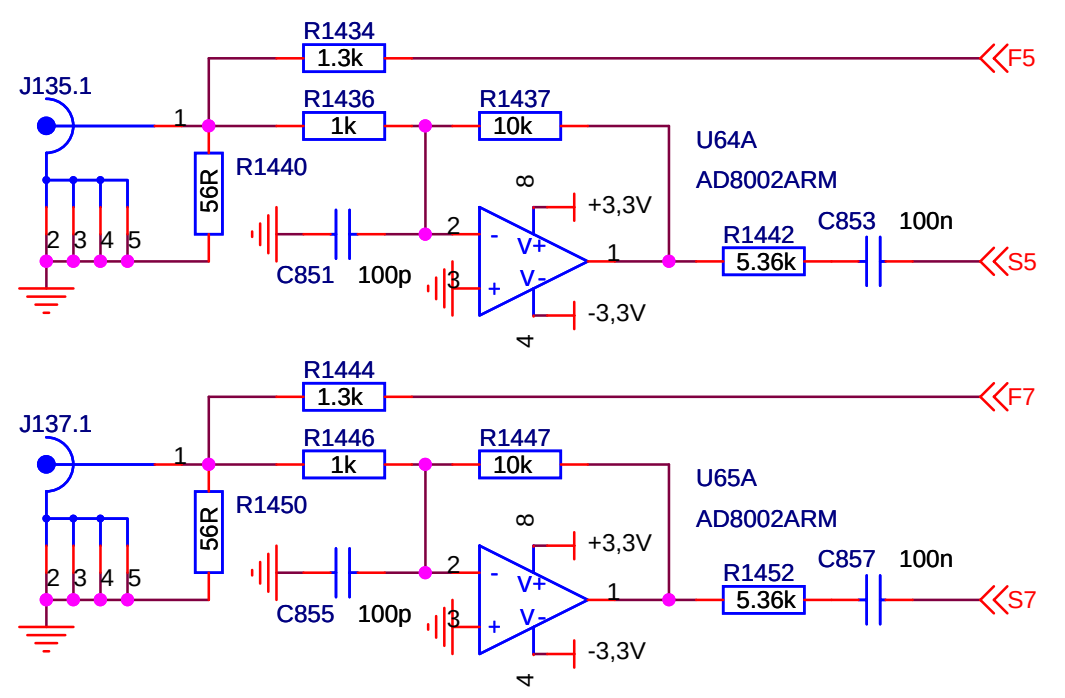
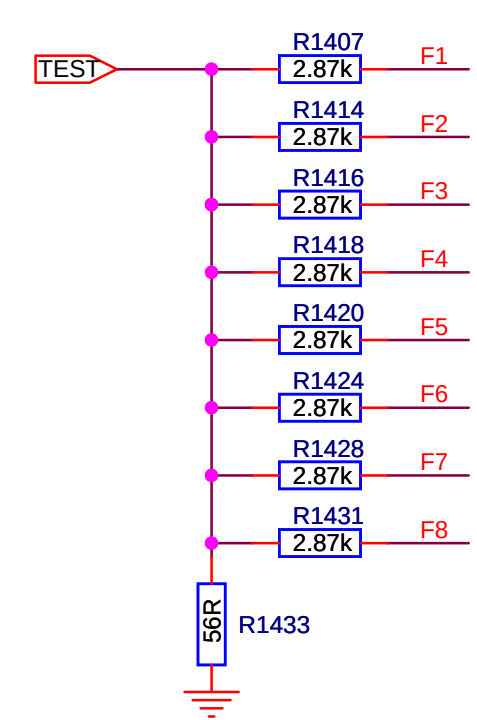
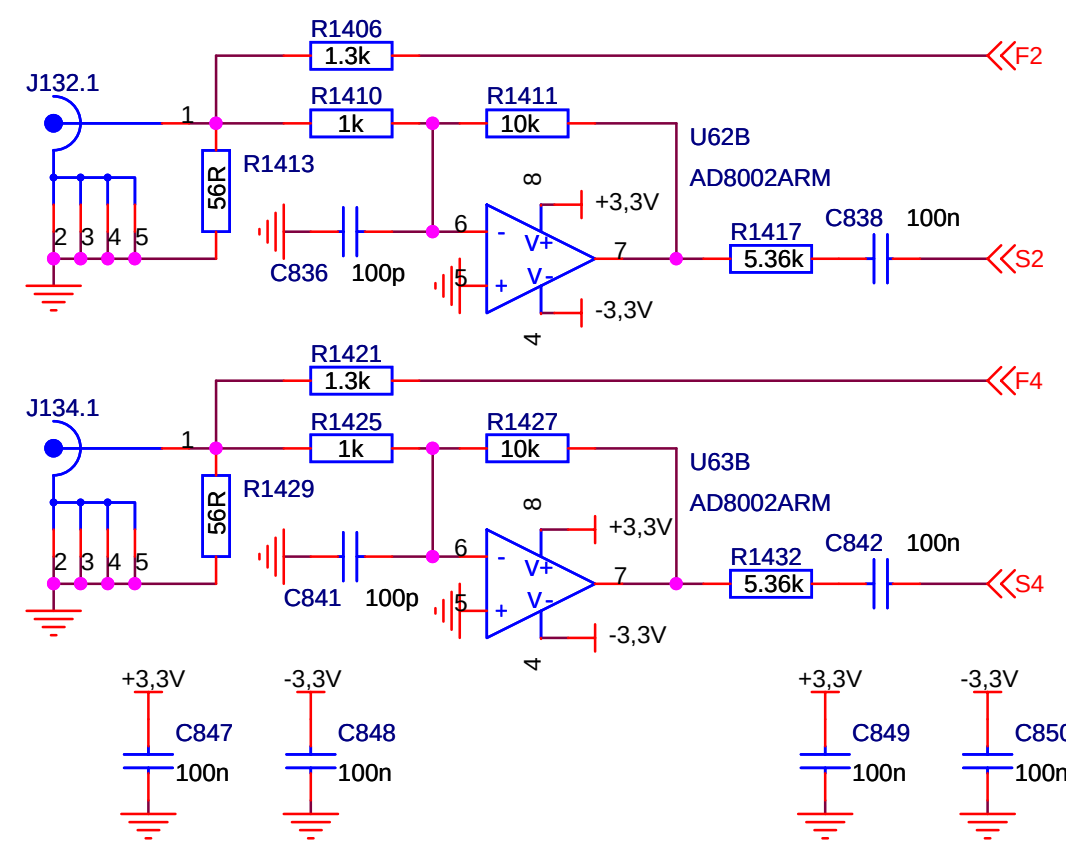
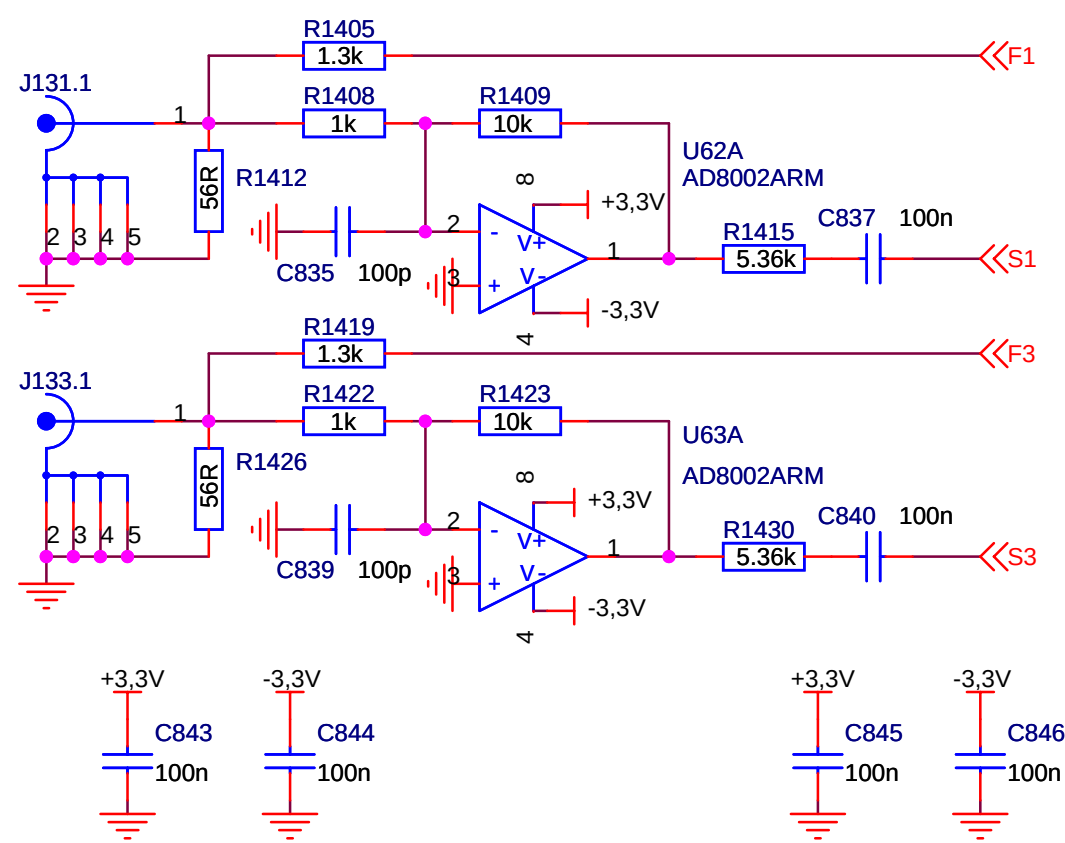




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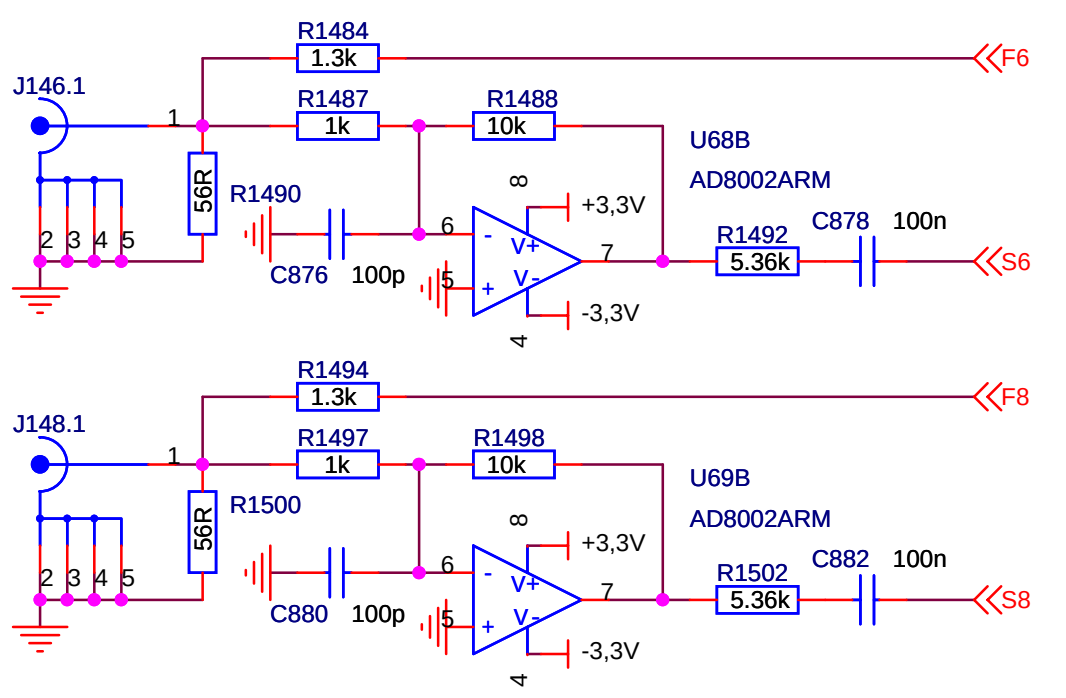
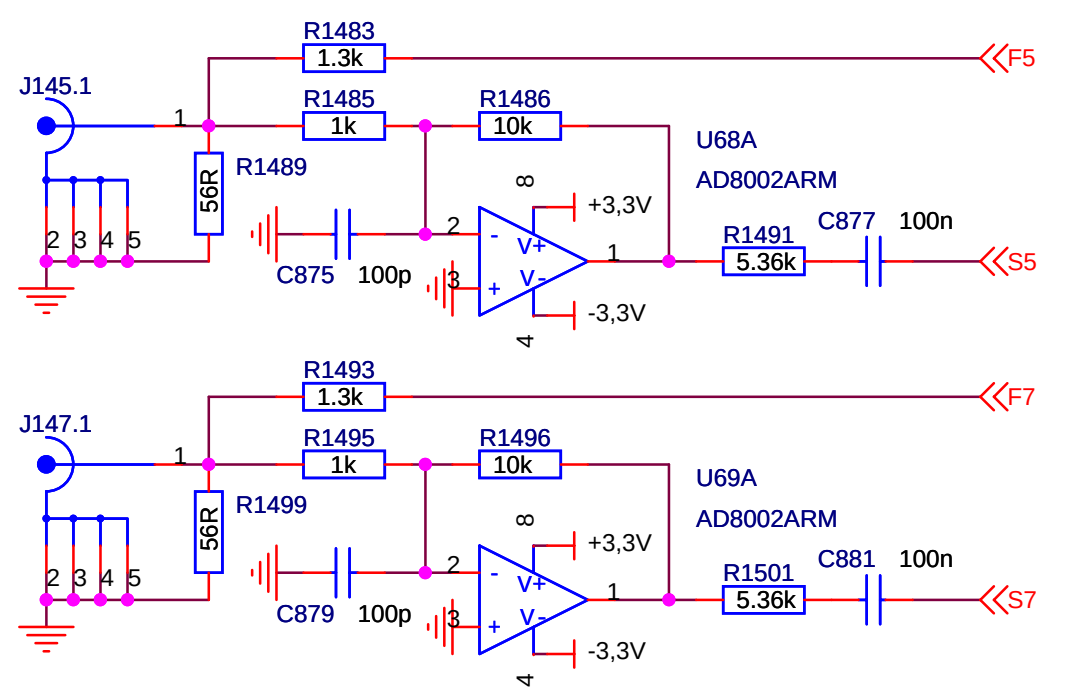
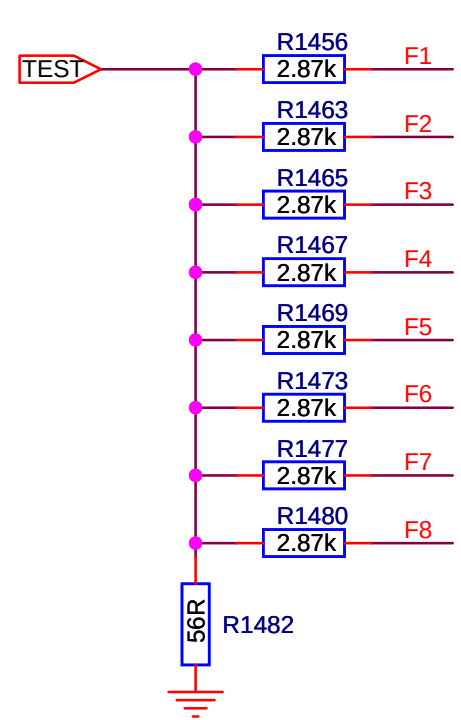
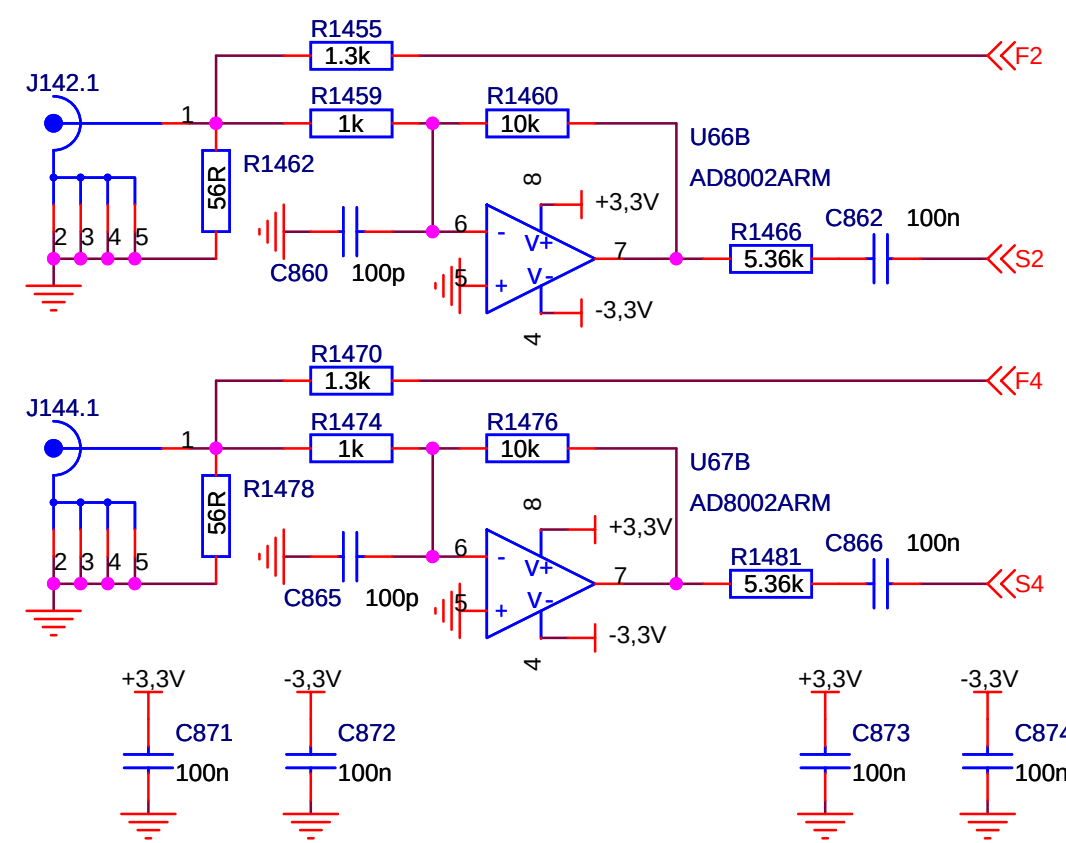
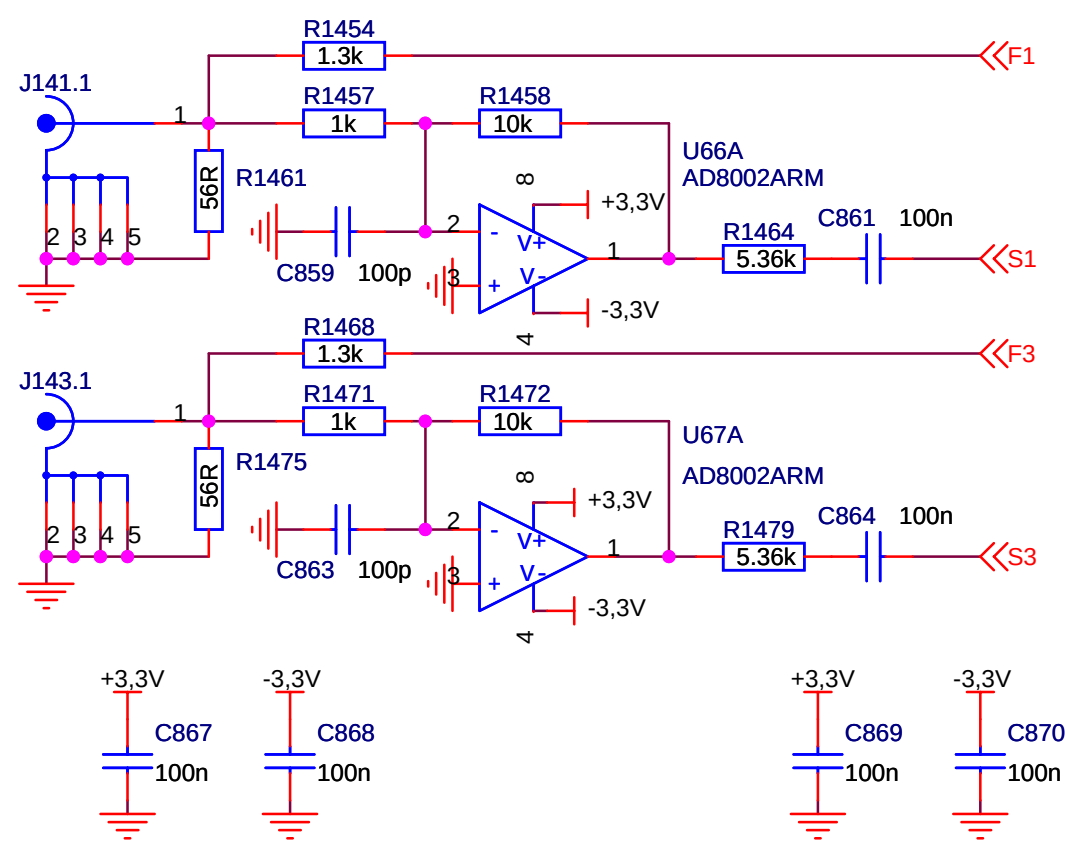




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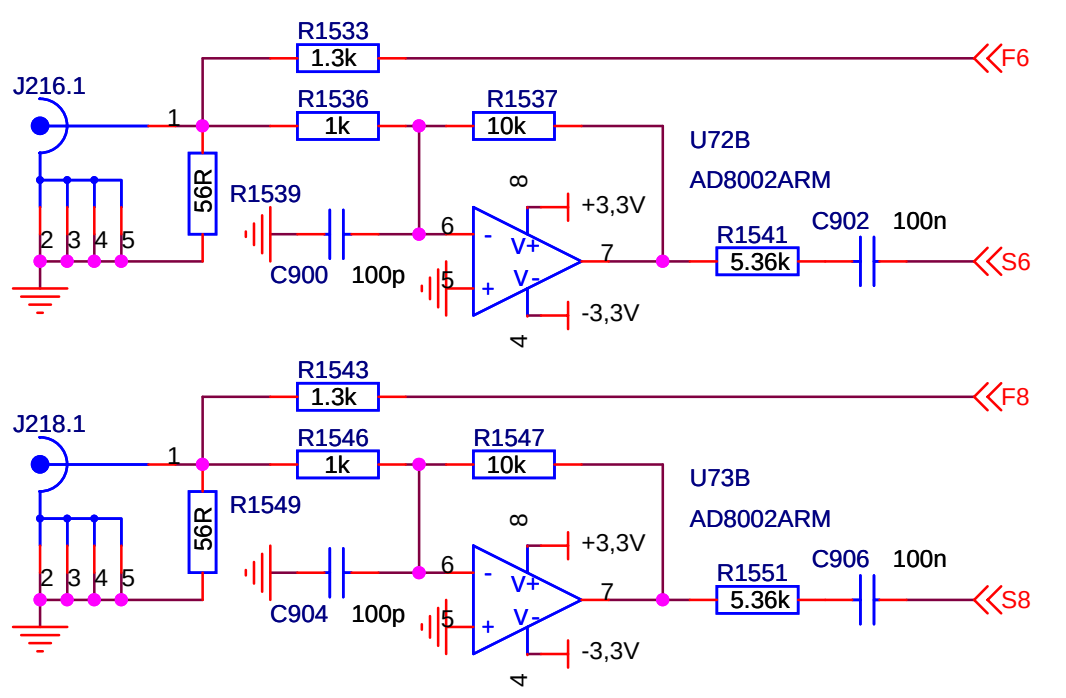
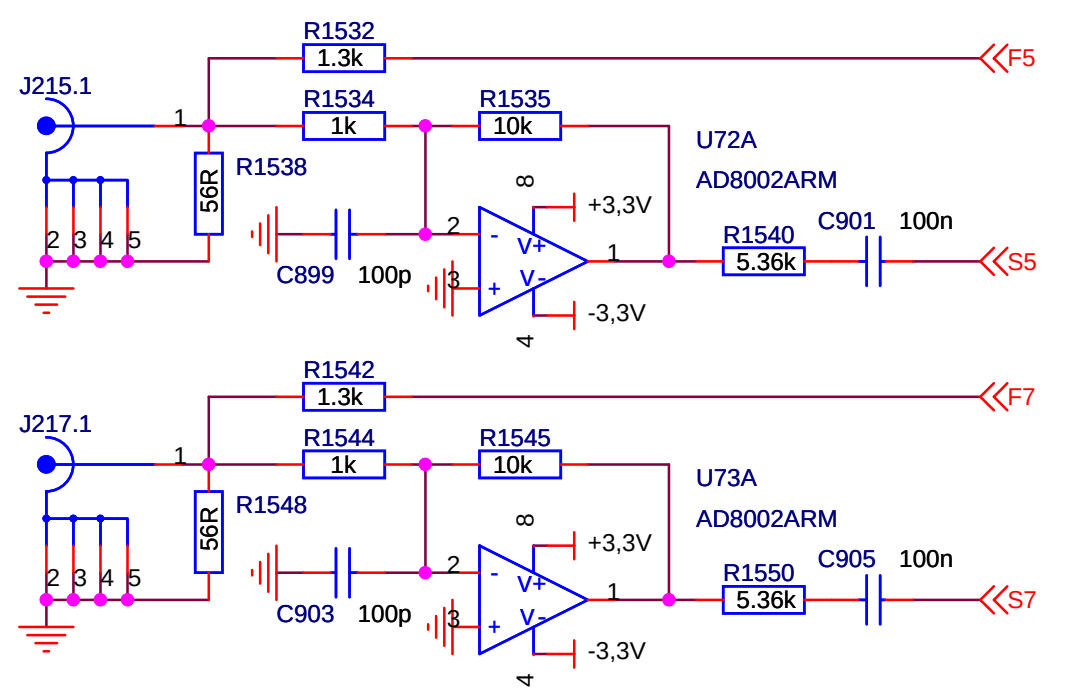
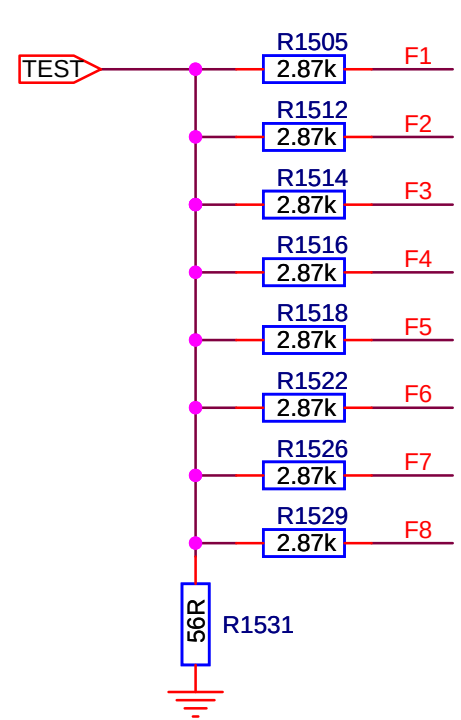
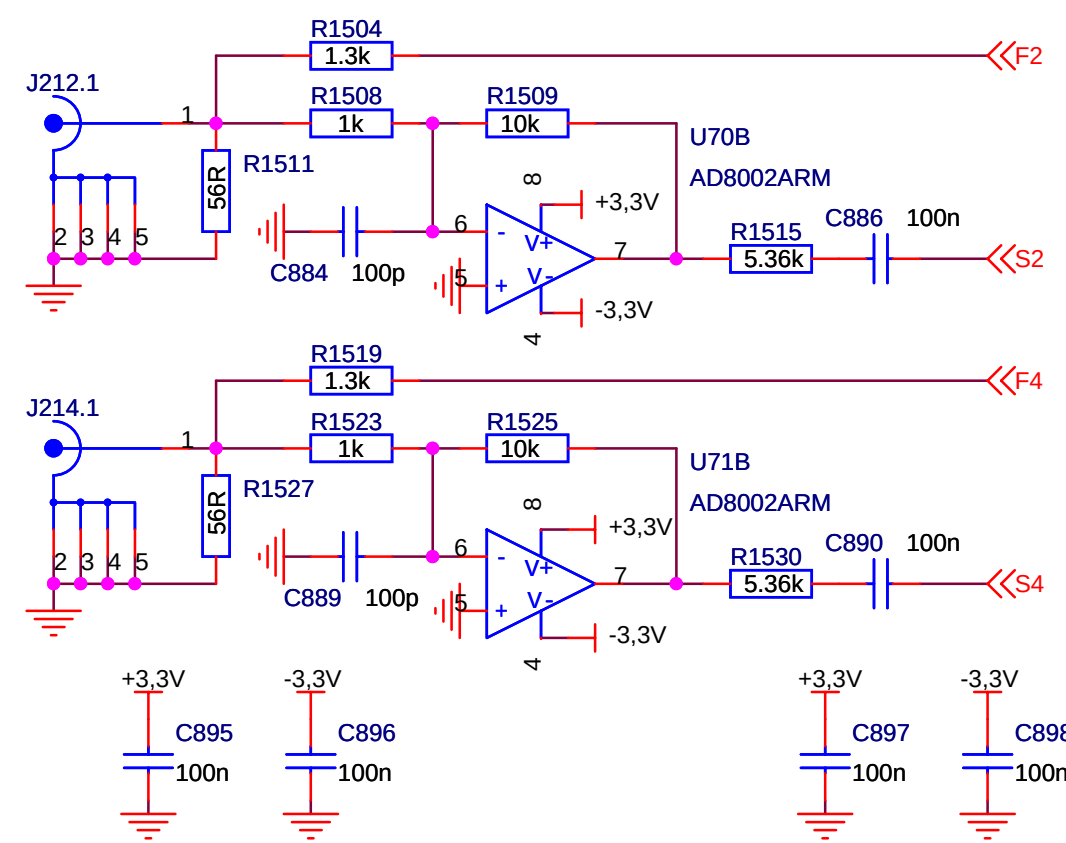
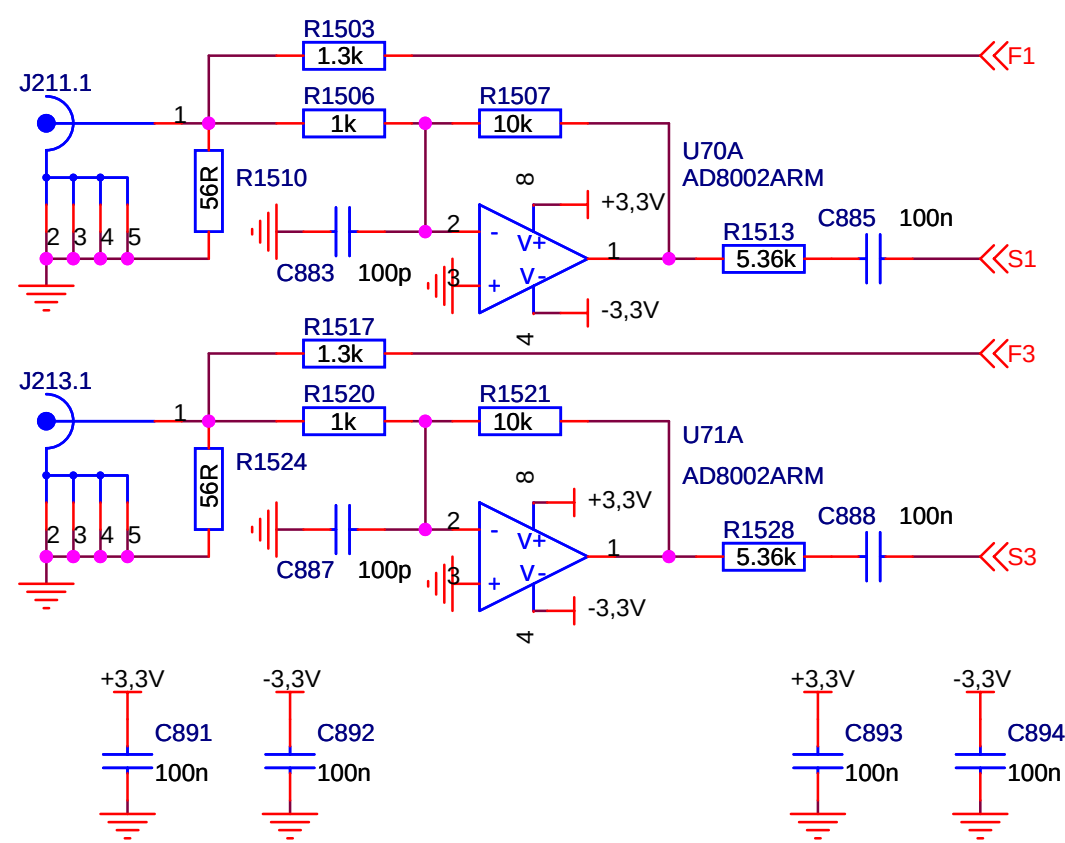




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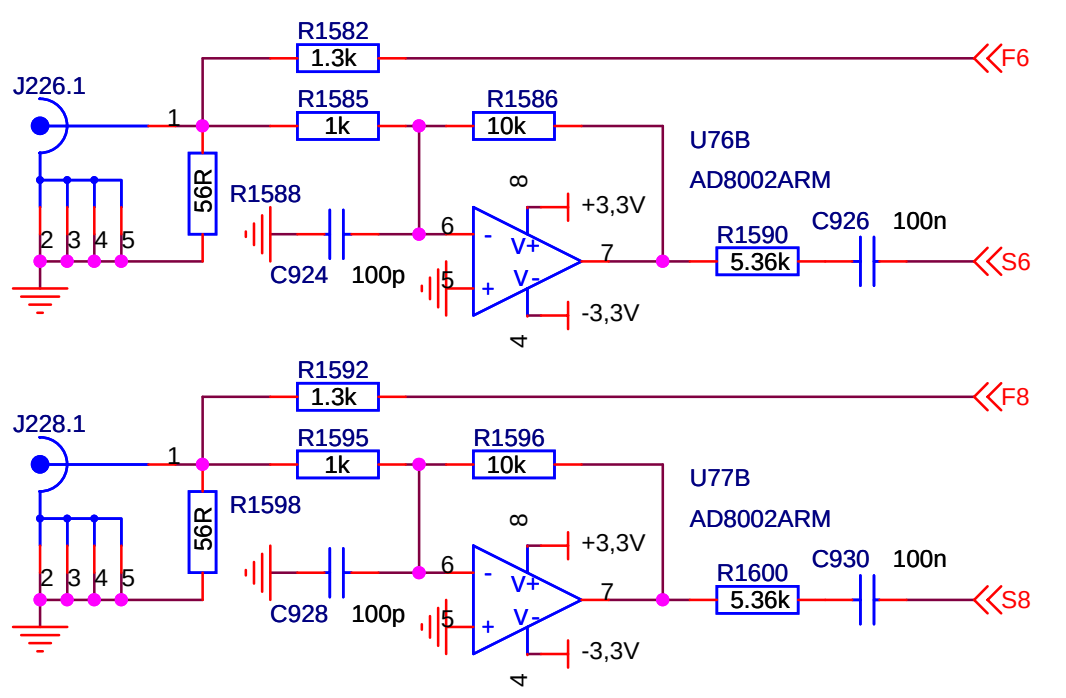
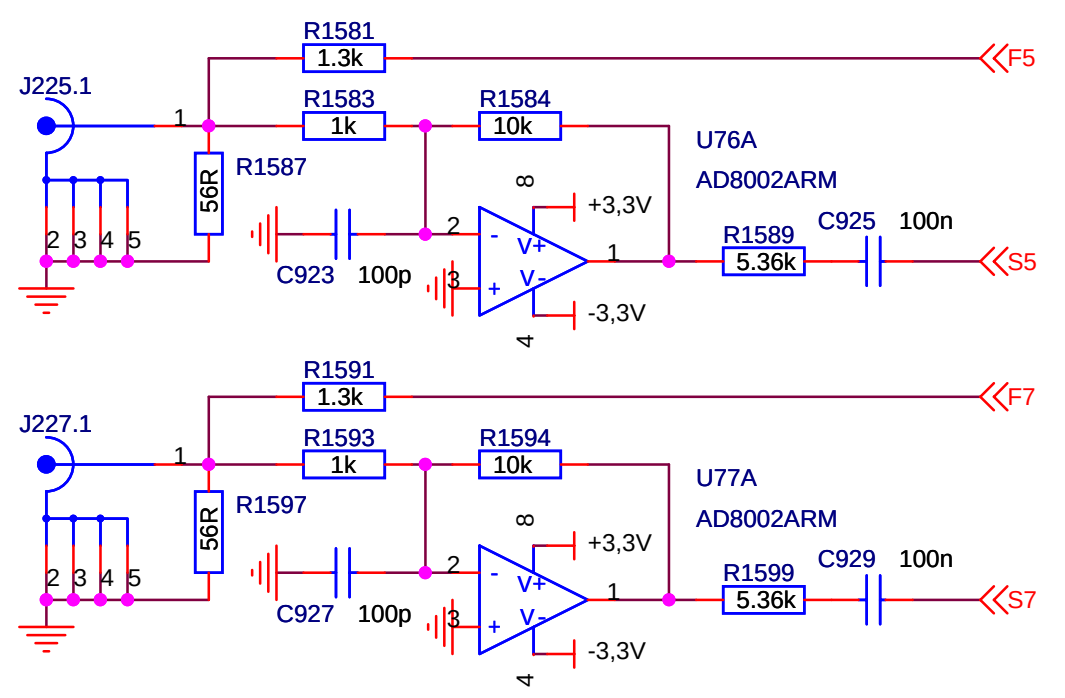
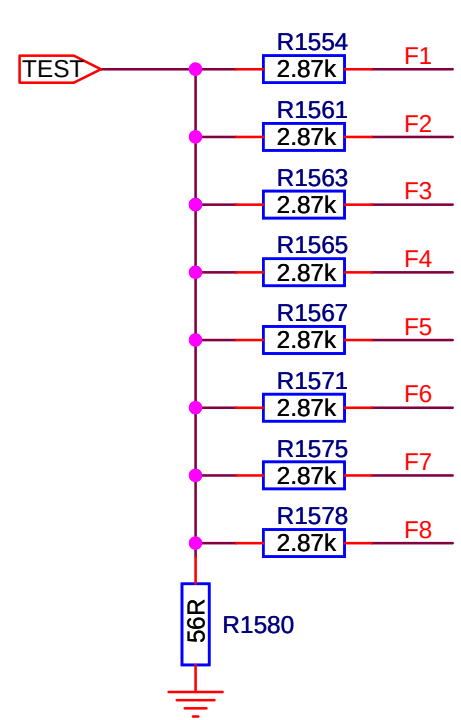
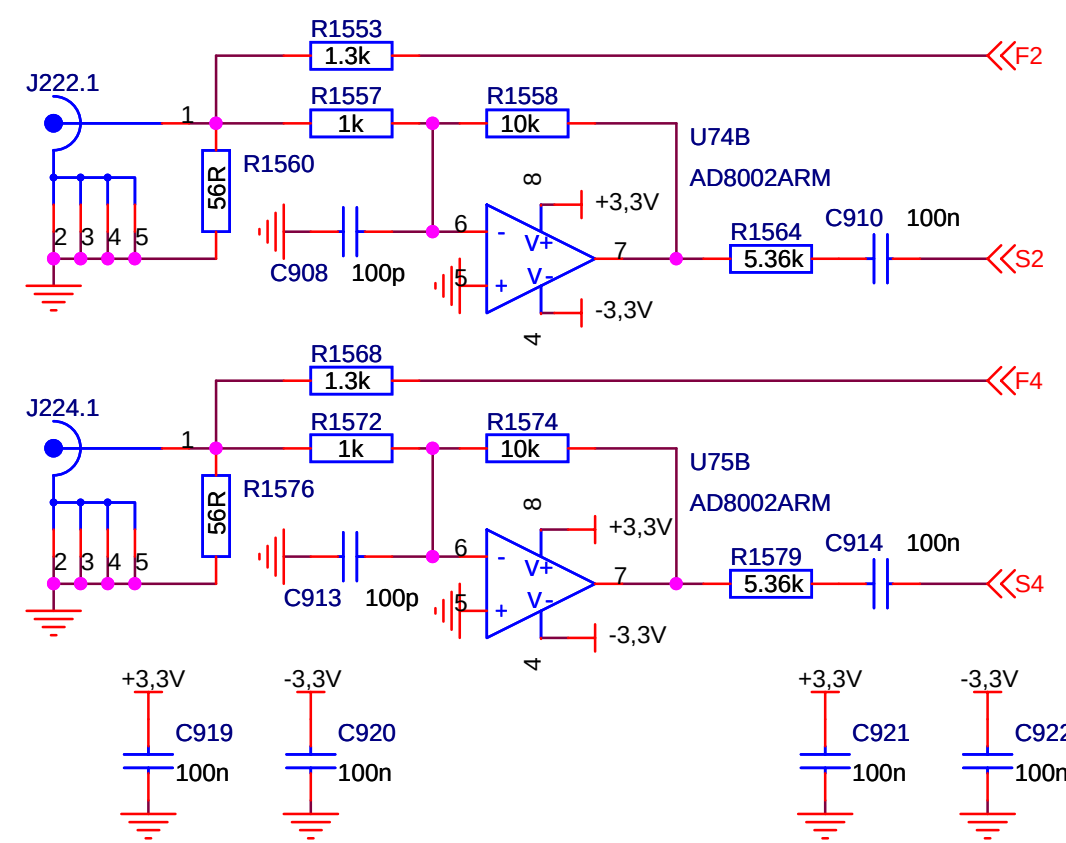
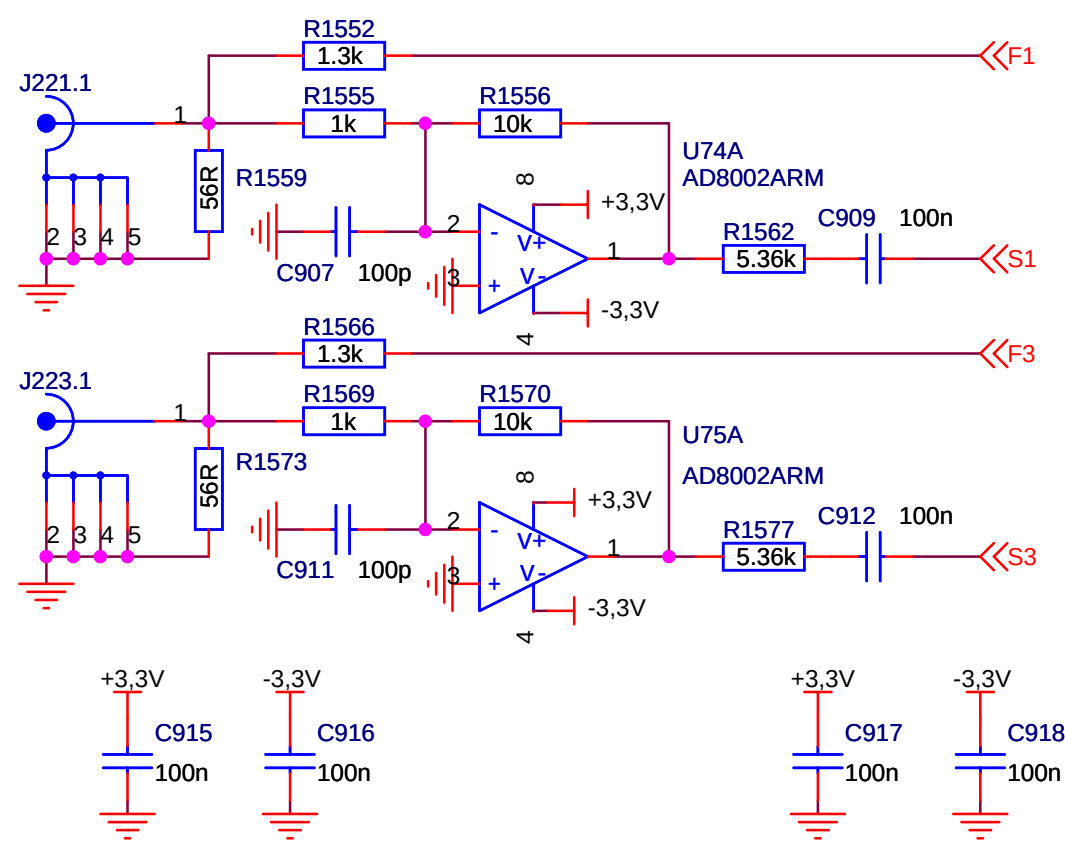
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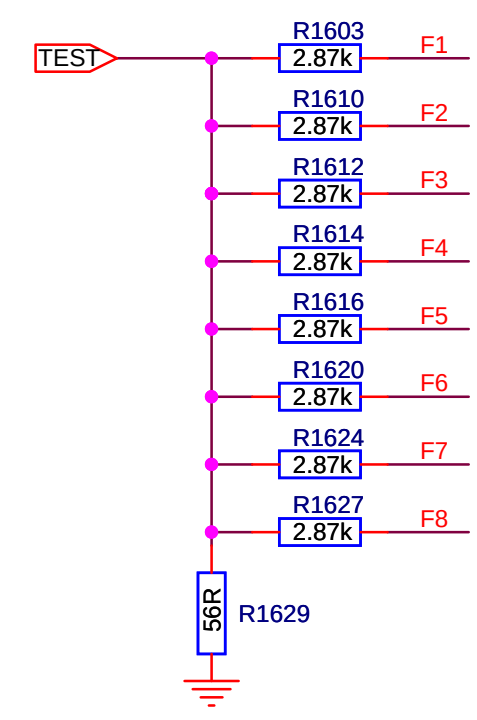
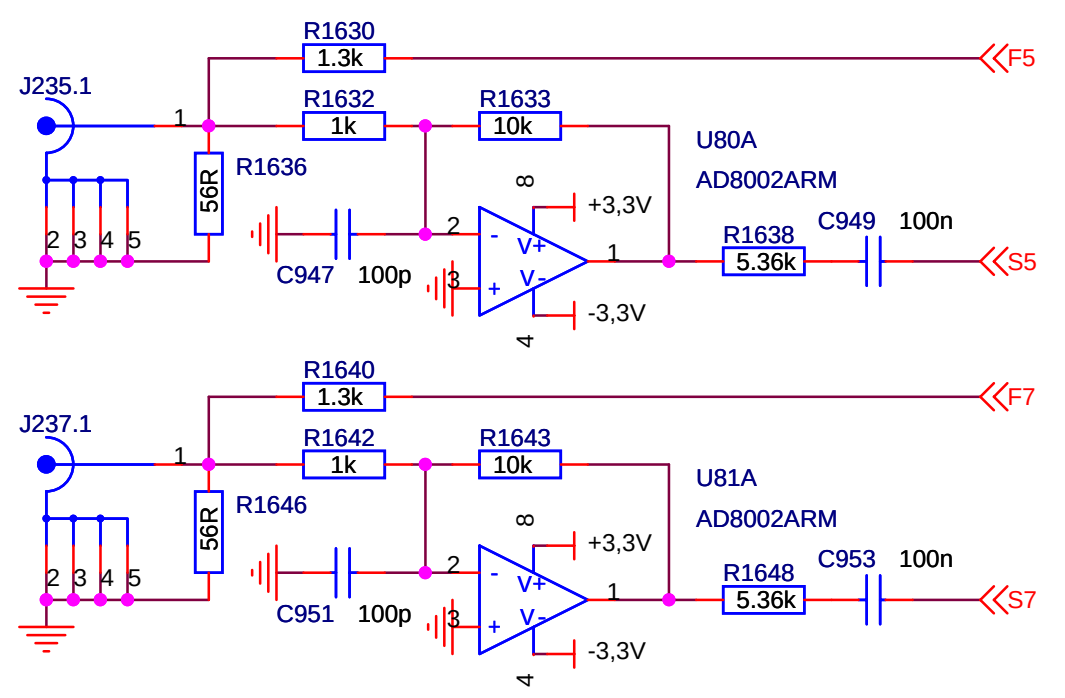
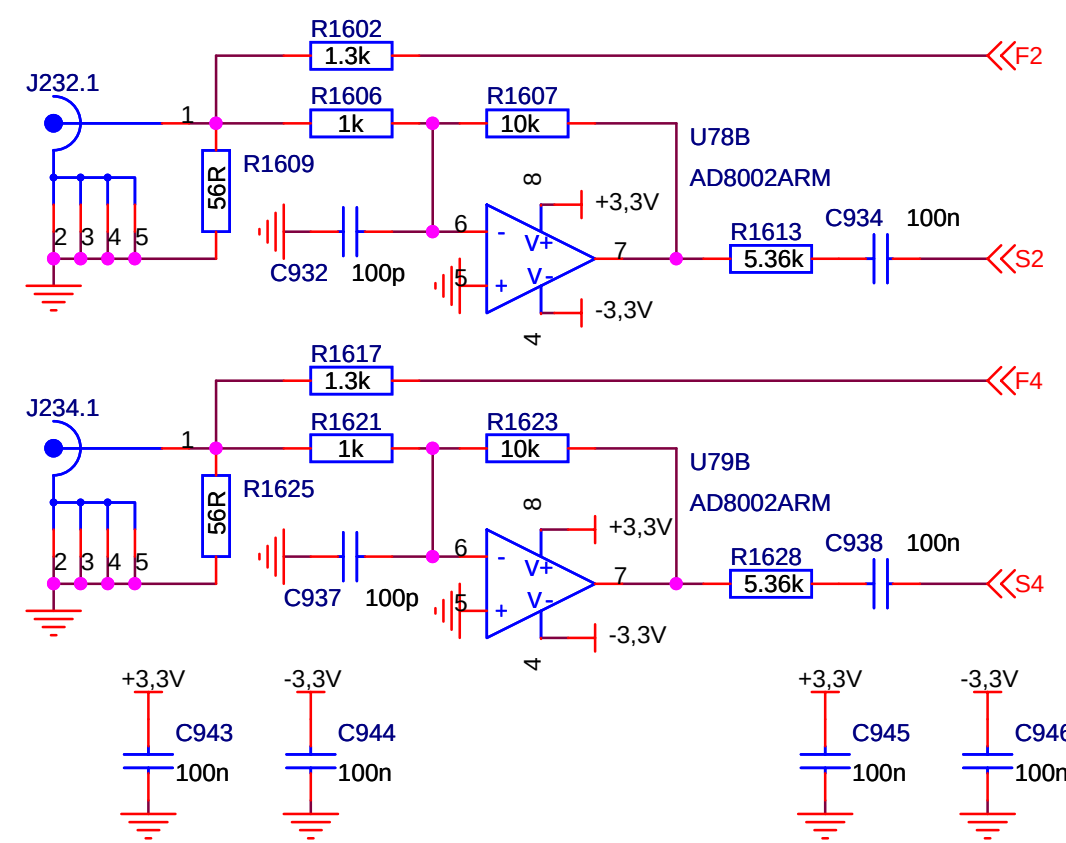
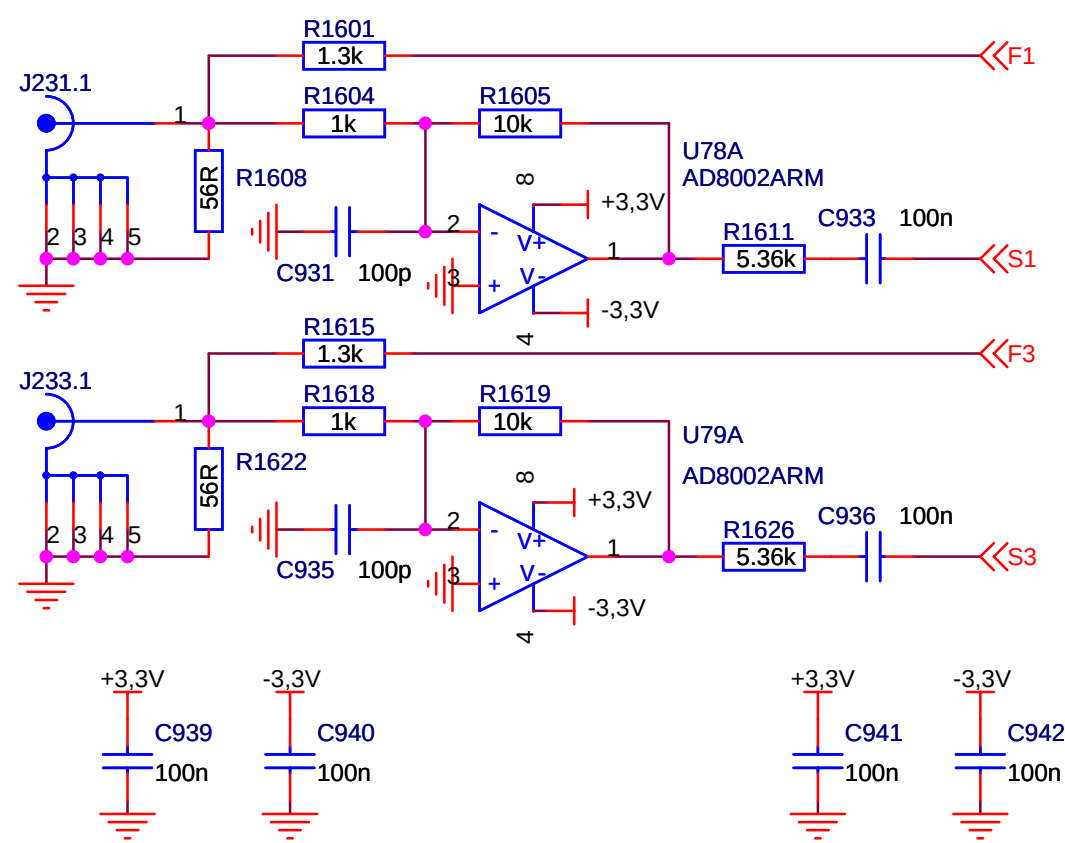
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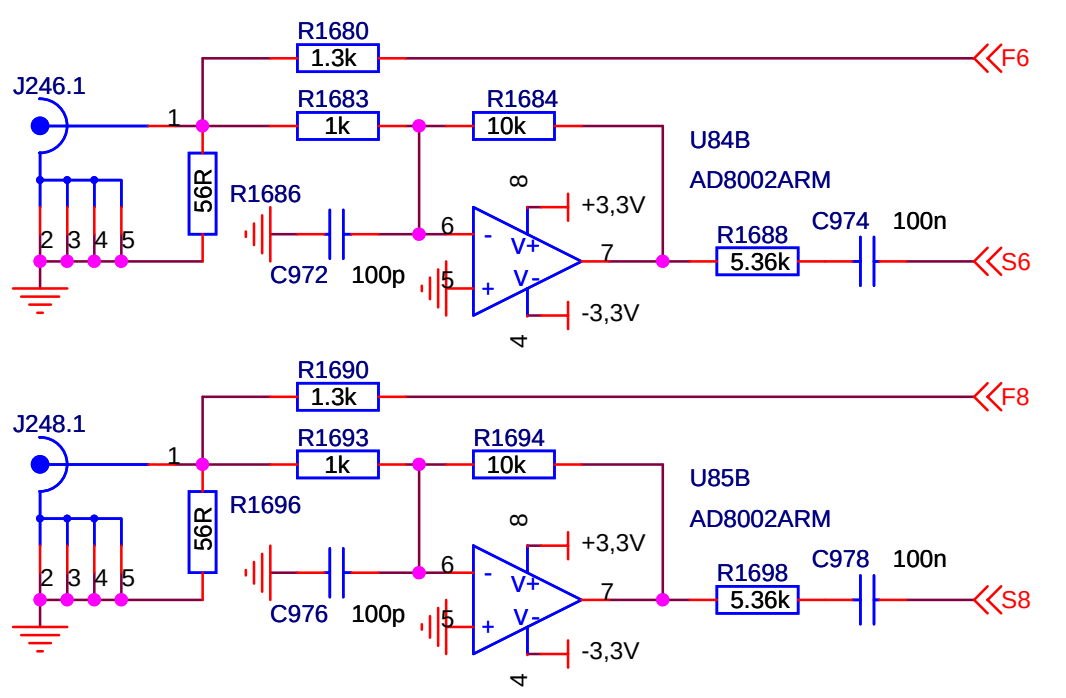
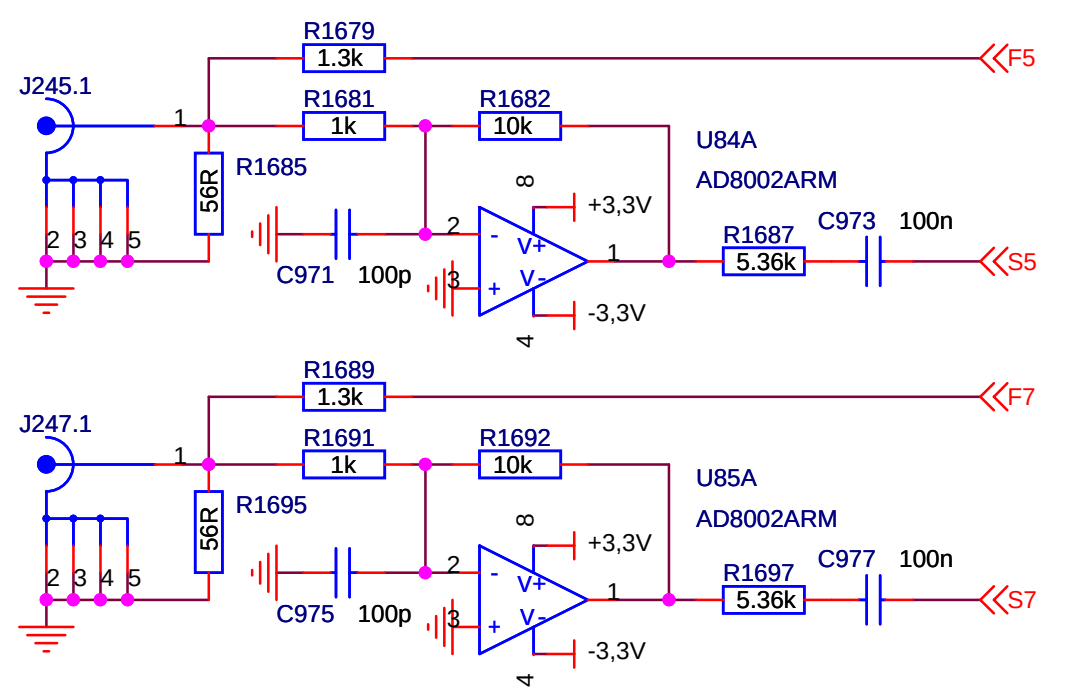
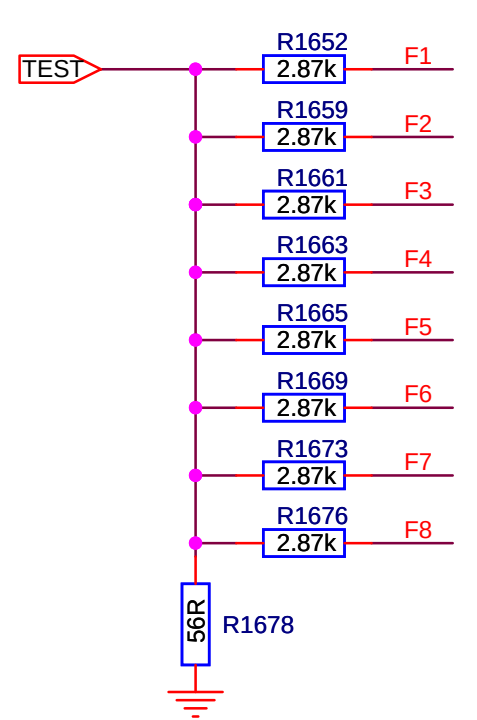
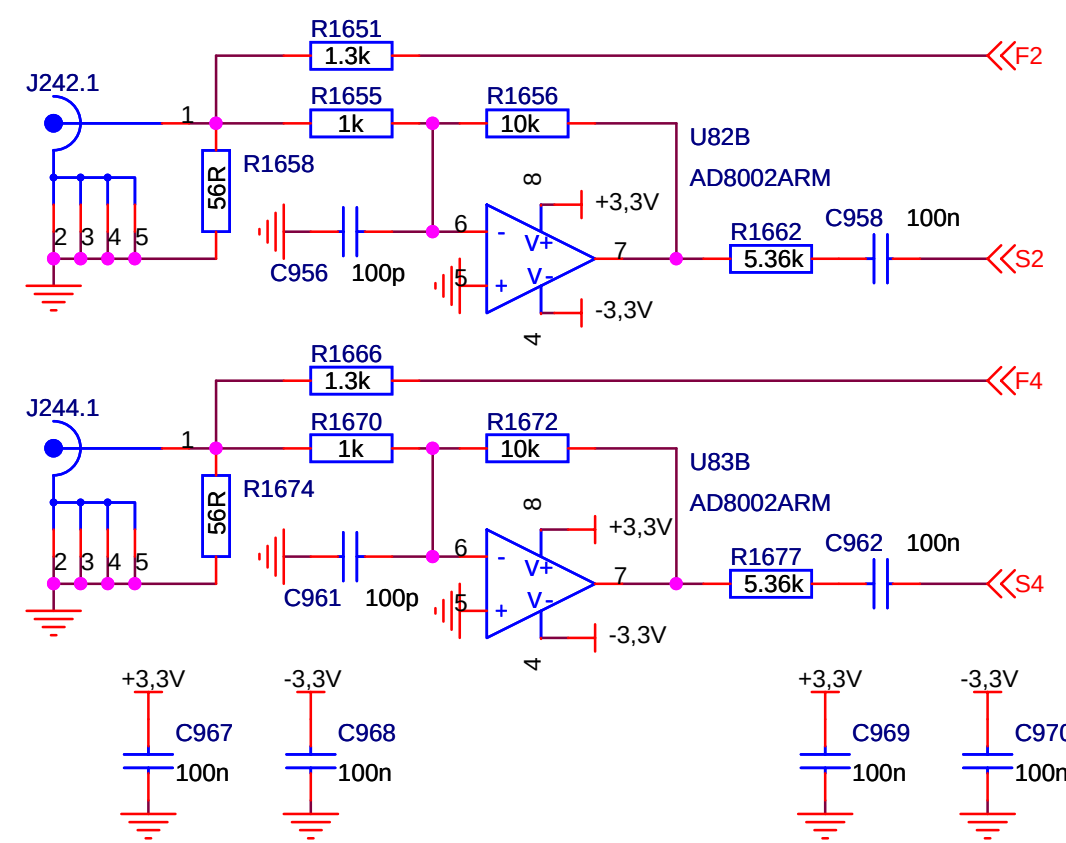
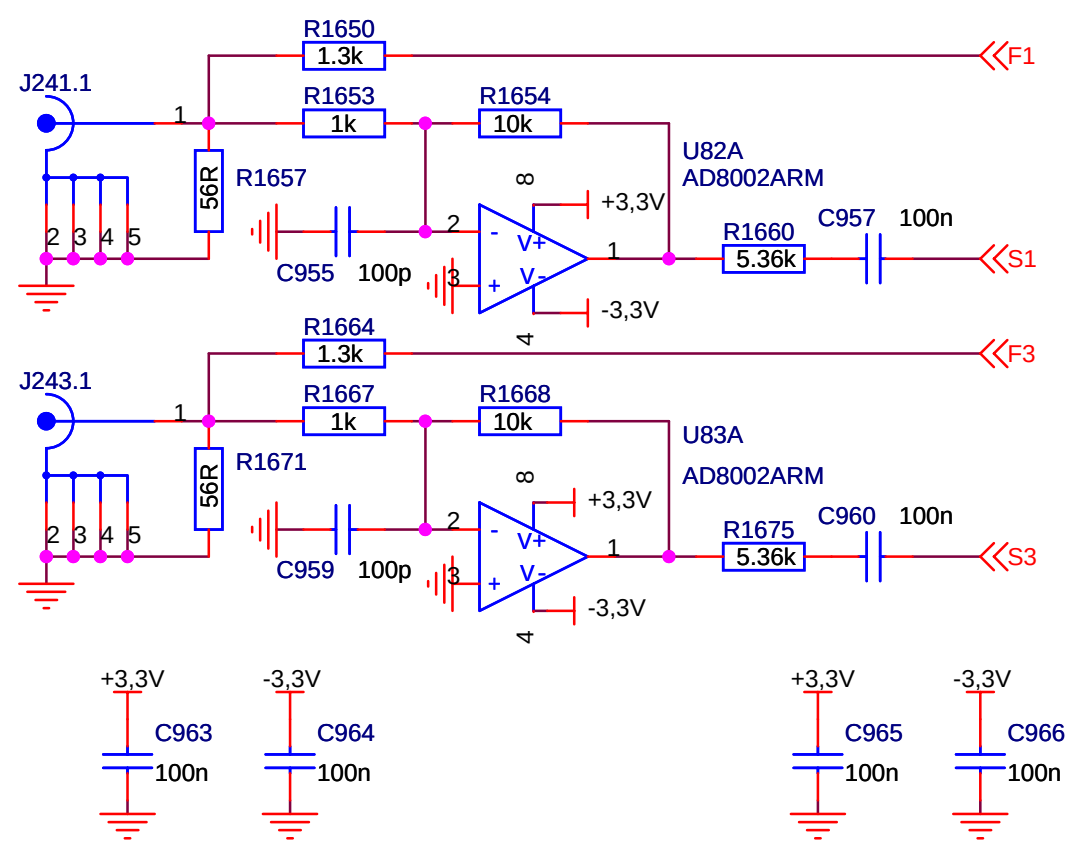




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Designer: <Designer>	Layouter: <Layouter>

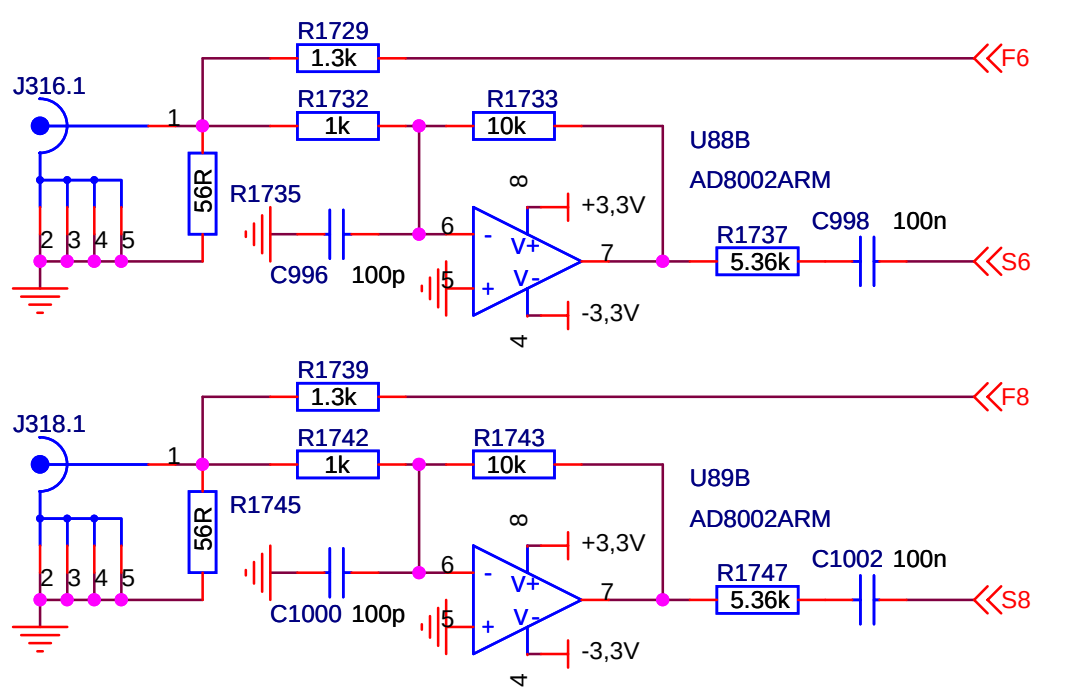
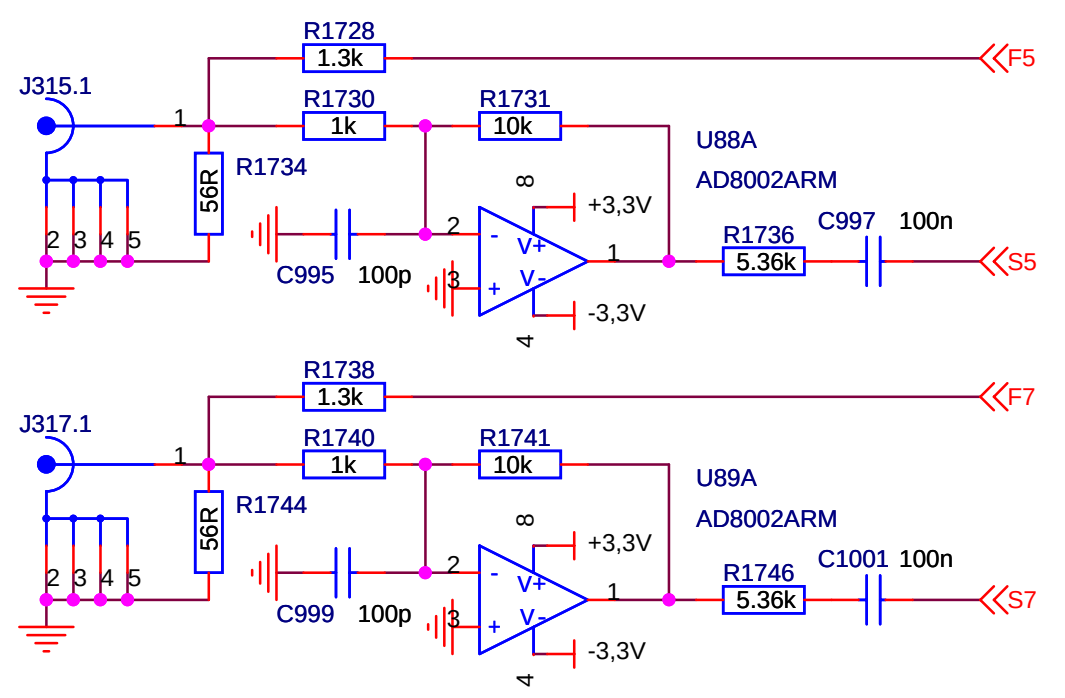
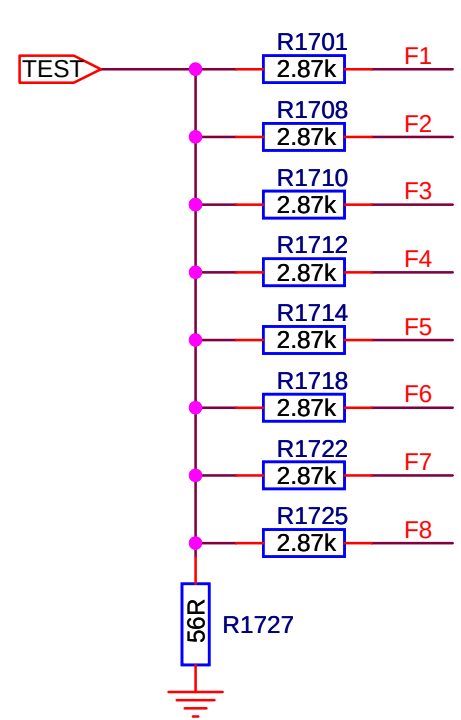
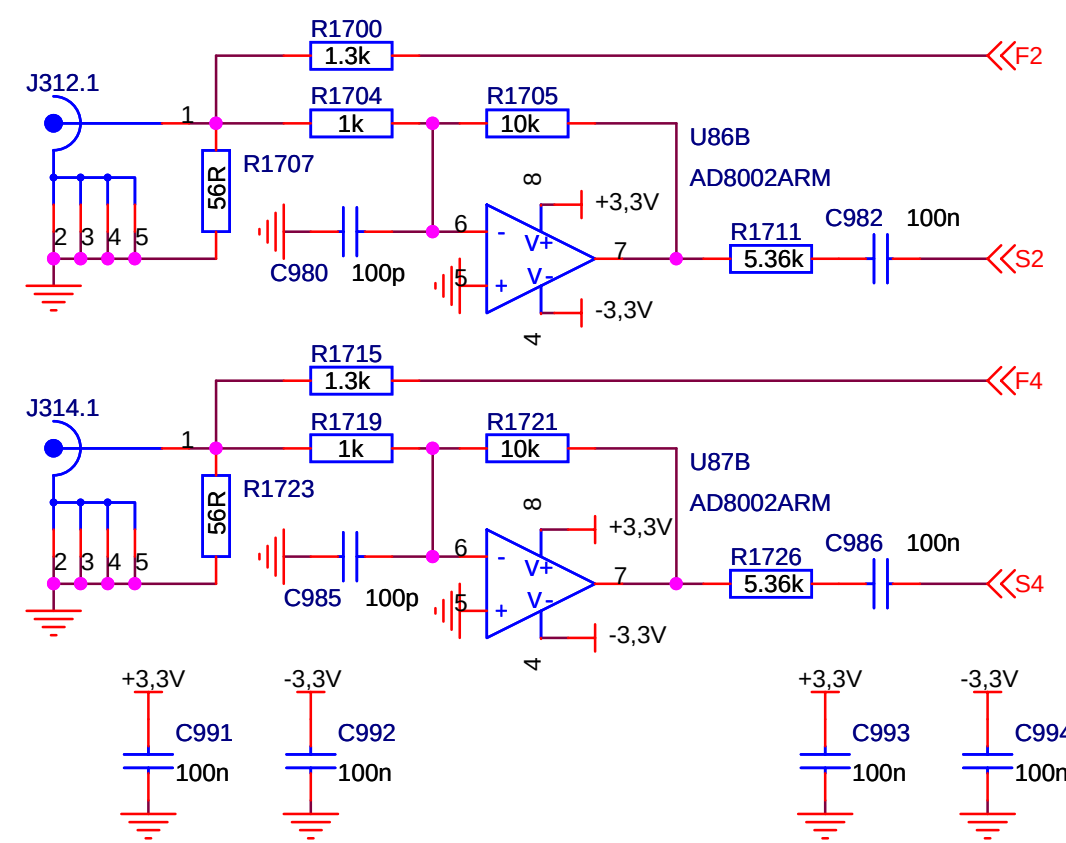
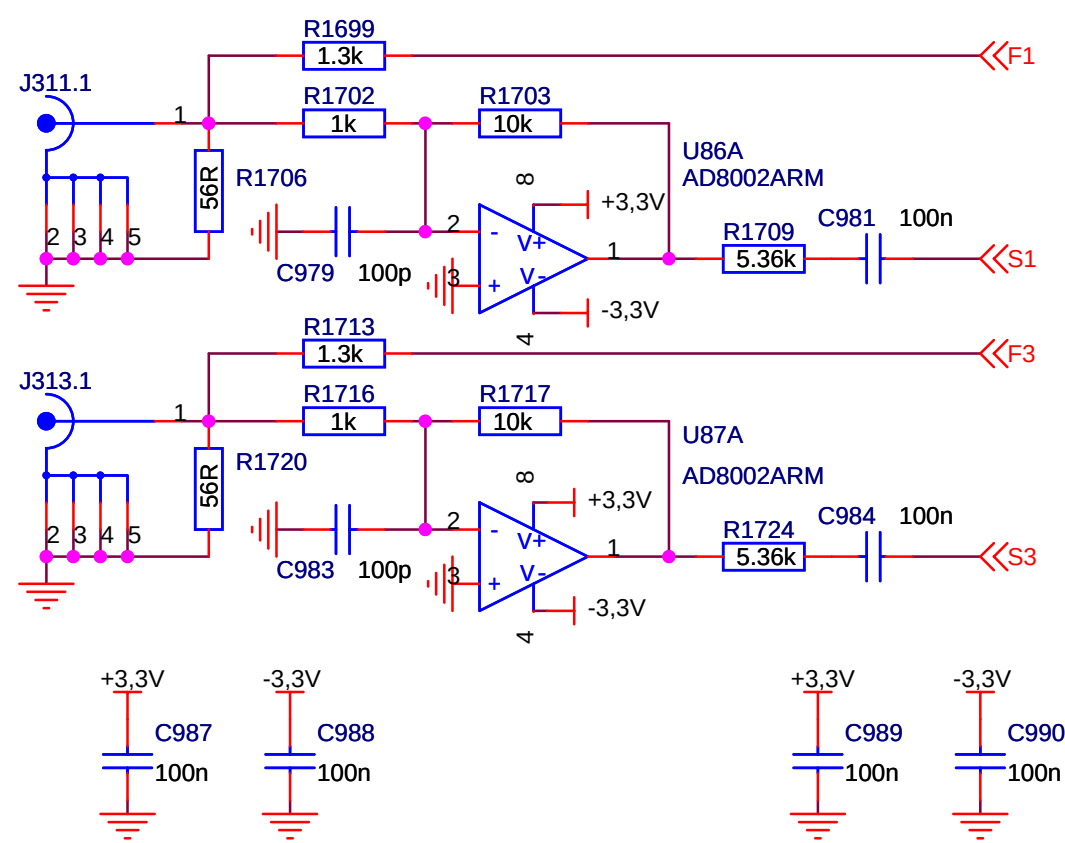




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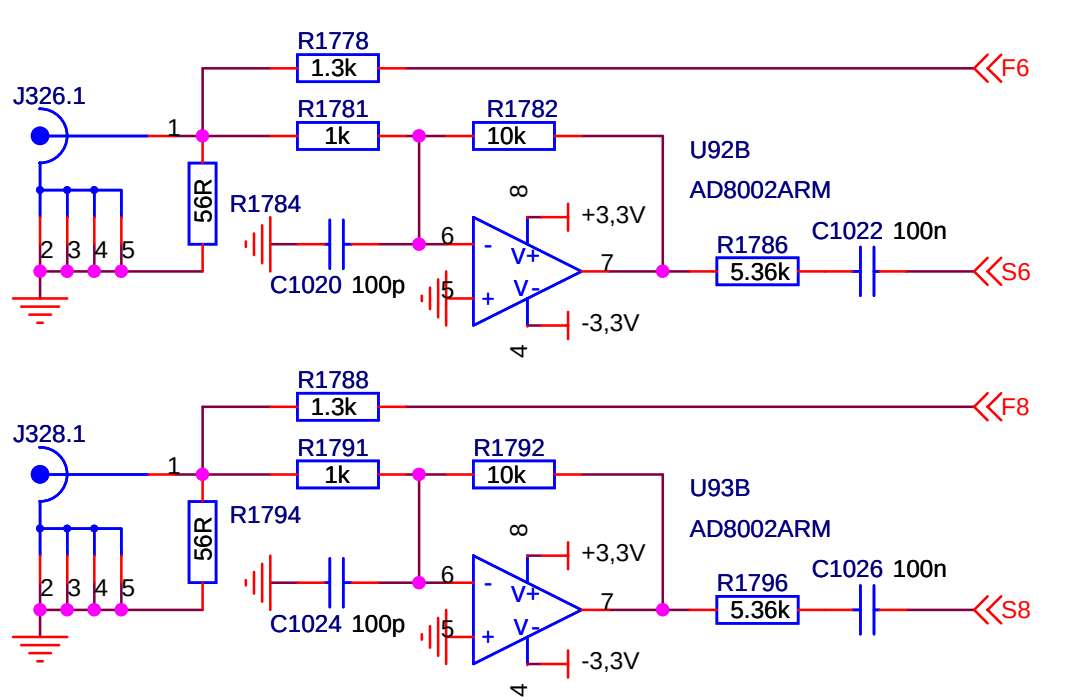
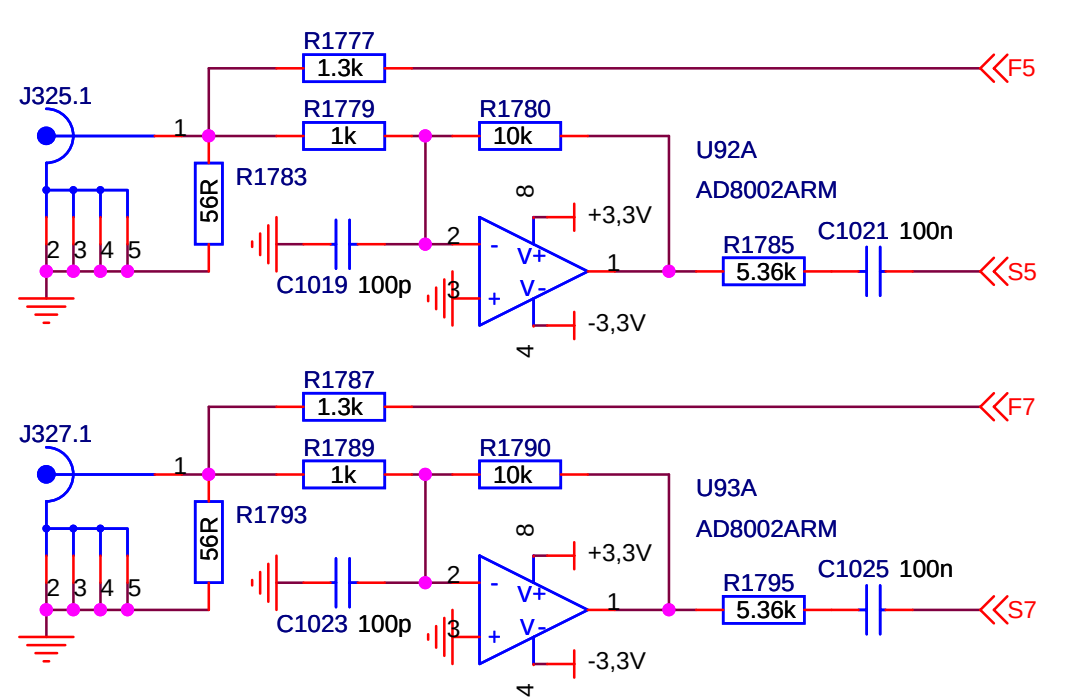
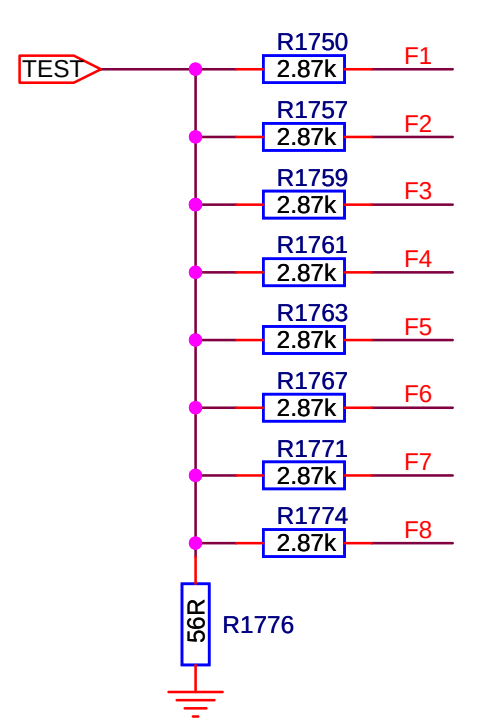
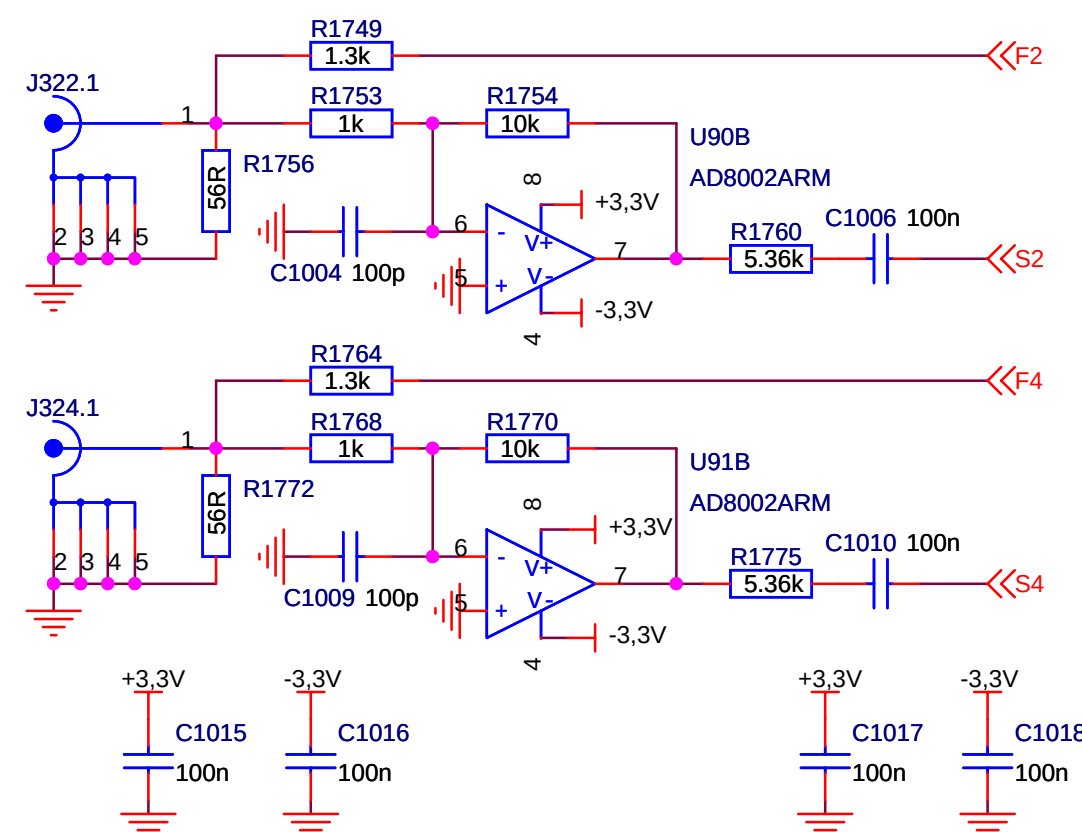
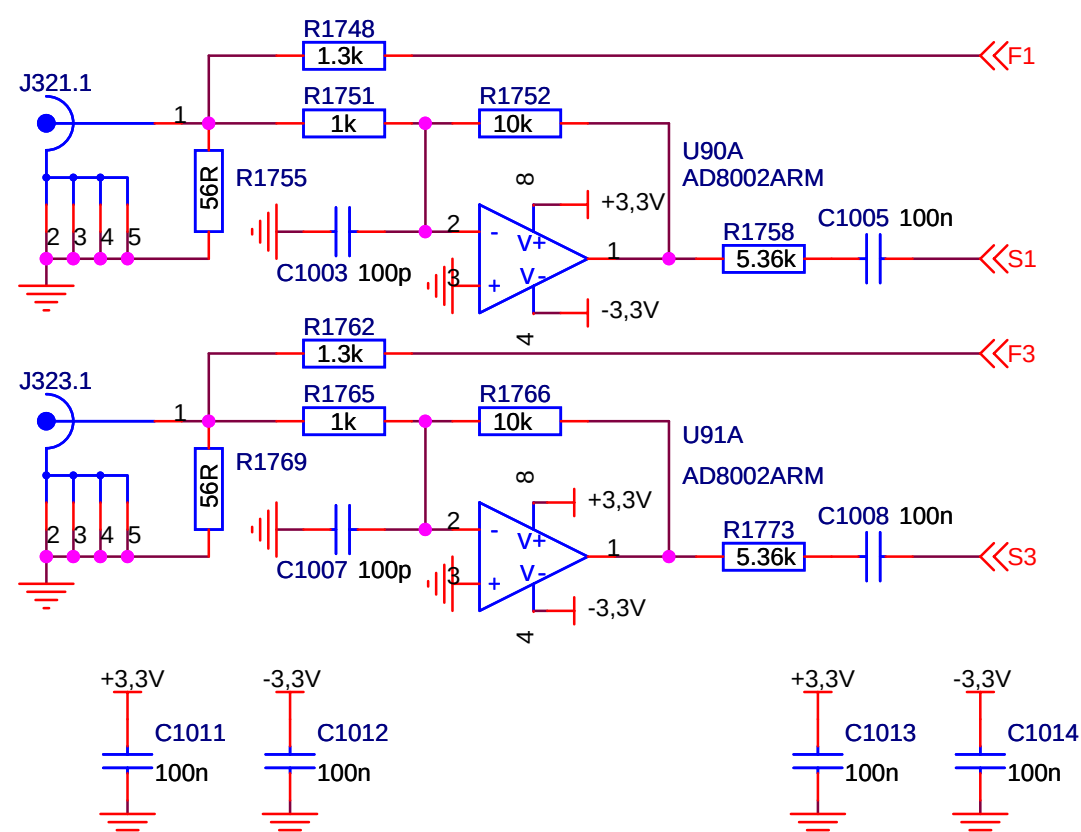




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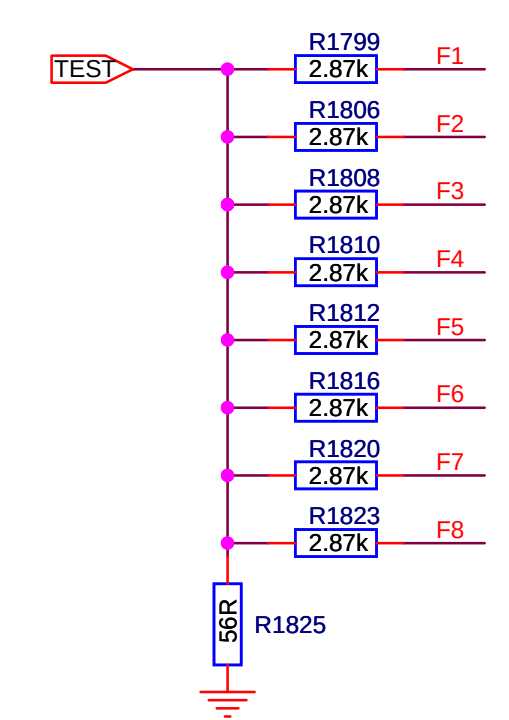
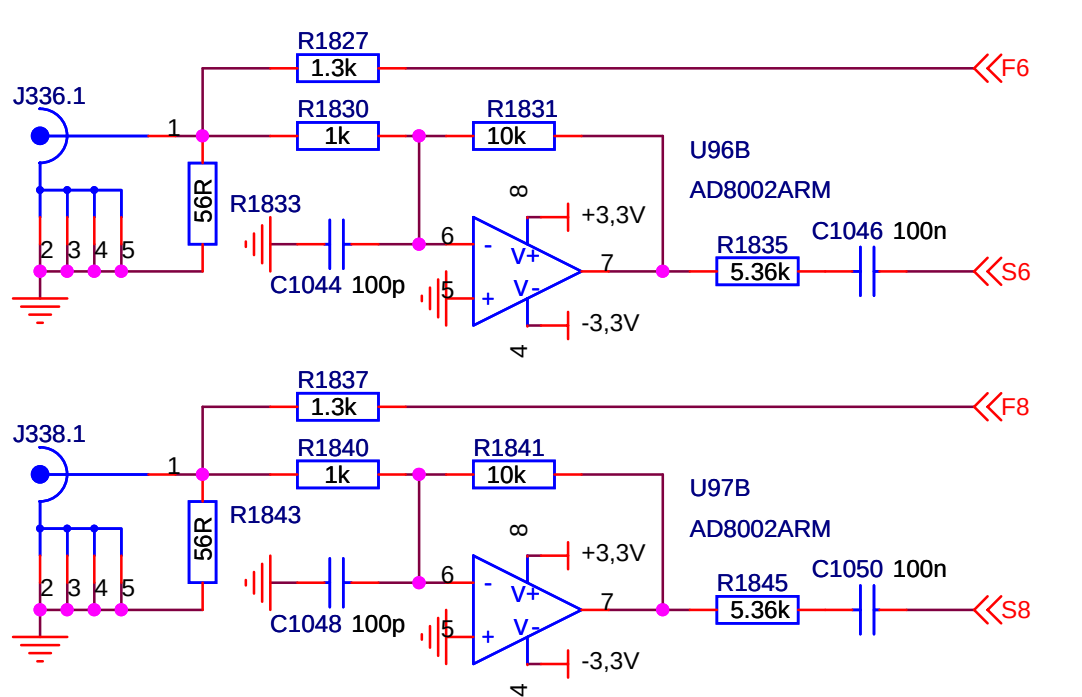
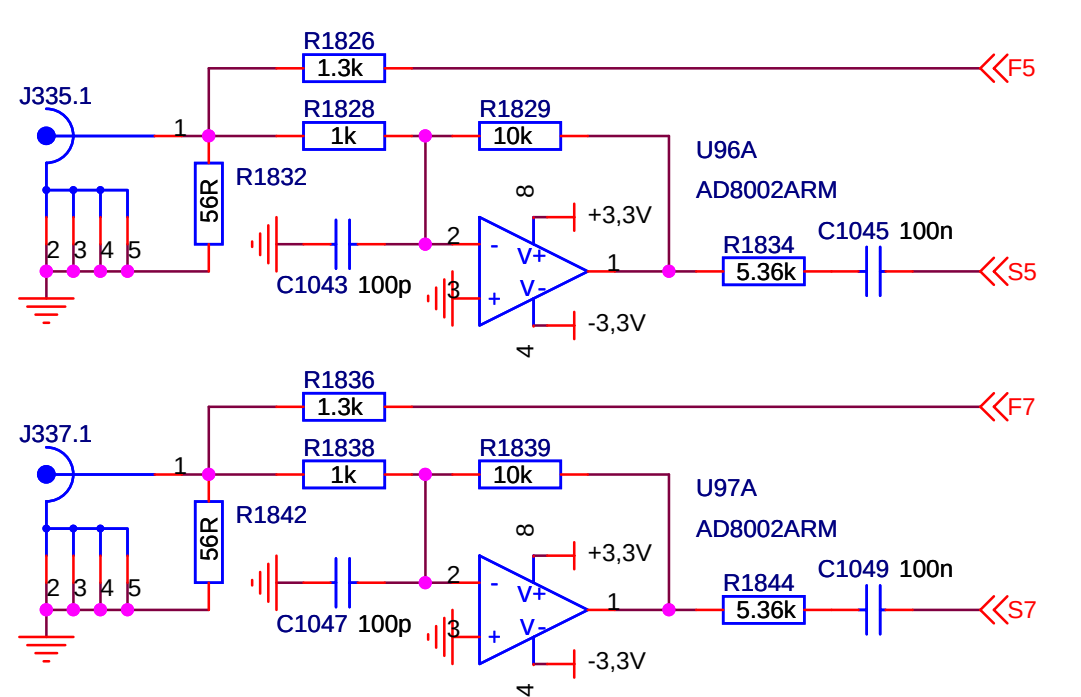
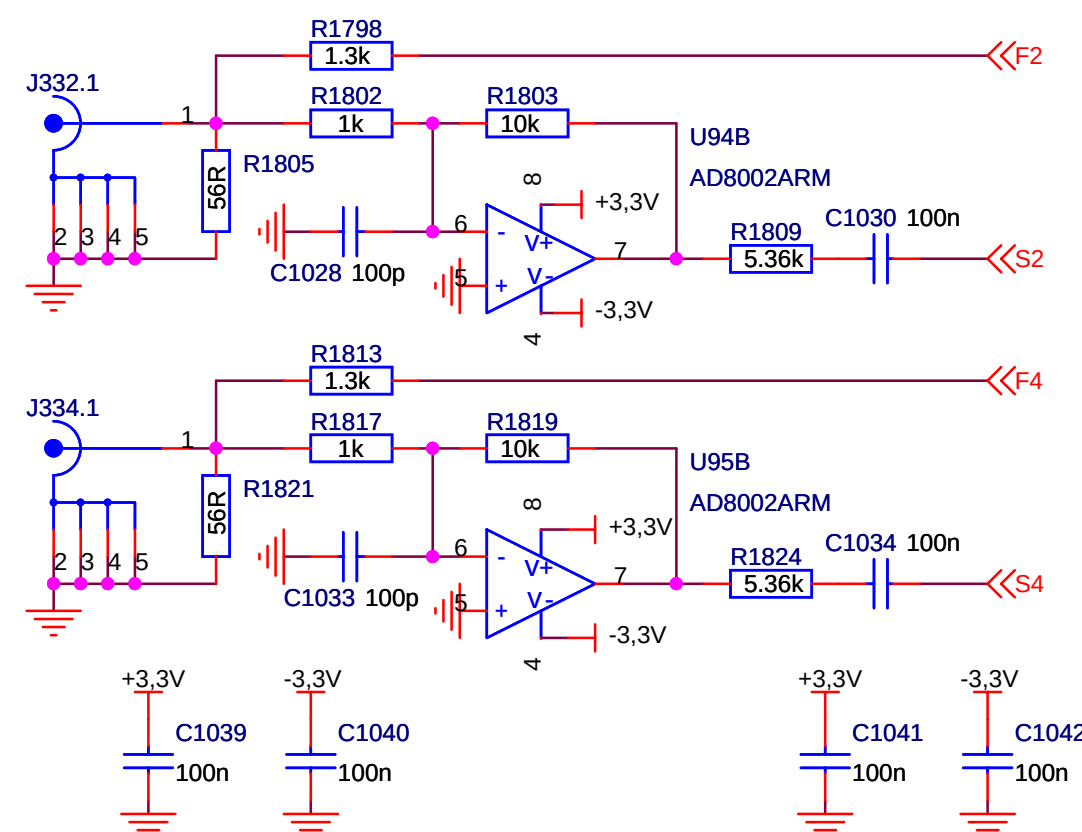
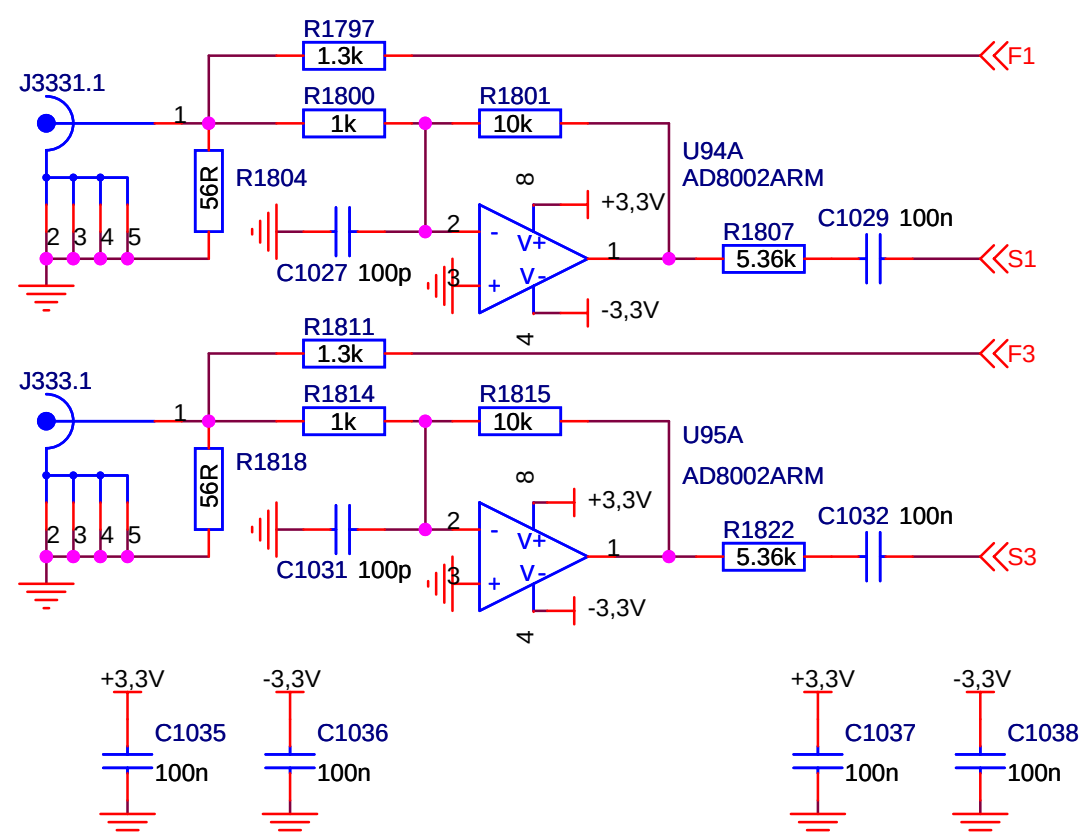
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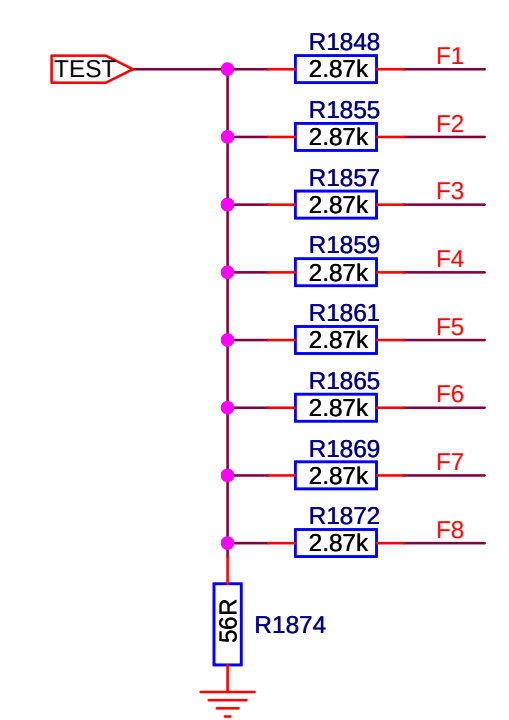
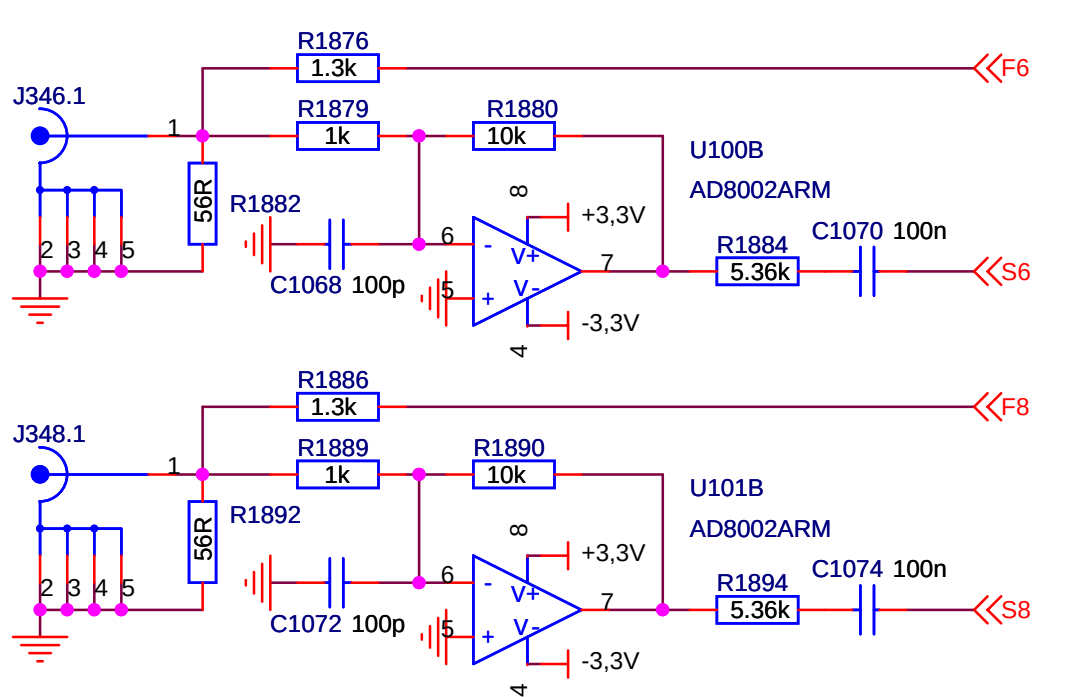
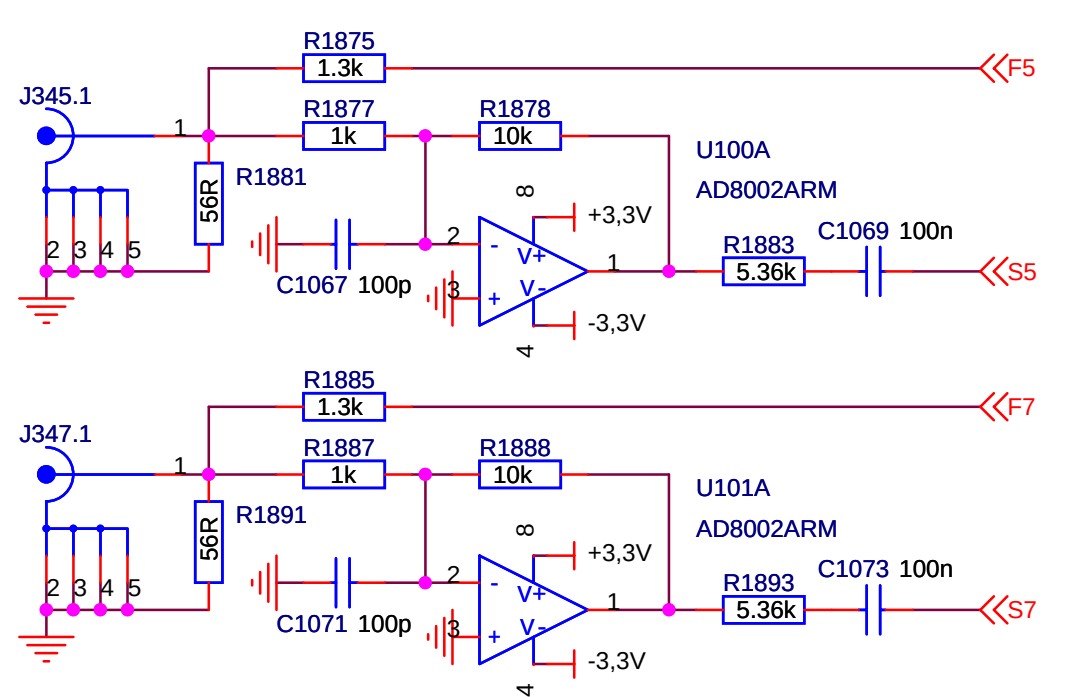
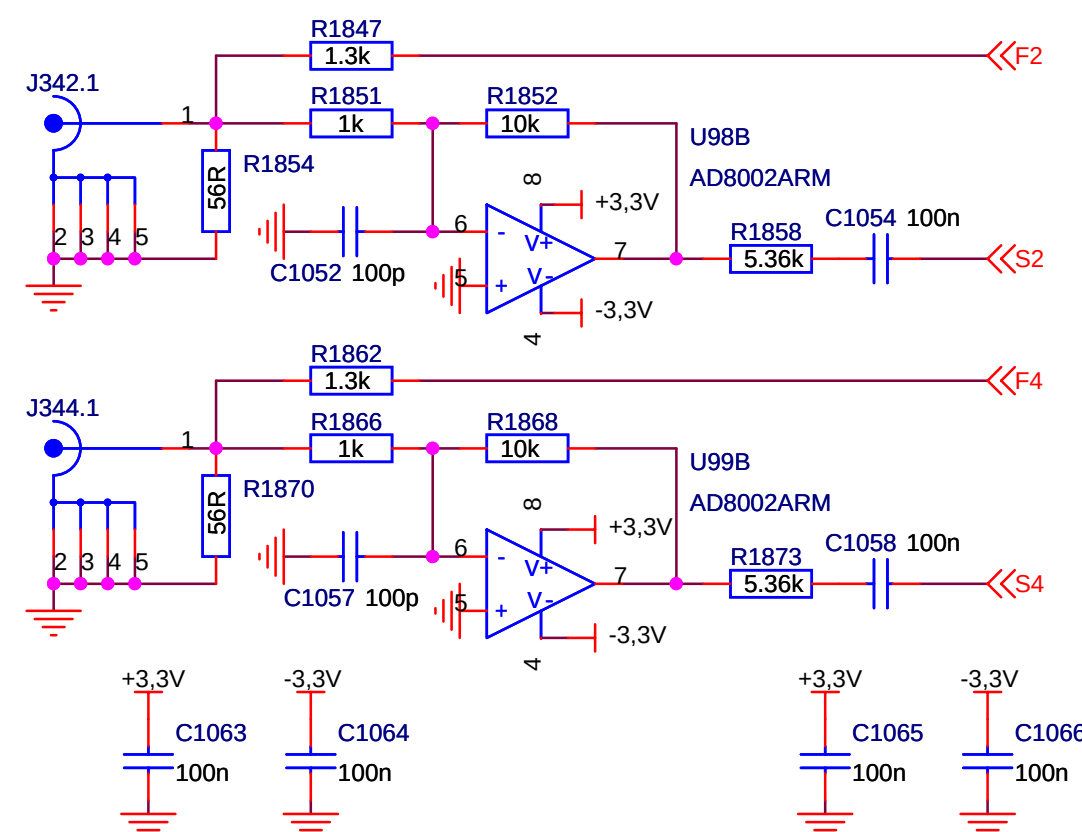
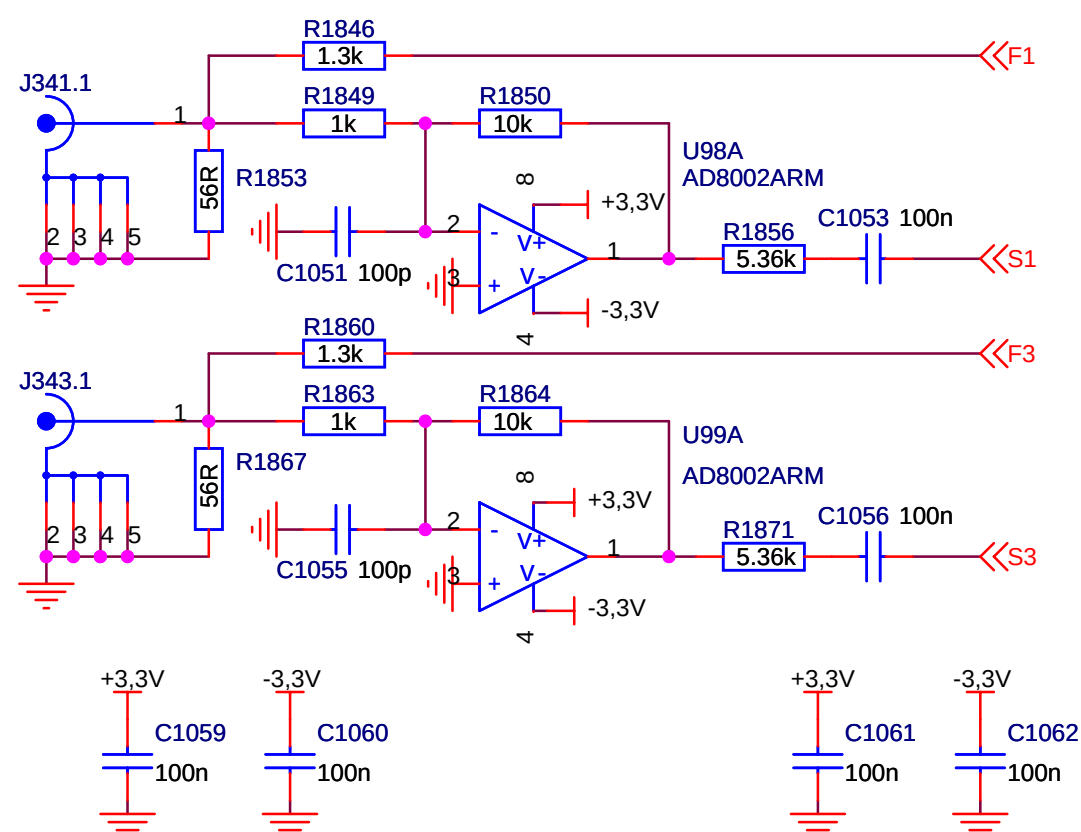
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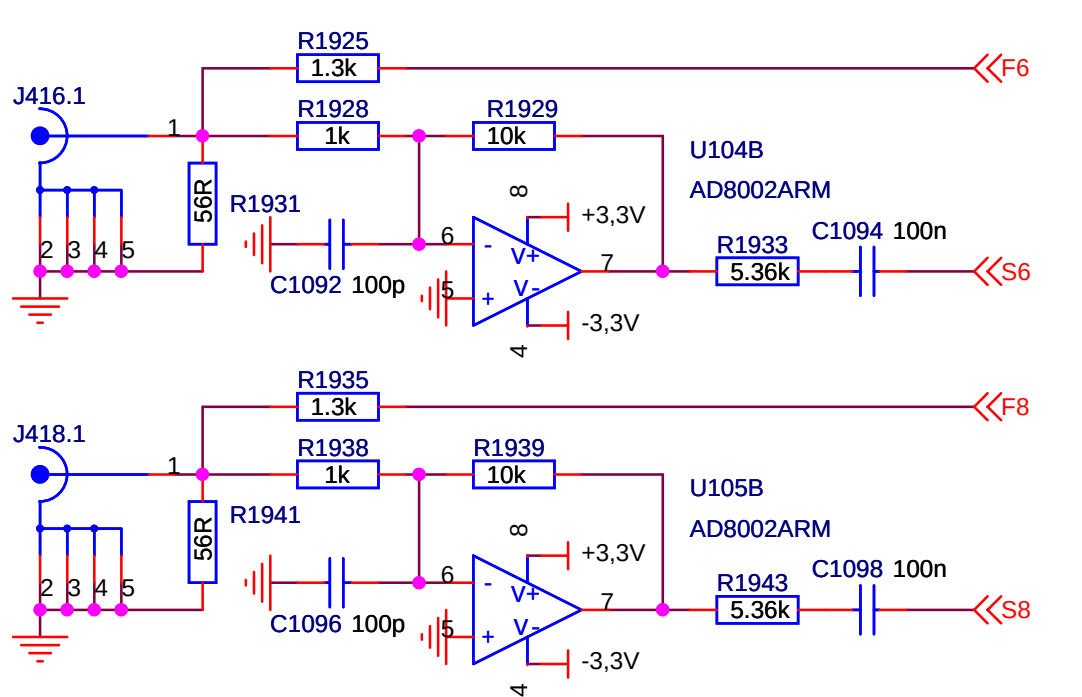
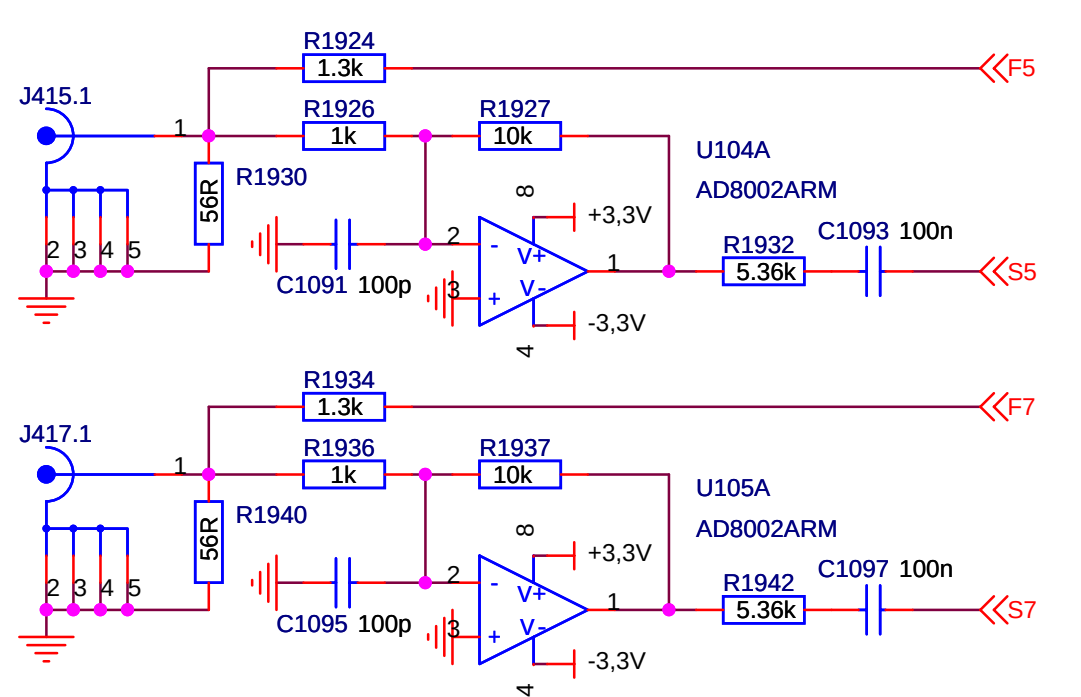
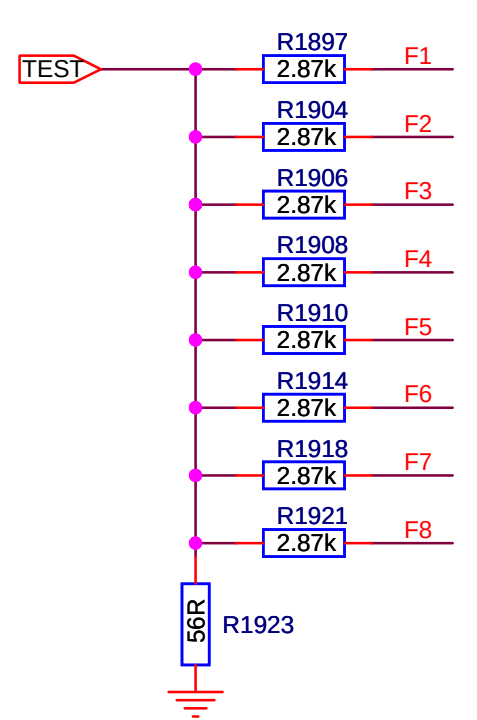
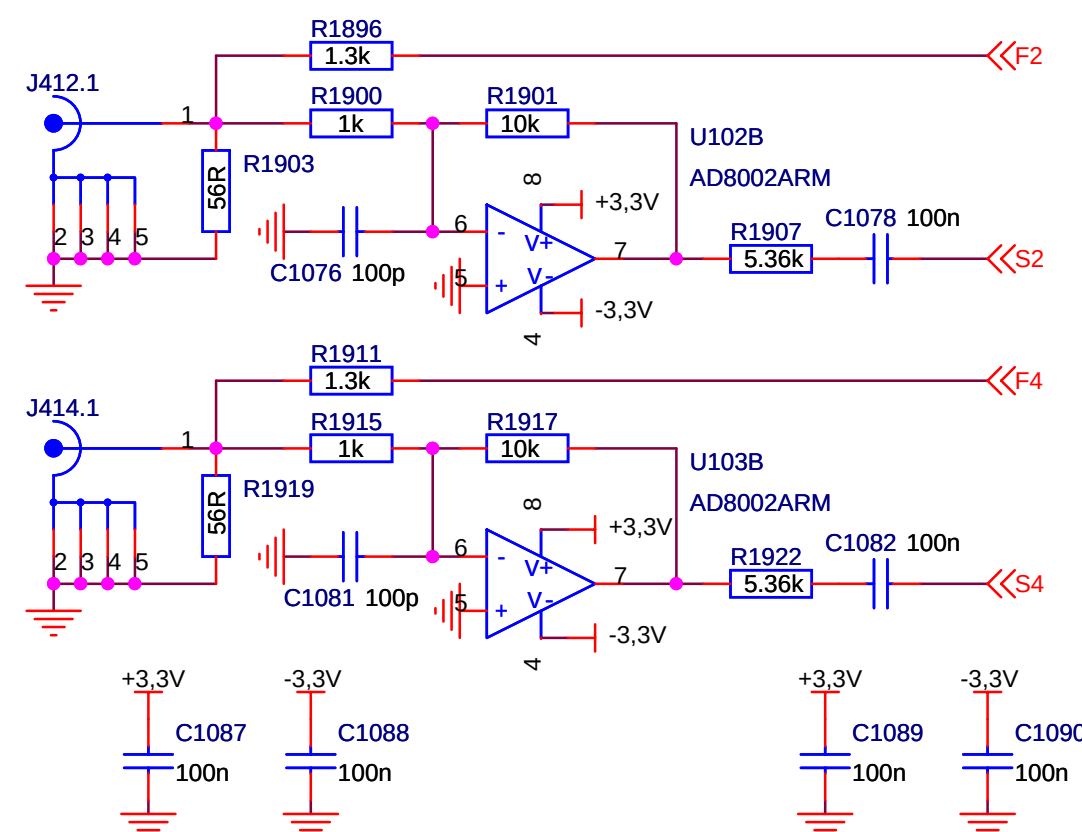
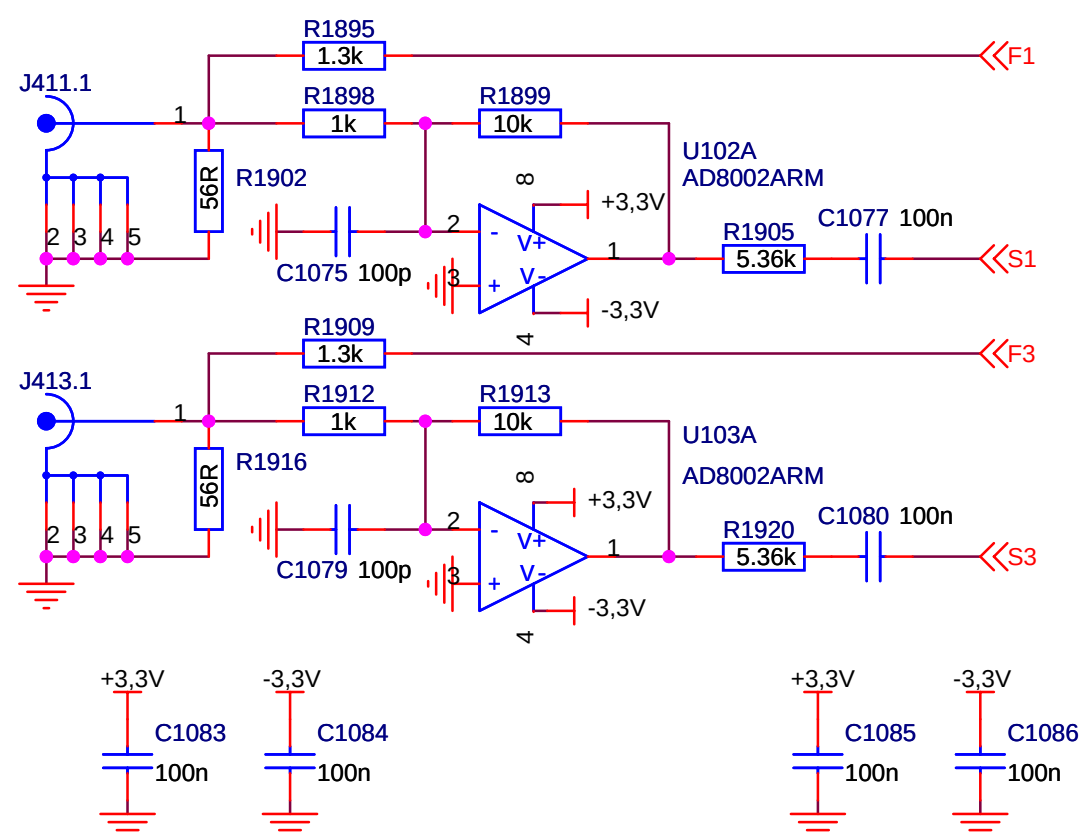


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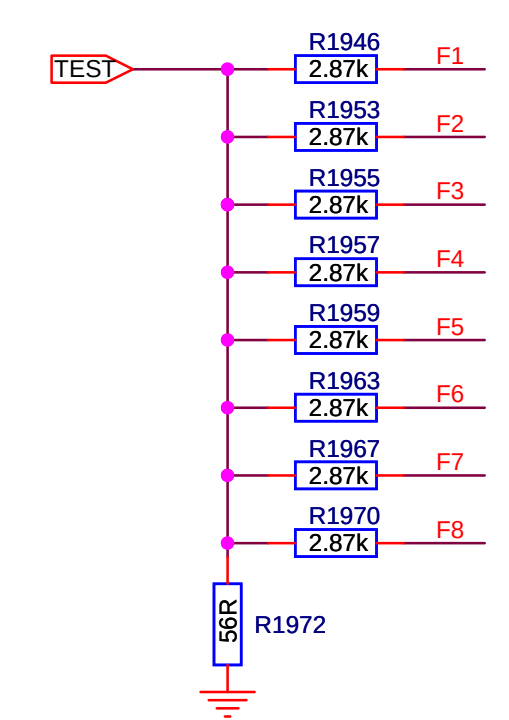
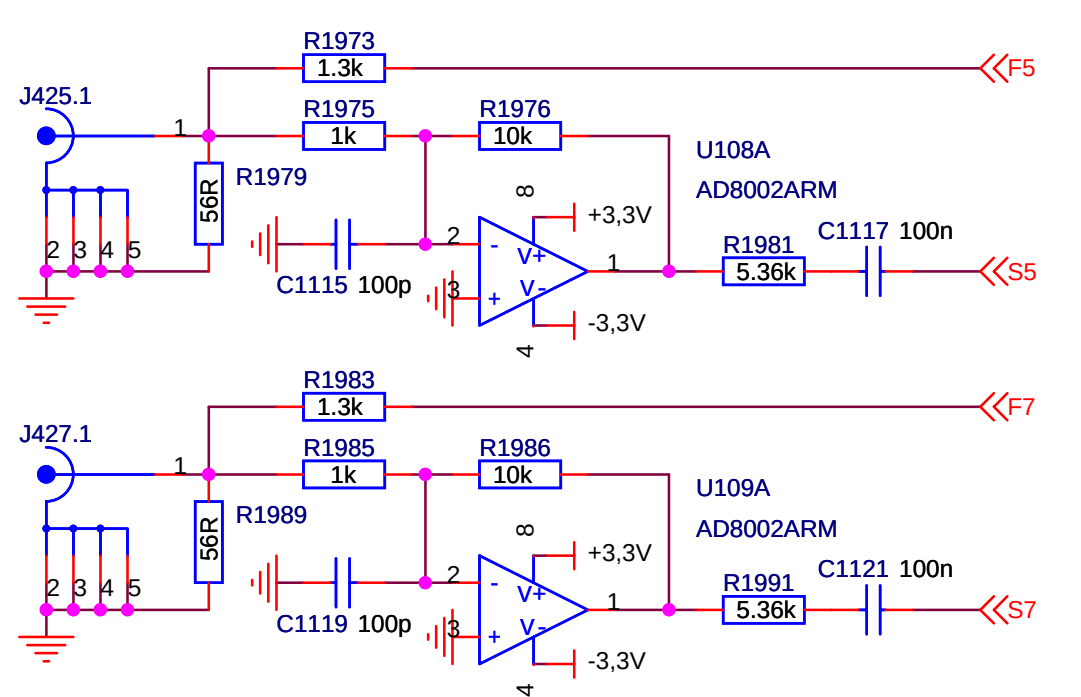
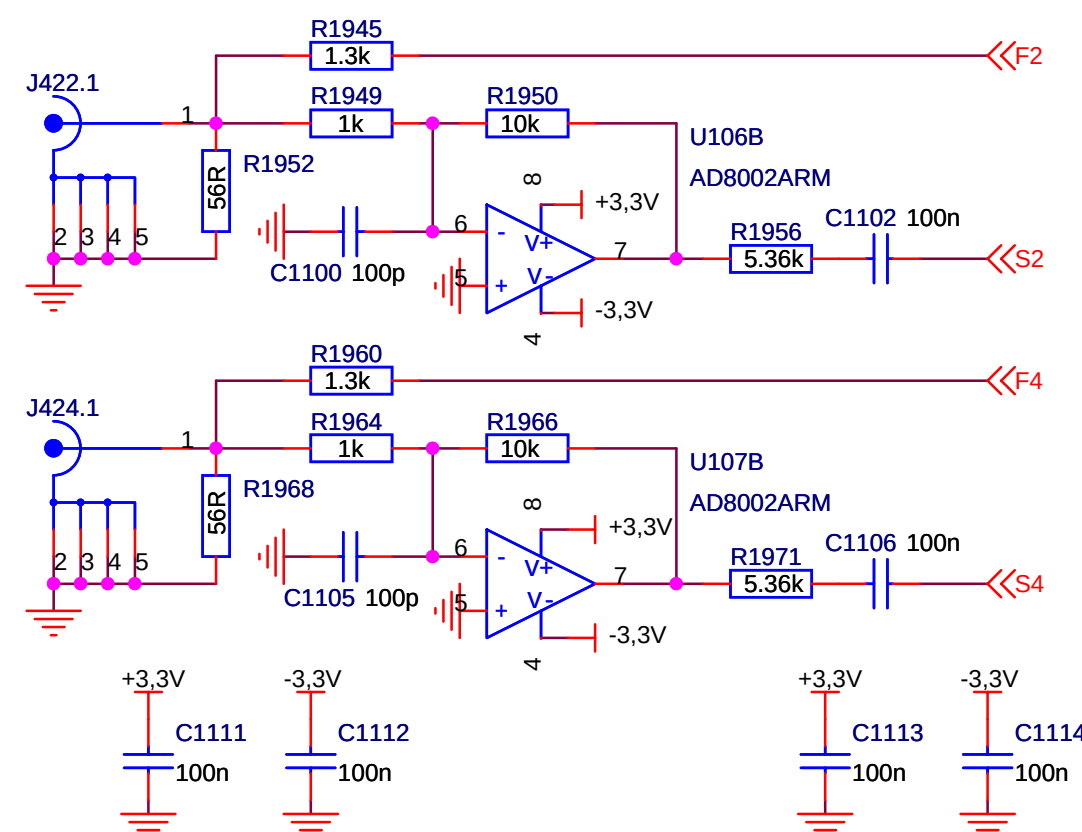
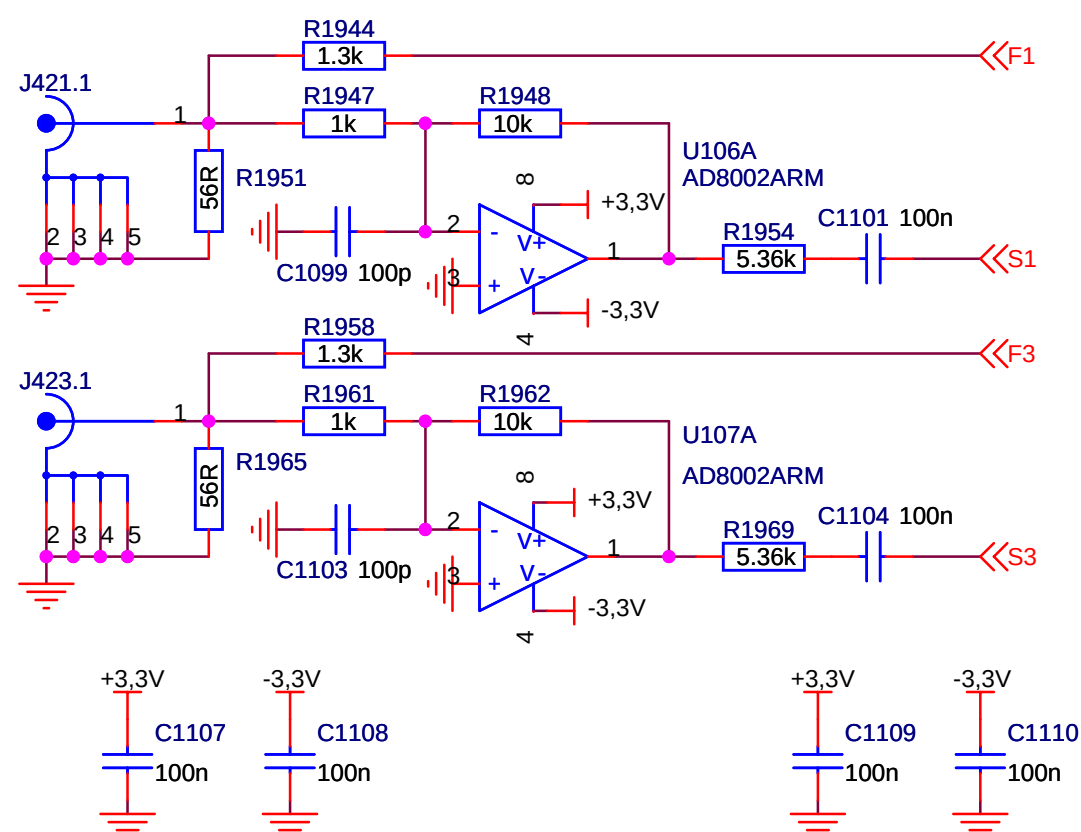




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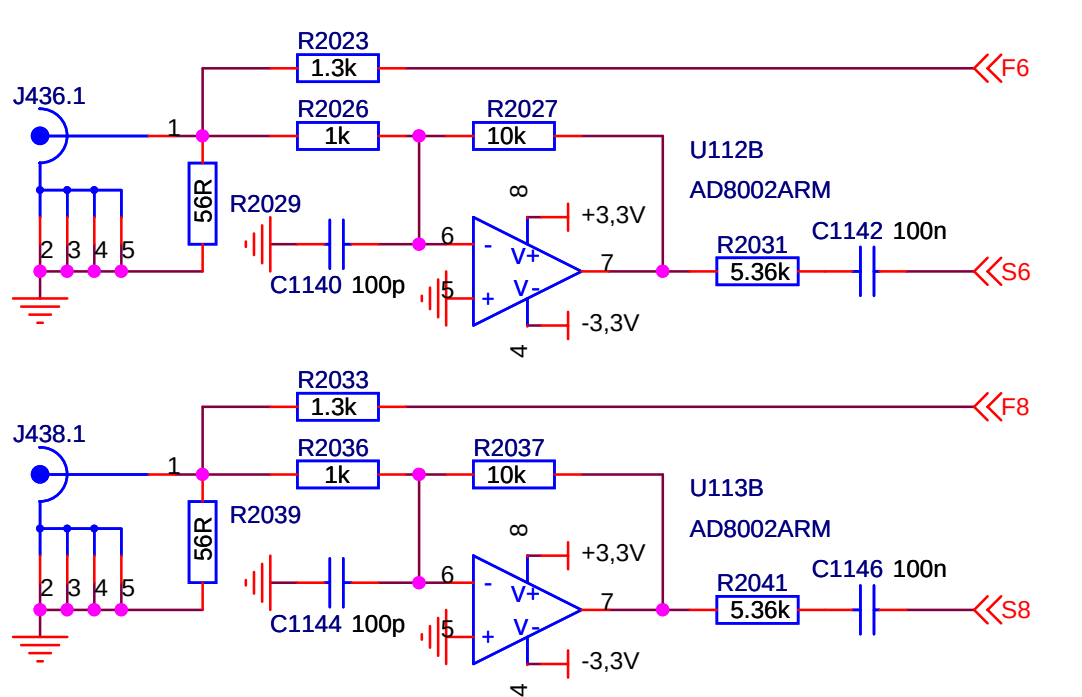
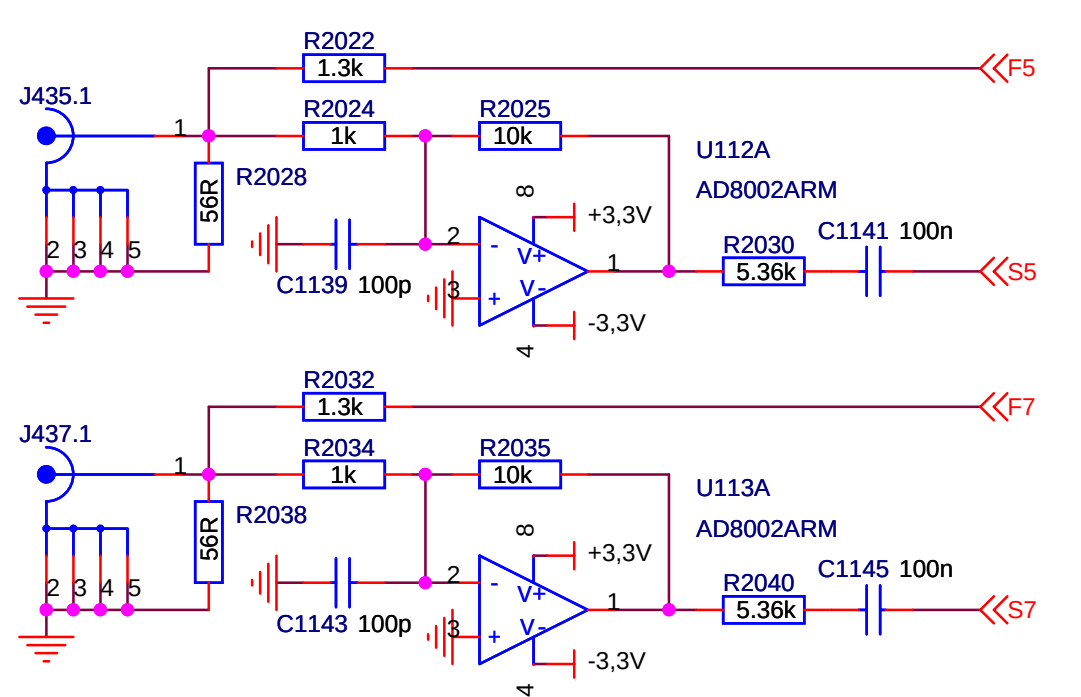
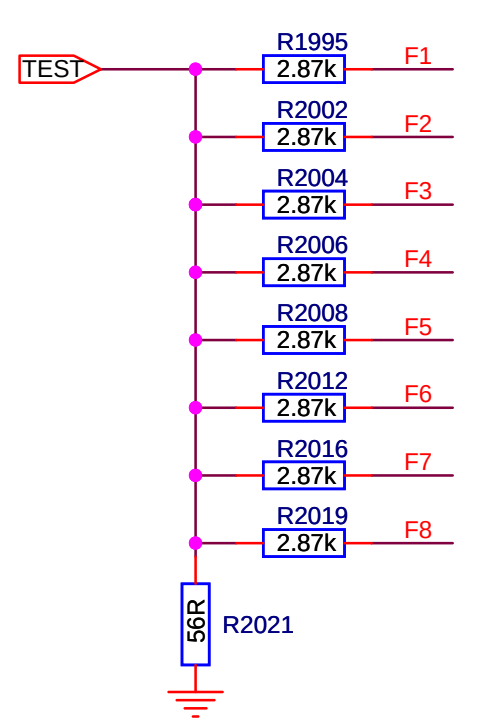
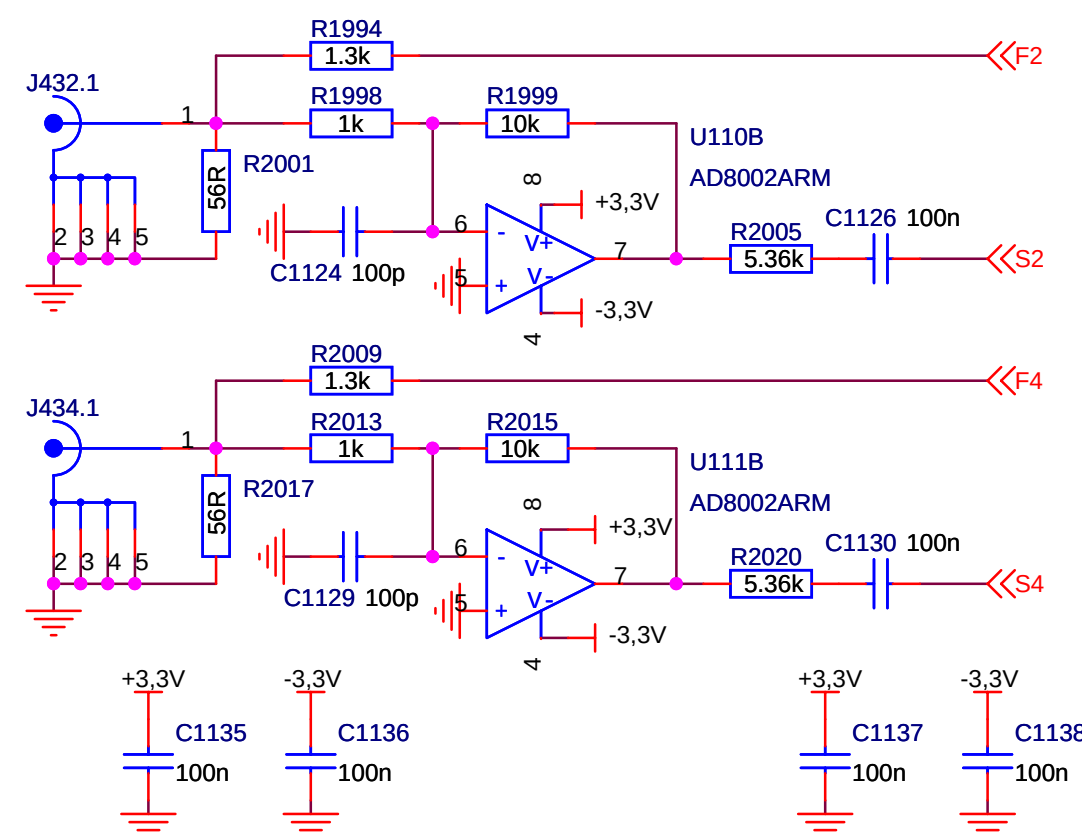
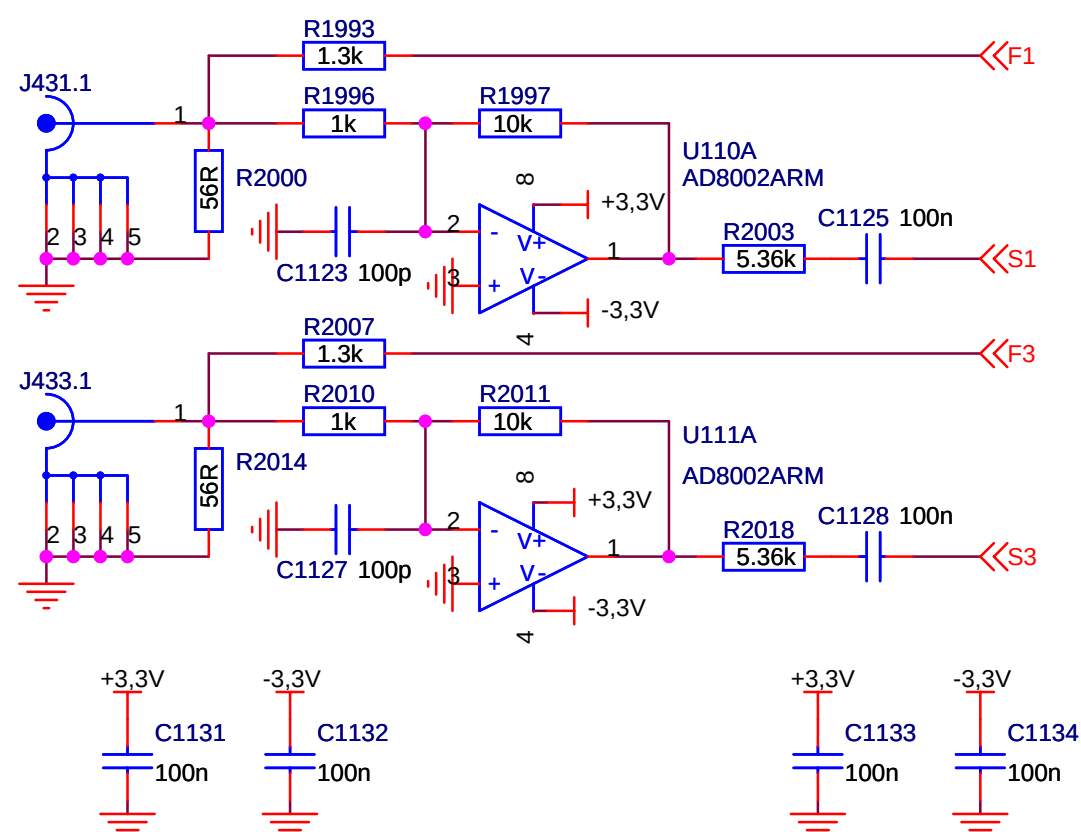




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