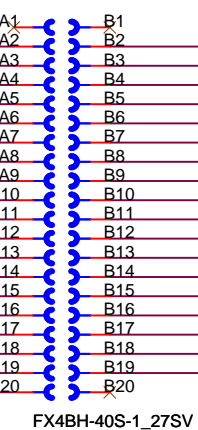


Voltage translators for 5V->3.3V and vice versa

Connectors to the Motherboard

All directions are seen from this "driver card"

DCON1



ADI[0..1]: Input not needed

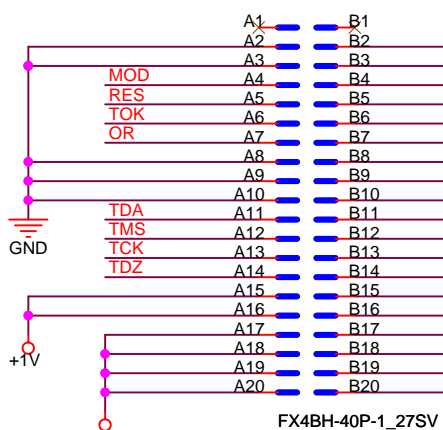
DRA, ENR, DRB, ENB, DRE, REN, CDE0 all inputs Signals for the Transceivers

AD[0..8]: output/input Address and Data

ADS0, ADS1: input count number of motherboards, not needed

RSV: input additional bit

DCON2

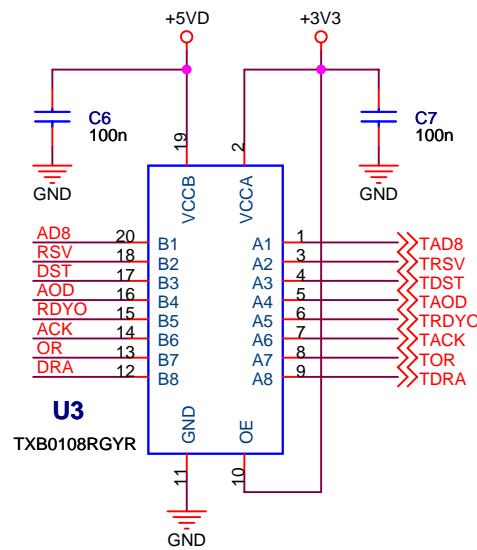
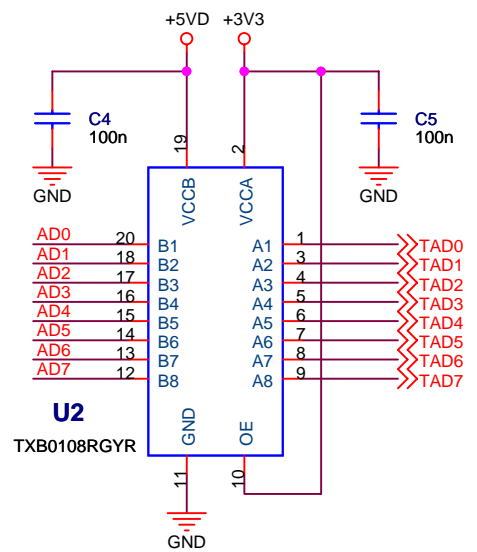
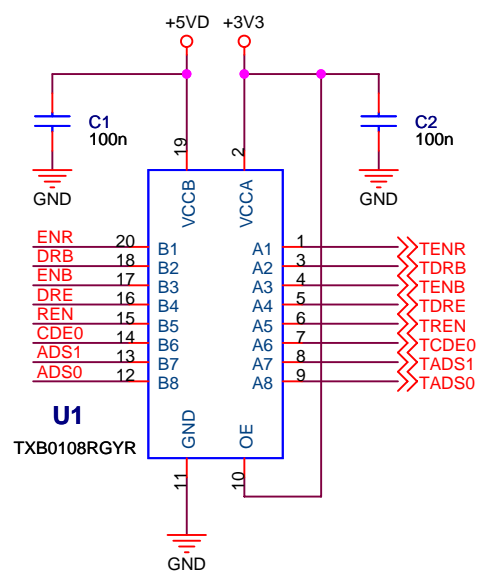


MOD, RES, TOK, OR: output modline

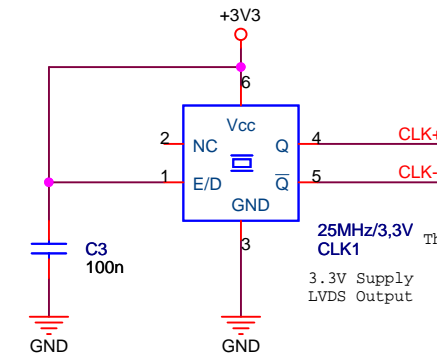
WRM: output (modline)  
DST: in/out (Data/Address Strobe)  
CMS: output (common stop signal)

TDA, TMD, TCK: input, JTAG  
TDZ: output, JTAG

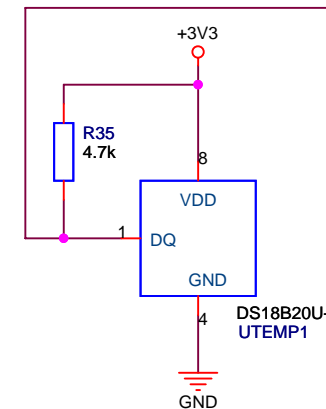
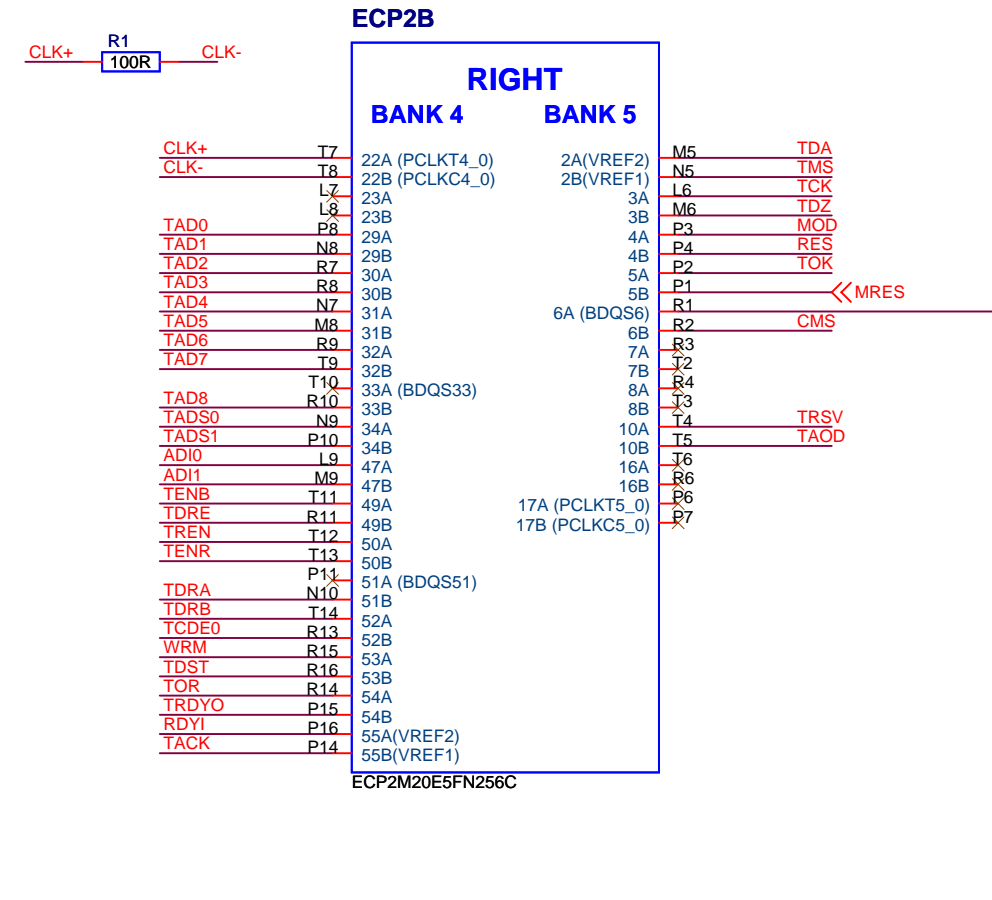
GDE: out (global disable for TDC)  
AOD: in/out (determines if data or address)  
RDYO: in (READY = Token-out of last TDC)  
RDYI: out (Token to TDC)  
ACK: in (sent before token)



System Clock



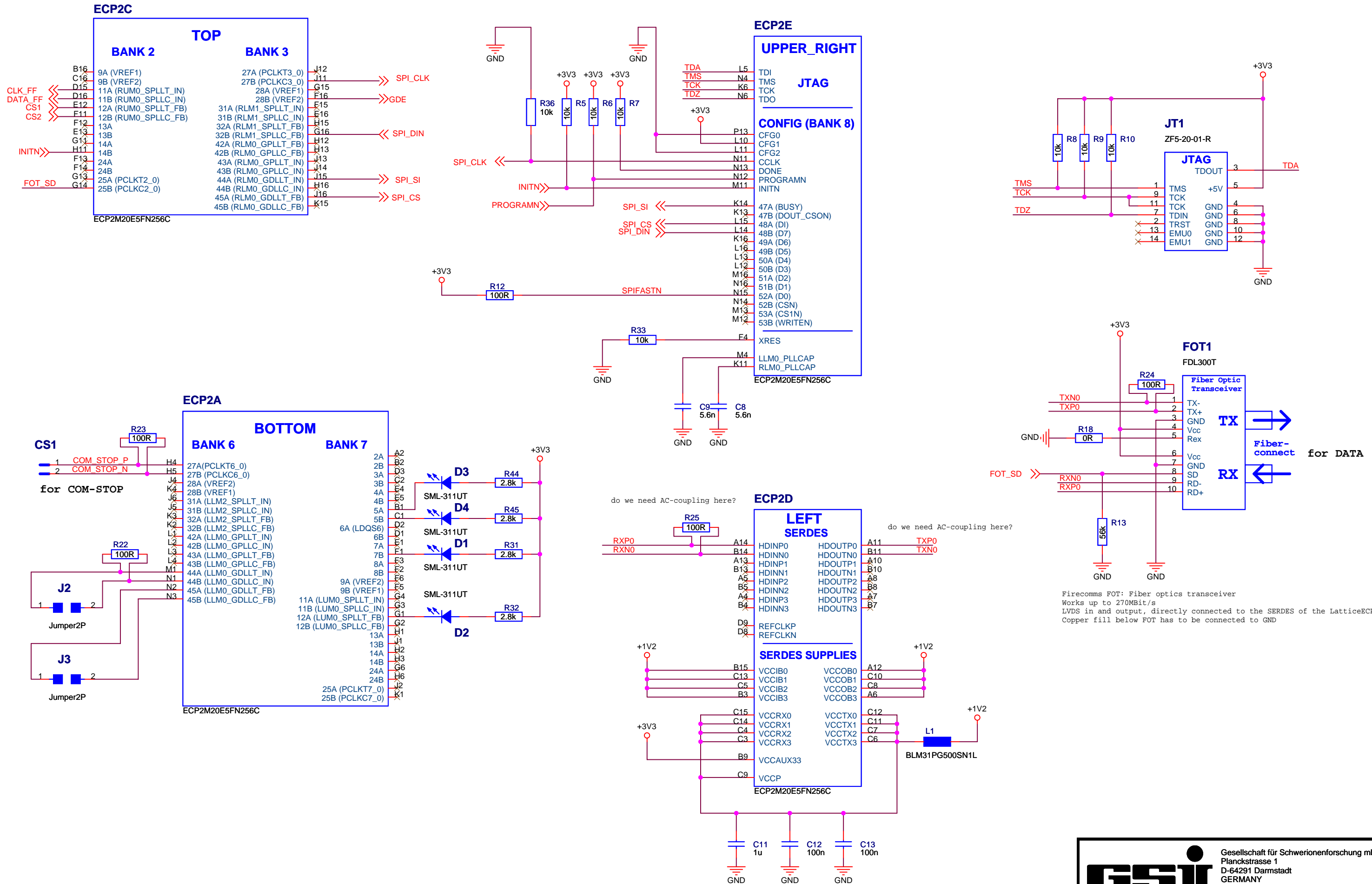
25MHz/3.3V CLK1 The frequency can be changed if needed...  
3.3V Supply LVDS Output



GSI Gesellschaft für Schwerionenforschung mbH  
Planckstrasse 1  
D-64291 Darmstadt  
GERMANY  
www.gsi.de

MDC-DC-LWL2

Banks 2,3,6 and 7 have 50% outputs with LVDS capability  
 For correct LVDS output levels the corresponding VCCIOs have to be 2.5V, which is not the case on this PCB  
 LVDS Input will work on all pairs, even with VCCIO at 3.3V

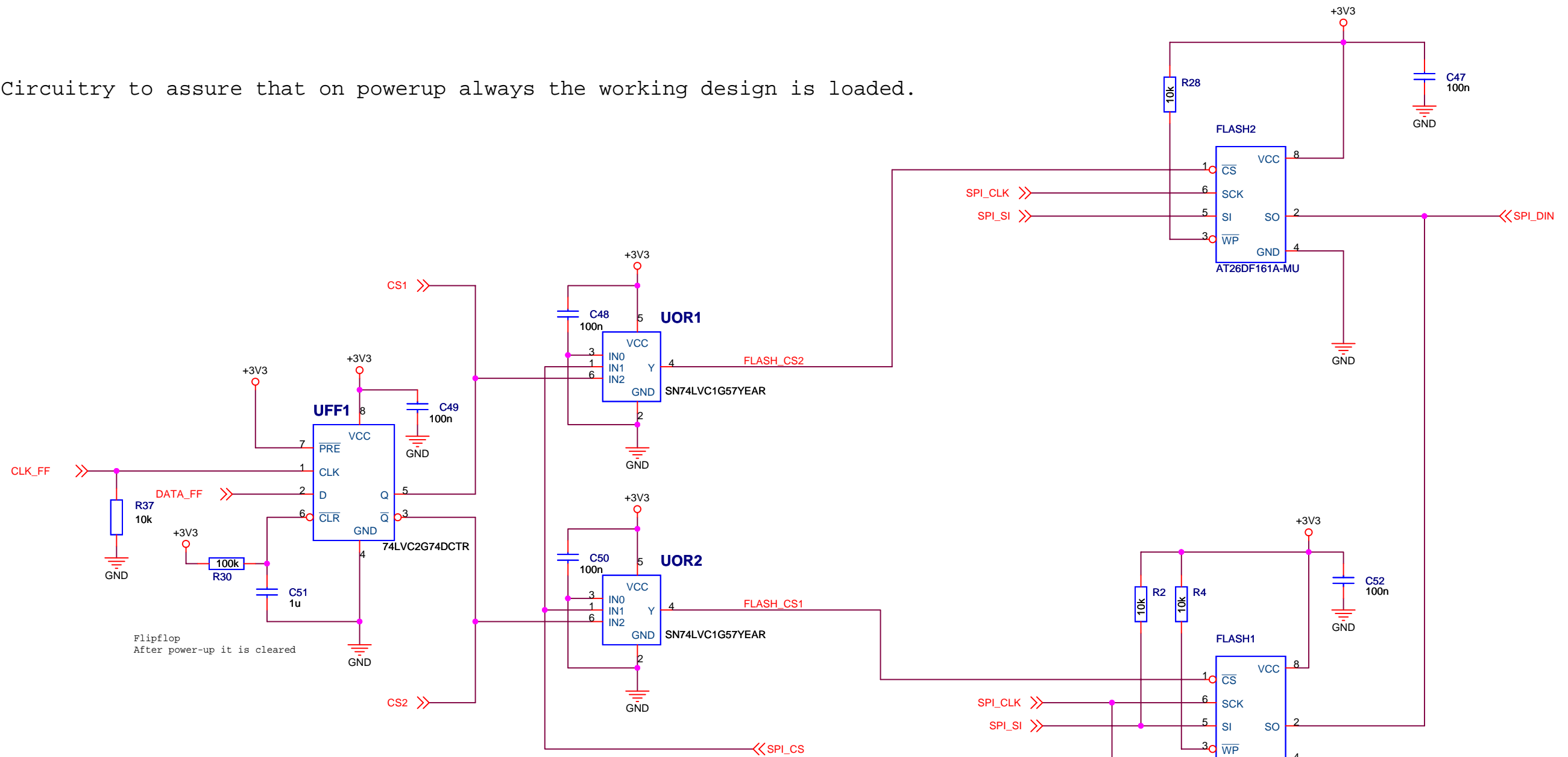


Firecomms FOT: Fiber optics transceiver  
 Works up to 270Mbit/s  
 LVDS in and output, directly connected to the SERDES of the LatticeECP2M  
 Copper fill below FOT has to be connected to GND



### MDC-DC-LWL2

Circuitry to assure that on powerup always the working design is loaded.



These are multi-purpose gates.  
 In this configuration (pin 3 to GND) they are OR gates with one input negated.  
 Therefore it is required, that the FPGA asserts (low) the ChipSelect (SPI\_CS) and additionally, that the CS1/2 is low, to assert a CS of Flash1 or Flash2.  
 After the first booting, the FPGA can put a '1' to the data input of the FlipFlop and give a clock, then the other FLASH is selected.  
 This then can be programmed and with asserting the ManualReset pin on the ResetChip, the FPGA will get a PROGRAMN pulse, which will reload the FPGA with the new design.

