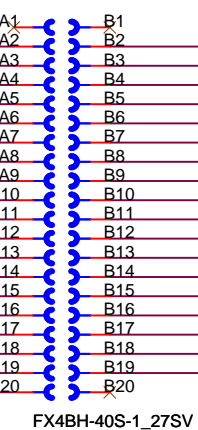


Voltage translators for 5V->3.3V and vice versa

Connectors to the Motherboard

All directions are seen from this "driver card"

DCON1

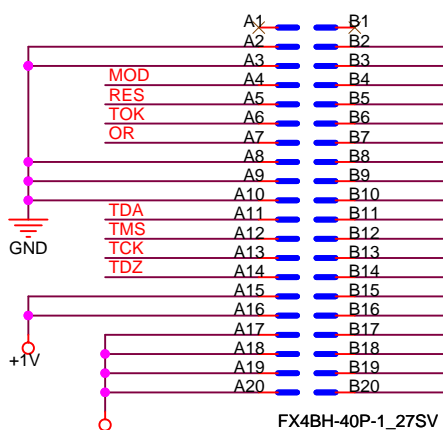


ADI[0..1]: Input not needed

DRA, ENR, DRB, ENB, DRE, REN, CDE0 all inputs Signals for the Transceivers

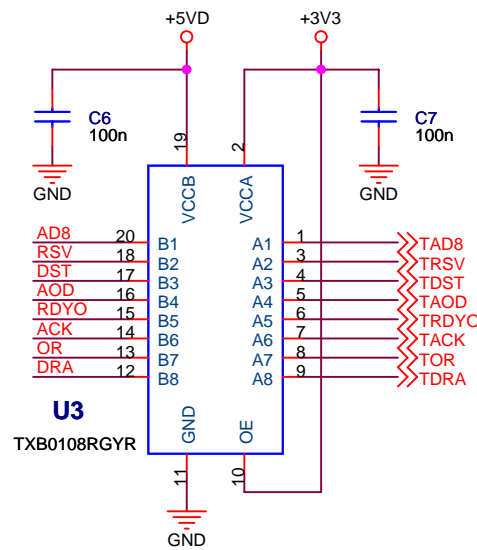
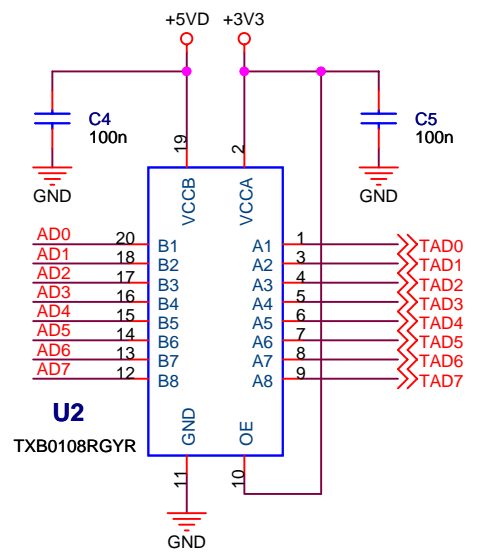
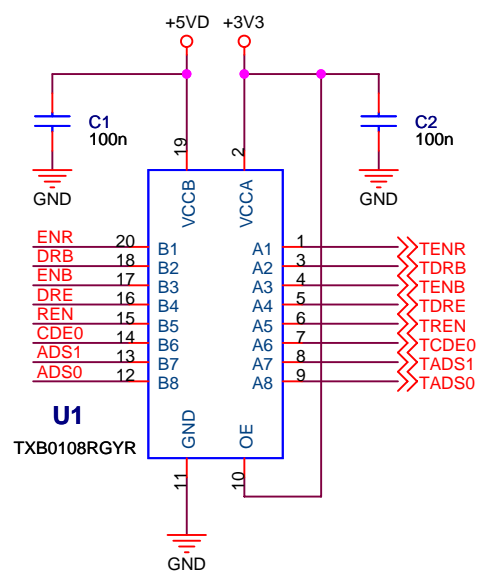
ADS0, ADS1: input count number of motherboards, not needed

DCON2

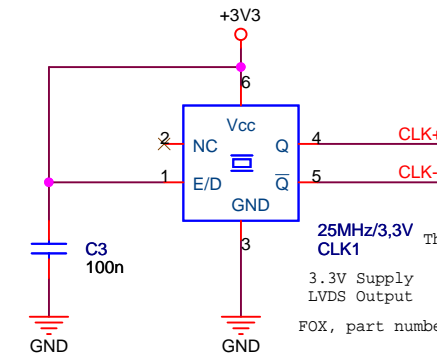


MOD, RES, TOK, OR: output modline

TDA, TMD, TCK: input, JTAG TDZ: output, JTAG

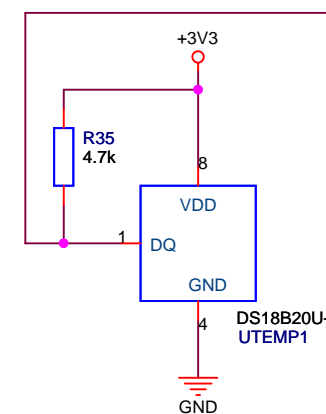
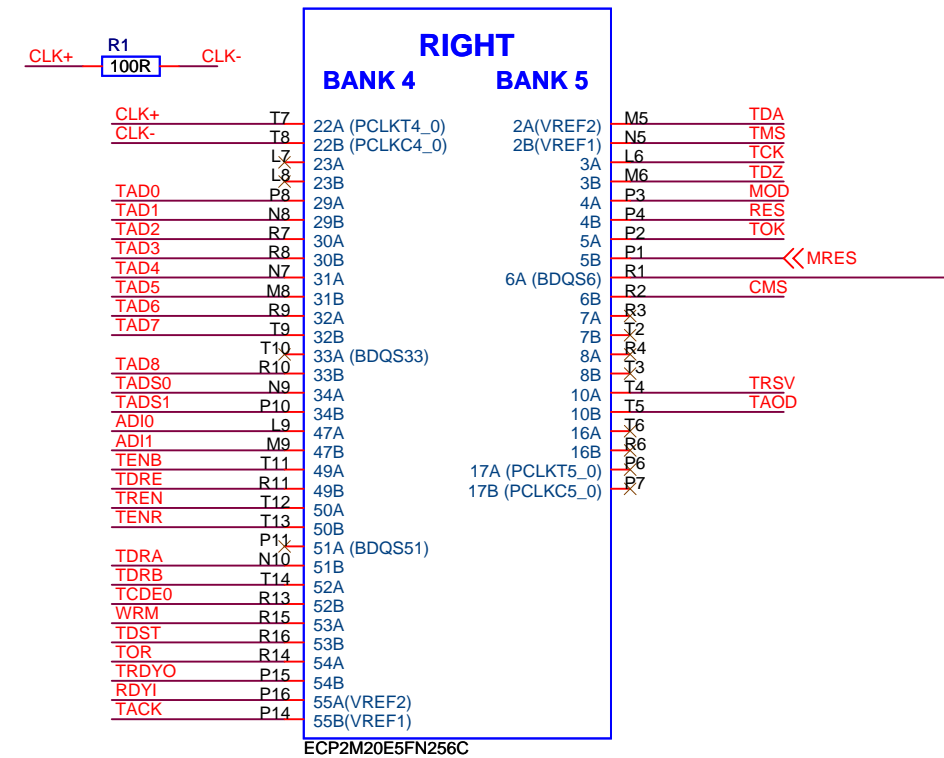


System Clock



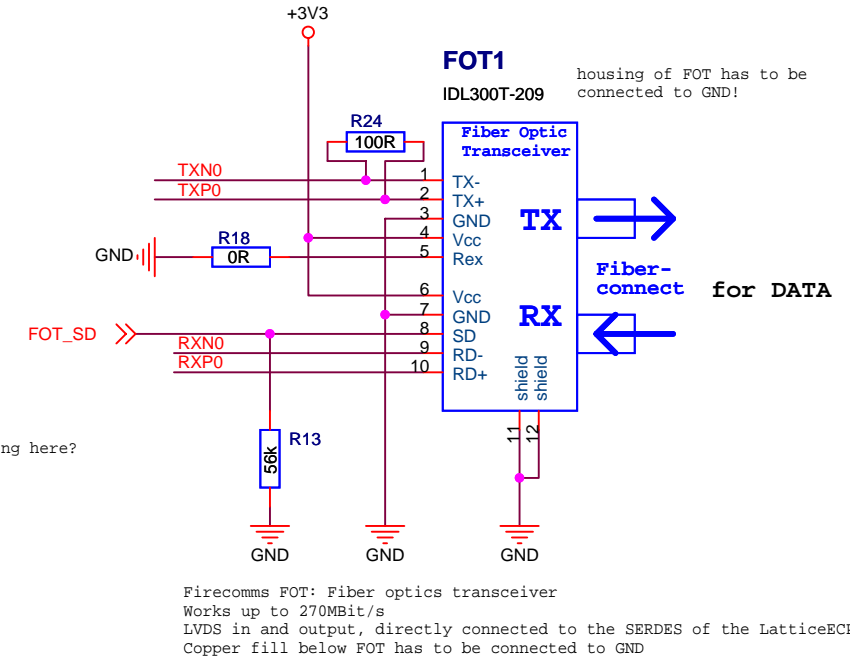
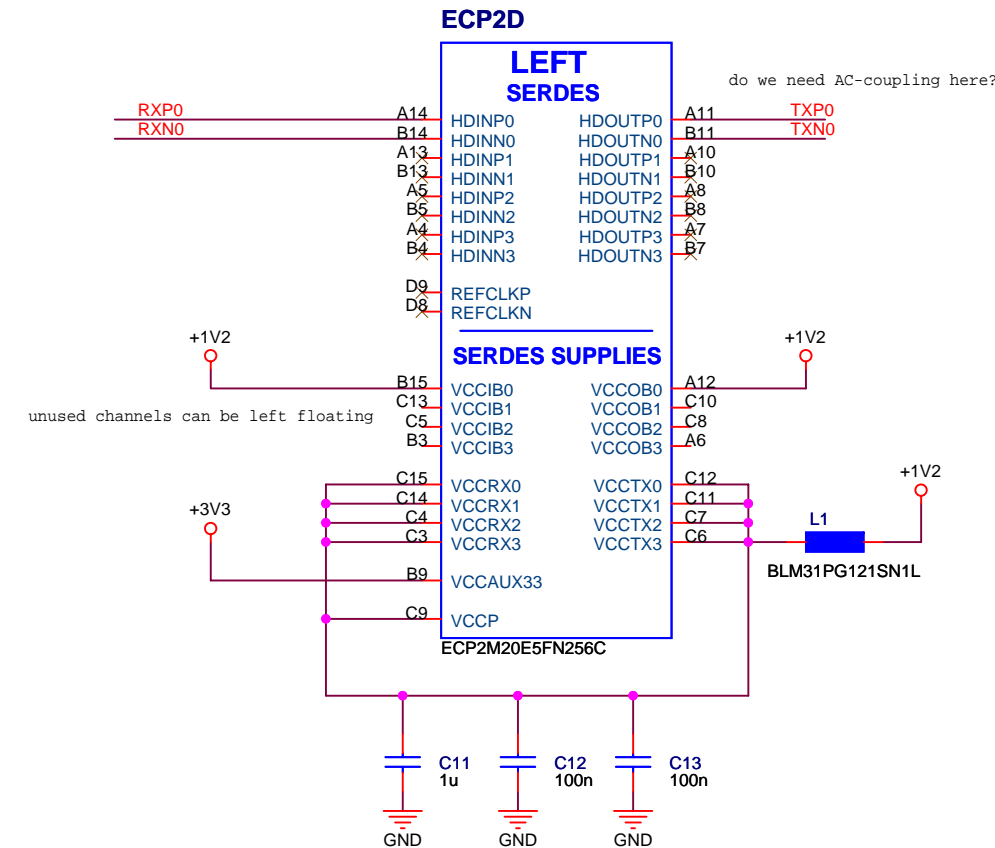
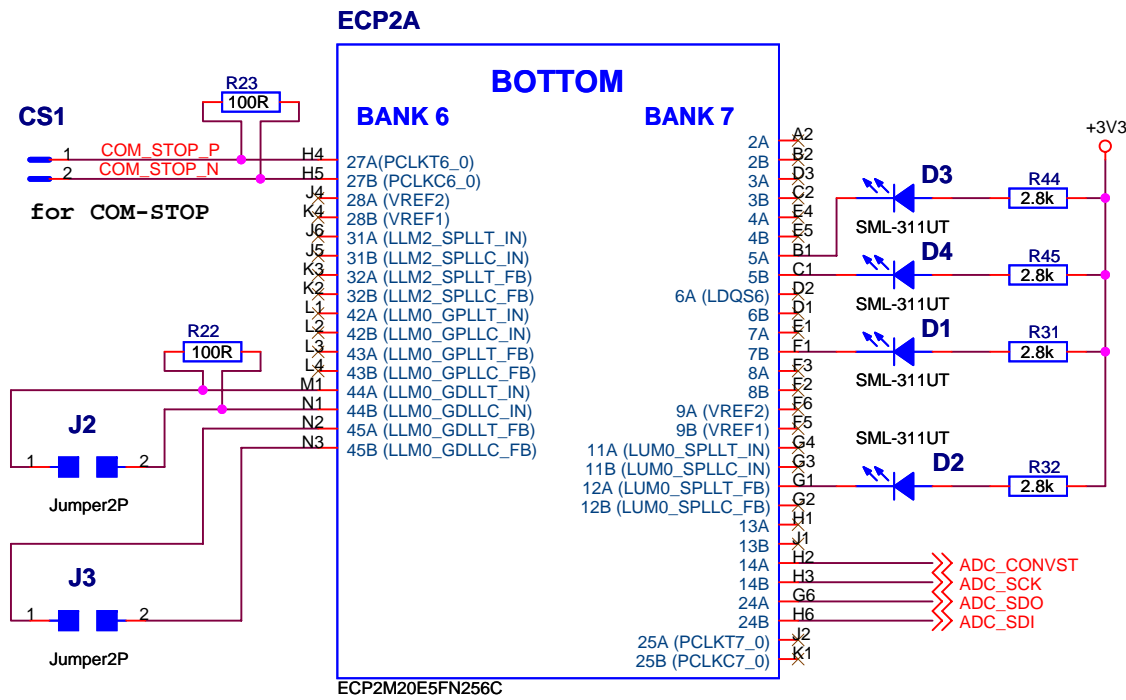
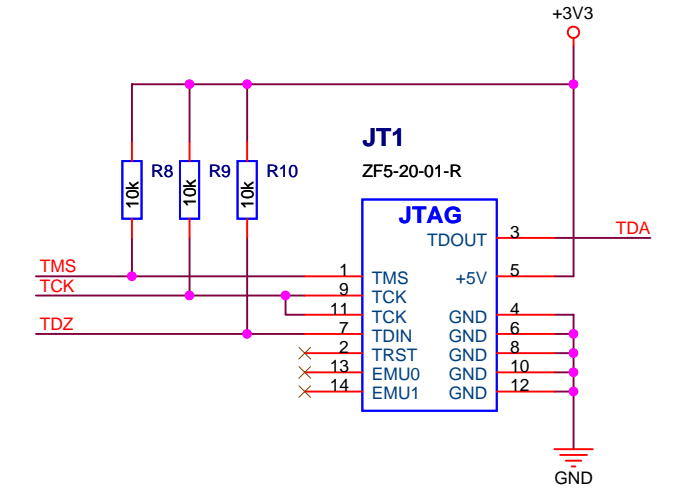
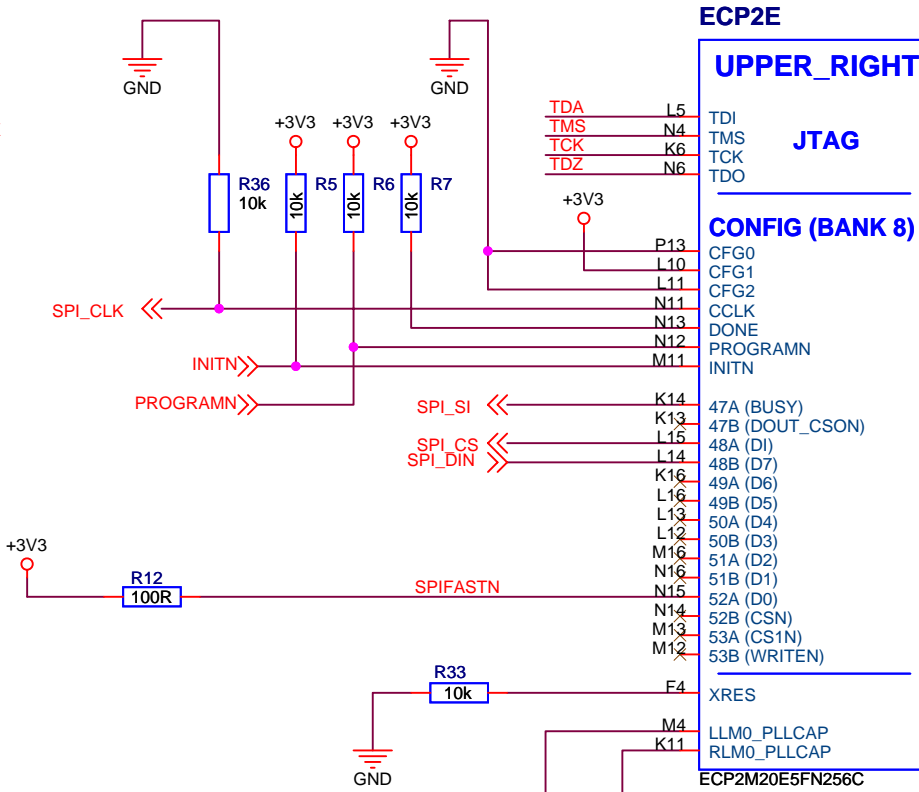
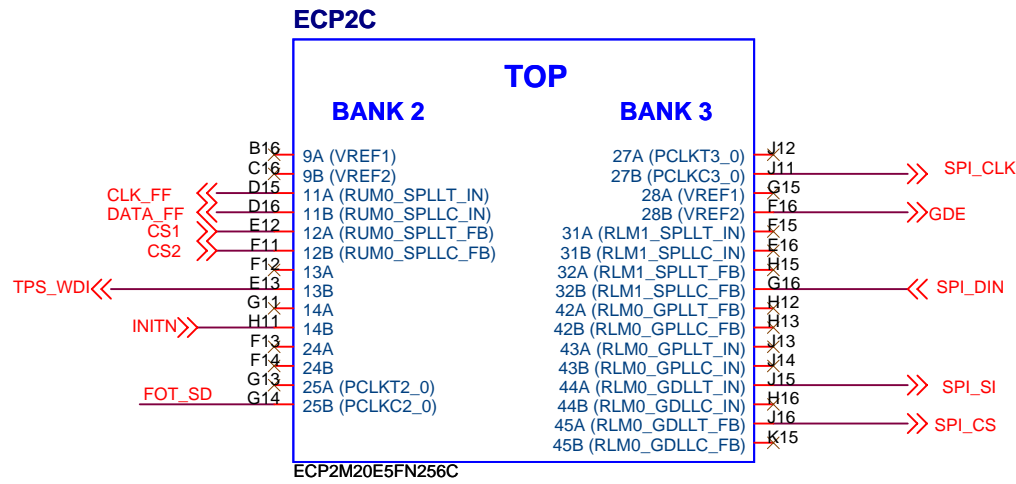
25MHz/3.3V CLK1 The frequency can be changed if needed...
3.3V Supply LVDS Output
FOX, part number: 770-25-7

ECP2B

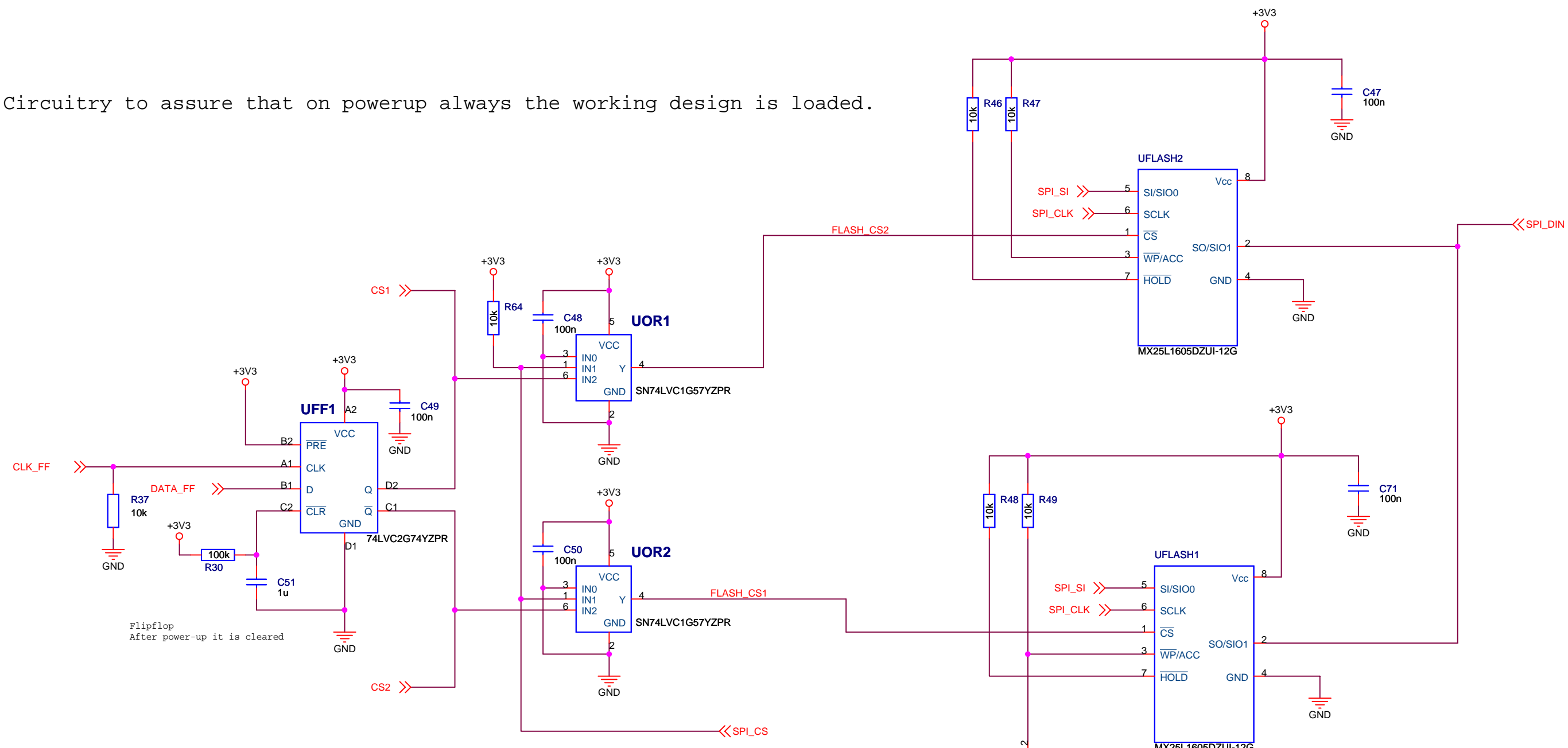


HADES-MDC-OEP3

Banks 2,3,6 and 7 have 50% outputs with LVDS capability
 For correct LVDS output levels the corresponding VCCIOs have to be 2.5V, which is not the case on this PCB
 LVDS Inputs will work on all pairs, even with VCCIO at 3.3V



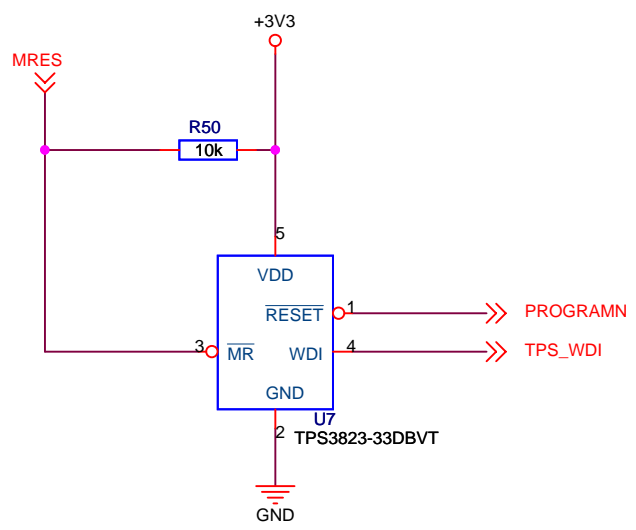
Circuitry to assure that on powerup always the working design is loaded.



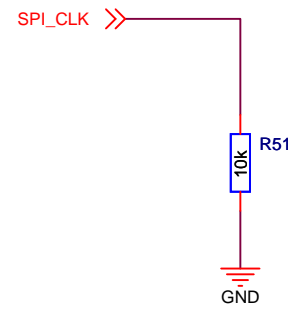
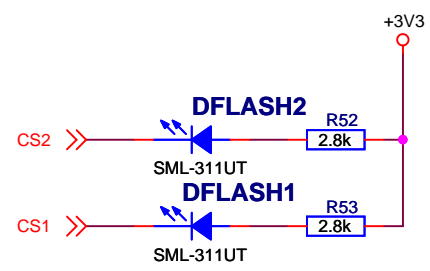
Flipflop
After power-up it is cleared

These are multi-purpose gates.
In this configuration (pin 3 to GND) they are OR gates with one input negated.
Therefore it is required, that the FPGA asserts (low) the ChipSelect (SPI_CS) and additionally, that the CS1/2 is low, to assert a CS of Flash1 or Flash2.
After the first booting, the FPGA can put a '1' to the data input of the FlipFlop and give a clock, then the other FLASH is selected.
This then can be programmed and with asserting the ManualReset pin on the ResetChip, the FPGA will get a PROGRAMN pulse, which will reload the FPGA with the new design.

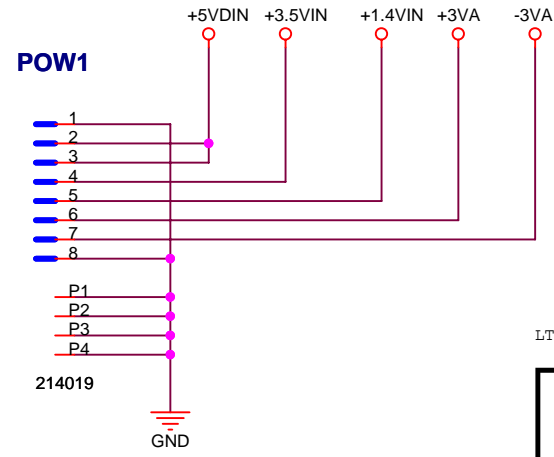
J4 Jumper2P
Close this jumper to permanently write protect the FLASH!
The pads of this jumper should very close to each other without any solder stop in between.



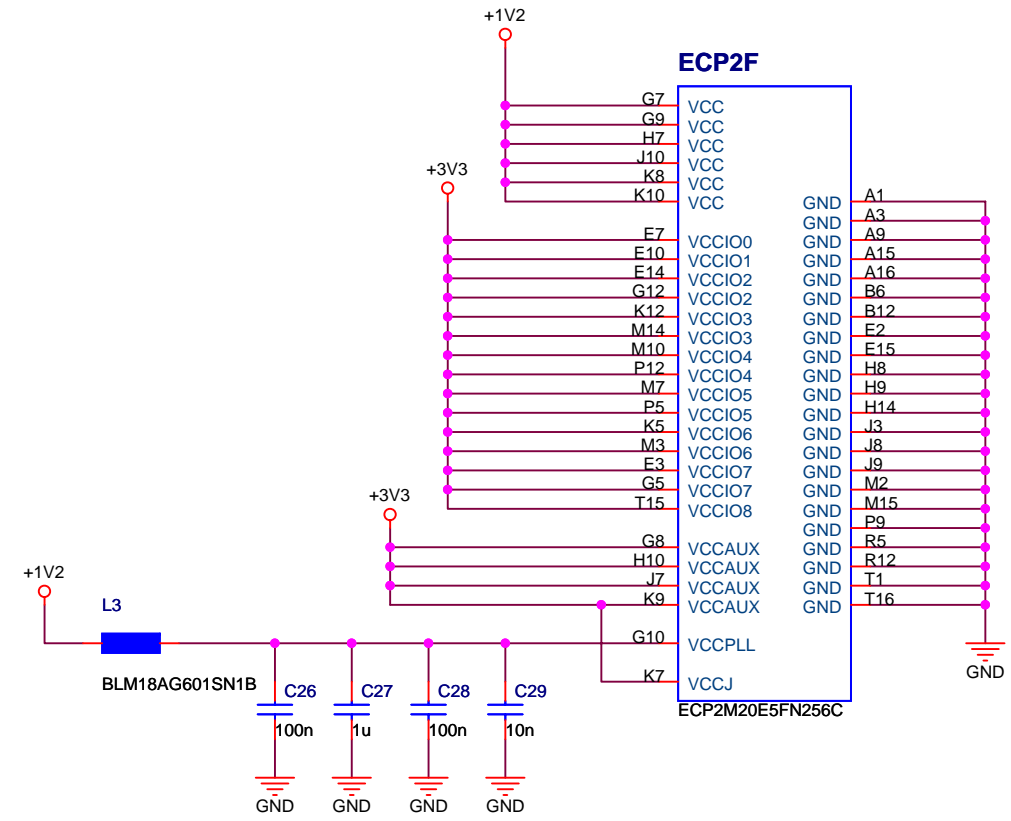
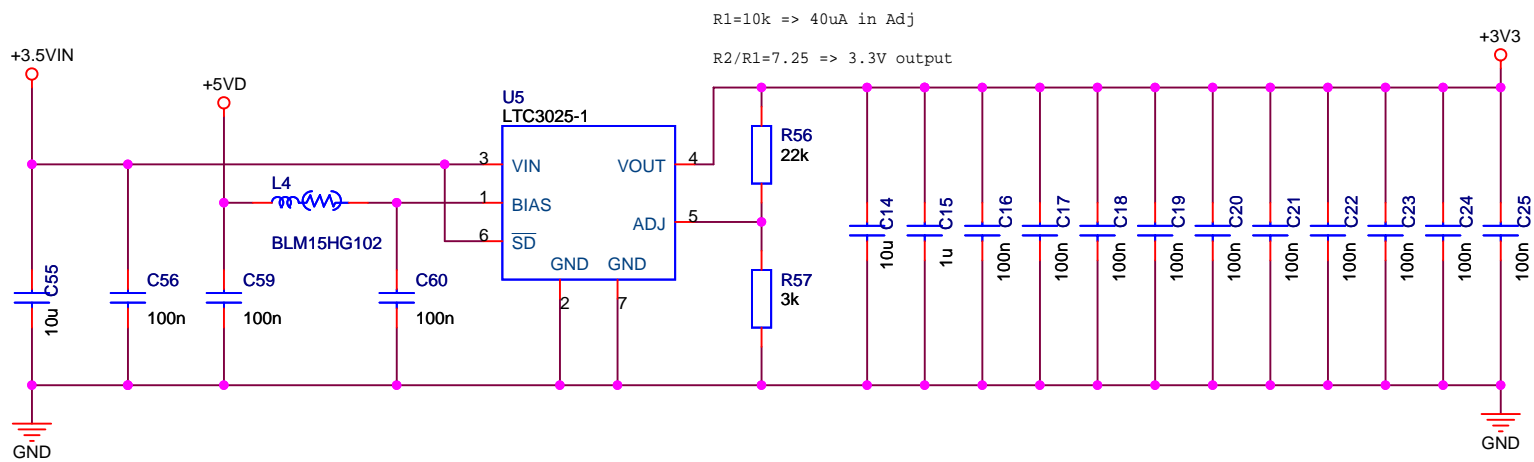
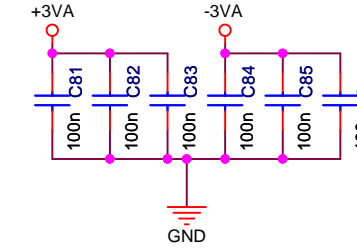
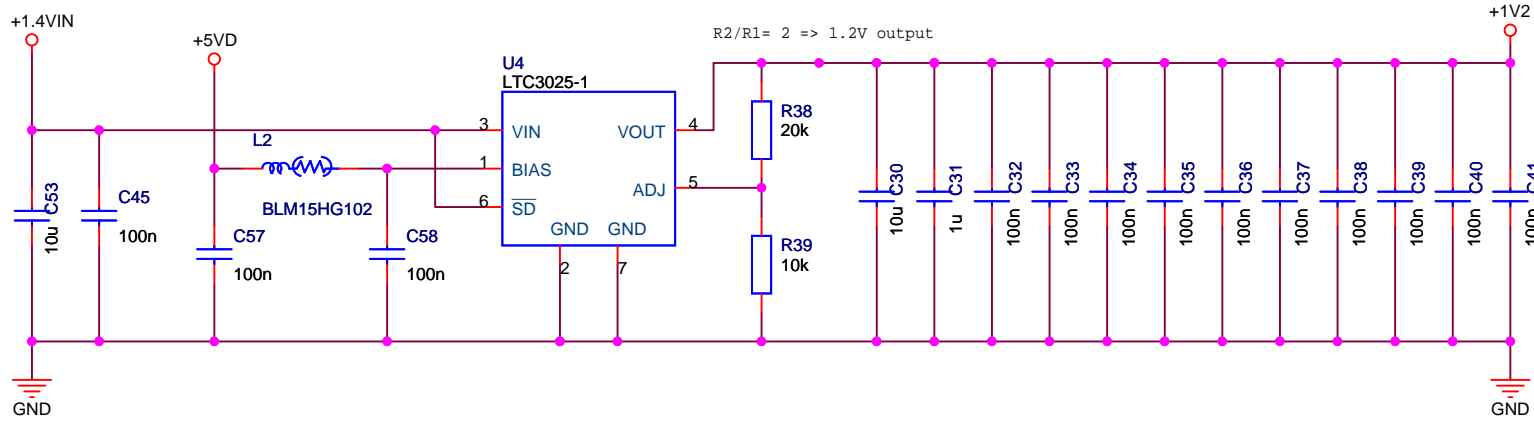
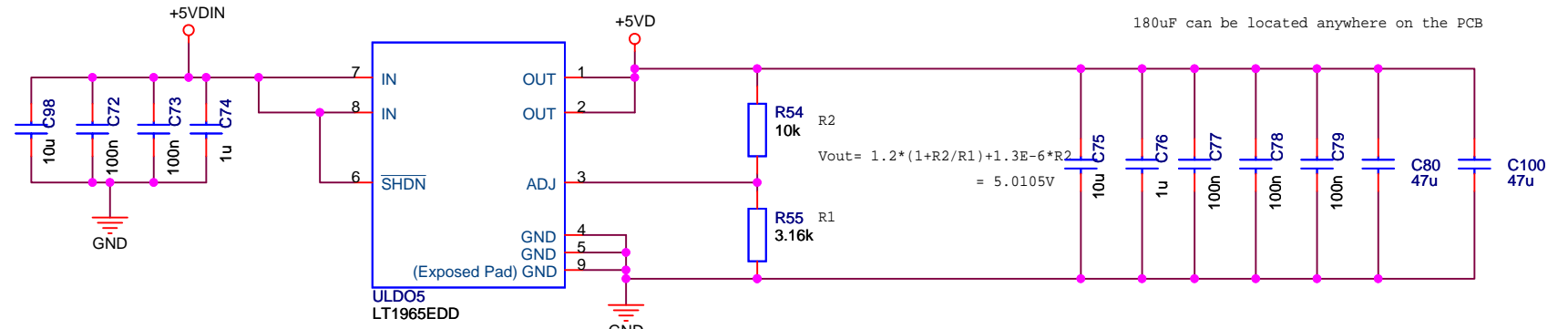
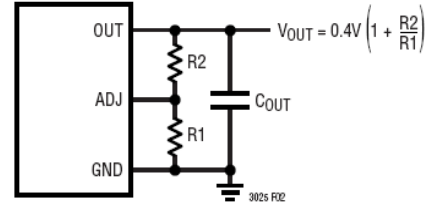
Do not equip with these LEDs for mass production



Hades-MDC-OEP3



LTC3025: 300mA



Hades-MDC-OEP3

The ADC has an input range from 0 - 4.096V

a divider ratio of 1/3 should raise the -3V to measure to +3V, provided that the +5VD is constant, which can even be corrected.

+5VD has to be divided to stay in the range of the ADC

+5VDIN has to be divided to stay in the range of the ADC

