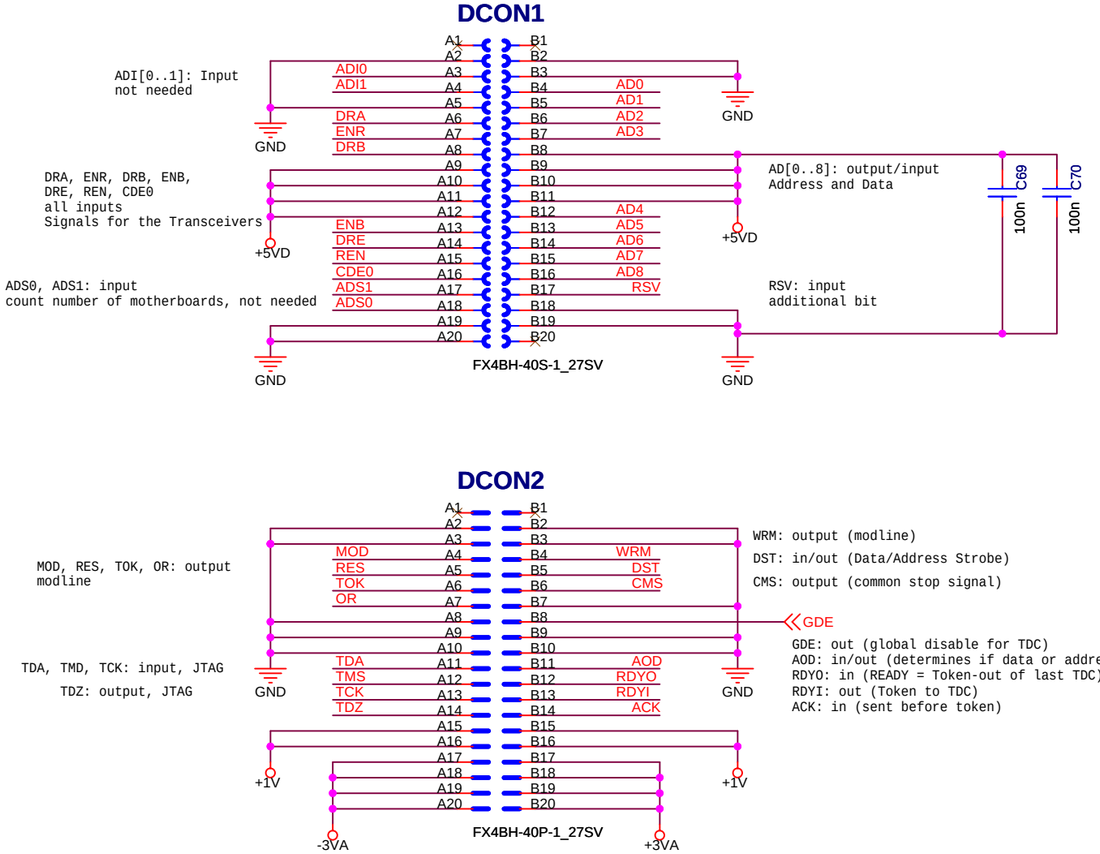
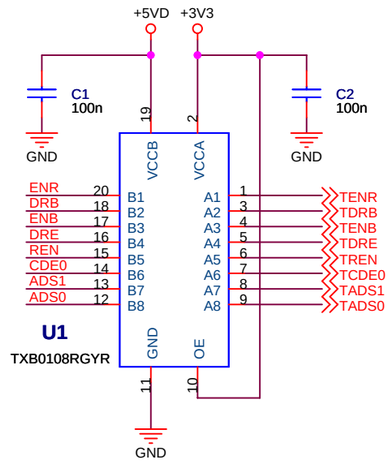
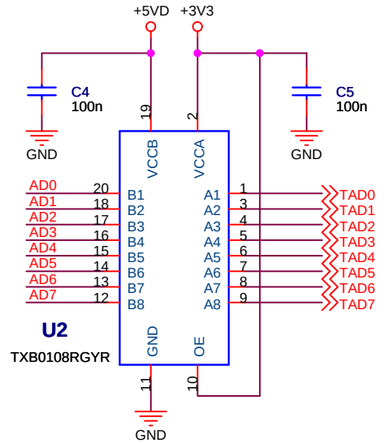
Voltage translators for 5V->3.3V and vice versa

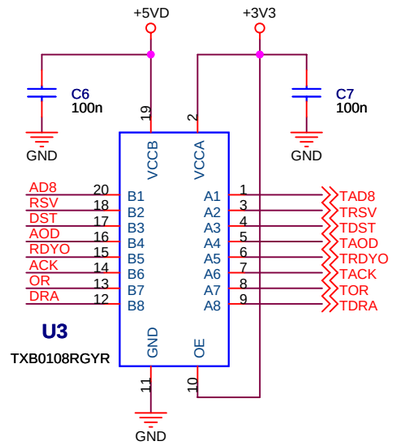
Connectors to the Motherboard

All directions are seen from this "driver card"

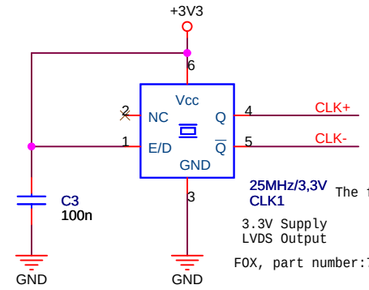


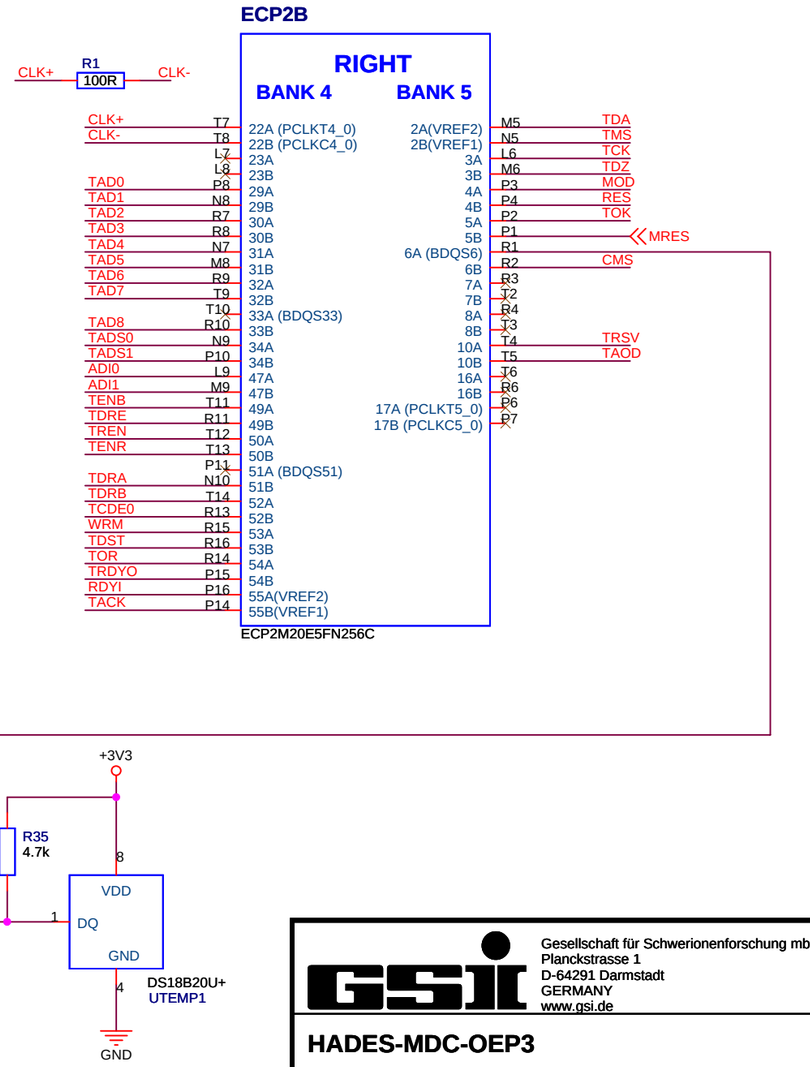






System Clock





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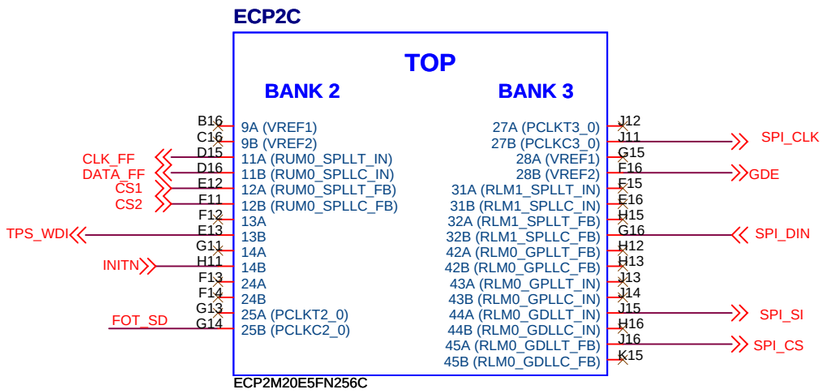
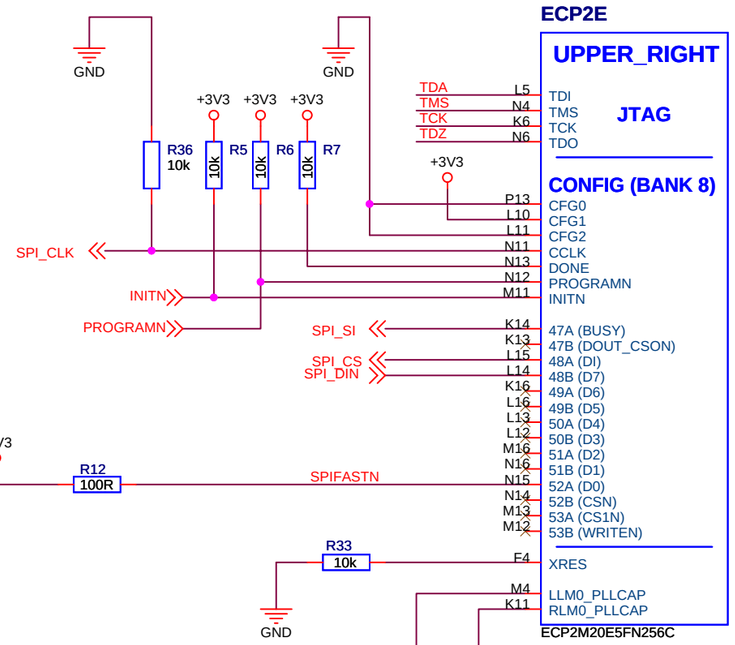
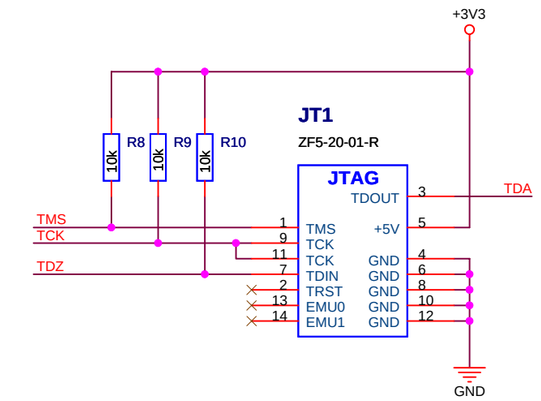
HADES-MDC-OEP3

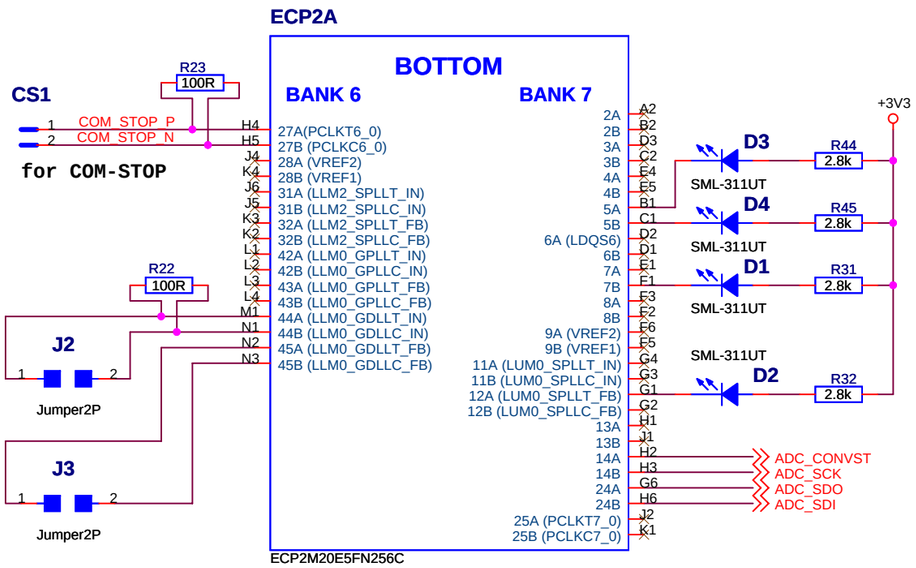
Design: K:\GSIJOB\HADES_MDC_OEP\MDC-OEP3\MDC_OEP3.DSN	
Modified: Friday, January 23, 2009	Size: A3 Page: 1 / 5
Designer: M.Traxler	Layouter: P.Skott

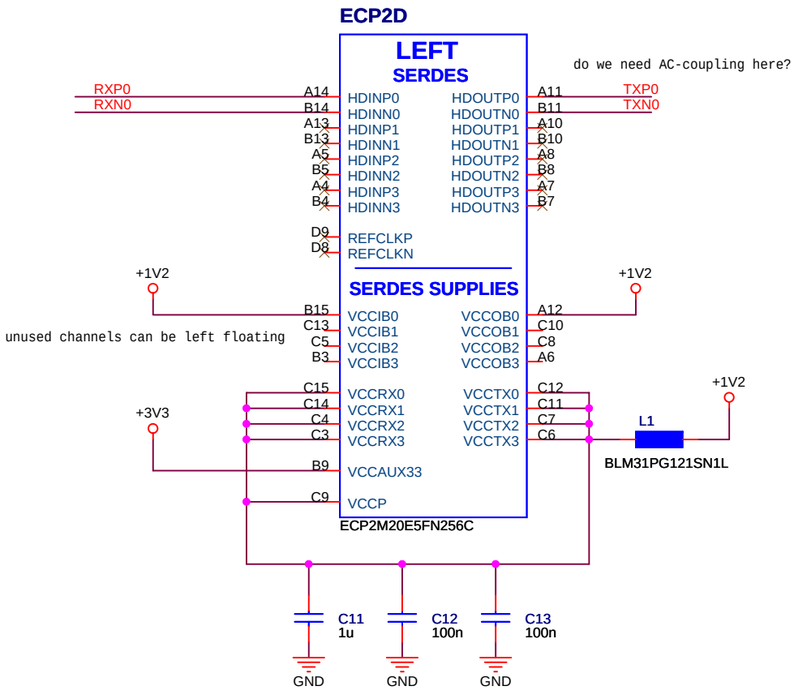
Banks 2,3,6 and 7 have 50% outputs with LVDS capability
For correct LVDS output levels the corresponding VCCIOs have to be 2.5V, which is not the case on this PCB
LVDS Inputs will work on all pairs, even with VCCIO at 3.3V

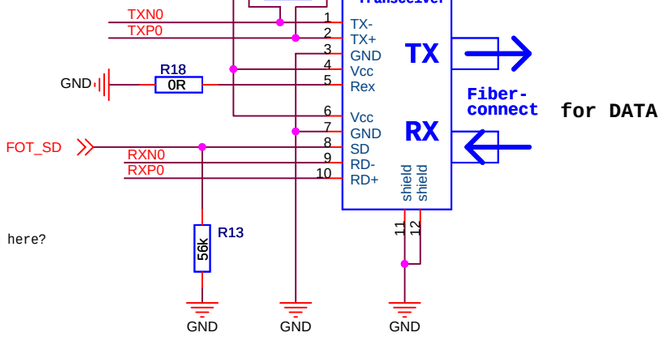












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Hades-MDC-OEP3

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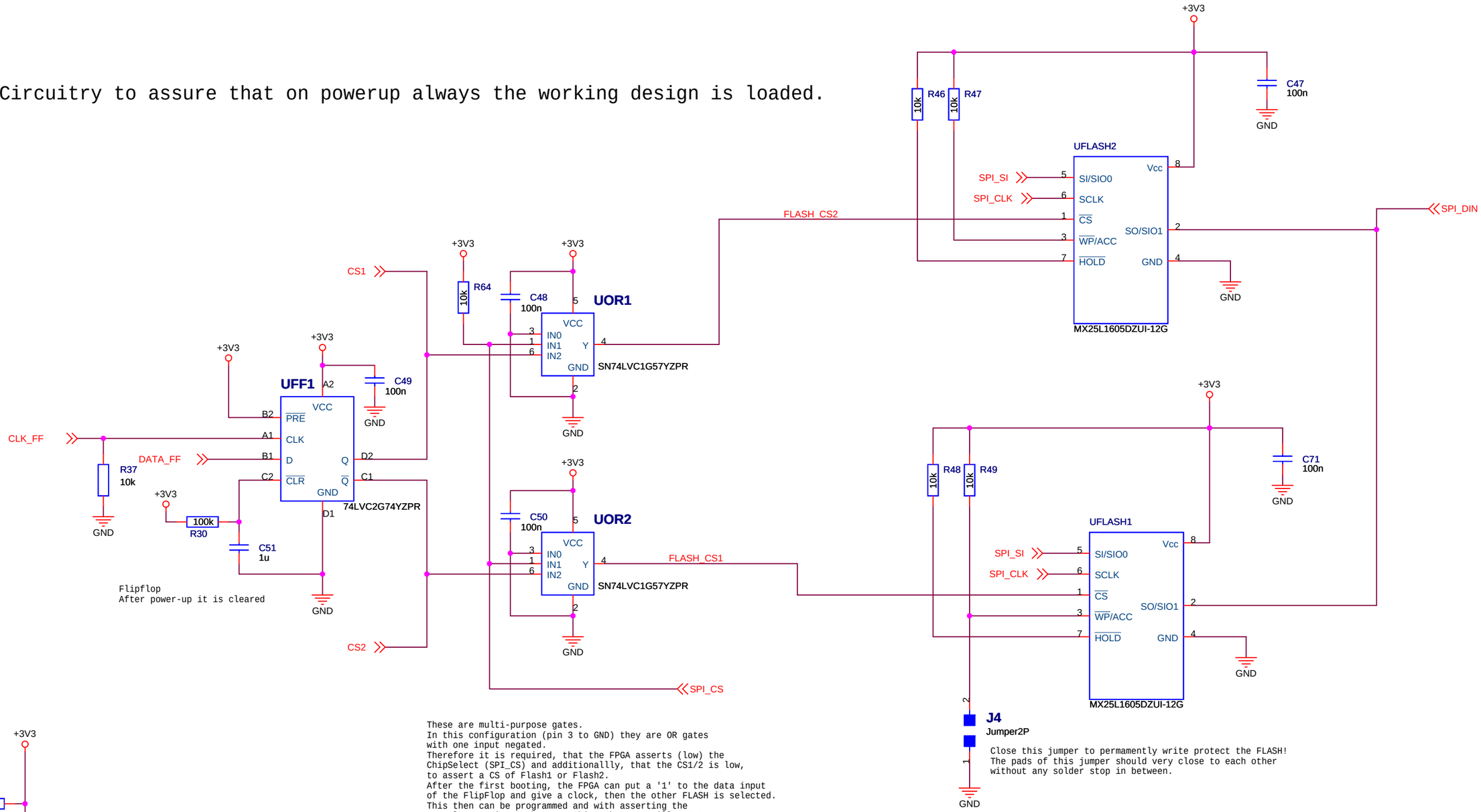
Modified: Friday, January 23, 2009	Size: A3	Page: 2 / 5
Designer: M.Traxler	Layouter: P.Skott	

Circuitry to assure that on powerup always the working design is loaded.



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Hades-MDC-OEP3	
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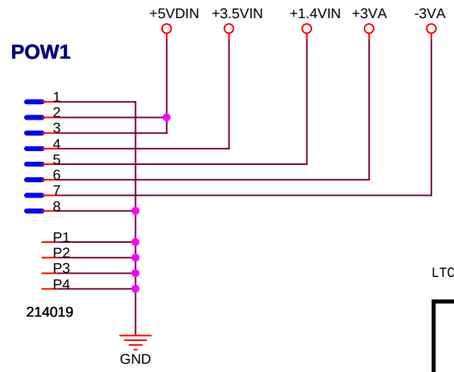
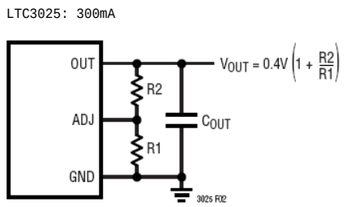
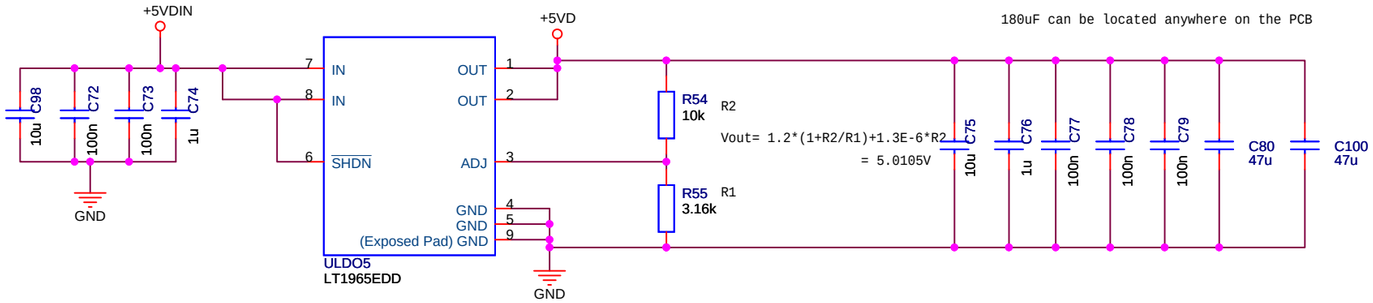
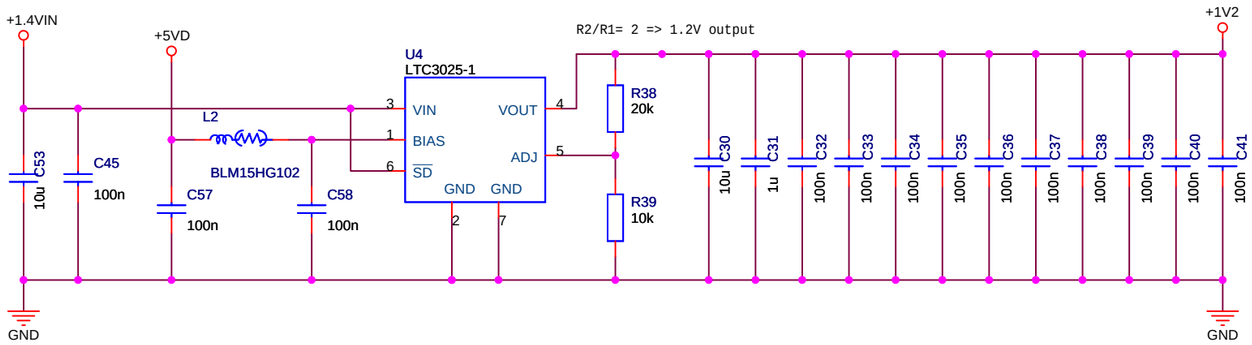
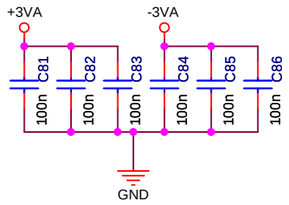
Modified: Friday, January 23, 2009	Size: A3 Page: 3 / 5
Designer: M.Traxler	Layouter: P.Skott

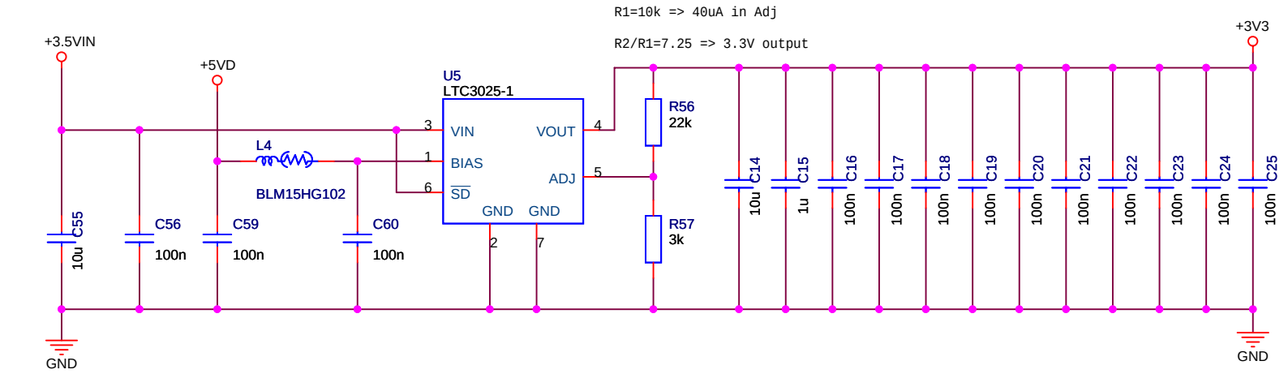


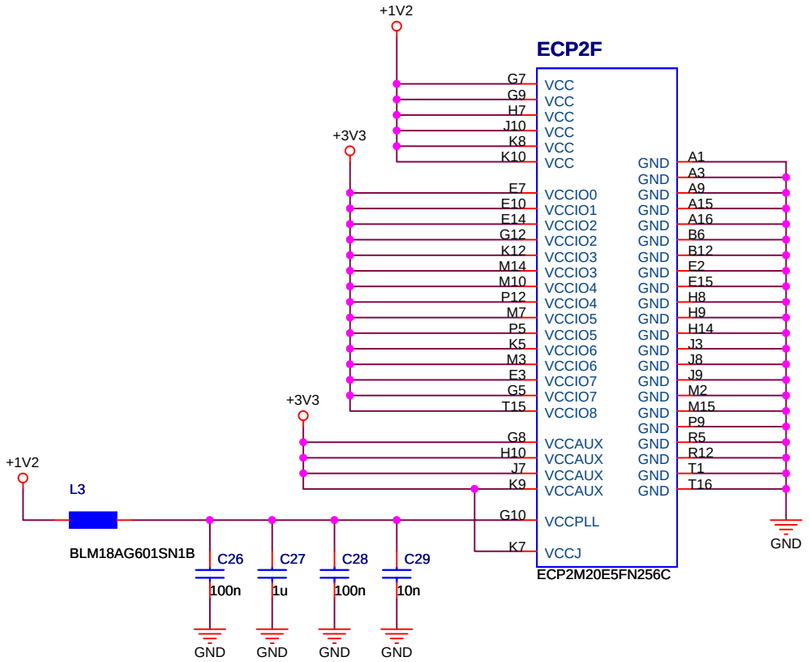


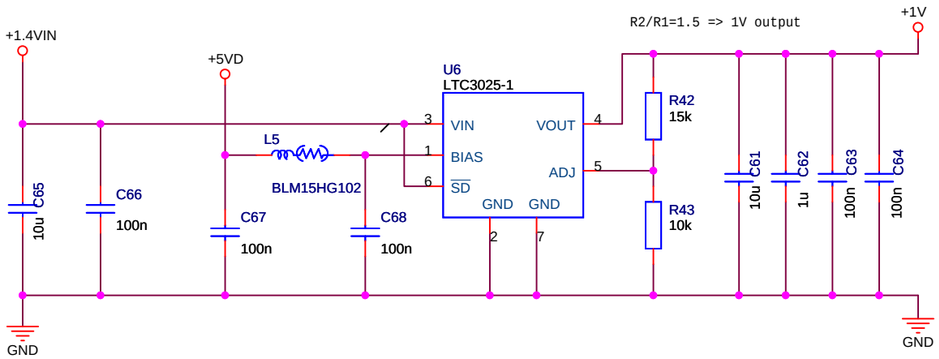












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Designer: M.Traxler	Layouter: P.Skott

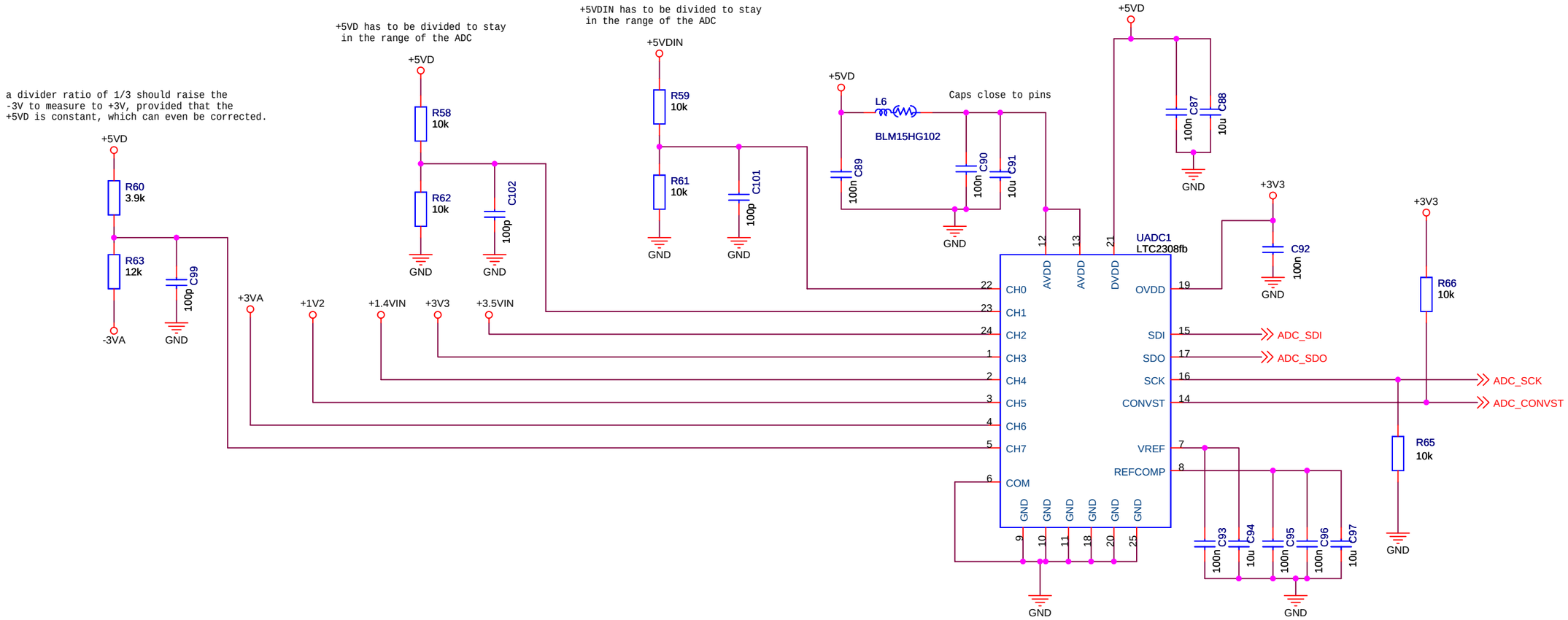
The ADC has an input range from
0 - 4.096V

a divider ratio of 1/3 should raise the
-3V to measure to +3V, provided that the
+5VD is constant, which can even be corrected.

+5VD has to be divided to stay
in the range of the ADC

+5VDIN has to be divided to stay
in the range of the ADC

Caps close to pins



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HadesMDC-OEP3	**ADC**
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Designer: M.Traxler	Layouter: P.Skott