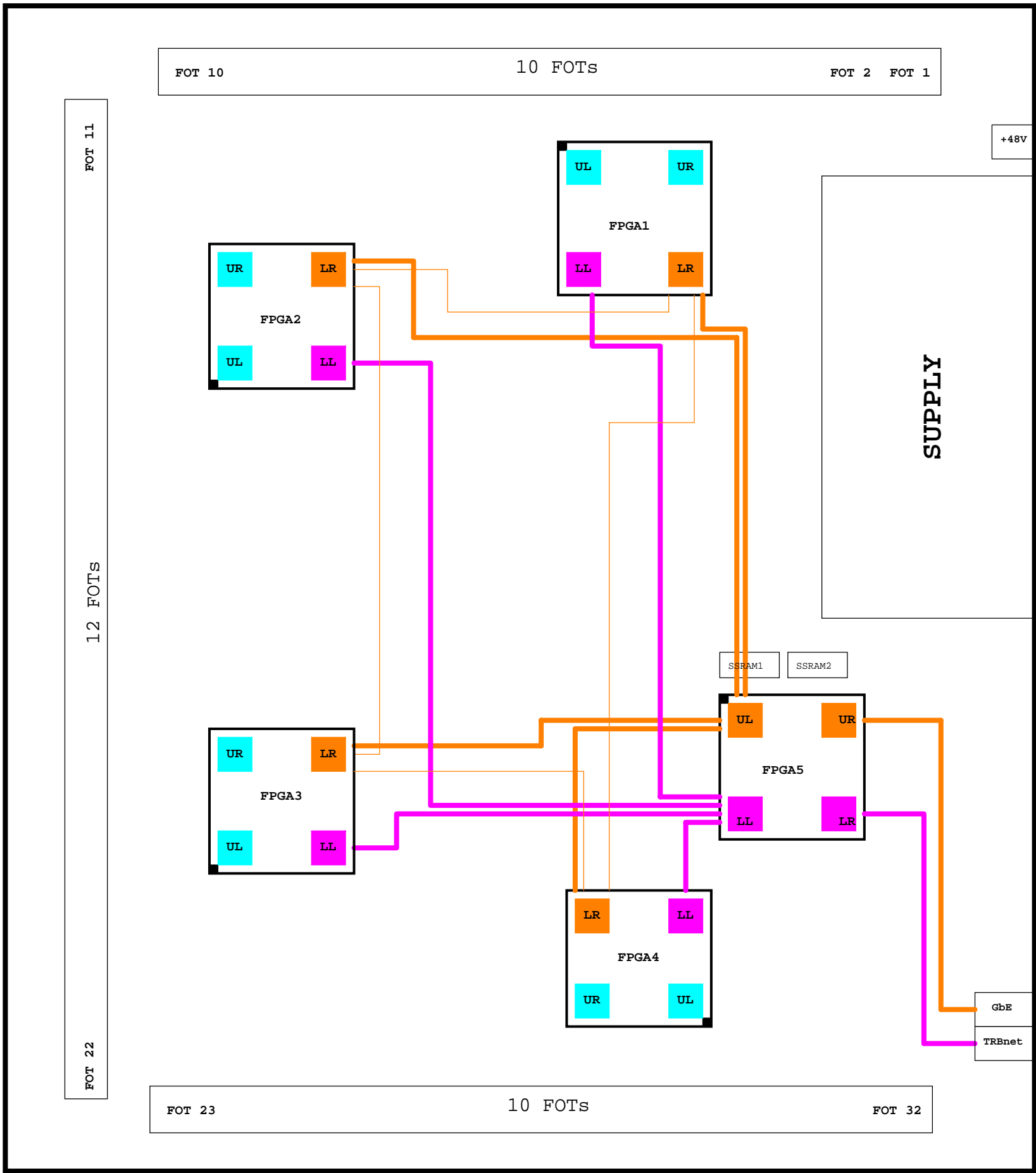


# TOP VIEW

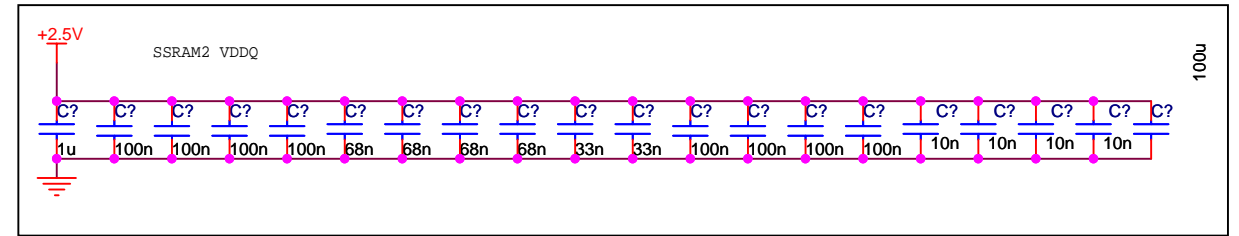
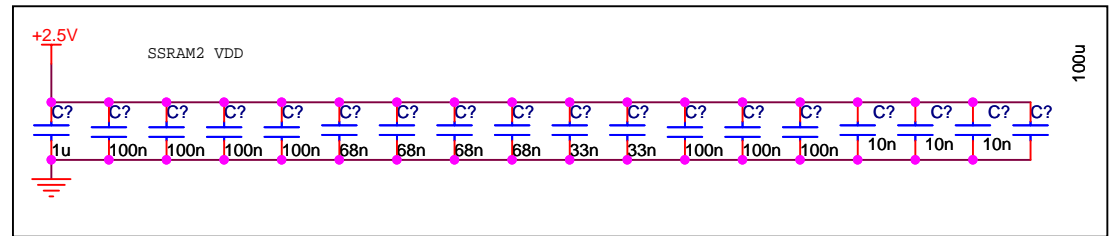
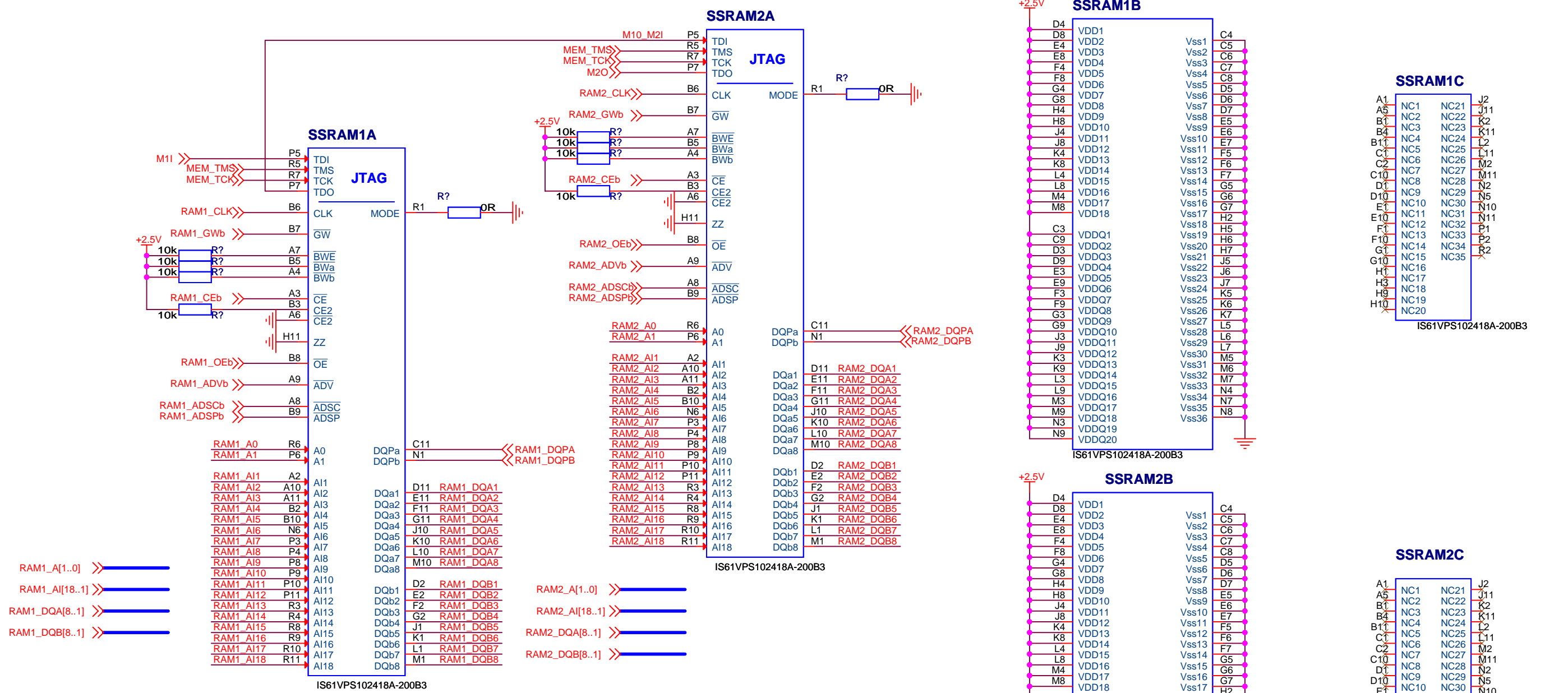
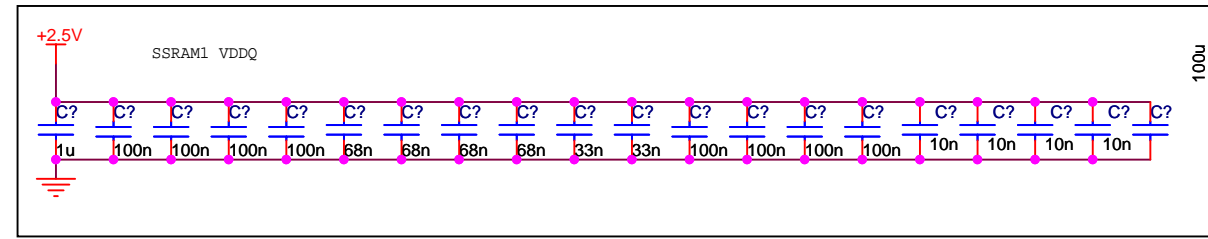
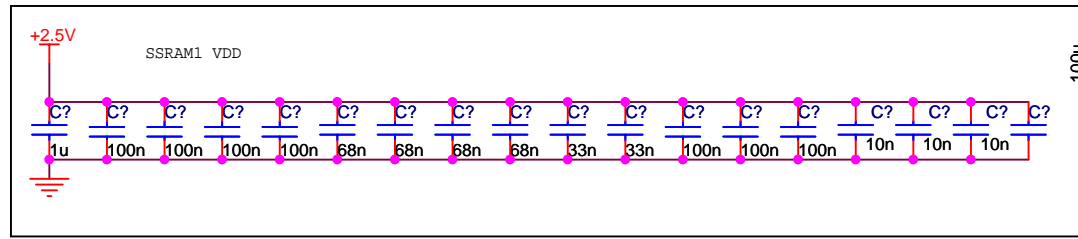
What one sees when addon card is connected to TRB and trb is under addon

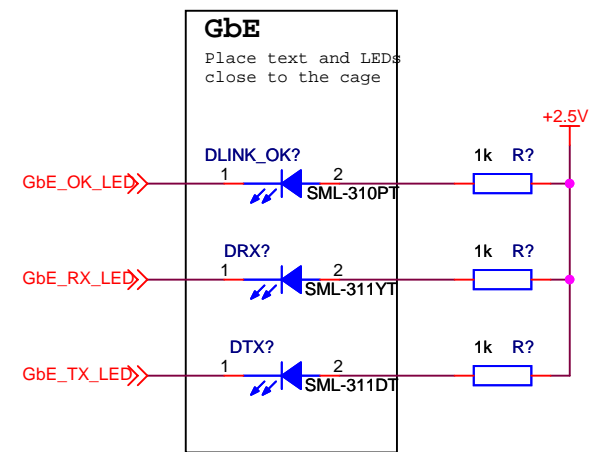
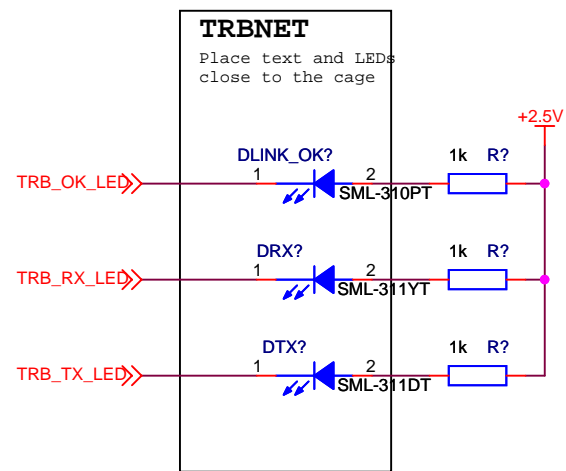
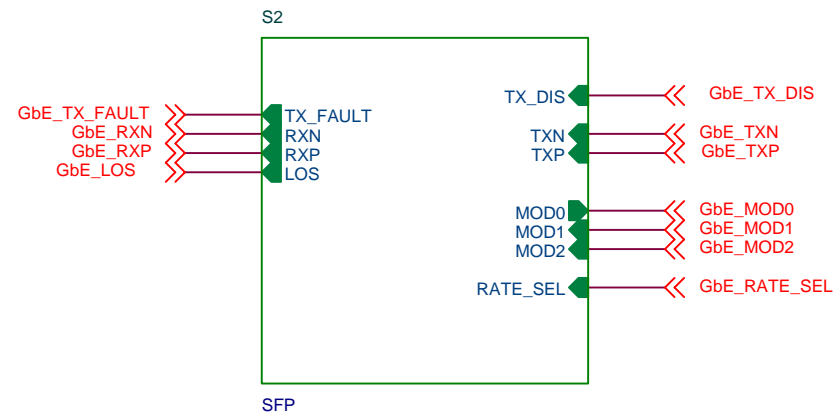
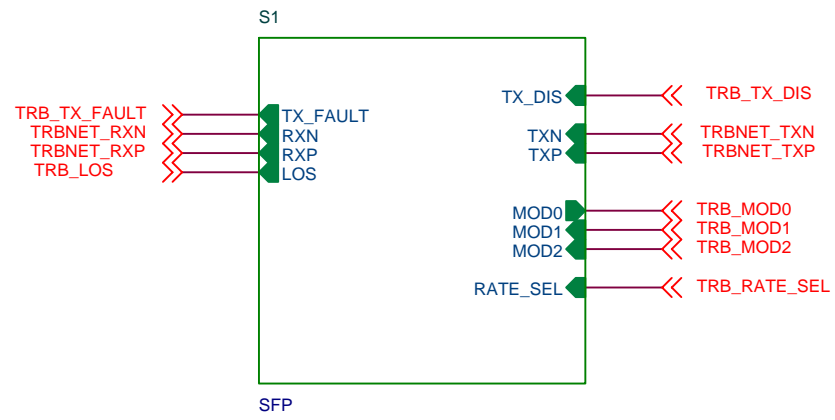


- 25 MHz
- 100 MHz
- 125 MHz
- MAIN DATA STREAM
- INTER FPGA COMM

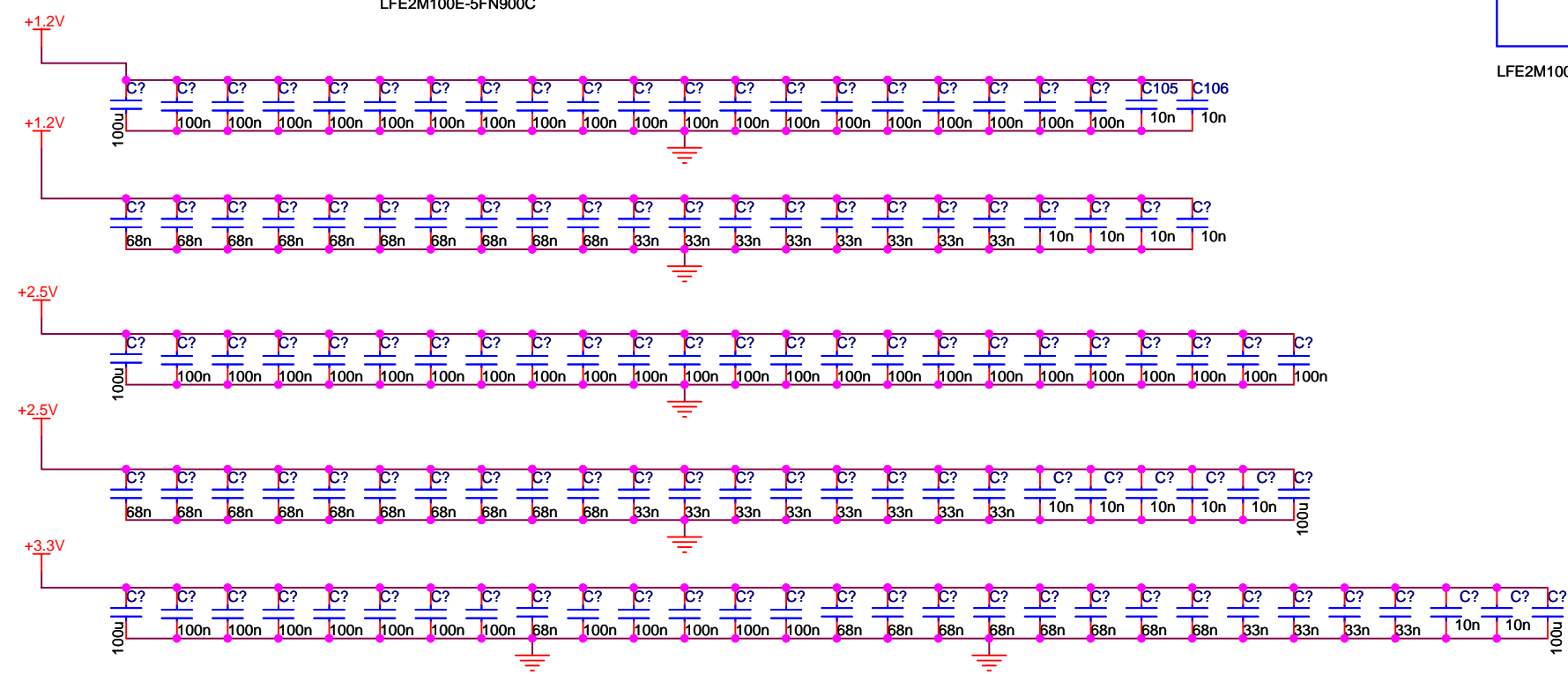
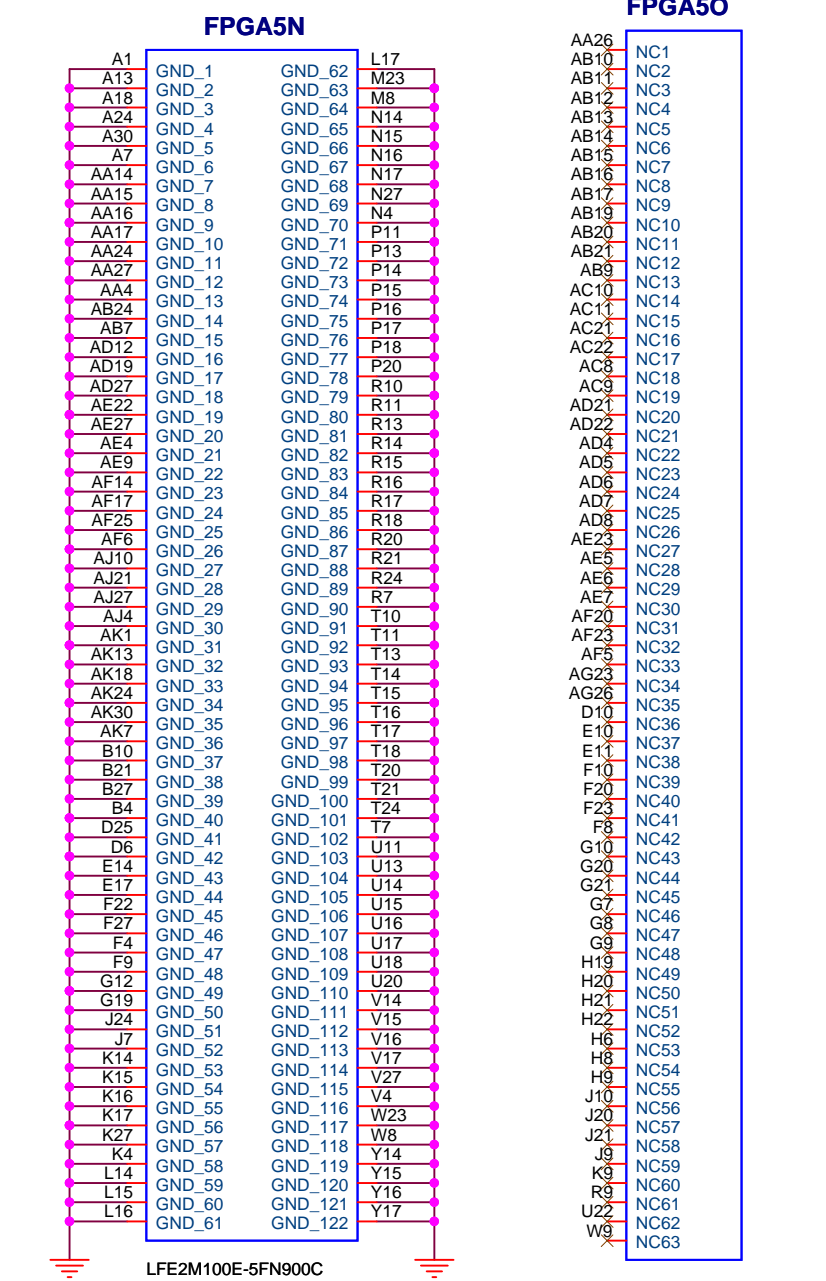
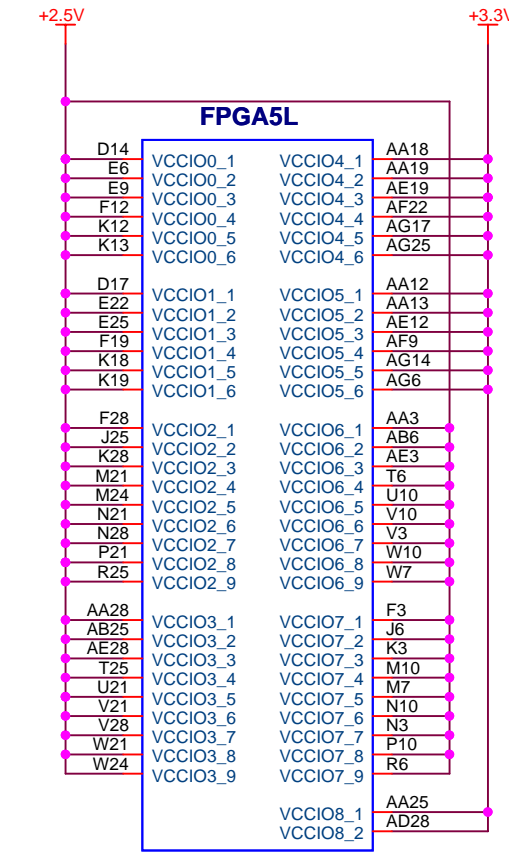
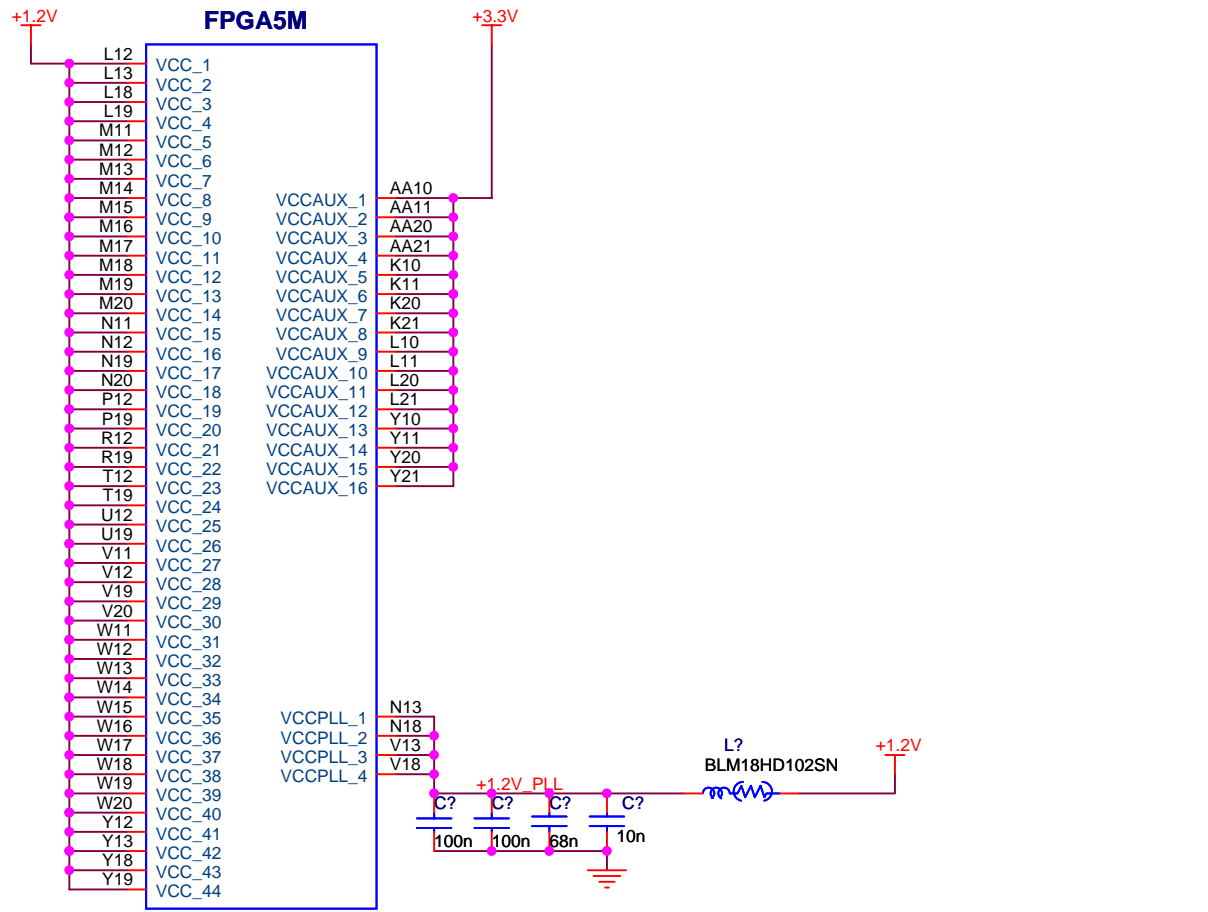


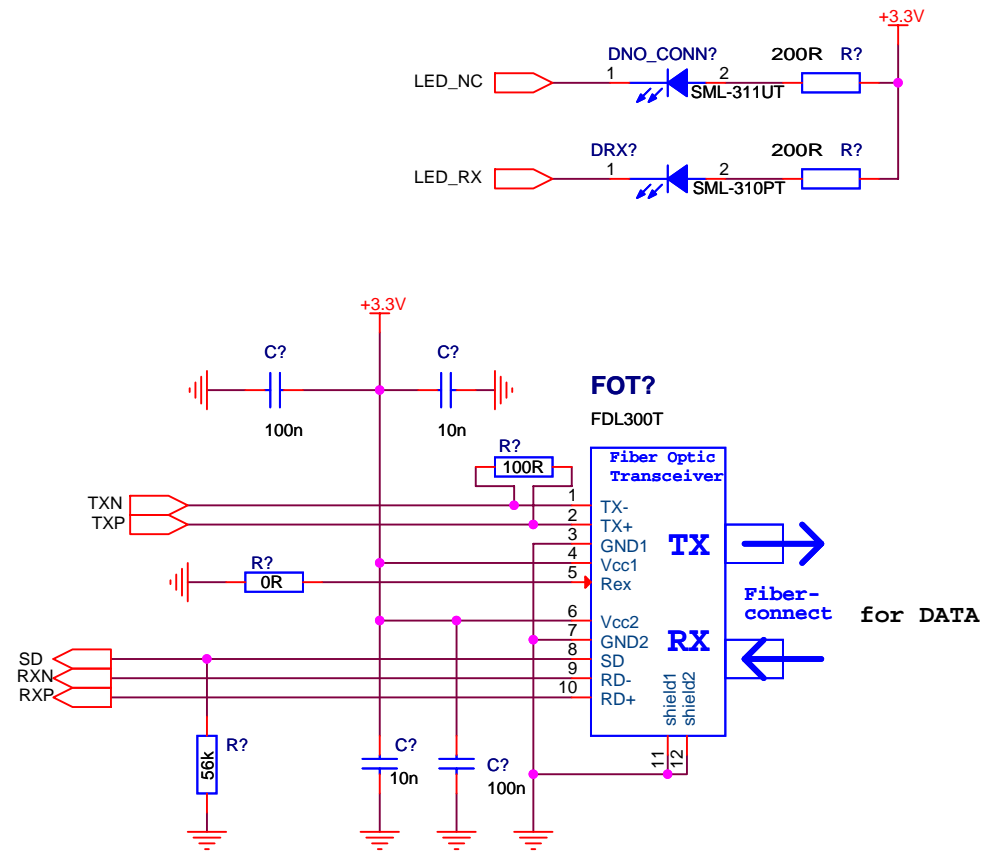
Title			<b>01_FOT_CONNECTS</b>		
Size	Document Number				Rev
A3	<Doc>				<RevC
Date:	Tuesday, February 09, 2010	Sheet	1	of	1



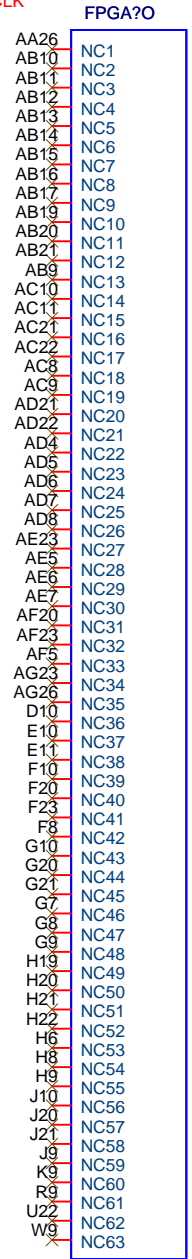
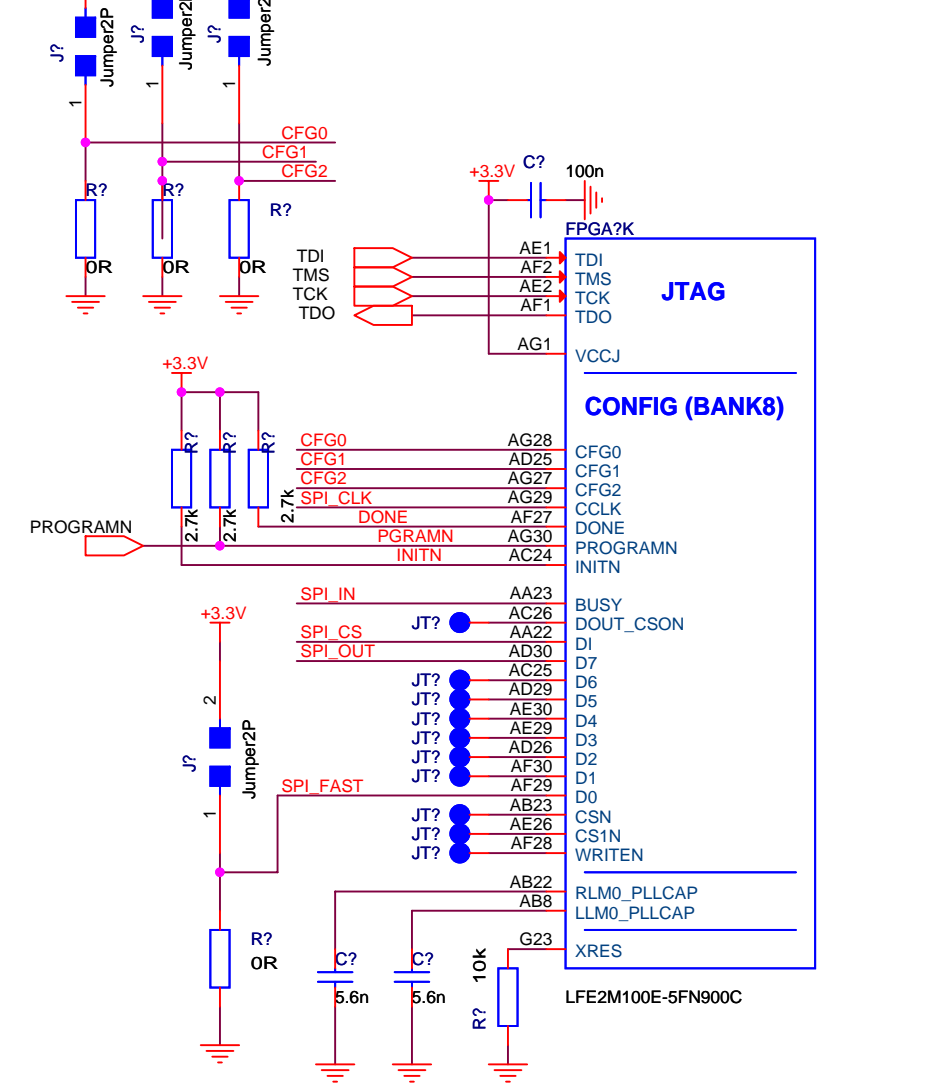
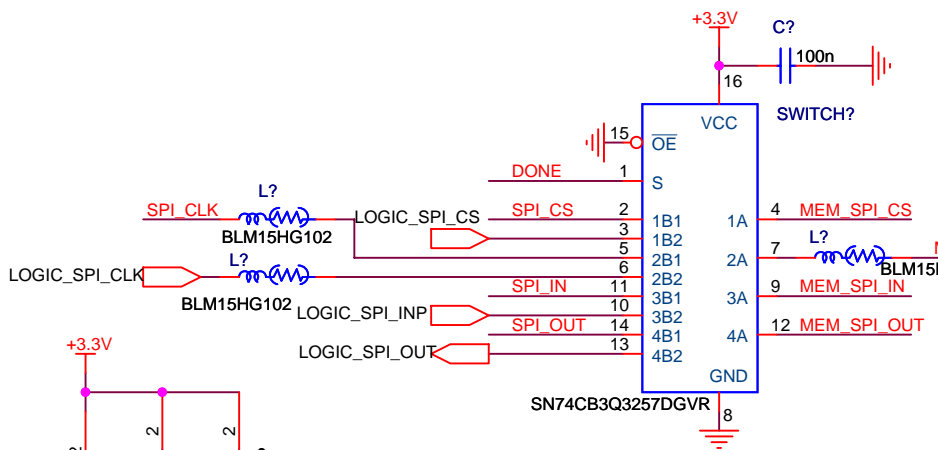
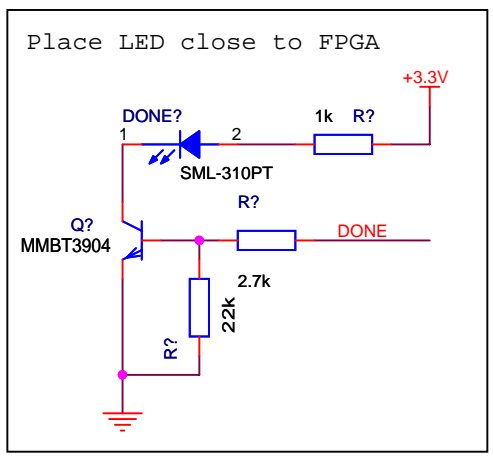
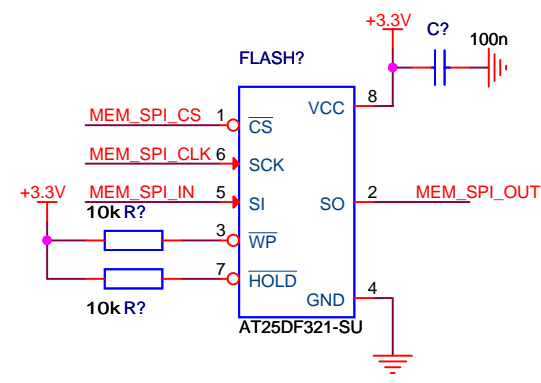


Title		
<b>03_SFP_CONNECTS</b>		
Size	Document Number	Rev
A3	<Doc>	<RevC
Date:	Monday, February 22, 2010	Sheet 1 of 1

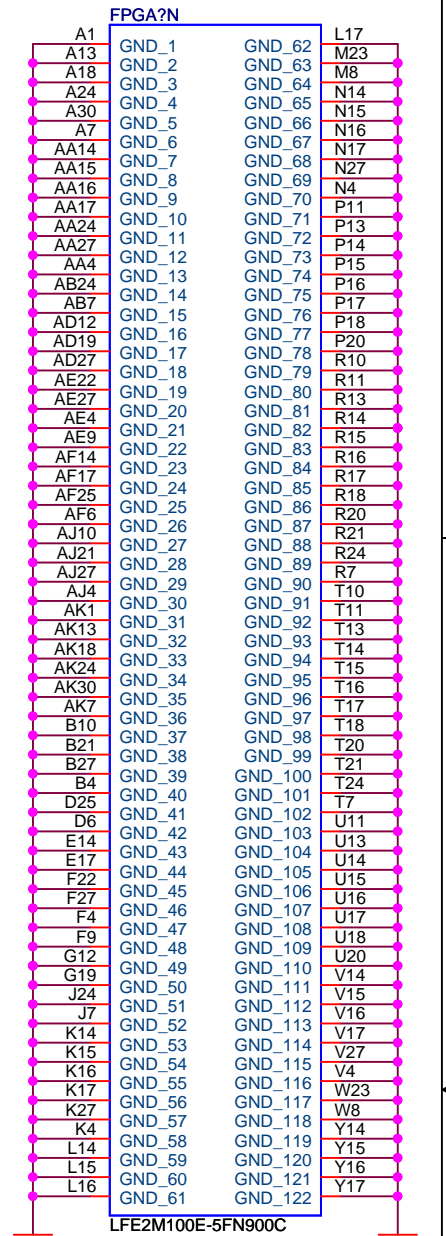
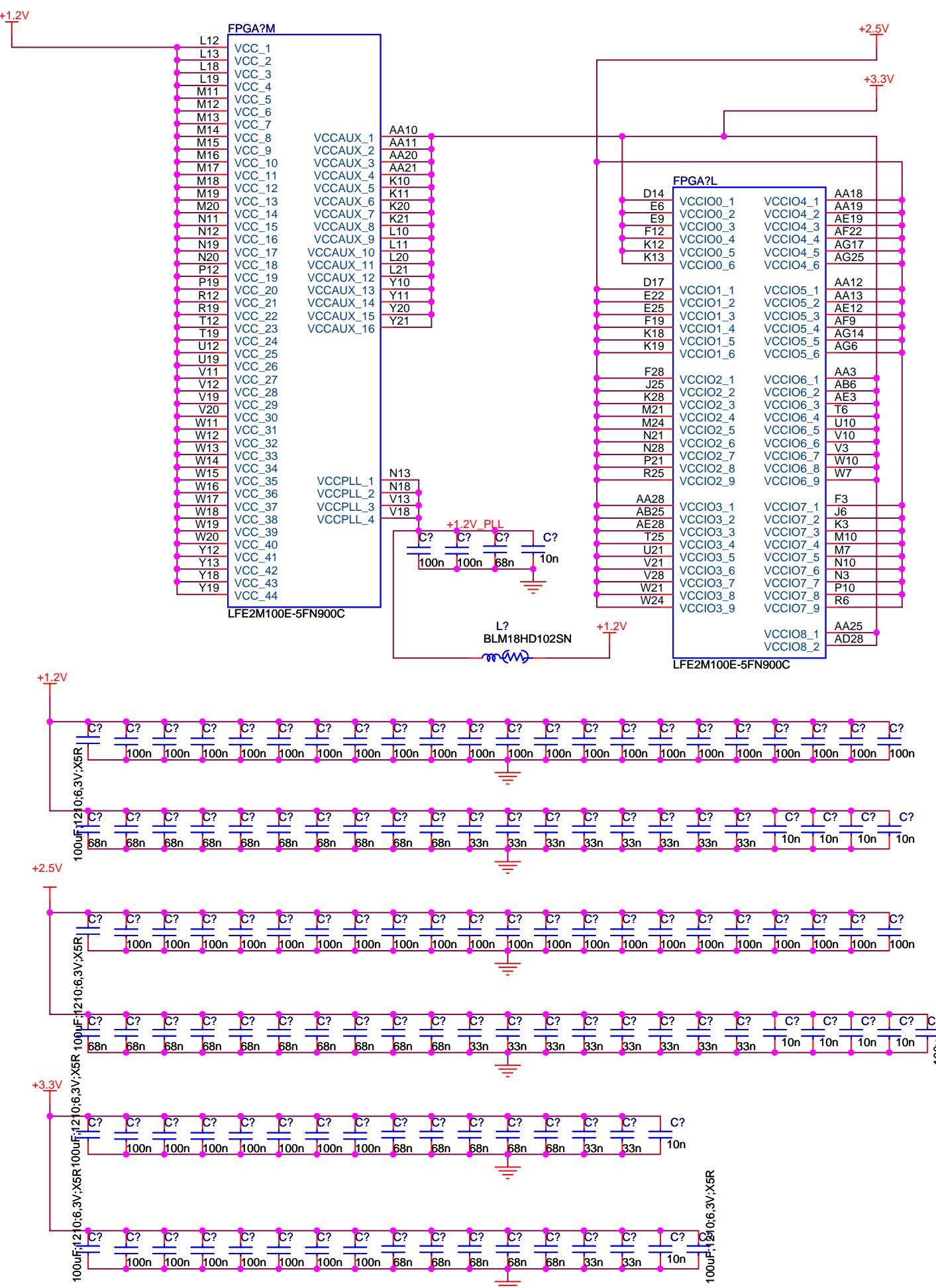




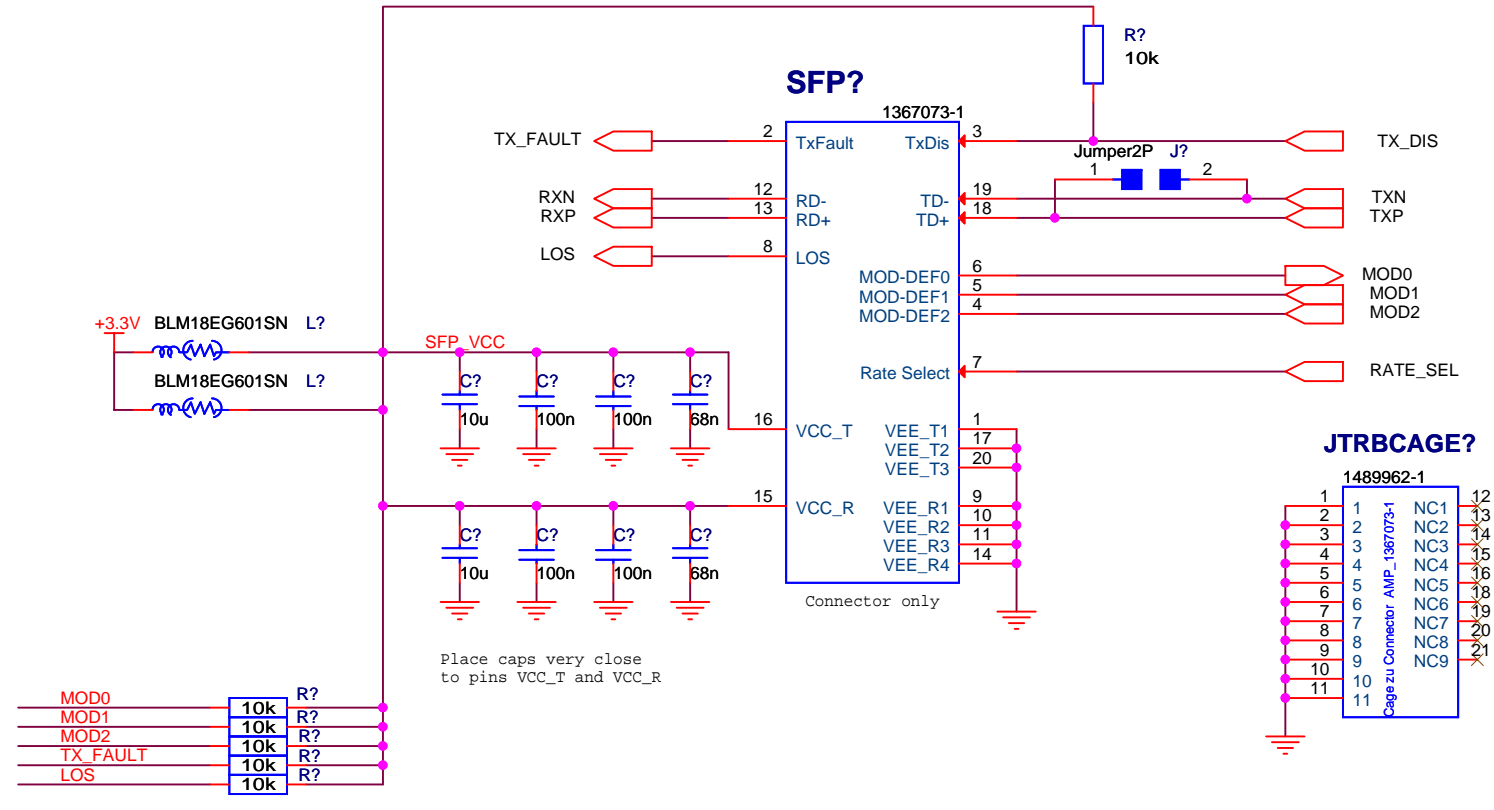
Title			<b>FOT</b>		
Size	Document Number	Rev			
A3	<Doc>	<RevC>			
Date:	Monday, February 22, 2010	Sheet	1	of	1



LFE2M100E-5FN900C

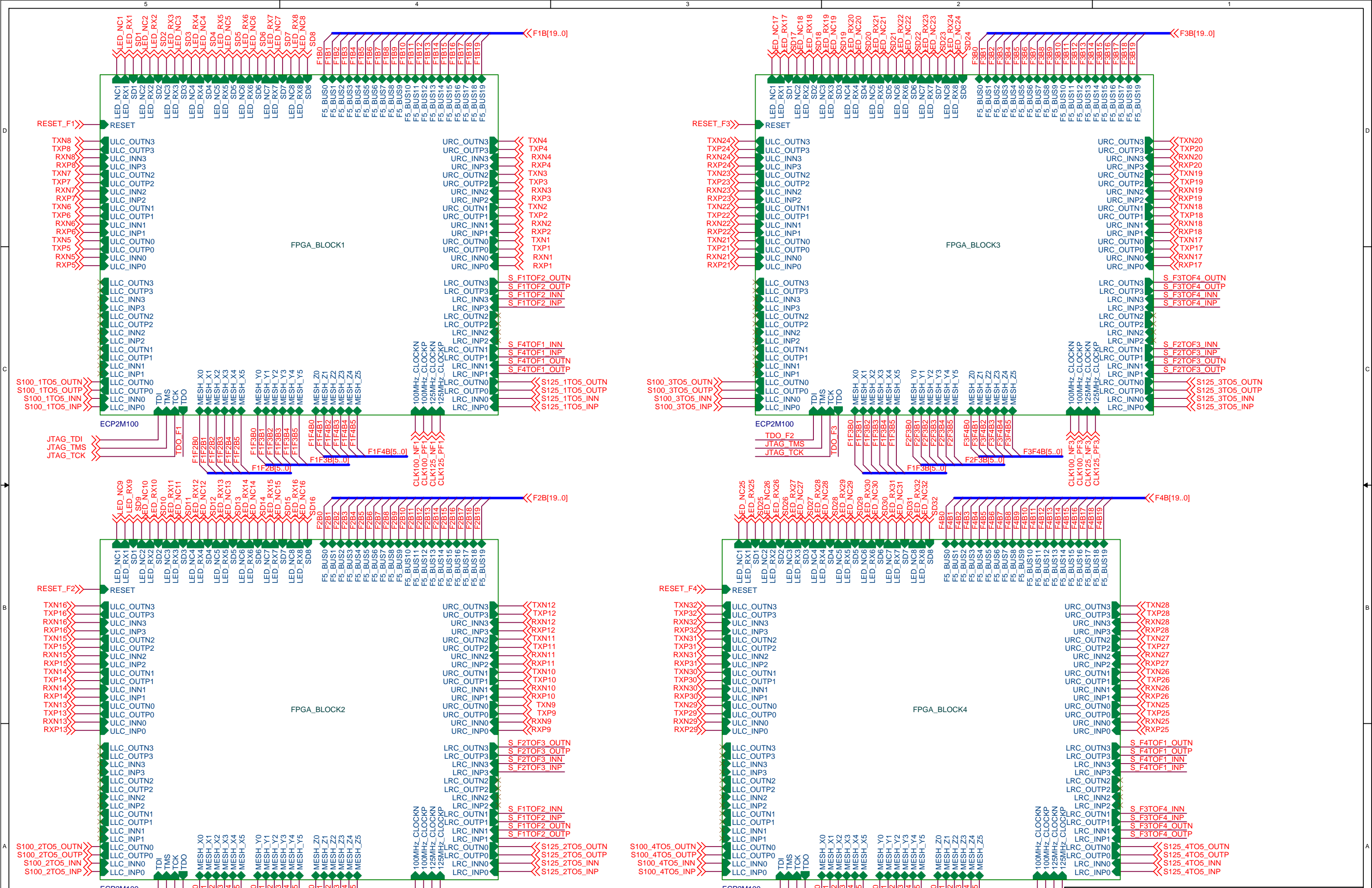


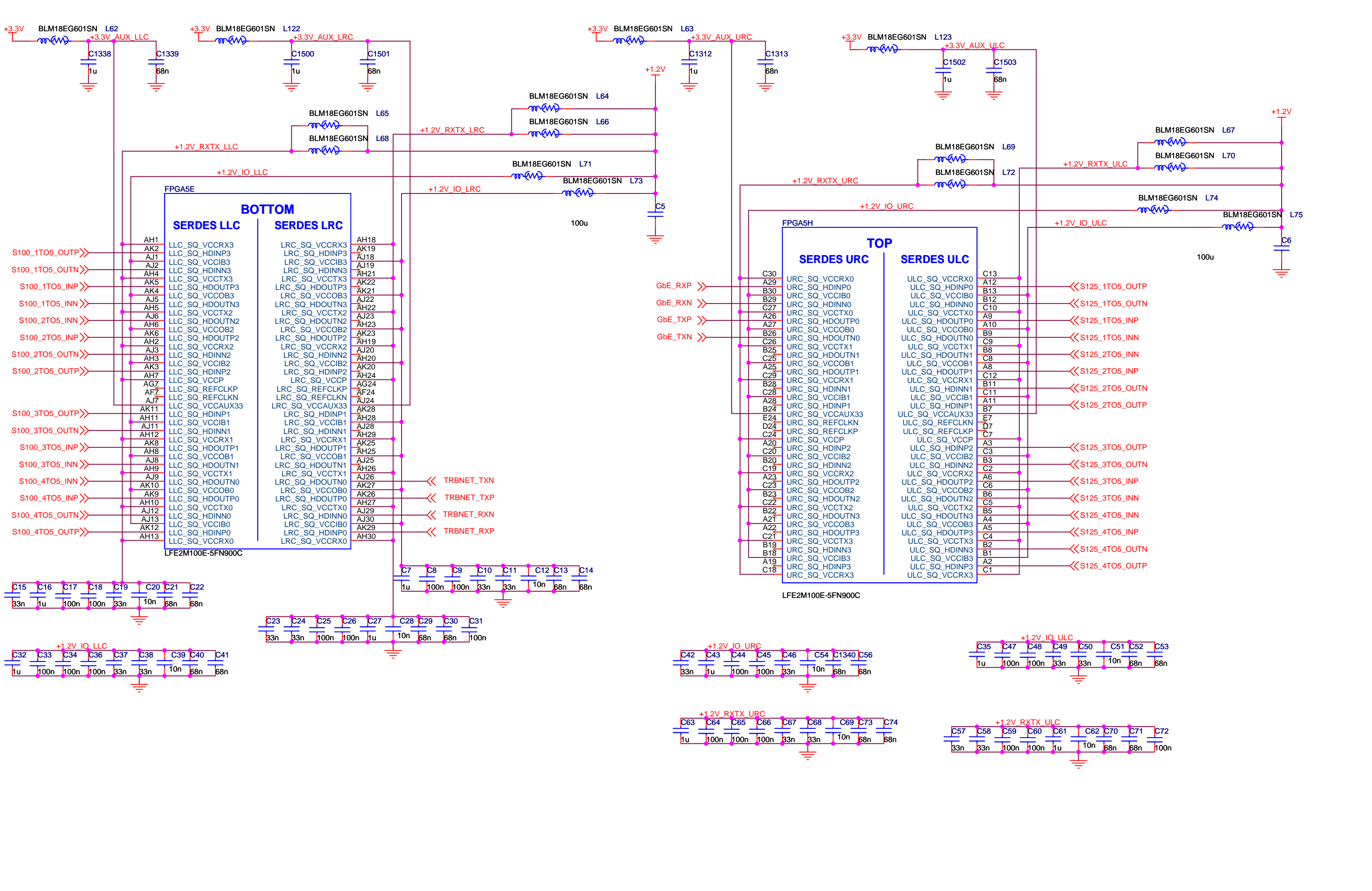
LFE2M100E-5FN900C



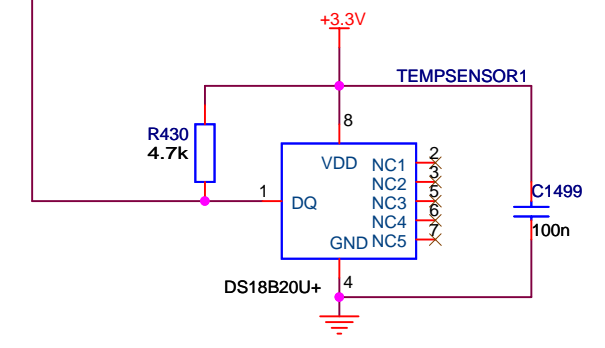
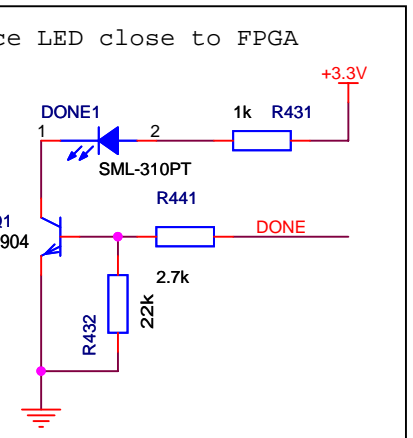
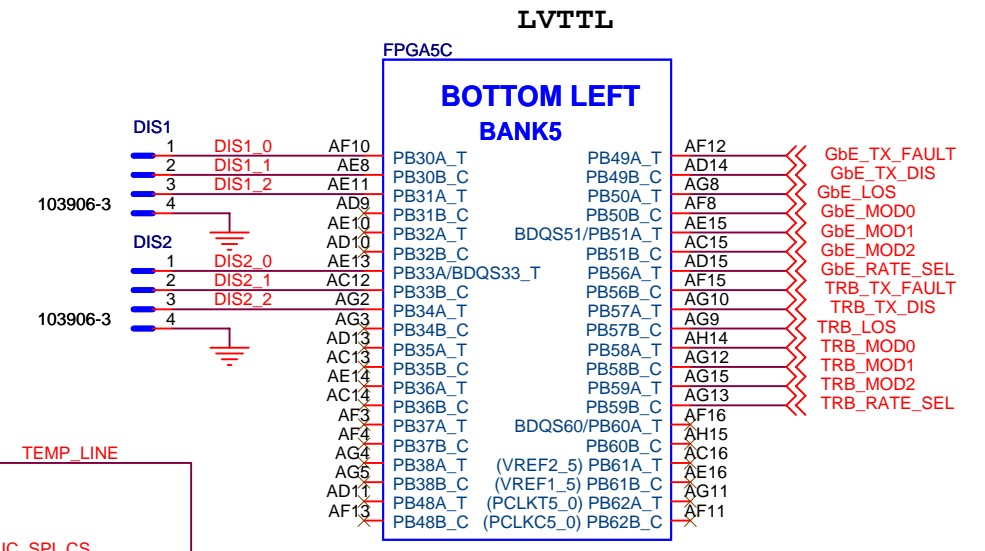
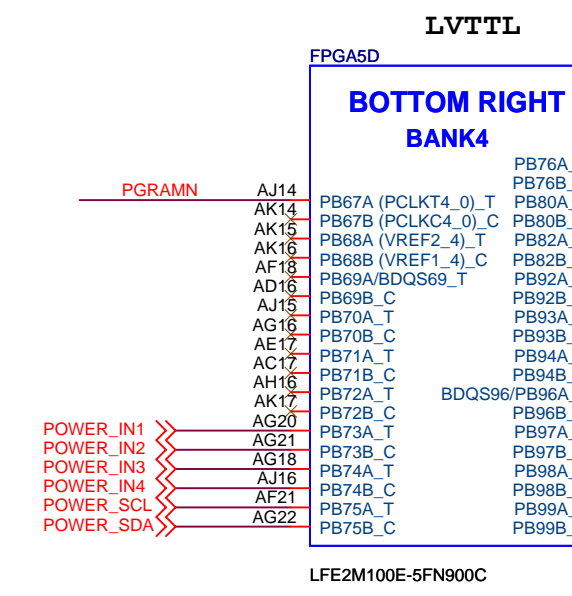
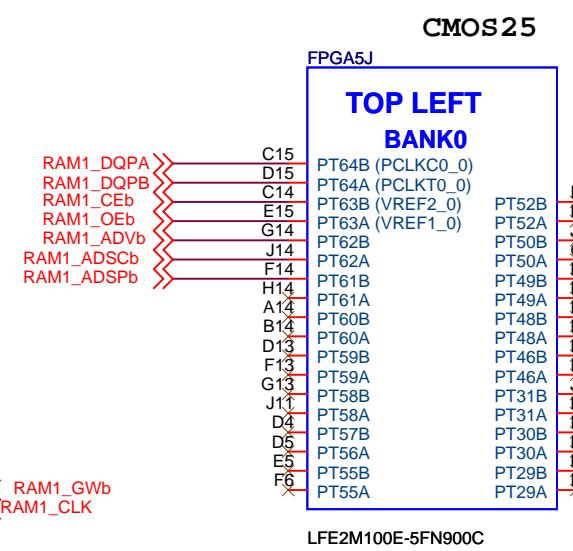
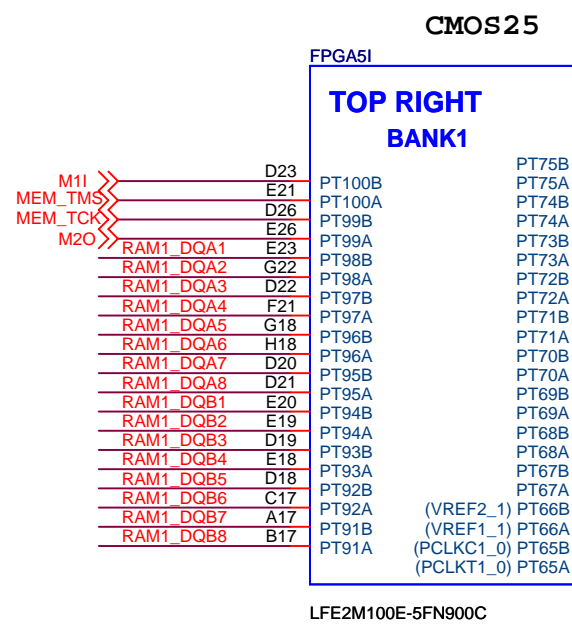
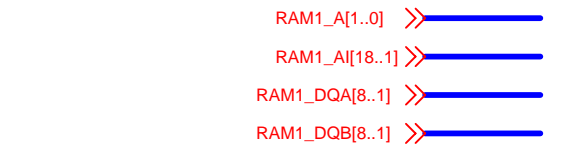
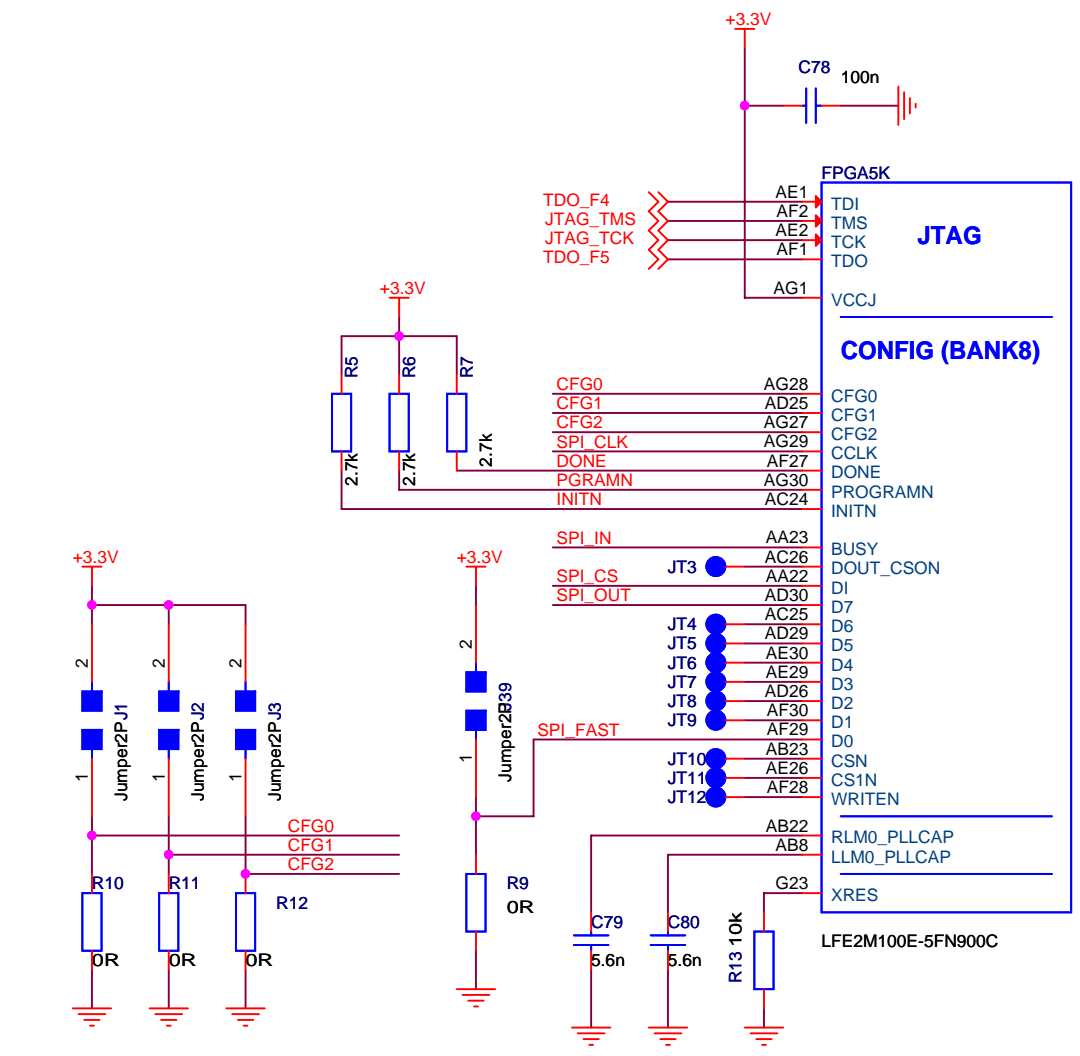
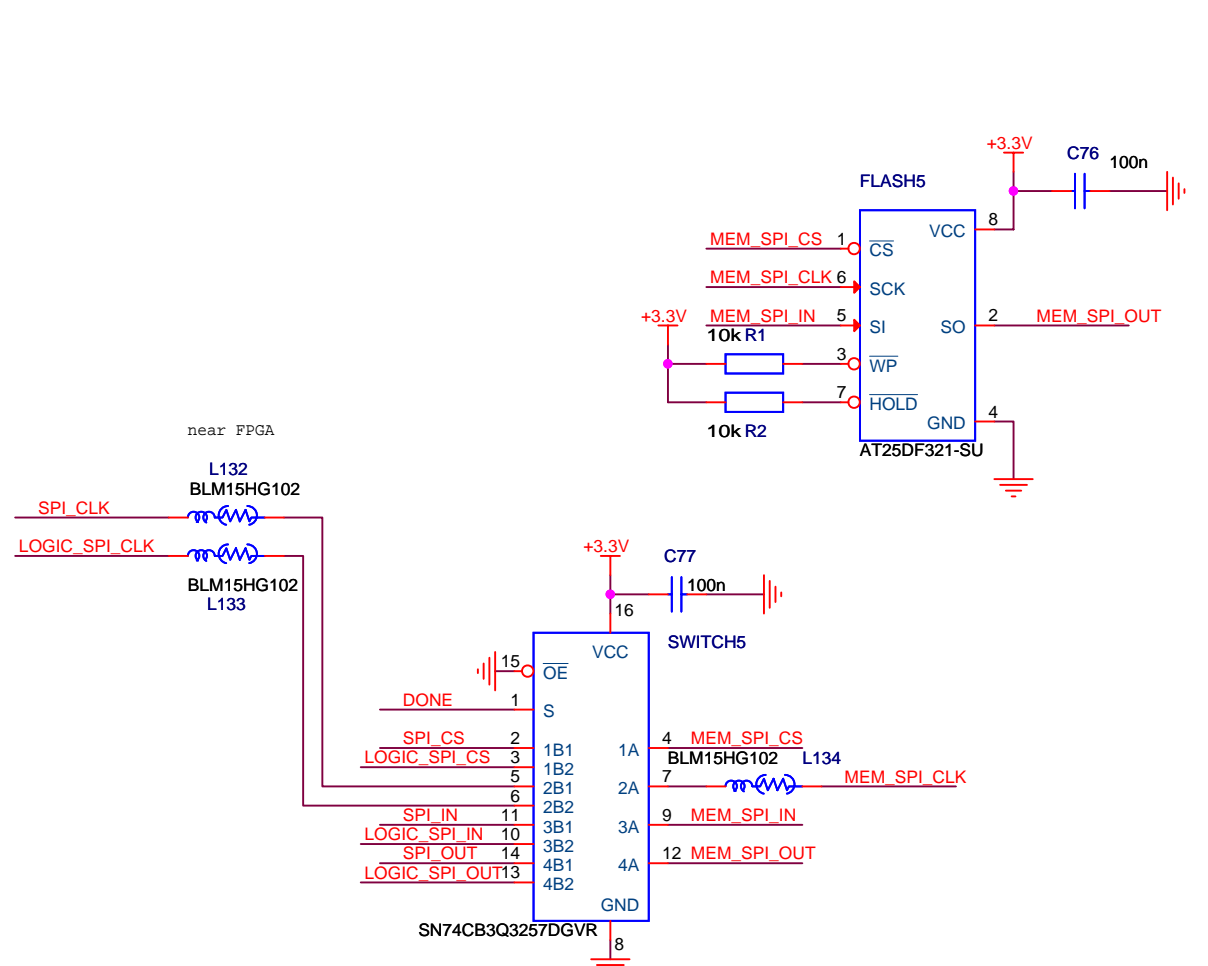
MODDEF0 is grounded by module when inserted





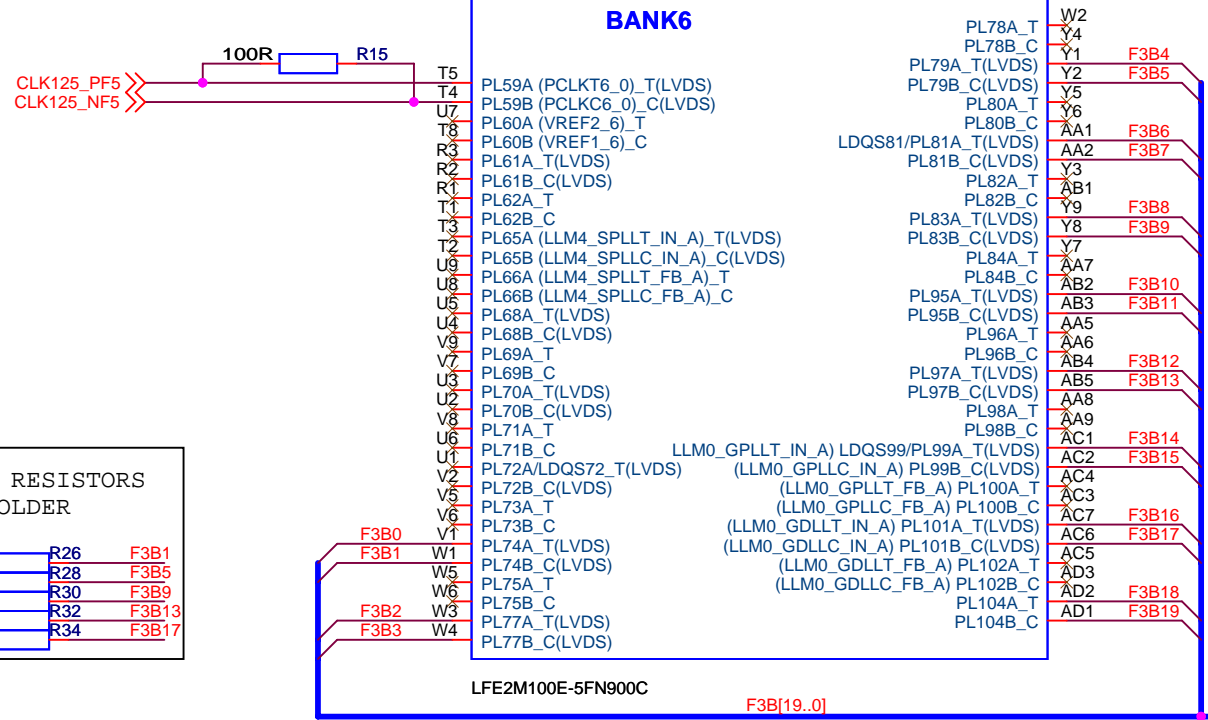


Title			<b>05_FPGA_5_SERDES</b>		
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### FPGA5B CMOS25/LVDS

#### LOWER LEFT BANK6

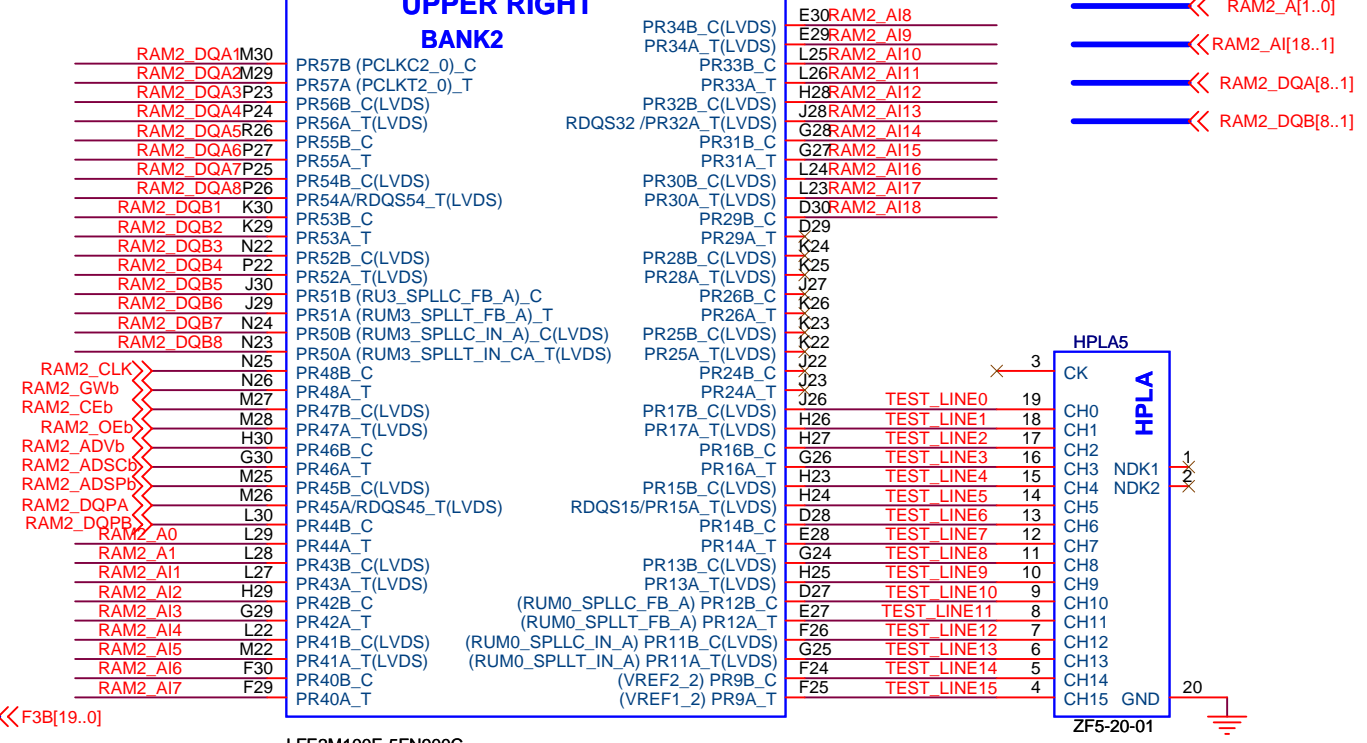


**OPTIONAL RESISTORS DO NOT SOLDER**

F3B0 100R	R26	F3B1
F3B4 100R	R28	F3B5
F3B8 100R	R30	F3B9
F3B12 100R	R32	F3B13
F3B16 100R	R34	F3B17

### FPGA5G CMOS25/LVDS

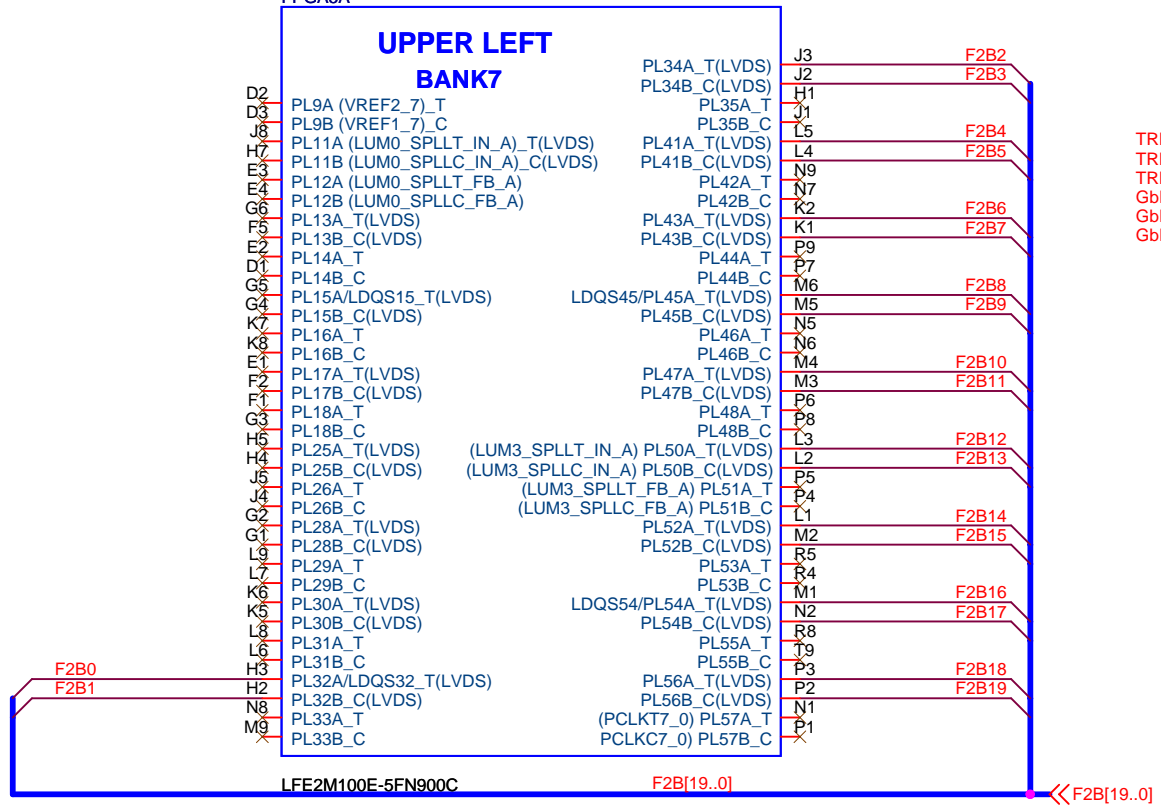
#### UPPER RIGHT BANK2



- RAM2\_A[1..0]
- RAM2\_AI[18..1]
- RAM2\_DQA[8..1]
- RAM2\_DQB[8..1]

### FPGA5A CMOS25/LVDS

#### UPPER LEFT BANK7

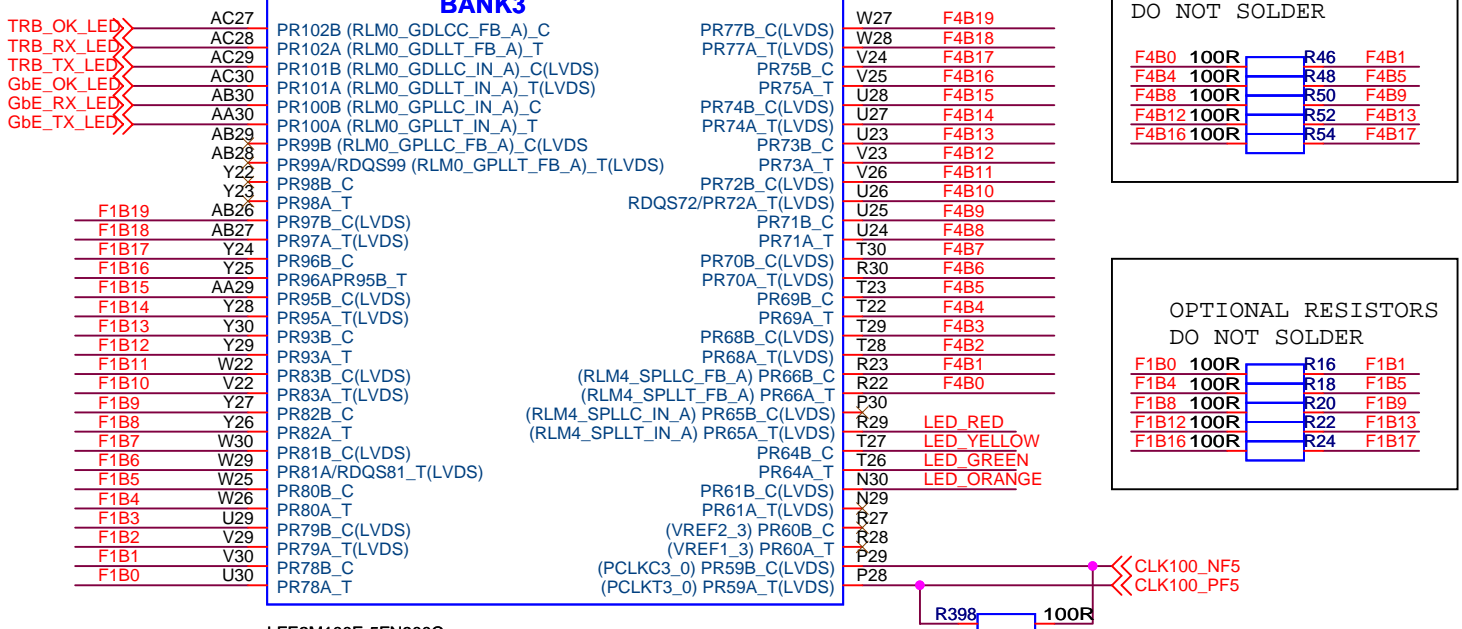


**OPTIONAL RESISTORS DO NOT SOLDER**

F2B0 100R	R40	F2B1
F2B4 100R	R36	F2B5
F2B8 100R	R38	F2B9
F2B12 100R	R42	F2B13
F2B16 100R	R44	F2B17

### FPGA5F CMOS25/LVDS

#### LOWER RIGHT BANK3

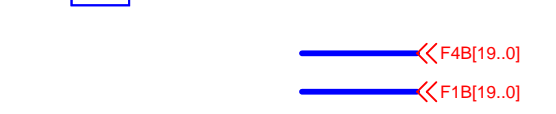


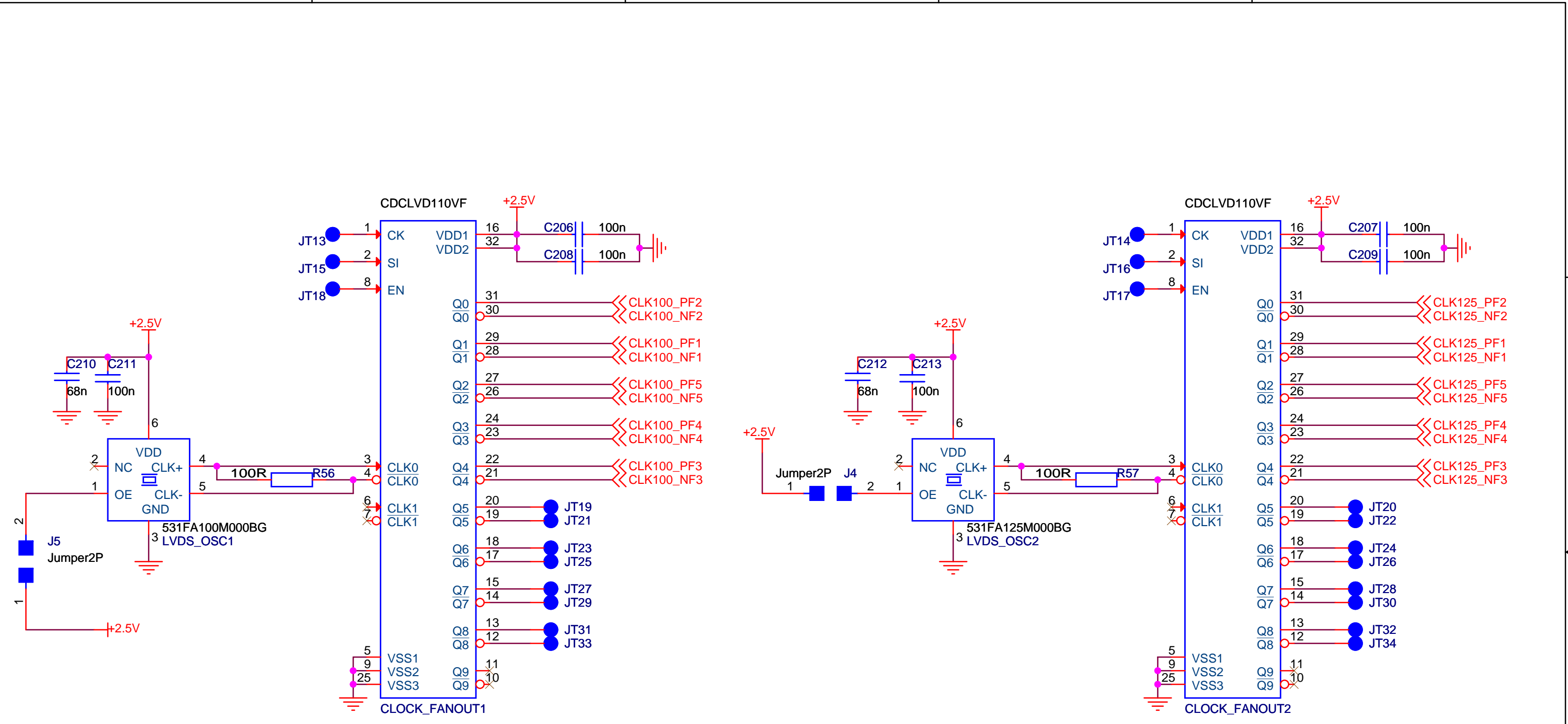
**OPTIONAL RESISTORS DO NOT SOLDER**

F4B0 100R	R46	F4B1
F4B4 100R	R48	F4B5
F4B8 100R	R50	F4B9
F4B12 100R	R52	F4B13
F4B16 100R	R54	F4B17

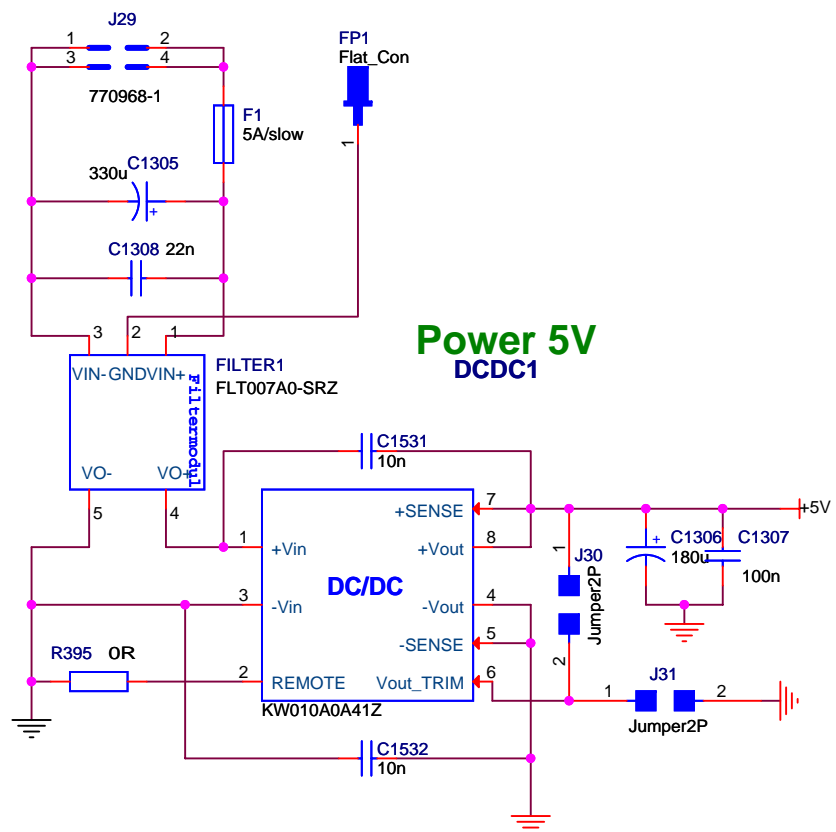
**OPTIONAL RESISTORS DO NOT SOLDER**

F1B0 100R	R16	F1B1
F1B4 100R	R18	F1B5
F1B8 100R	R20	F1B9
F1B12 100R	R22	F1B13
F1B16 100R	R24	F1B17



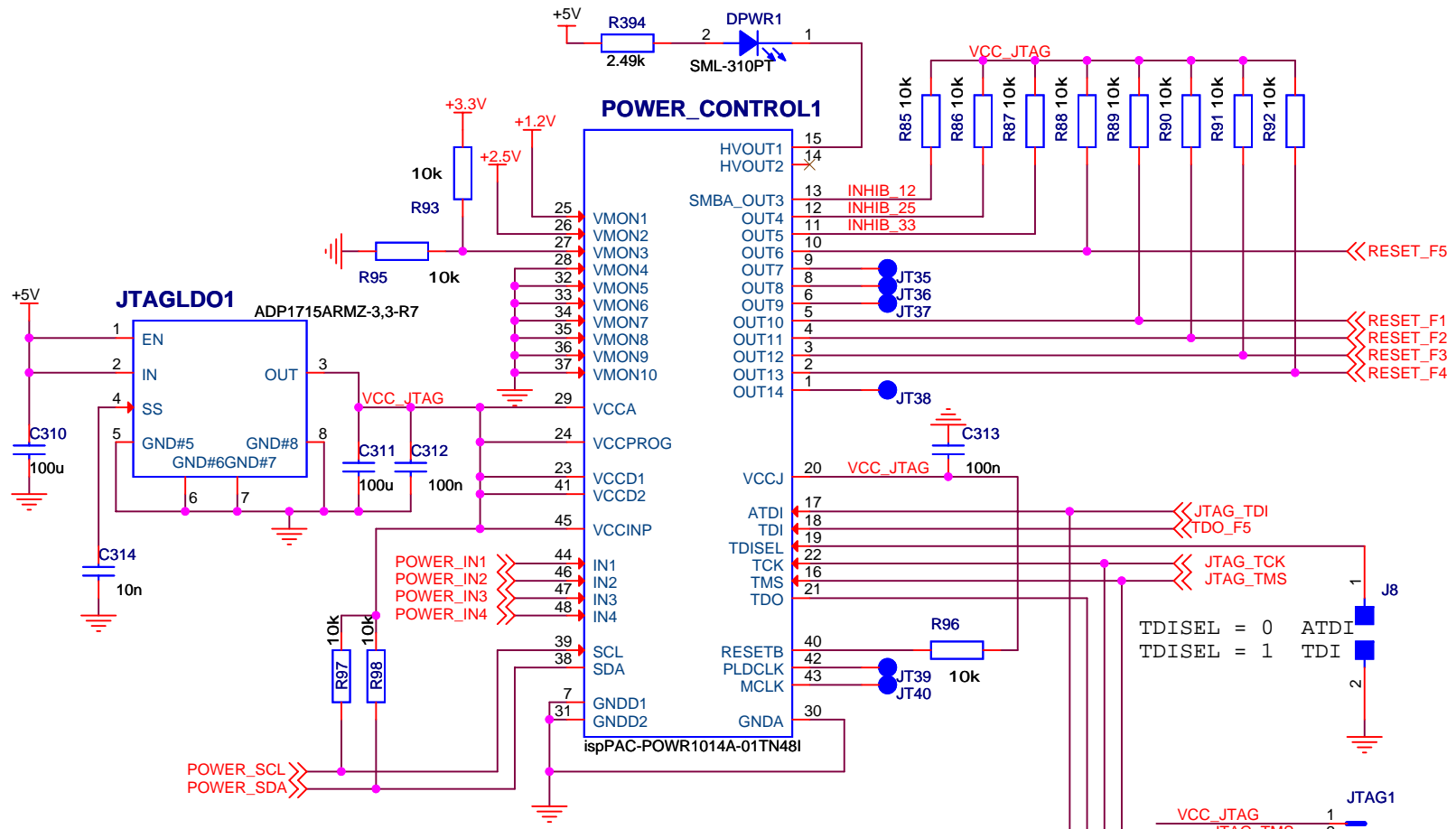


Title			<b>09_CLOCKING</b>		
Size	Document Number				Rev
A4	<Doc>				<RevCo
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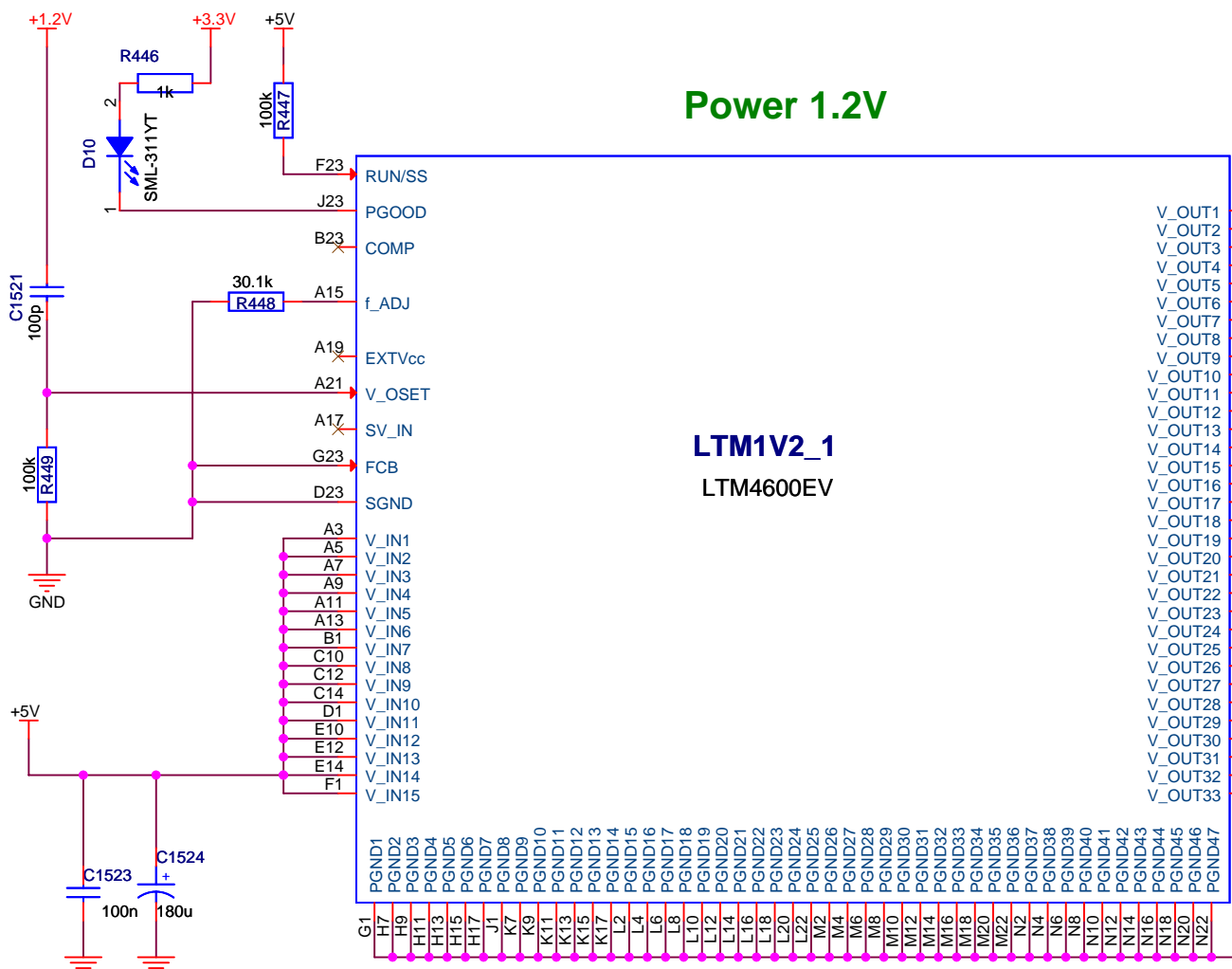
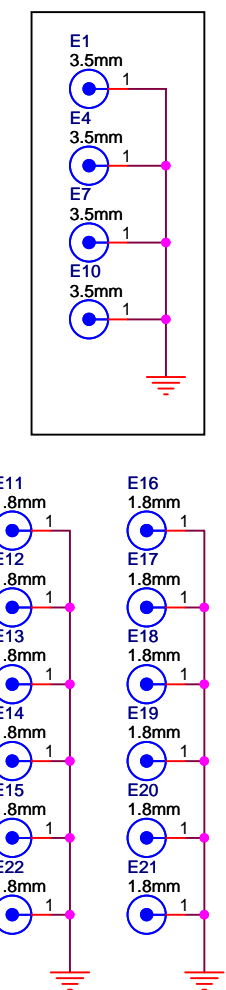
**Power 5V  
DCDC1**

PLEASE PROVIDE THE SPACE FOR THE CAGE  
TO COVER DCDC CONVERTERS - GND PINS



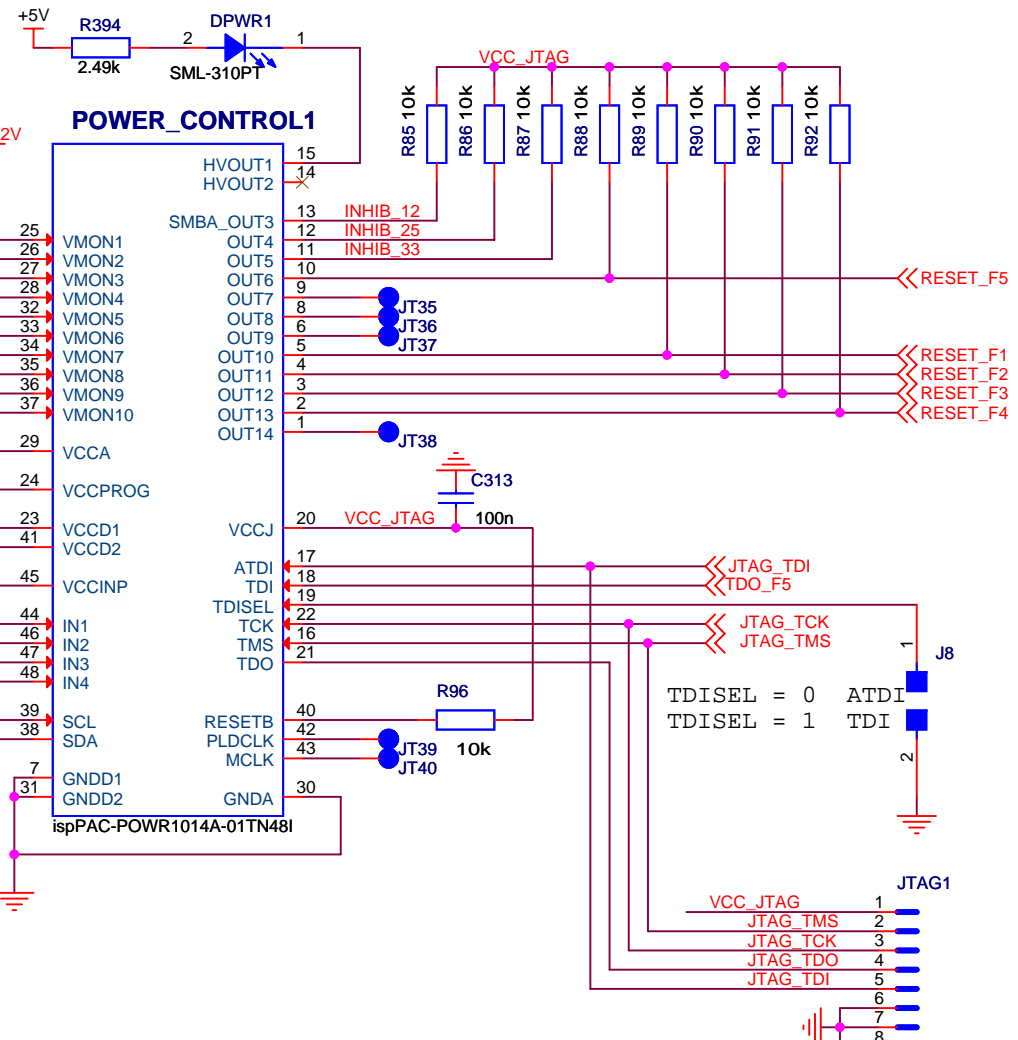
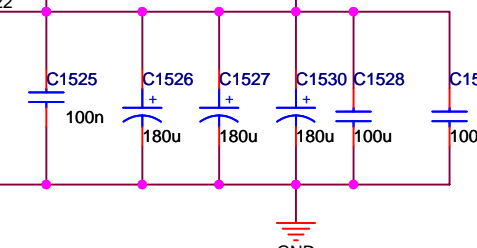
**Power 1.2V**

**Board-Mounting-Hole**

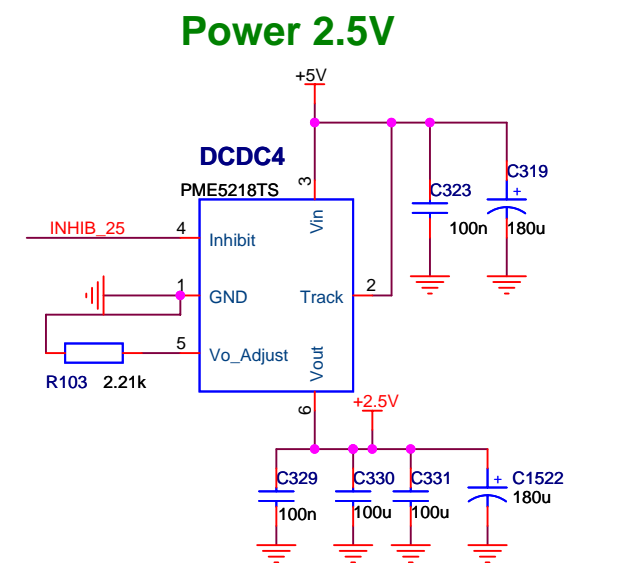
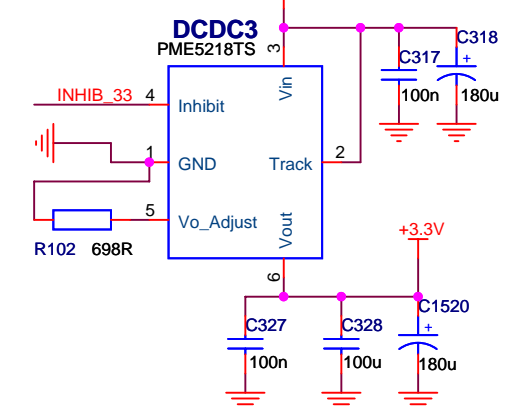


**LTM1V2\_1  
LTM4600EV**

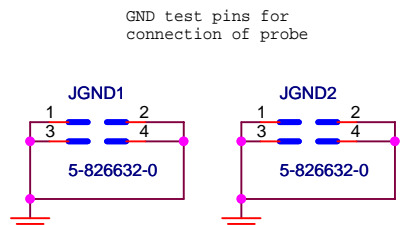
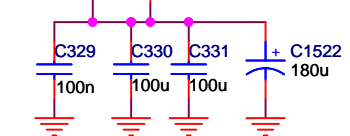
**+1.2V  
OUT**



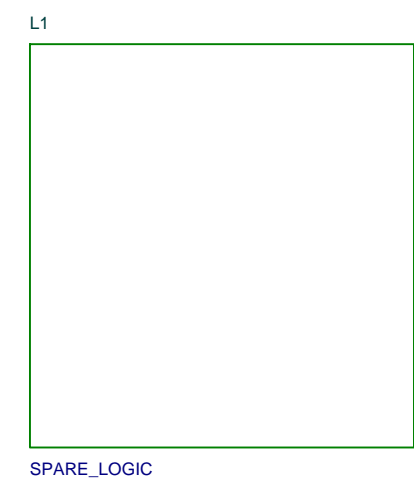
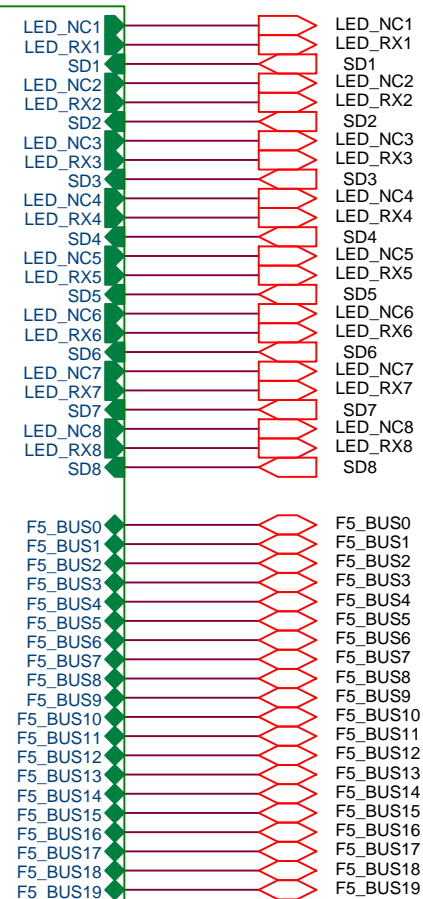
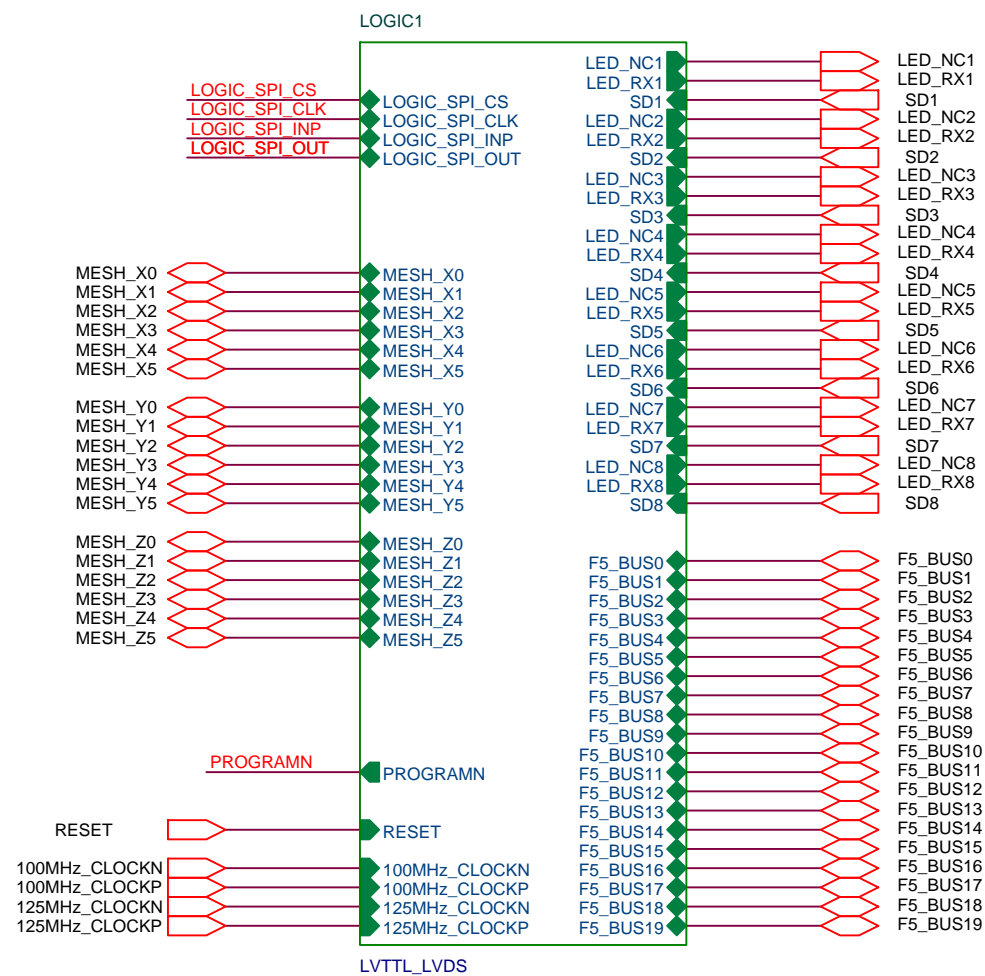
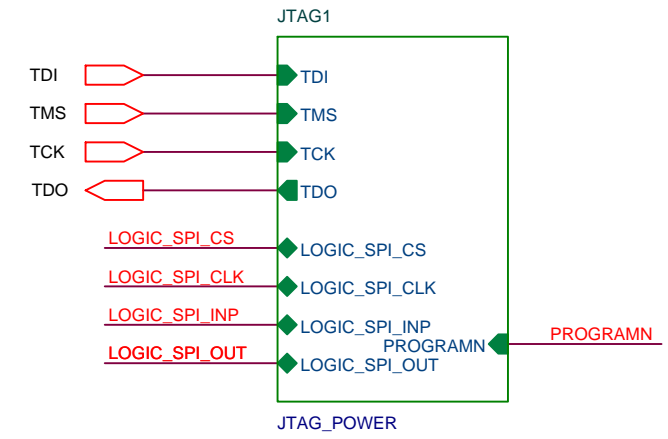
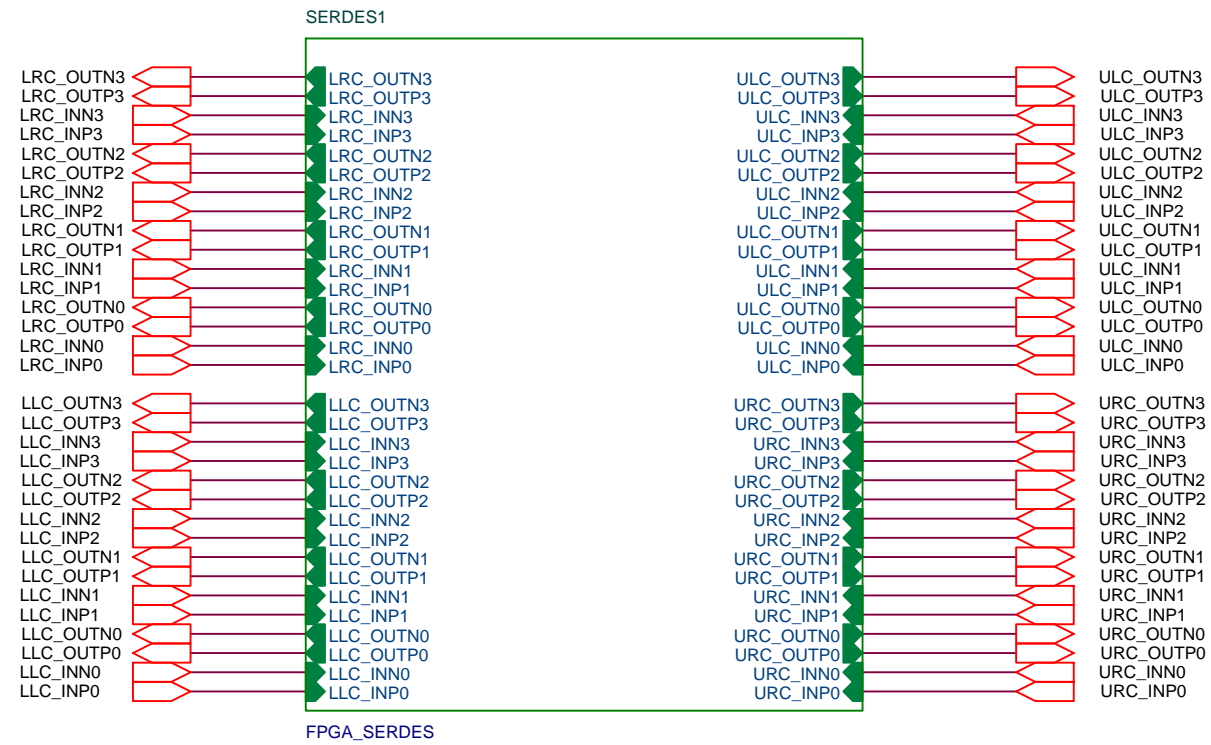
**Power 3.3V**



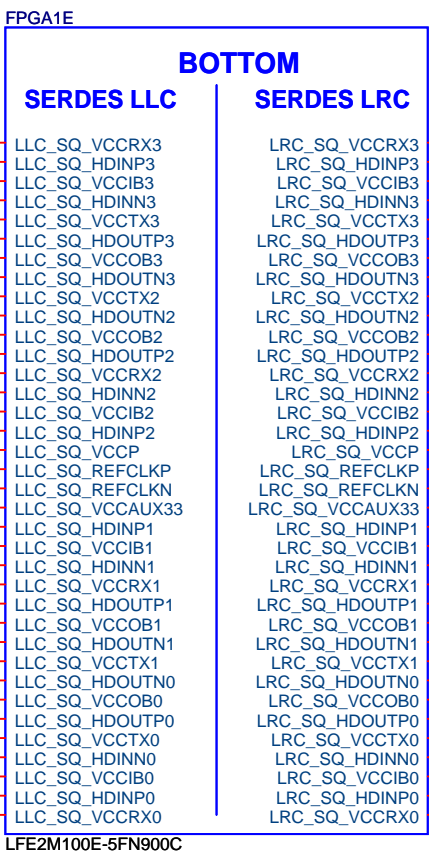
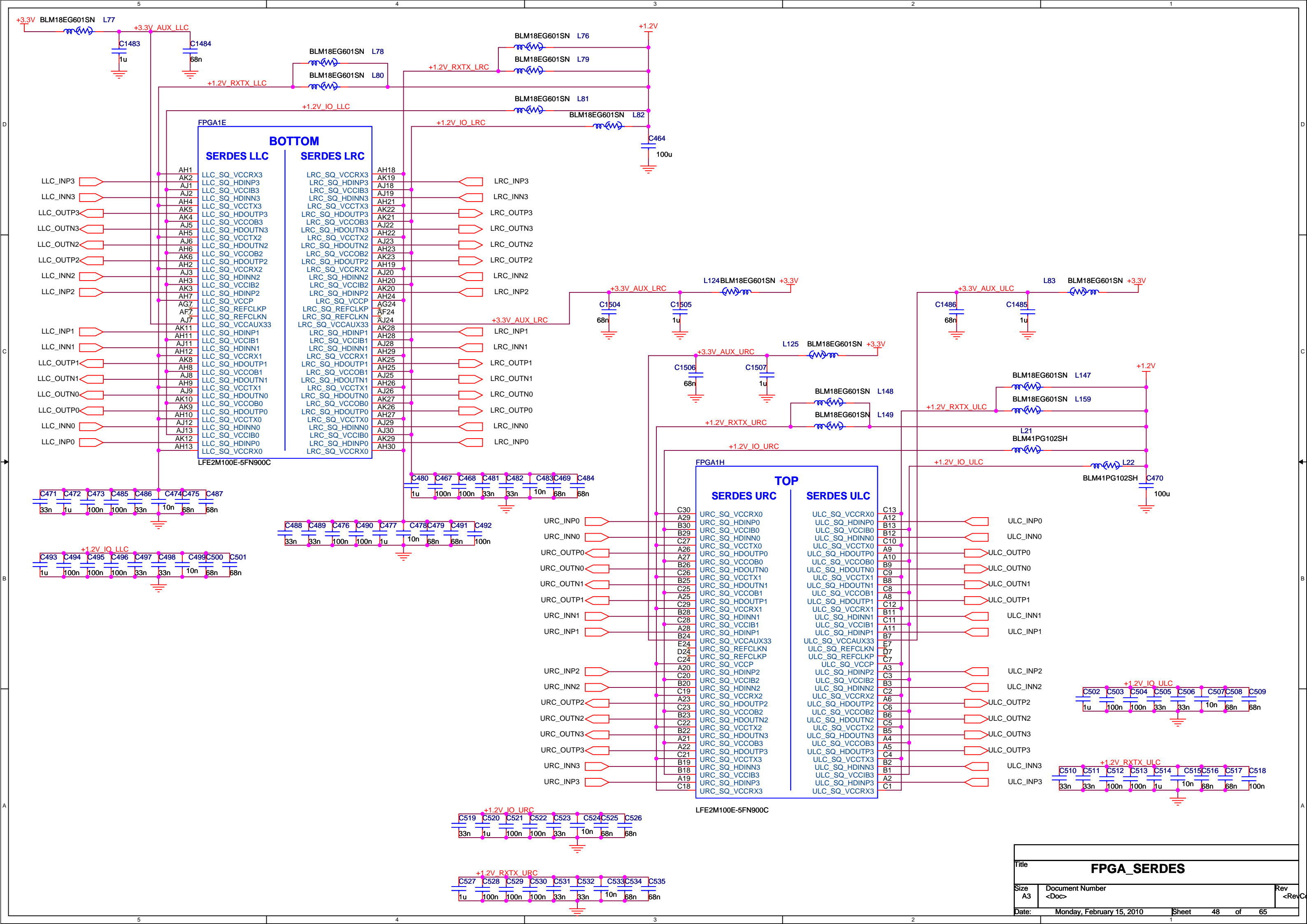
**Power 2.5V**



Title			<b>11_POWER_SOURCE</b>		
Size	Document Number		Rev		
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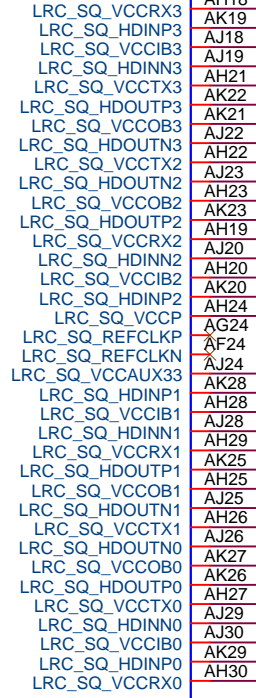


Title			<b>FPGA_BLOCK</b>		
Size	Document Number				Rev
A3	<Doc>				<RevC>
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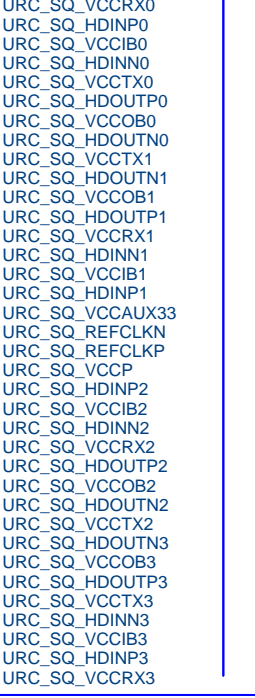
**BOTTOM**

**SERDES LRC**



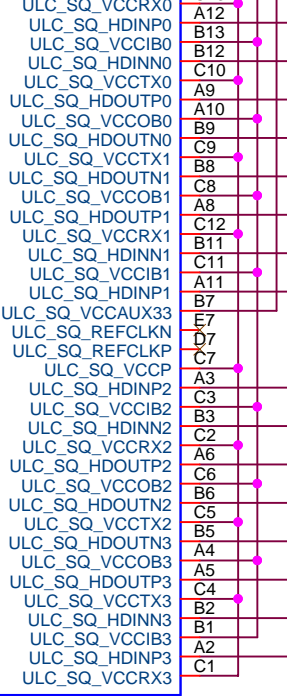
**FPGA1H**

**SERDES URC**



**TOP**

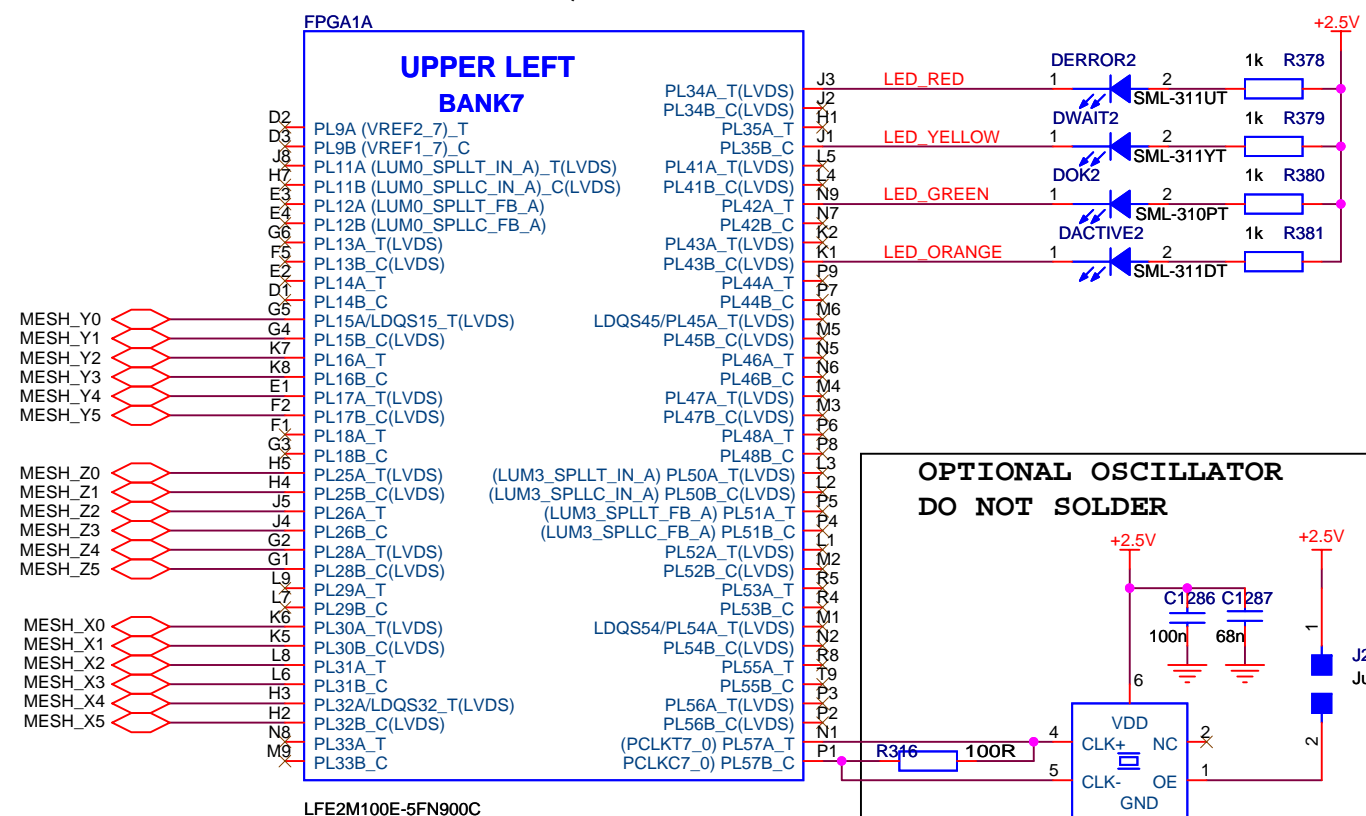
**SERDES ULC**



Title			<b>FPGA_SERDES</b>		
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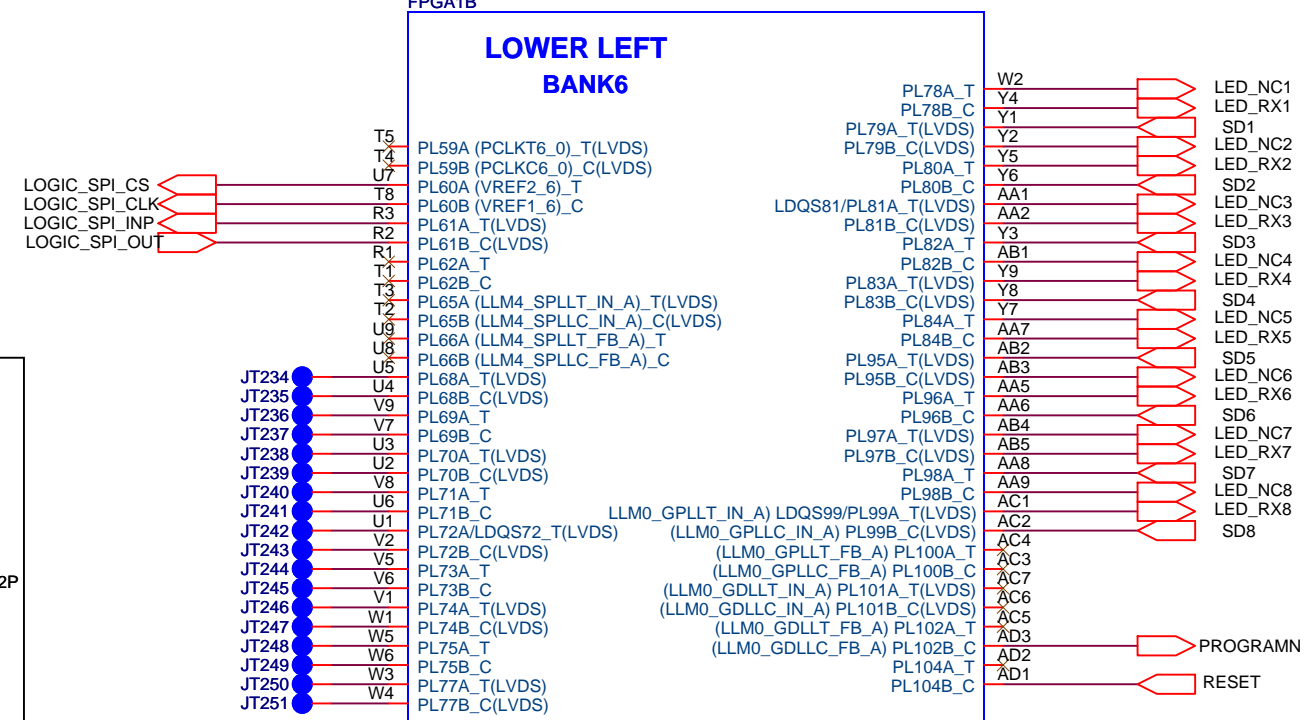


CMOS25 / LVDS



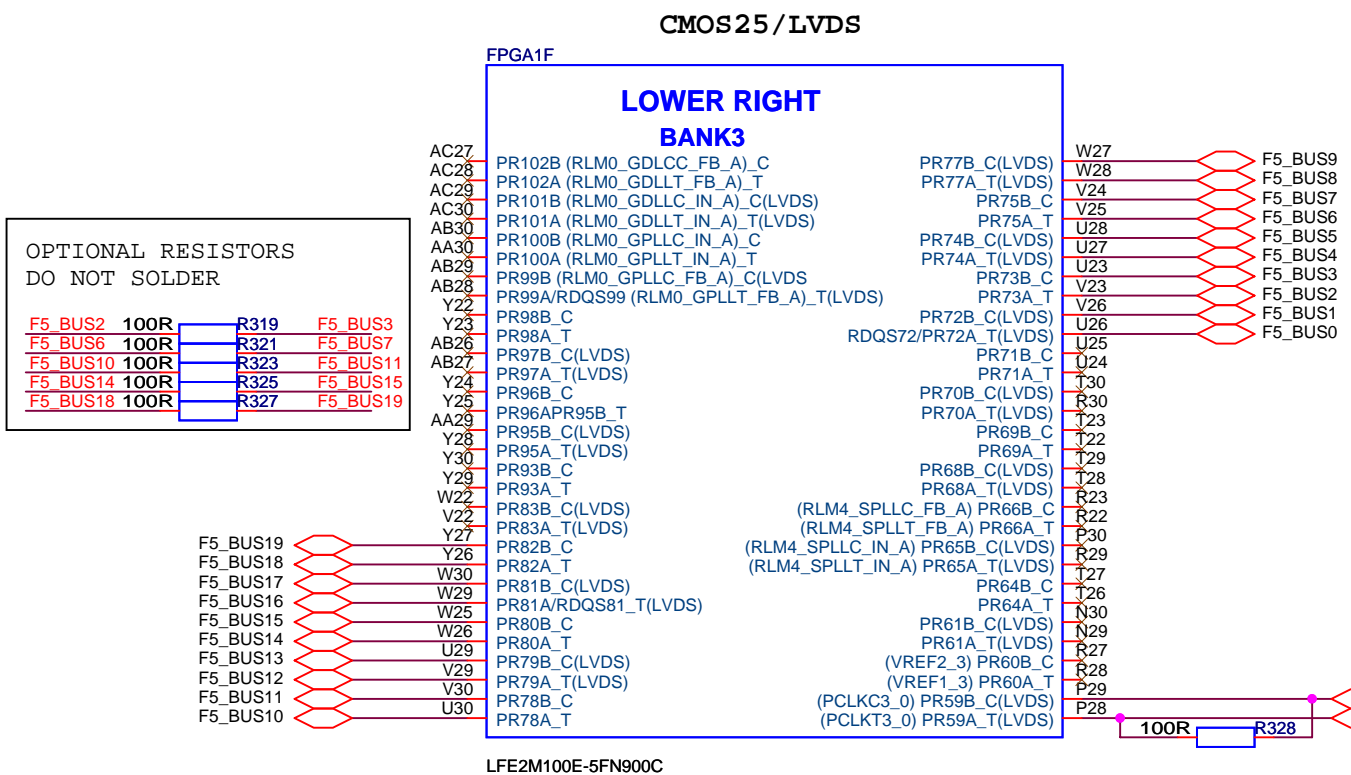
OPTIONAL OSCILLATOR  
DO NOT SOLDER

LVTTTL



SOLDER PADS SHOULD BE  
IN PLUGGED VIAS

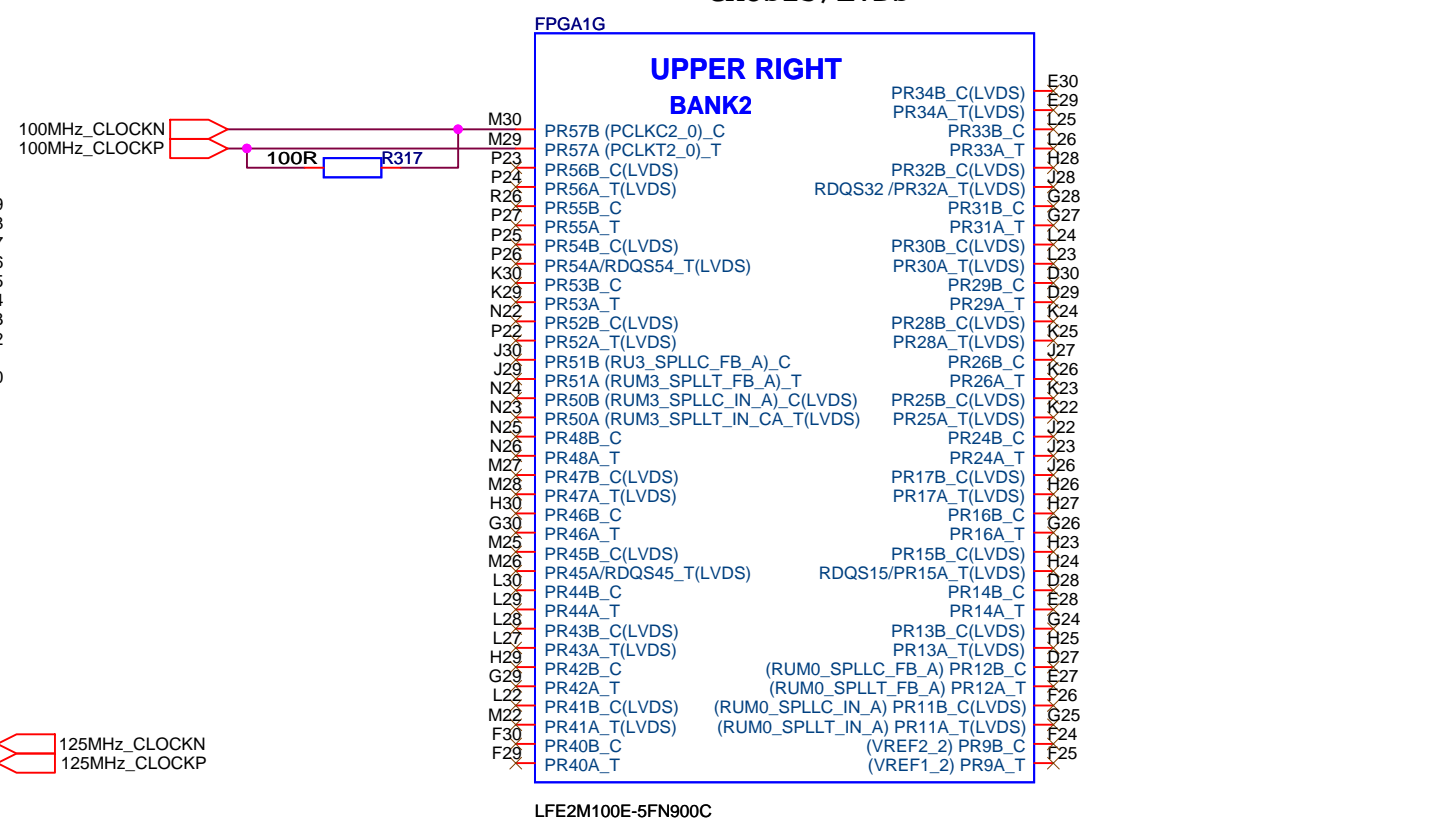
CMOS25 / LVDS



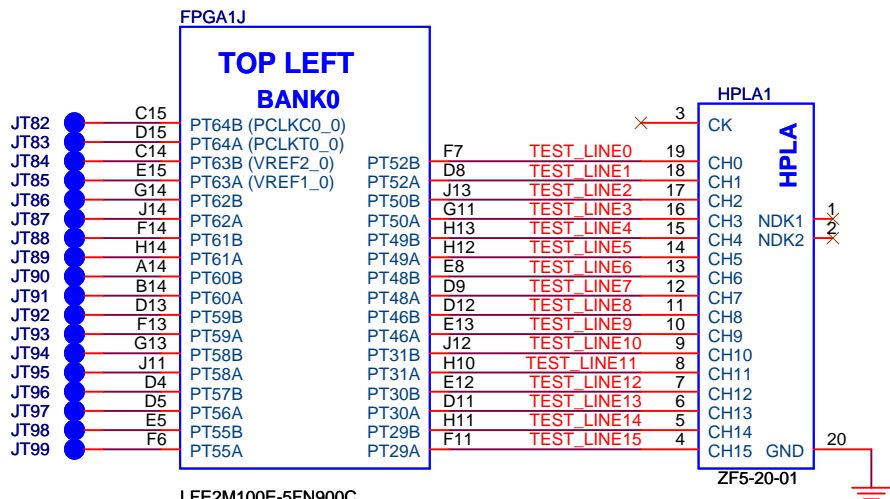
OPTIONAL RESISTORS  
DO NOT SOLDER

F5_BUS2 100R	R319	F5_BUS3
F5_BUS6 100R	R321	F5_BUS7
F5_BUS10 100R	R323	F5_BUS11
F5_BUS14 100R	R325	F5_BUS15
F5_BUS18 100R	R327	F5_BUS19

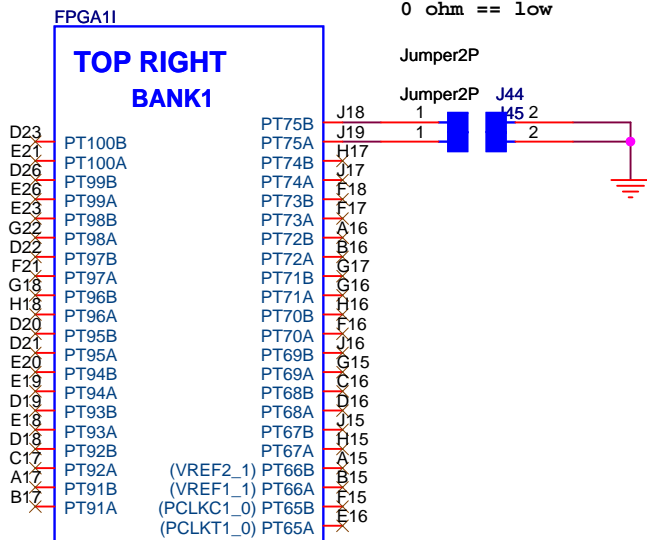
CMOS25 / LVDS



**LVTTTL**

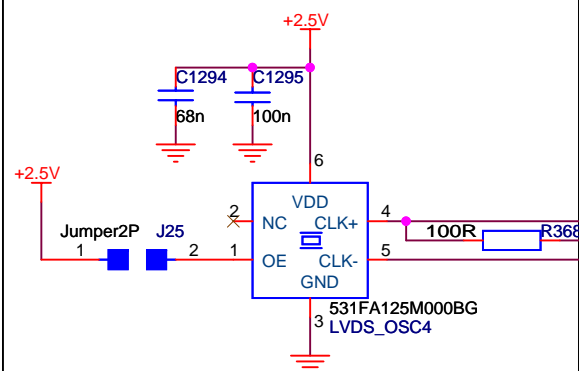


**CMOS25/LVDS**



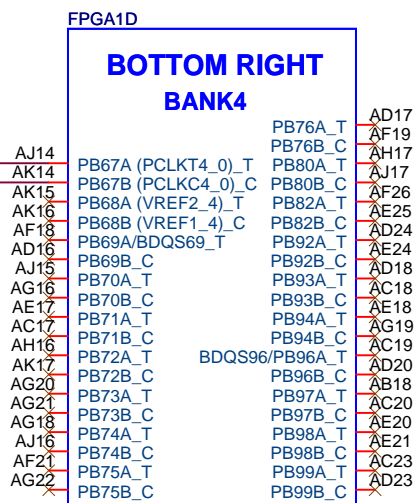
Please code the FPGA number here:  
 open == high  
 0 ohm == low

**OPTIONAL OSCILLATOR  
DO NOT SOLDER**



**SOLDER PADS SHOULD BE  
IN PLUGGED VIAS**

**CMOS25/LVDS**



**CMOS25/LVDS**

