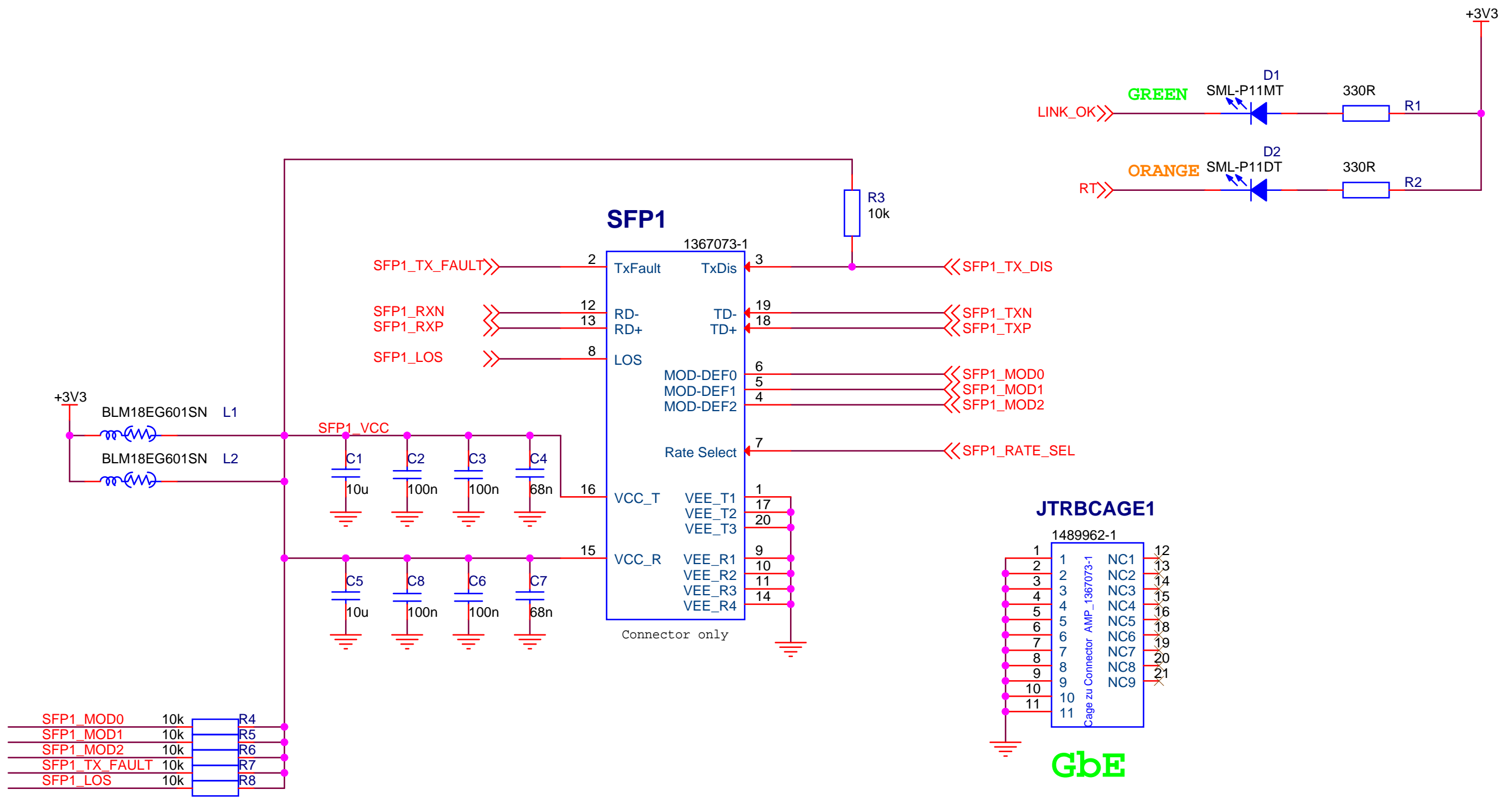


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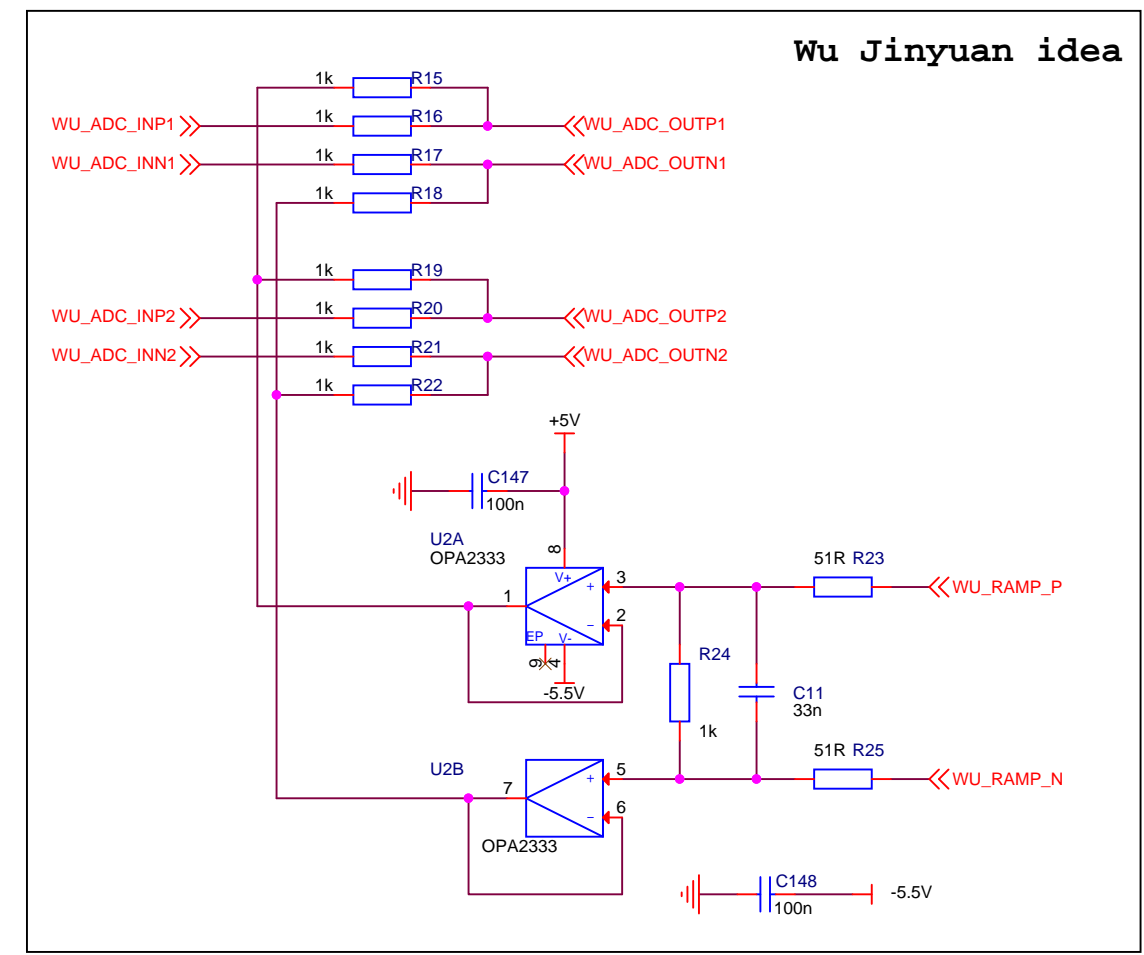
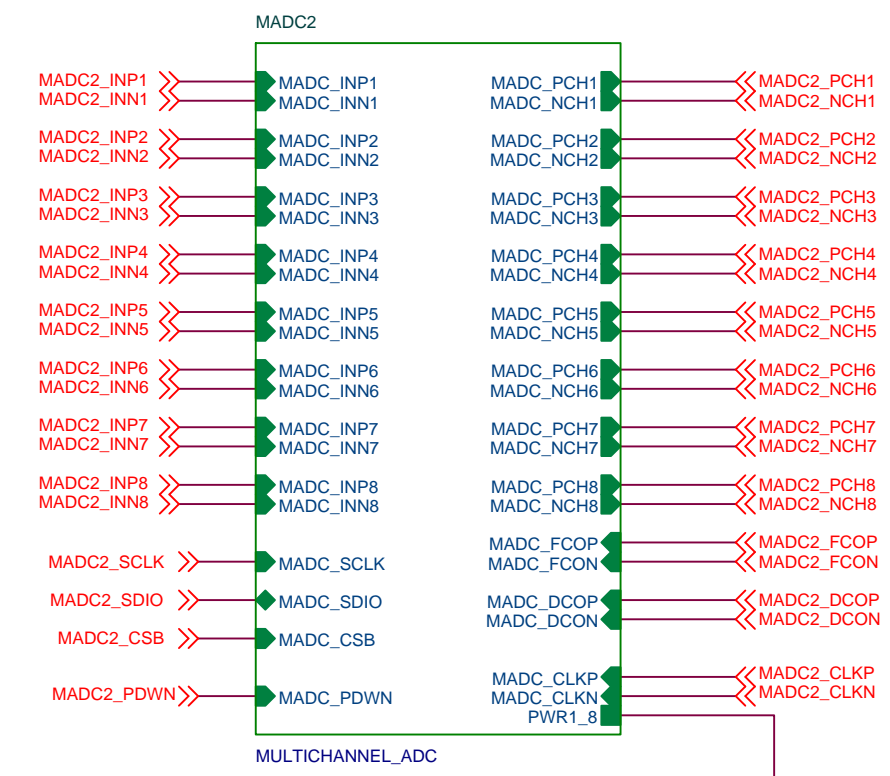
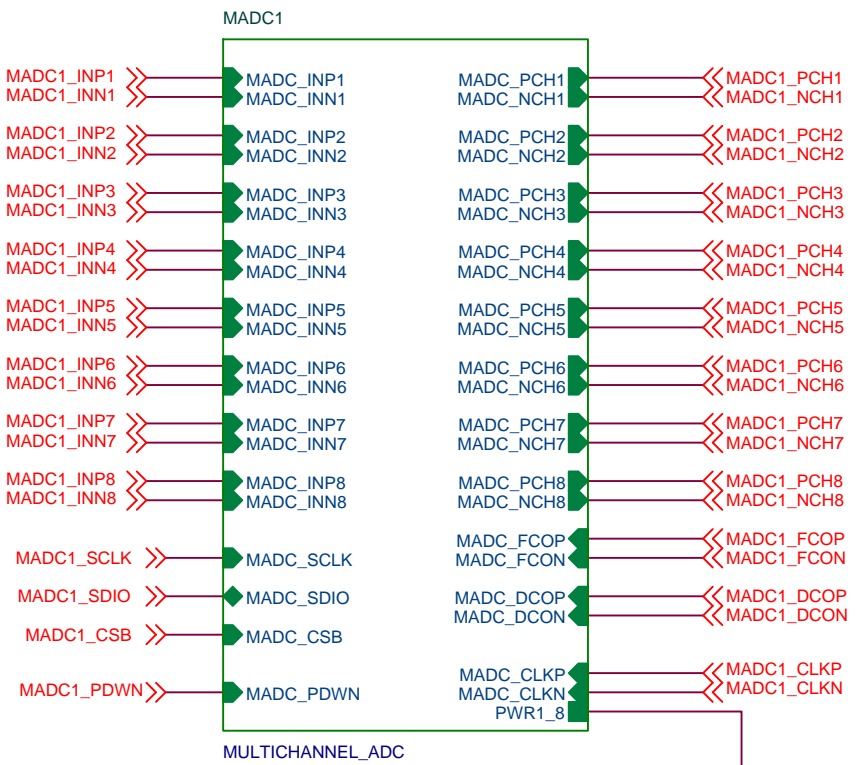
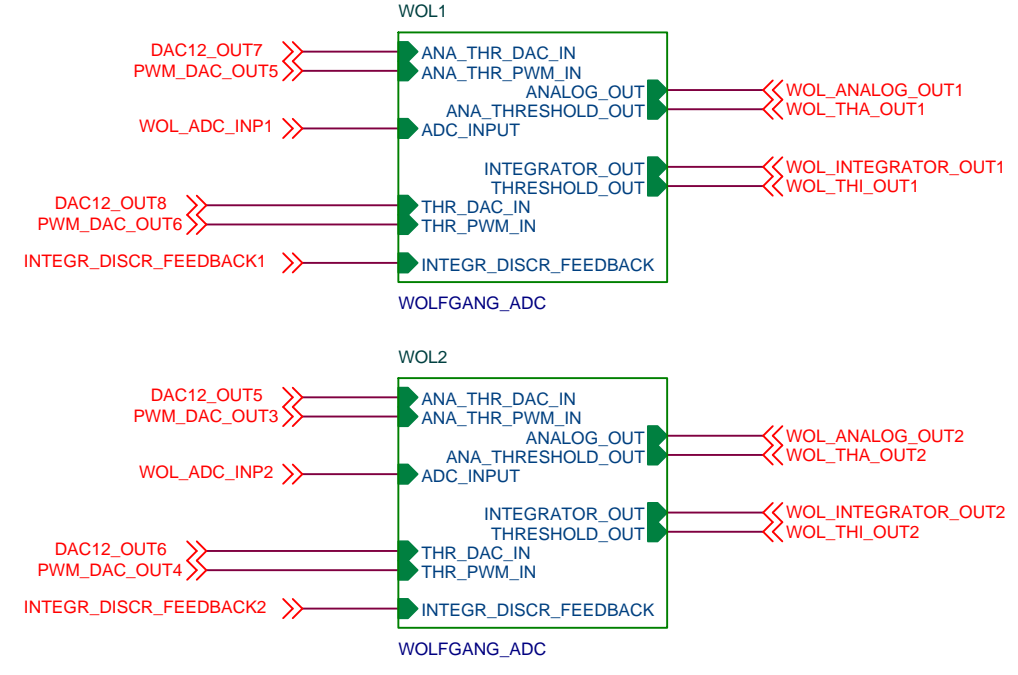
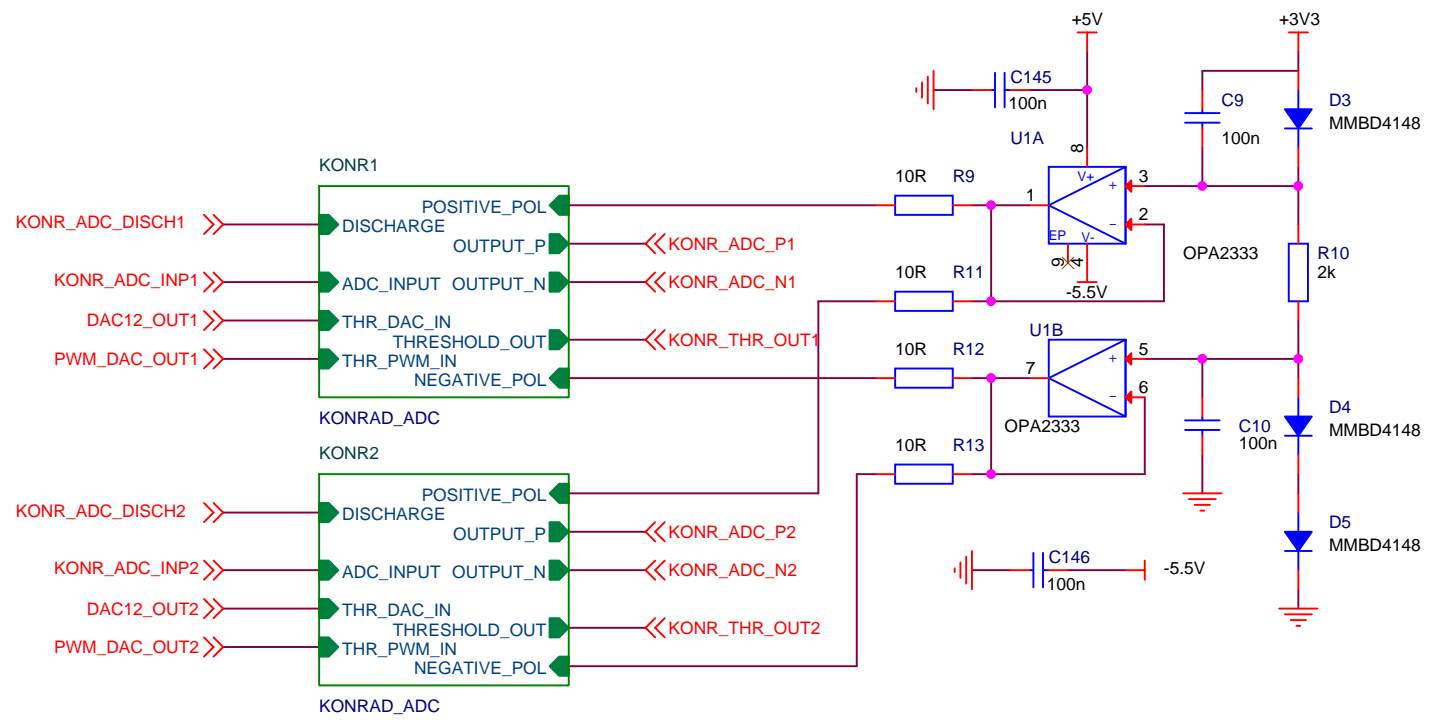
## 01\_FRONT\_CONNECTORS

Design: K:\GSIJOB\HADES\TRBV3\MULTITESTADDON1\MULTITESTADDON1.DSN	Size: A4	Page: 1 / 13
Modified: Wednesday, January 04, 2012	Designer: M.Kajetanowicz	Layouter: S.Voltz



MODDEF0 is grounded by module when inserted

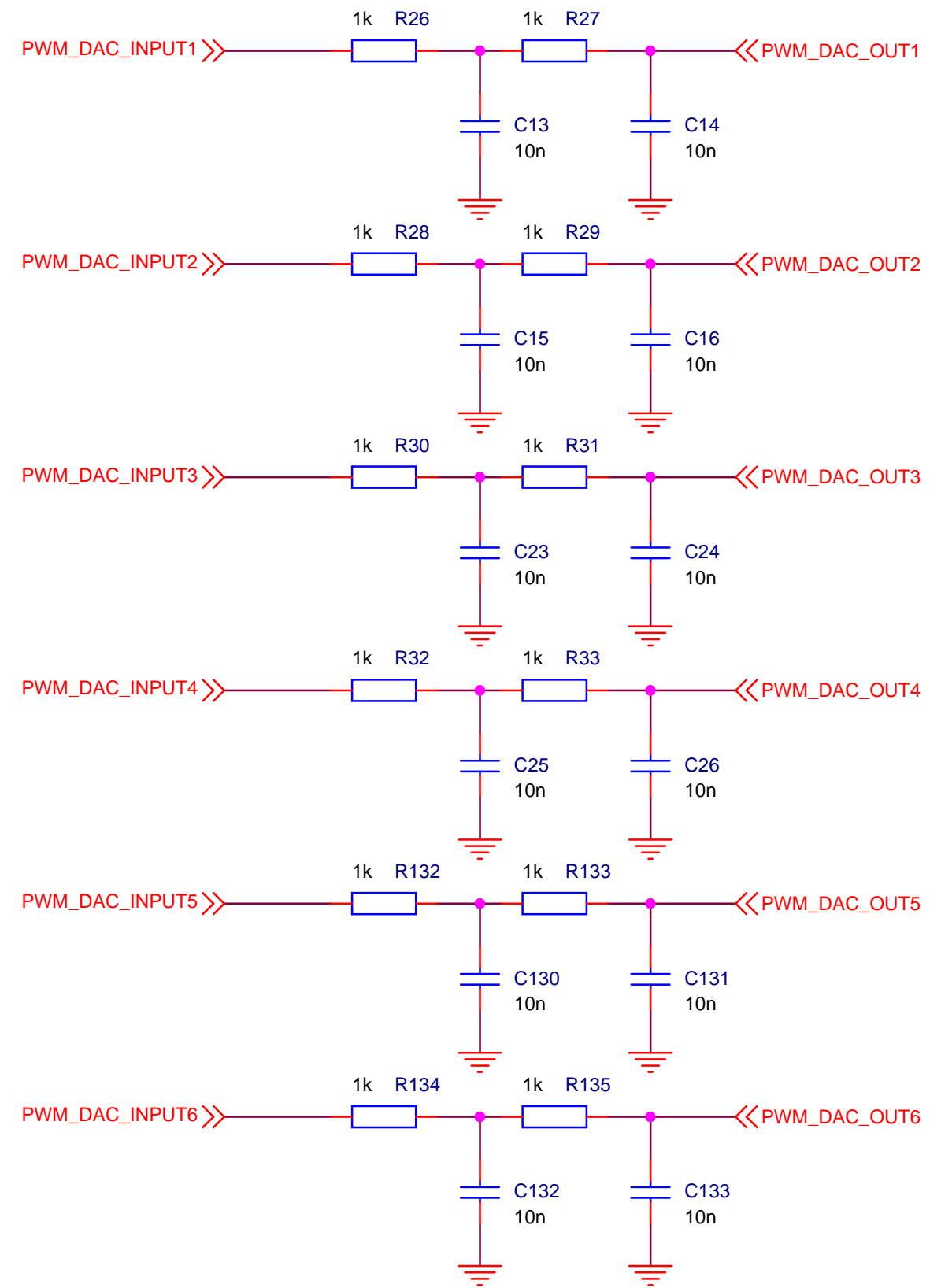
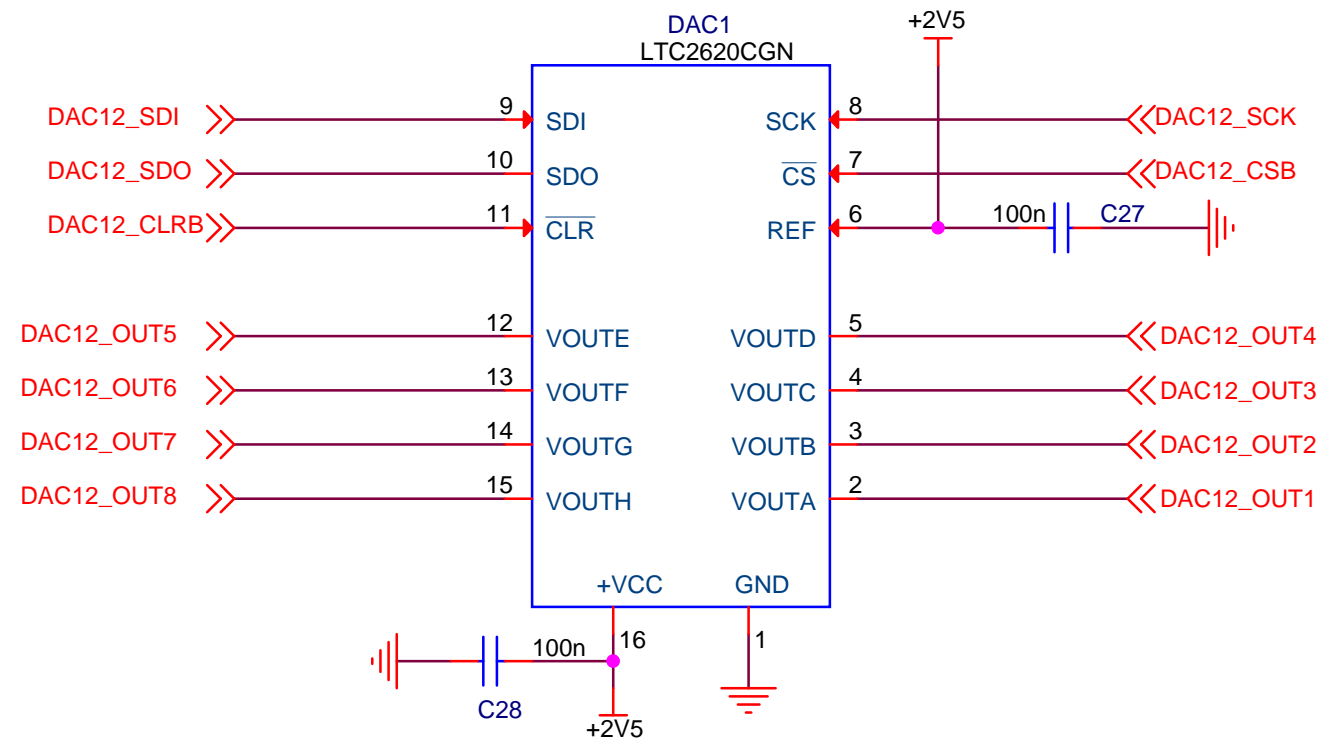
		Gesellschaft für Schwerionenforschung mbH Planckstrasse 1 D-64291 Darmstadt GERMANY www.gsi.de	
		<h2>02_SFP</h2>	
Design: K:\GSIJOB\HADES\TRBV3\MULTITESTADDON1\MULTITESTADDON1.DSN		Modified: Wednesday, January 04, 2012	
Designer: M.Kajetanowicz		Size: A4 Page: 2 / 13	
		Layouter: S.Voltz	



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**03\_ADCS**

Design: K:\GSI\JOB\HADEST\RBV3\MULTITEST\ADDON1\MULTITEST\ADDON1.DSN	Size: A3
Modified: Wednesday, January 04, 2012	Page: 3 / 13
Designer: M.Kajetanowicz	Layouter: S.Voltz



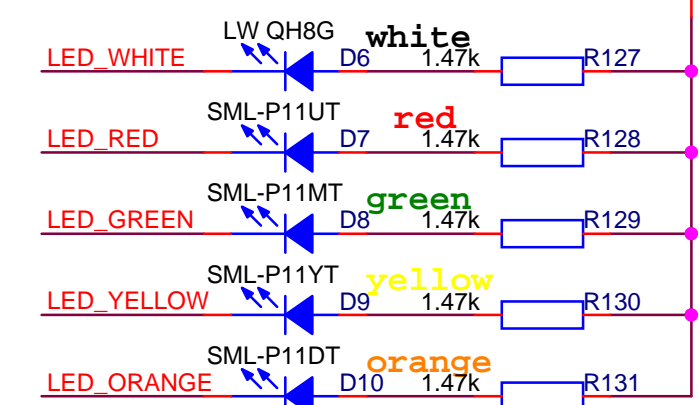
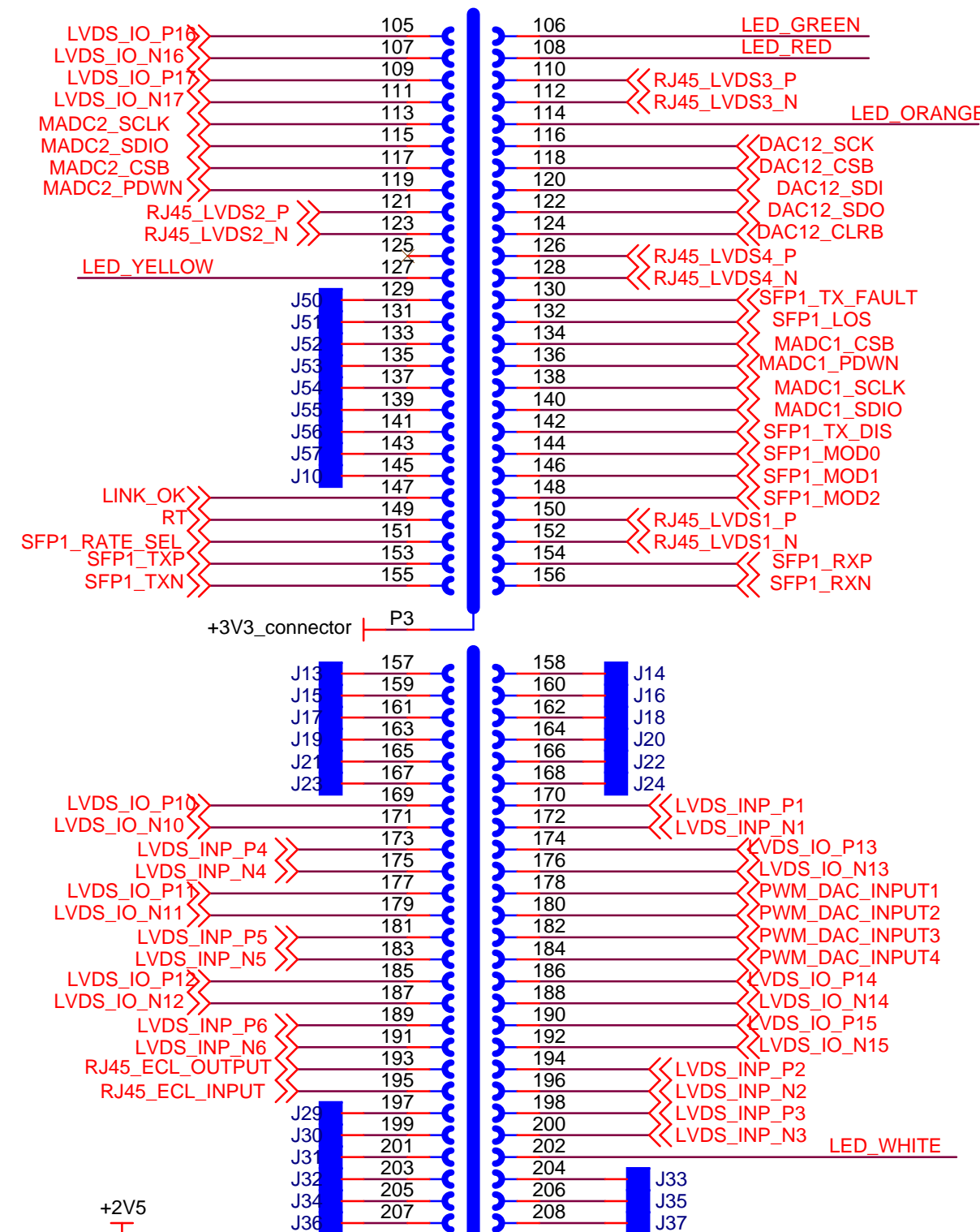
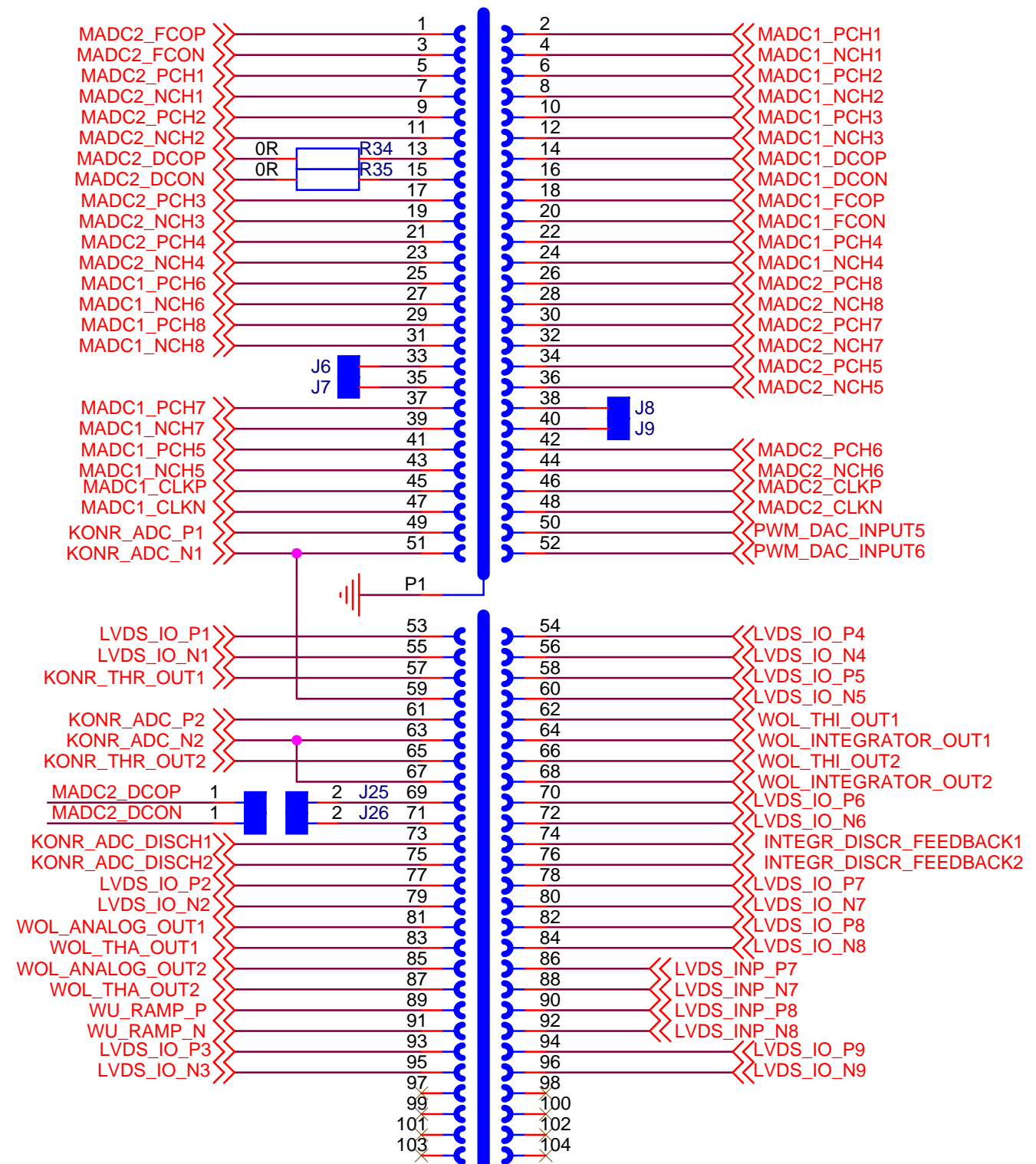
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**04\_DACS**

Design: K:\GSIJOB\HADES\TRBV3\MULTITESTADDON1\MULTITESTADDON1.DSN	Size: A4	Page: 4 / 13
Modified: Wednesday, January 04, 2012	Designer: M.Kajetanowicz	Layouter: S.Voltz

# TRB\_CONNECTOR1A

# TRB\_CONNECTOR1B

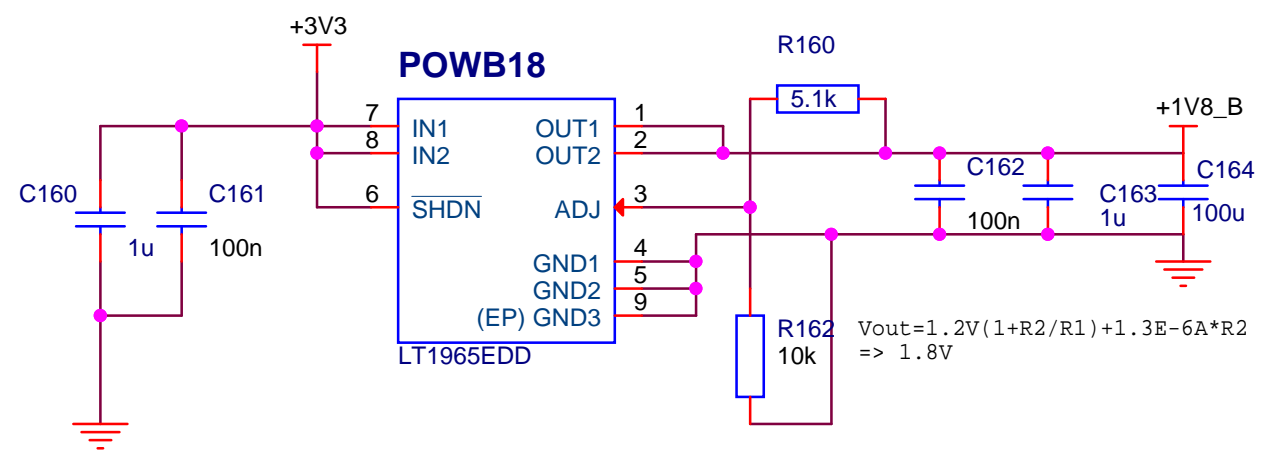
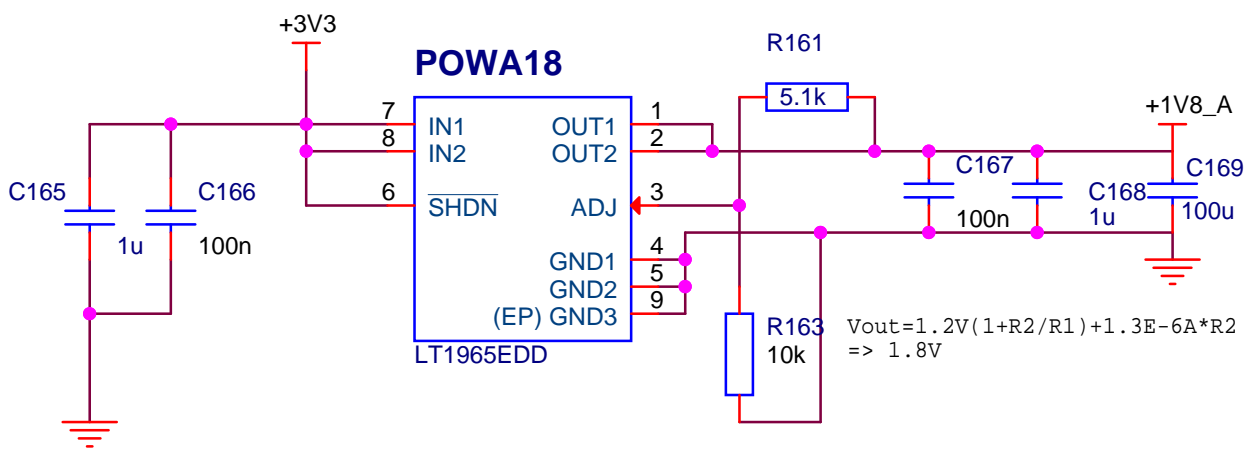
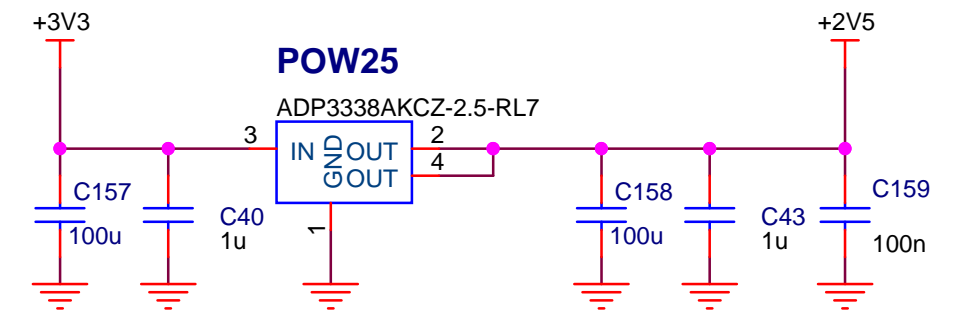
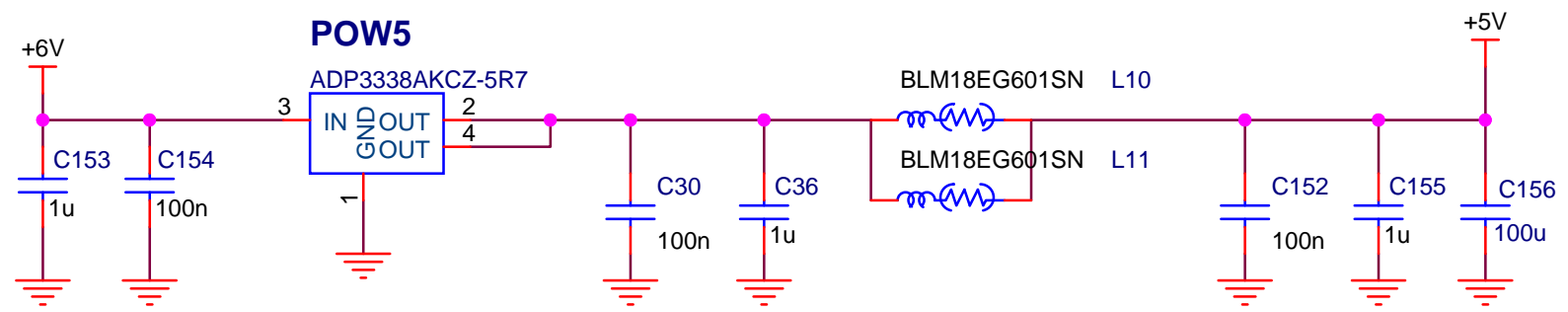
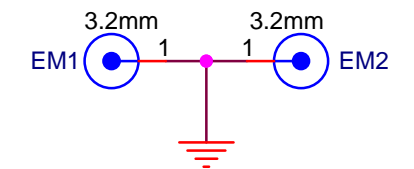
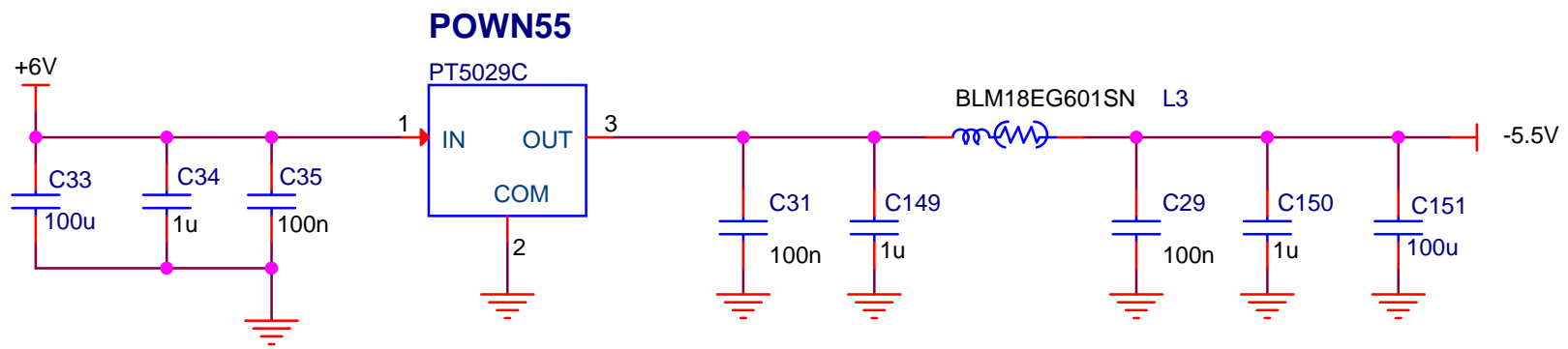




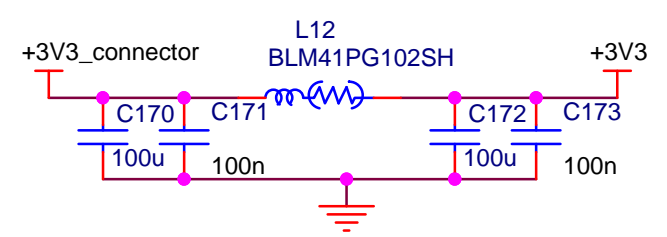
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## 05\_TRB\_CONNECTOR

Design: K:\GSIJOB\HADES\TRBV3\MULTITESTADDON1\MULTITESTADDON1.DSN	Size: A4	Page: 5 / 13
Modified: Wednesday, January 04, 2012	Designer: M.Kajetanowicz	Layouter: S.Voltz



Power for the two ADCs, they need around 600mA each...

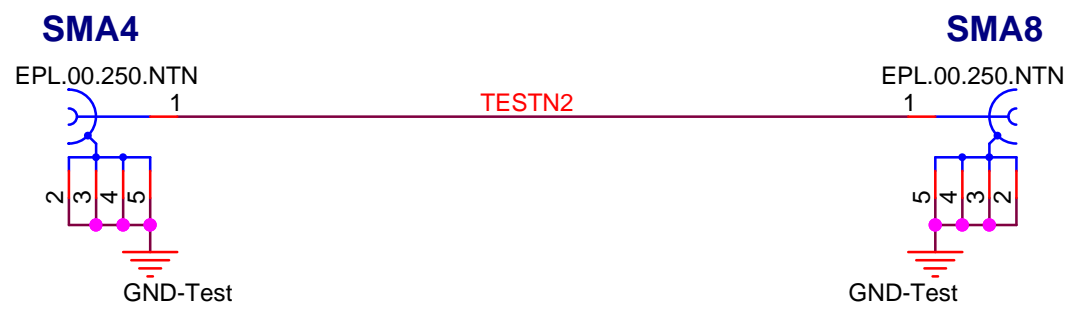
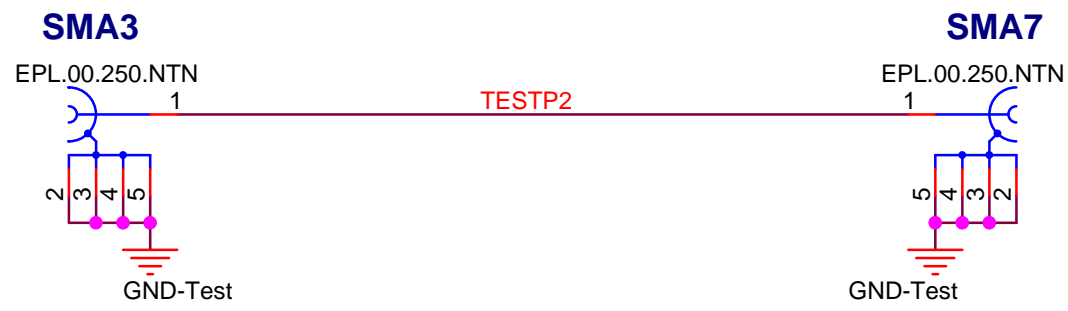
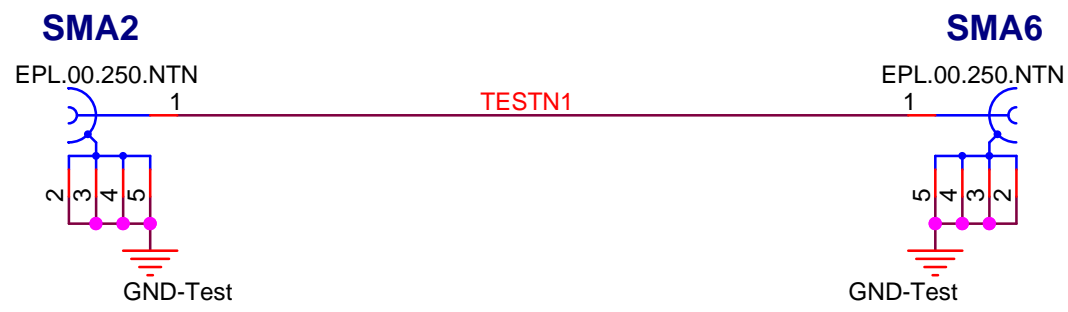




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## 06\_SUPPLY

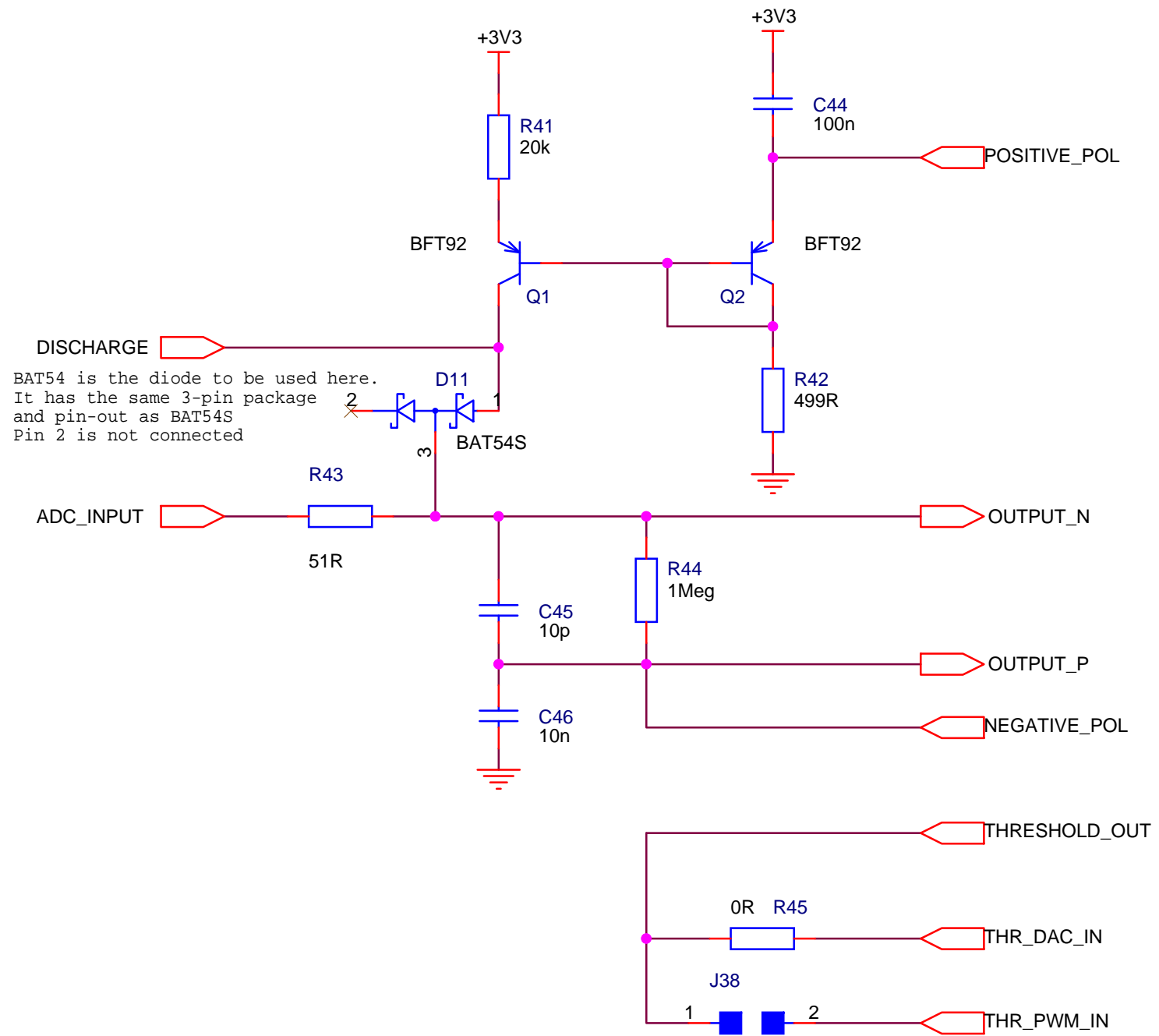
Design: K:\GSIJOB\HADES\TRBV3\MULTITESTADDON1\MULTITESTADDON1.DSN	Modified: Wednesday, January 04, 2012	Size: A4	Page: 6 / 13
Designer: M.Kajetanowicz	Layouter: S.Voltz		



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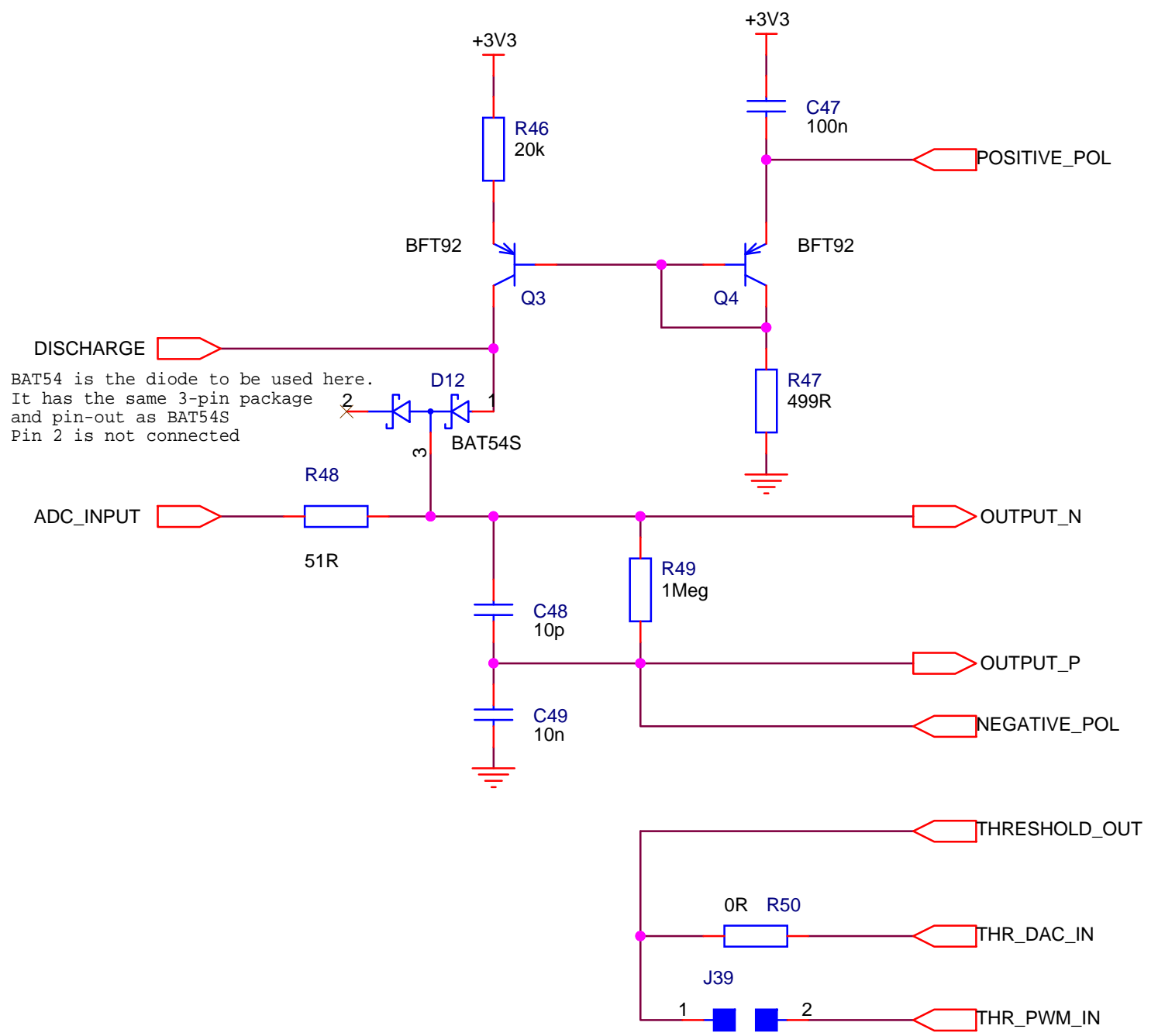
**07\_TDR-Test**

Design: K:\GSIJOB\HADES\TRBV3\MULTITESTADDON1\MULTITESTADDON1.DSN	Size: A4	Page: 7 / 13
Modified: Wednesday, January 04, 2012	Designer: M.Kajetanowicz	Layouter: S.Voltz



## KONRAD\_ADC





BAT54 is the diode to be used here.  
 It has the same 3-pin package  
 and pin-out as BAT54S  
 Pin 2 is not connected

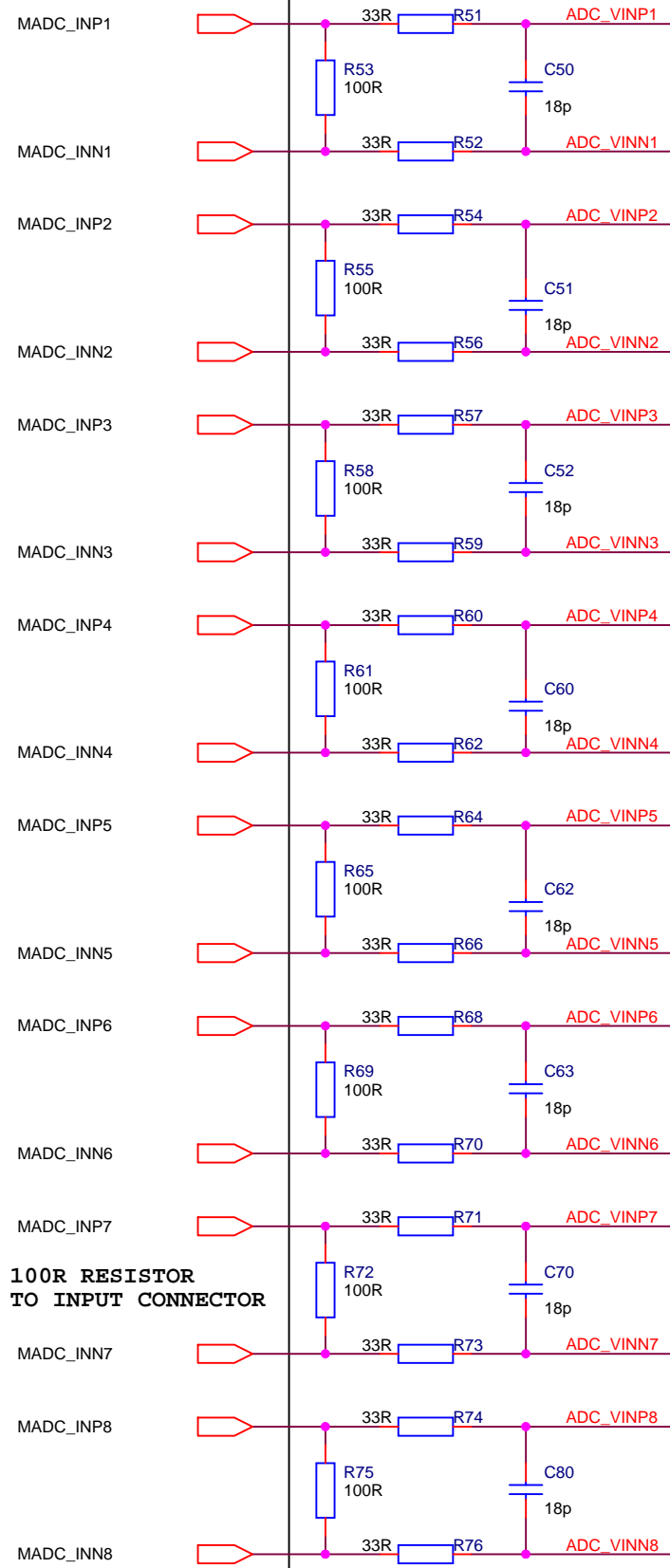
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**KONRAD\_ADC**

Design: K:\GSIJOB\HADES\TRBV3\MULTITESTADDON1\MULTITESTADDON1.DSN
Modified: Wednesday, January 04, 2012
Designer: M.Kajetanowicz

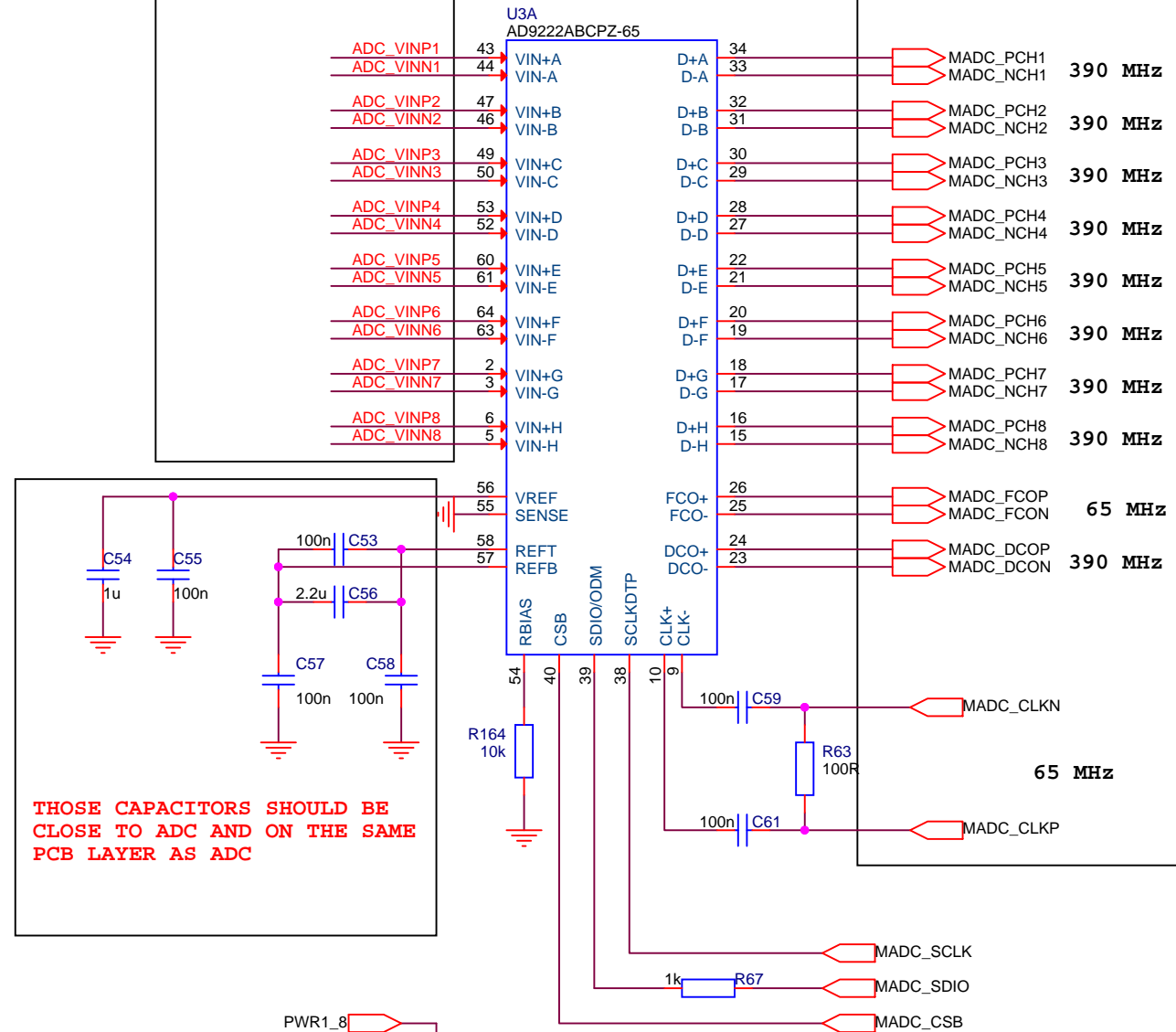
Size: A4	Page: 9 / 13
Layouter: S.Voltz	

ALL PIRS HERE ARE DIFFERENTIAL



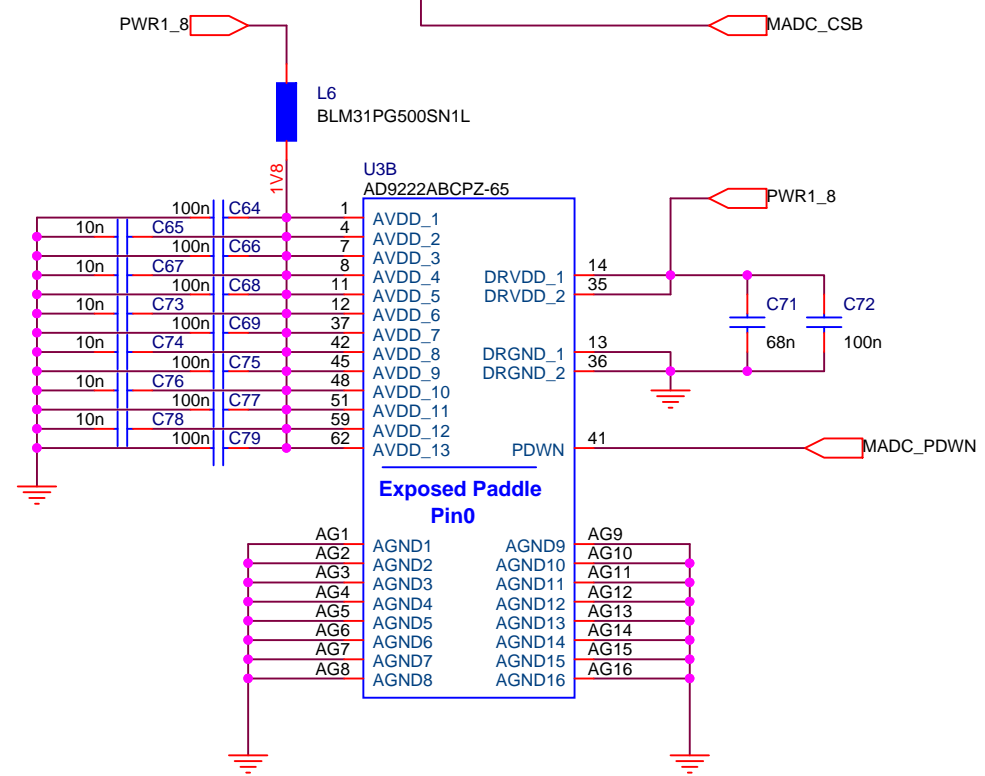
PLACE 100R RESISTOR CLOSE TO INPUT CONNECTOR

ALL SIGNALS HERE ARE DIFFERENTIAL



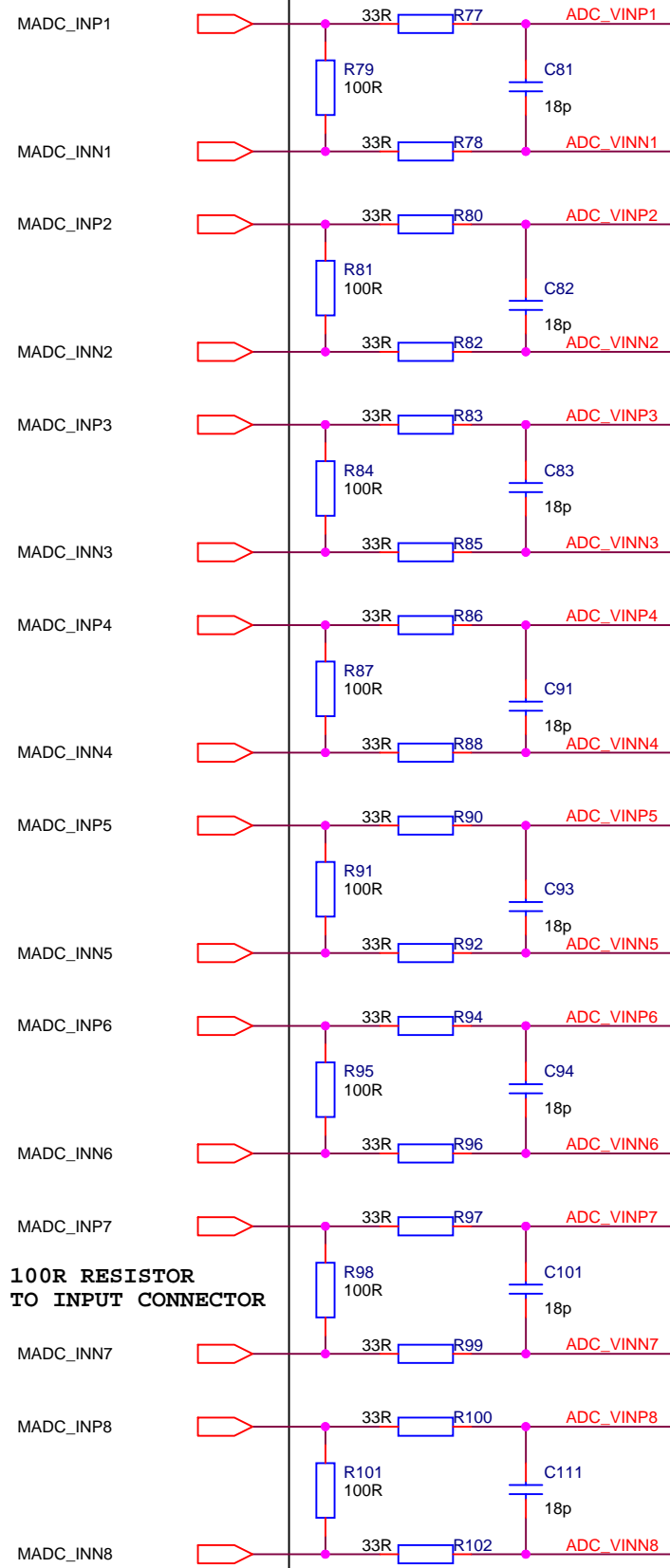
THOSE CAPACITORS SHOULD BE CLOSE TO ADC AND ON THE SAME PCB LAYER AS ADC

ALL SIGNALS HERE ARE DIFFERENTIAL



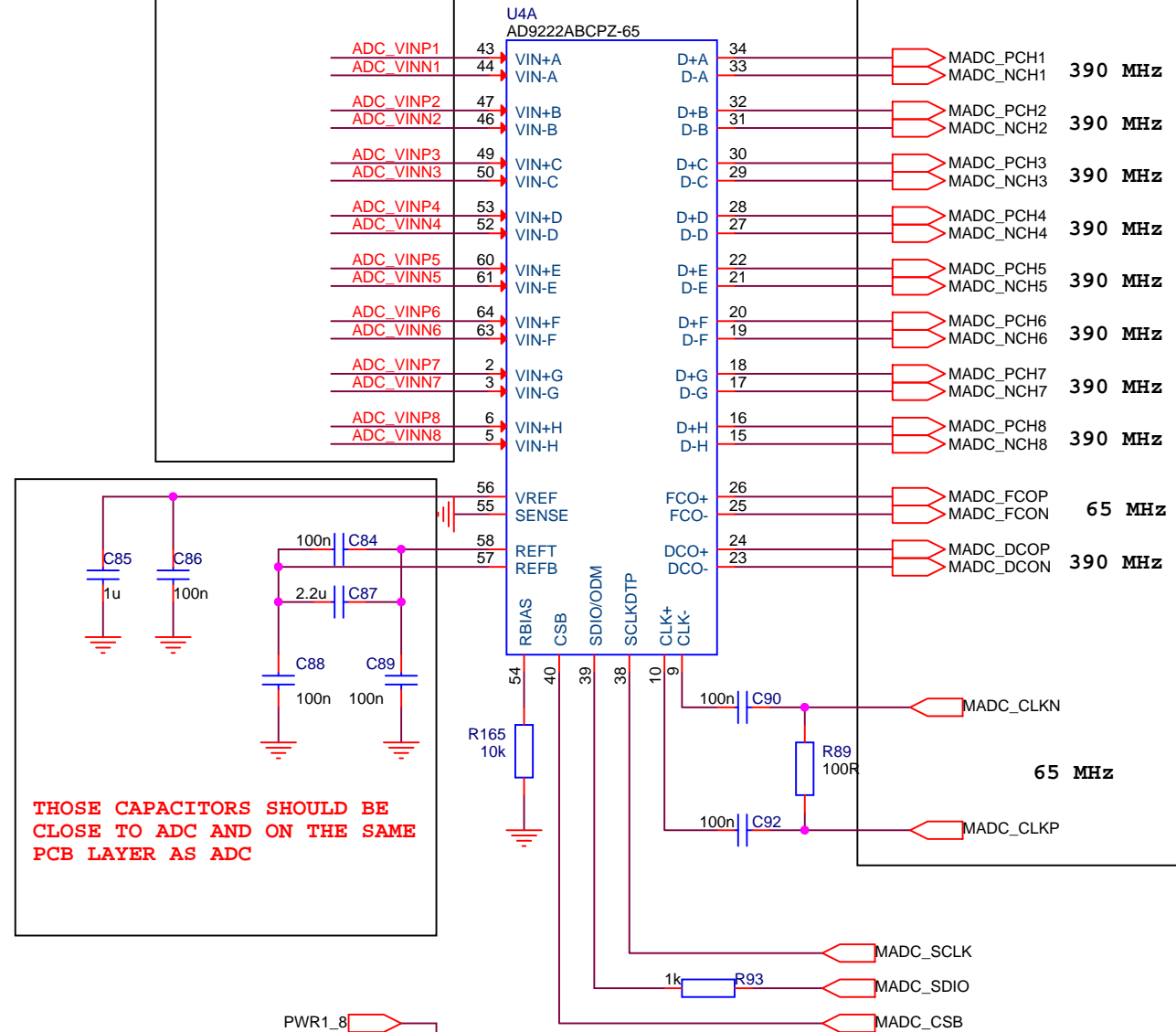
### MULTICHANNEL ADC

ALL PIRS HERE ARE DIFFERENTIAL



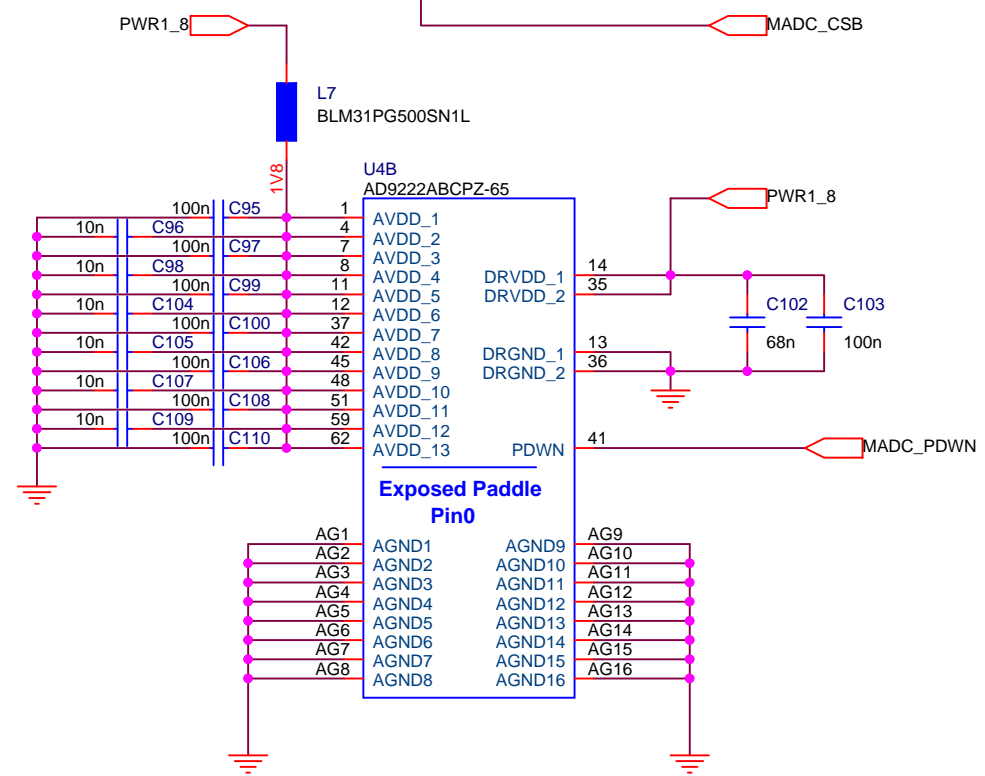
PLACE 100R RESISTOR CLOSE TO INPUT CONNECTOR

ALL SIGNALS HERE ARE DIFFERENTIAL

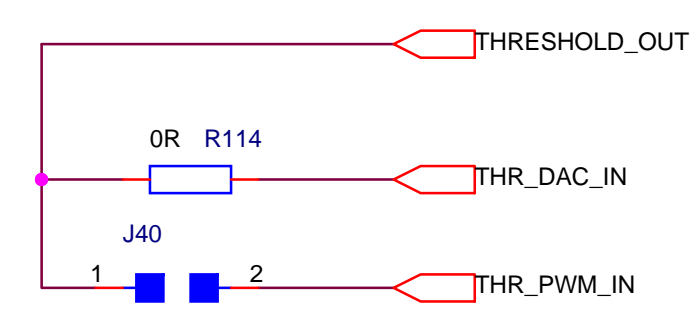
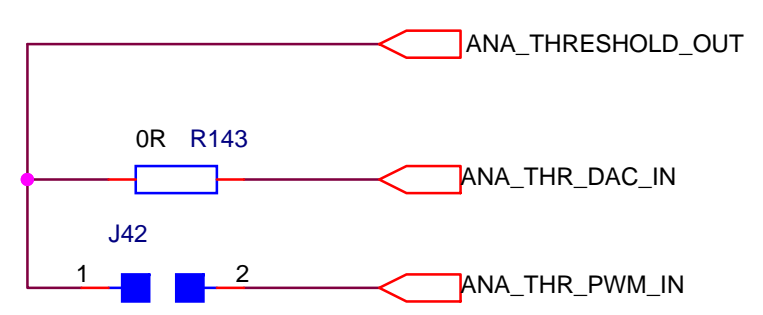
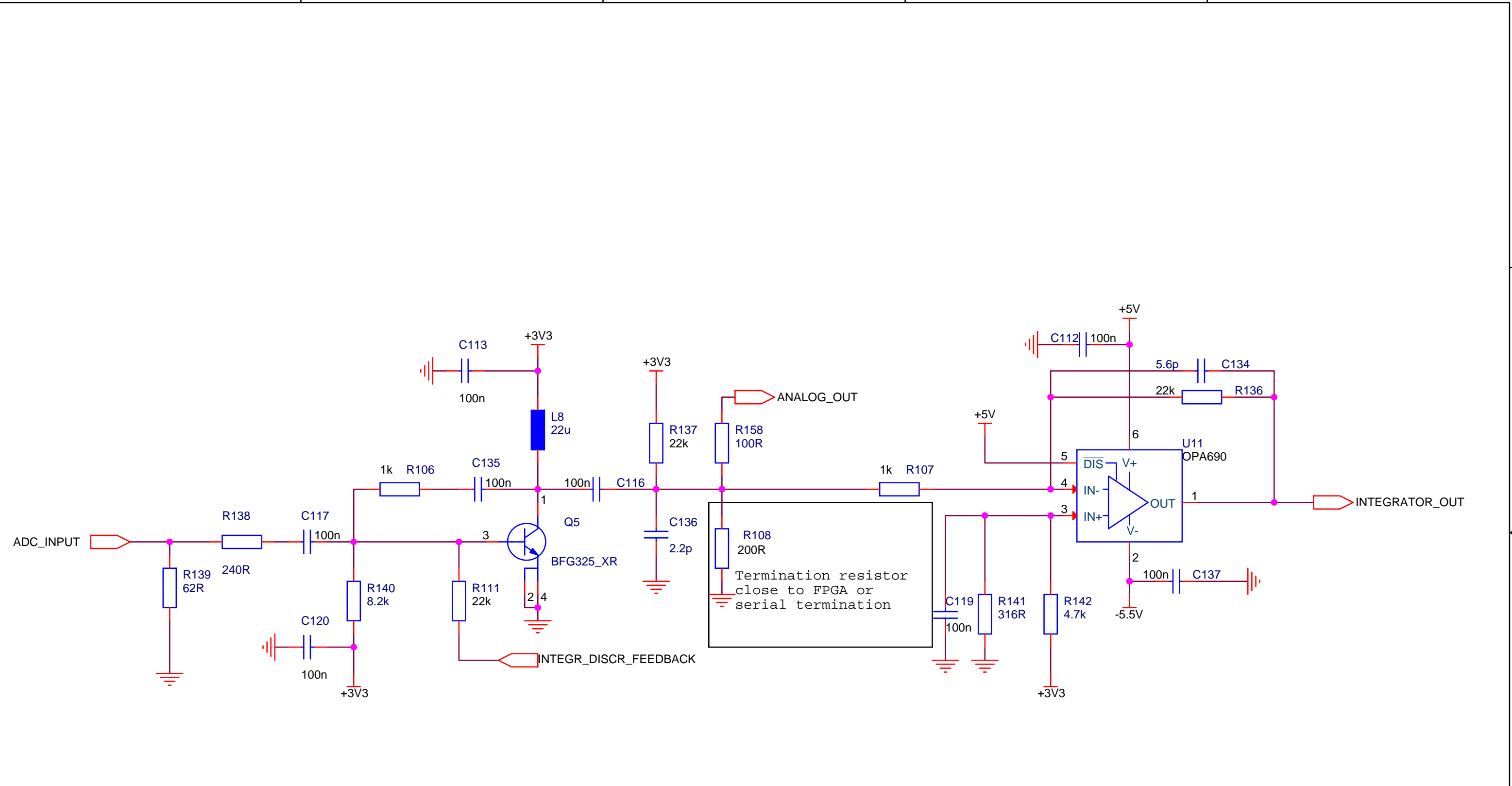


THOSE CAPACITORS SHOULD BE CLOSE TO ADC AND ON THE SAME PCB LAYER AS ADC

ALL SIGNALS HERE ARE DIFFERENTIAL



### MULTICHANNEL ADC

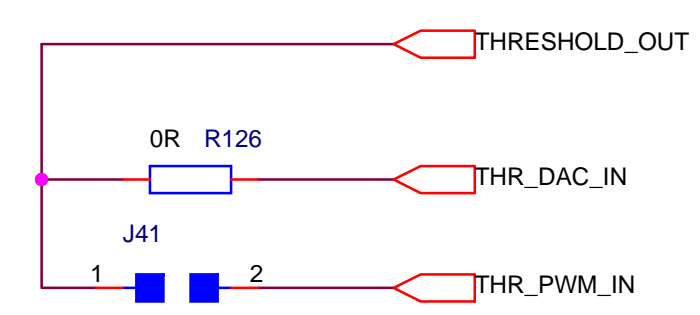
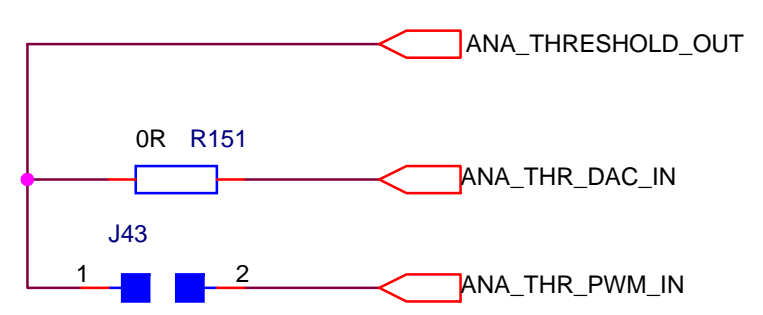
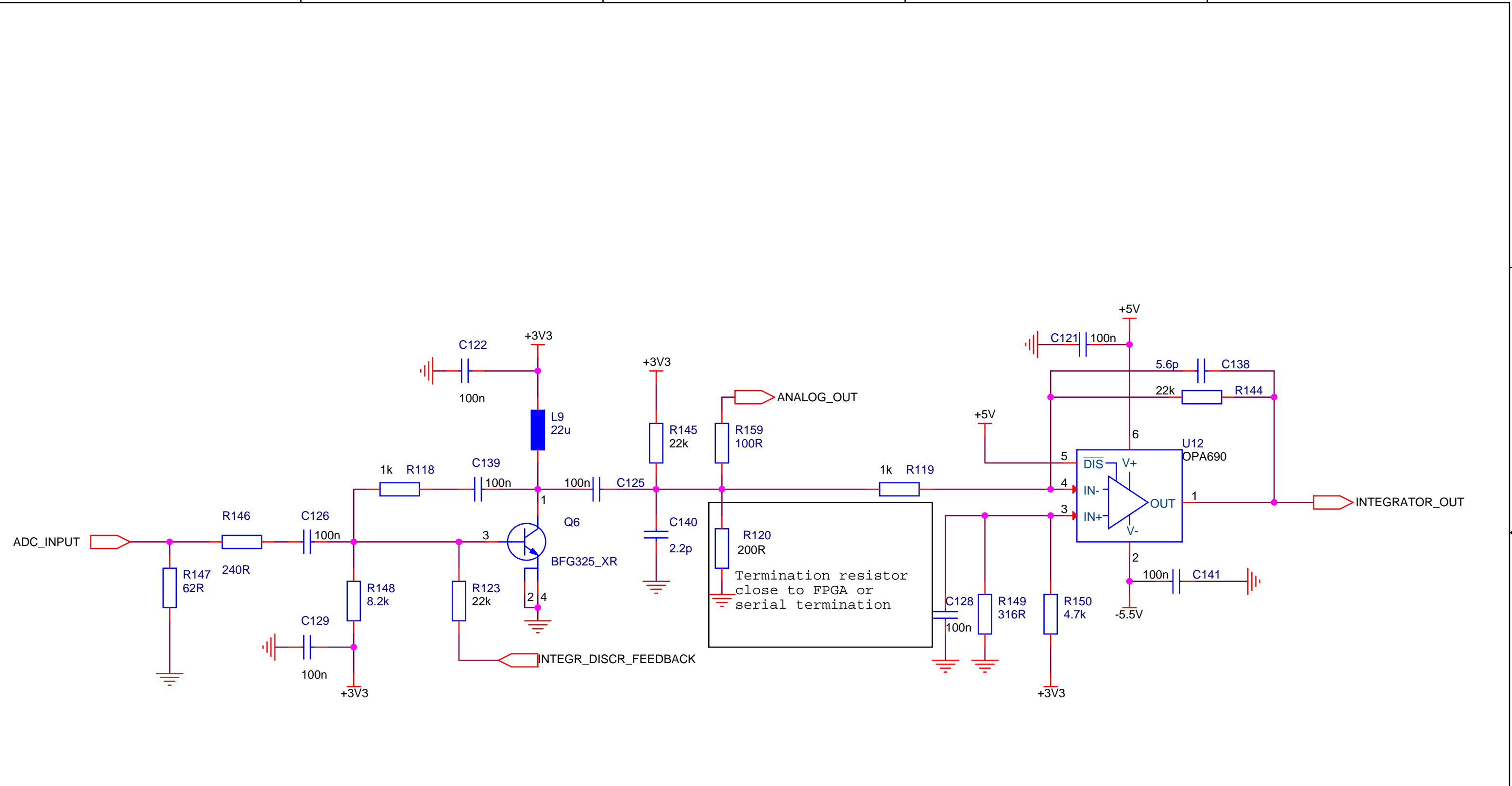




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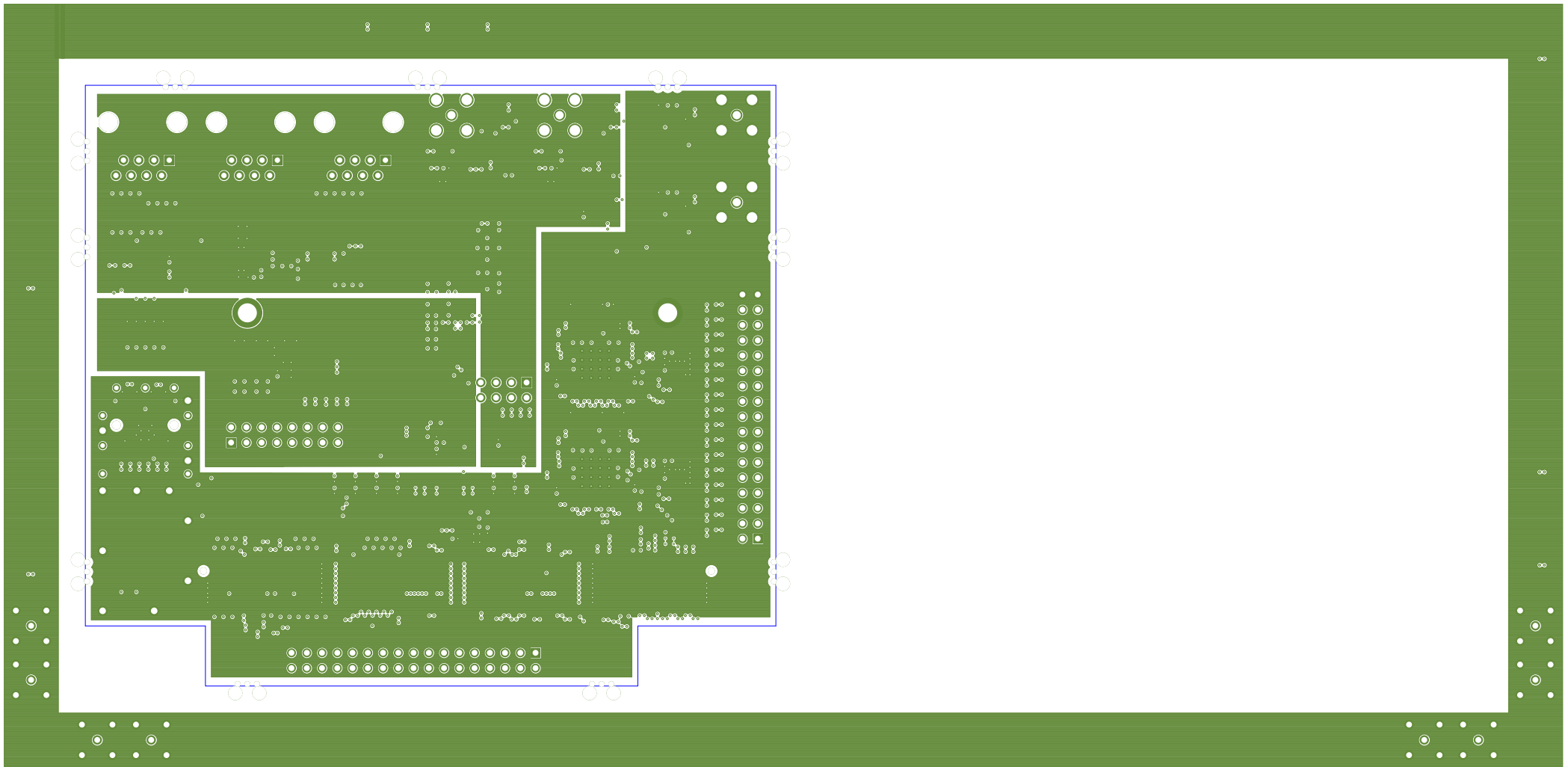
## WOLFGANG\_ADC

Design: K:\GSIJOB\HADES\TRBV3\MULTITESTADDON1\MULTITESTADDON1.DSN	
Modified: Wednesday, January 04, 2012	Size: A4 Page: 12/ 13
Designer: M.Kajetanowicz	Layouter: S.Voltz



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# WOLFGANG\_ADC

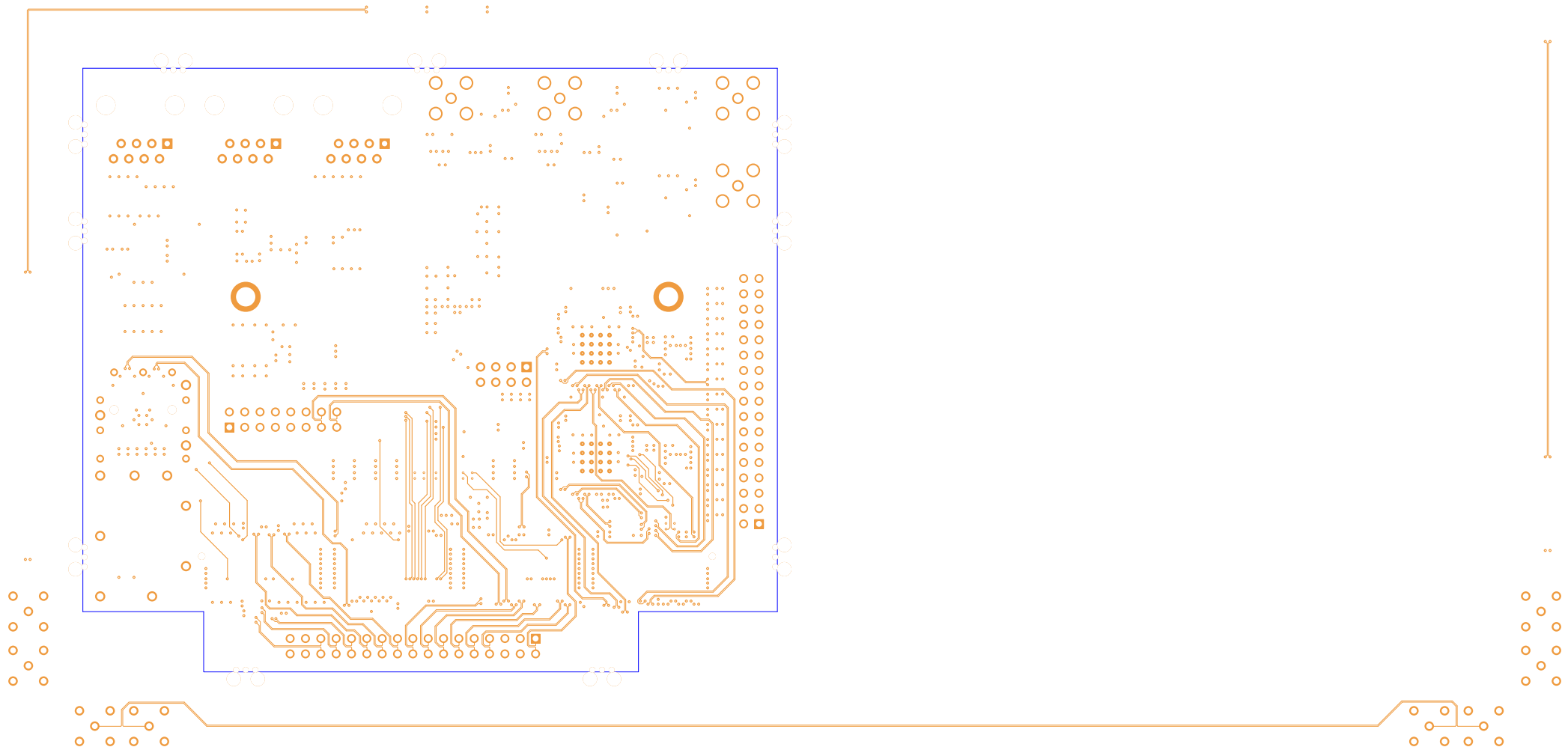


Jobname	Date	Designer	Layouter
MultiTestAddon1	01.2012	M.Kajetanowicz M.Traxler	S.Voltz

Layer Nickname

106

IN6- Planes: +2.5V, +5V, GND

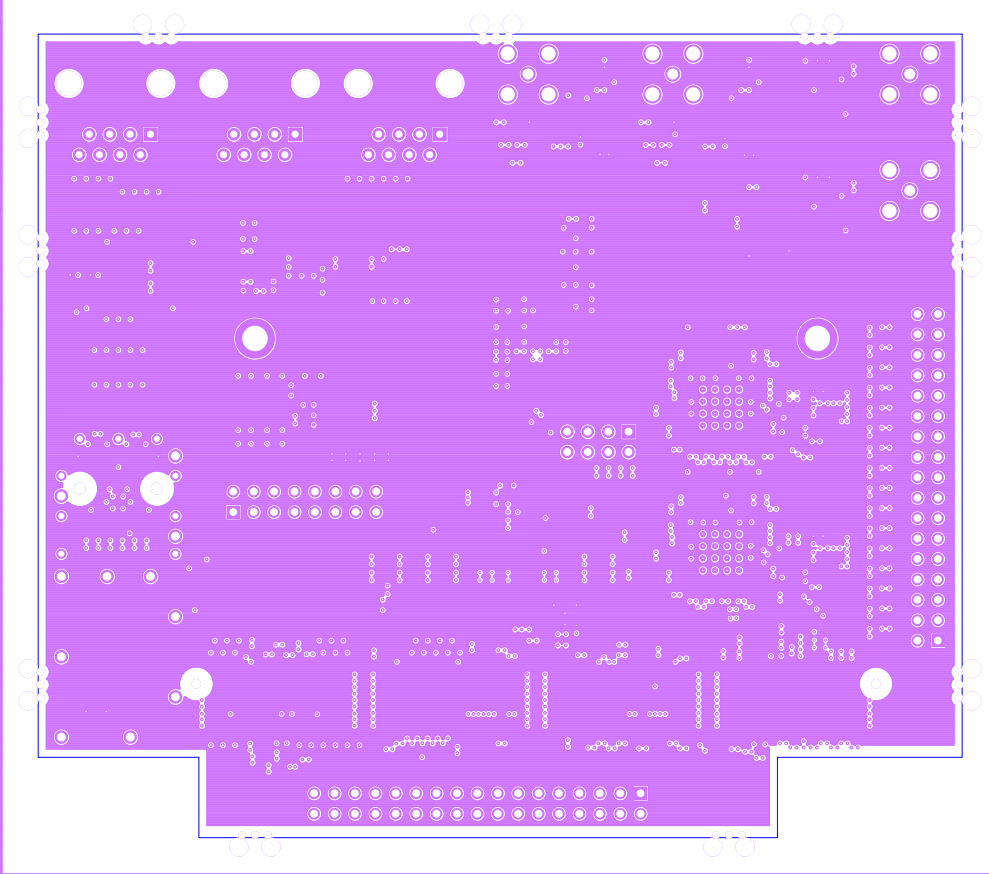


Jobname	Date	Designer	Layouter
MultiTestAddon1	01.2012	M.Kajetanowicz M.Traxler	S.Voltz

Layer Nickname

I05

IN5- Diff.Pairs



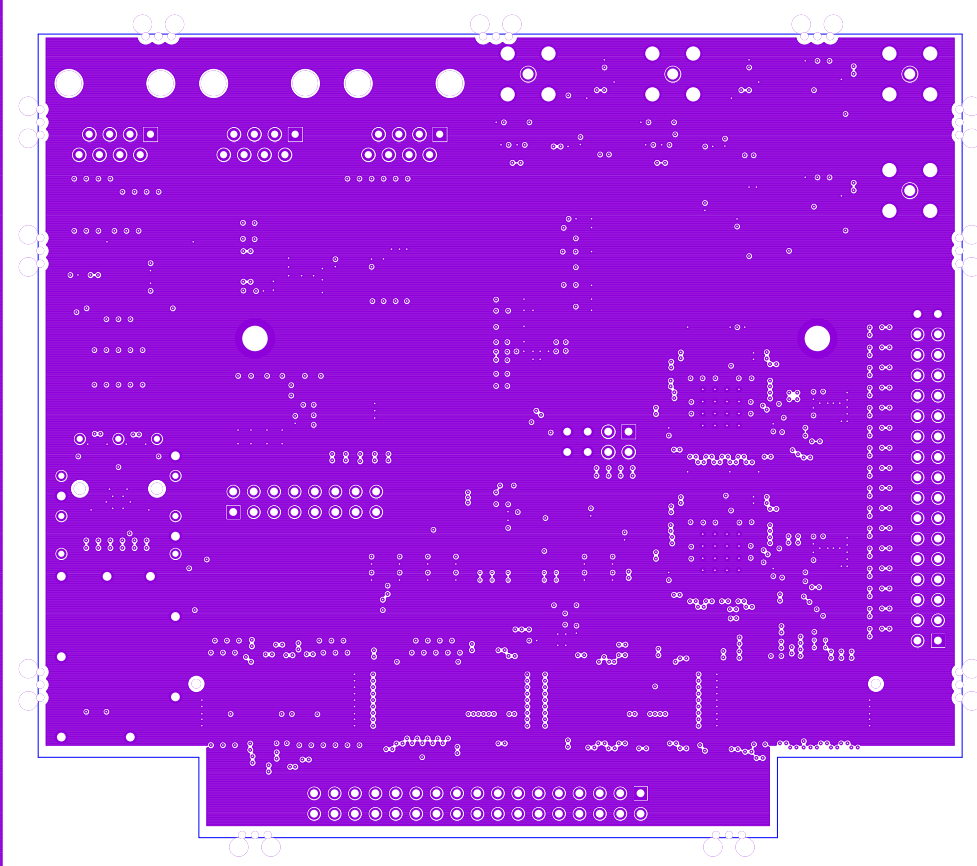
Jobname	Date	Designer	Layouter
MultiTestAddon1	01.2012	M.Kajetanowicz M.Traxler	S.Voltz

Layer Nickname

104

IN4- +3.3V-Plane

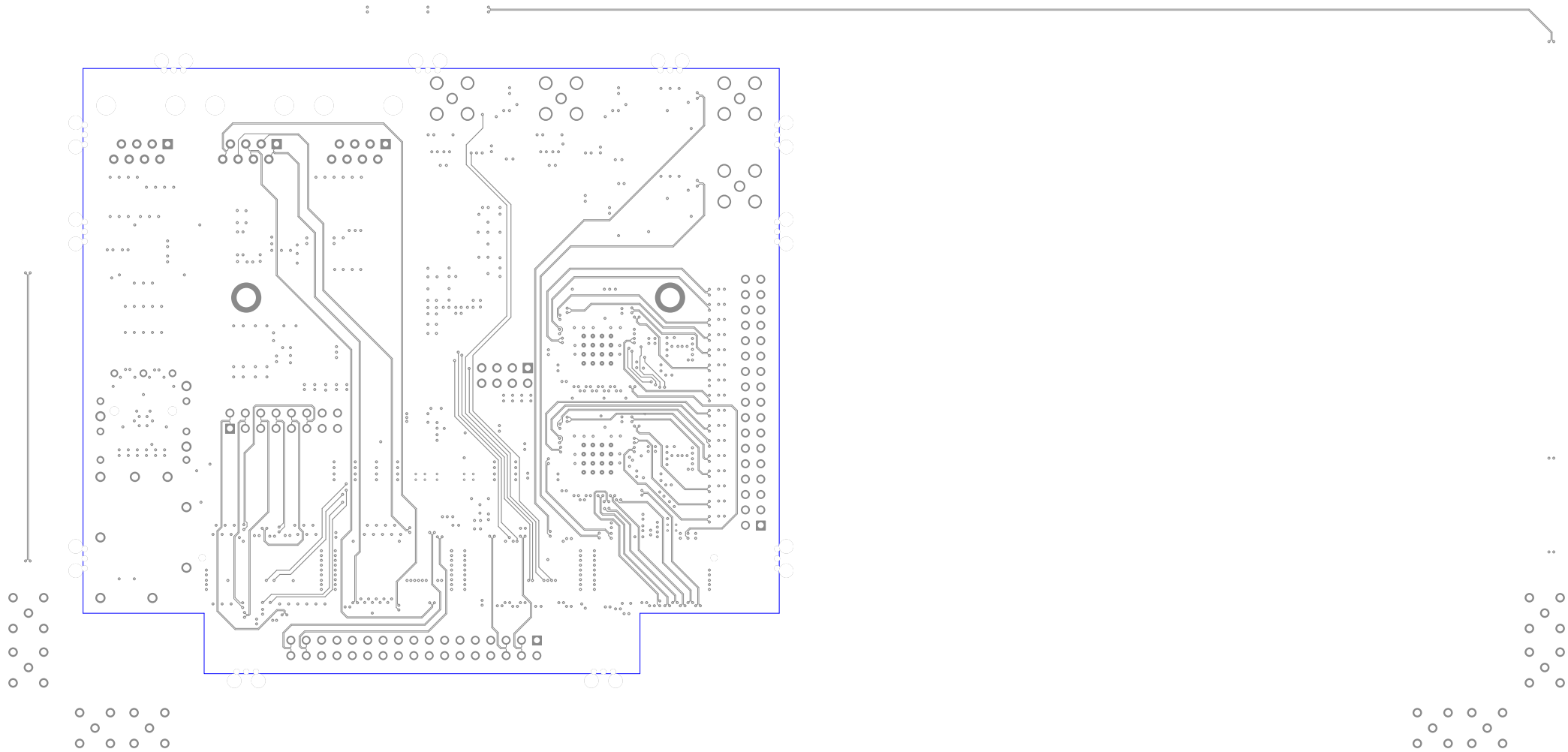




Jobname	Date	Designer	Layouter
MultiTestAddon1	01.2012	M.Kajetanowicz M.Traxler	S.Voltz

### IN3- GND-Plane

Layer Nickname

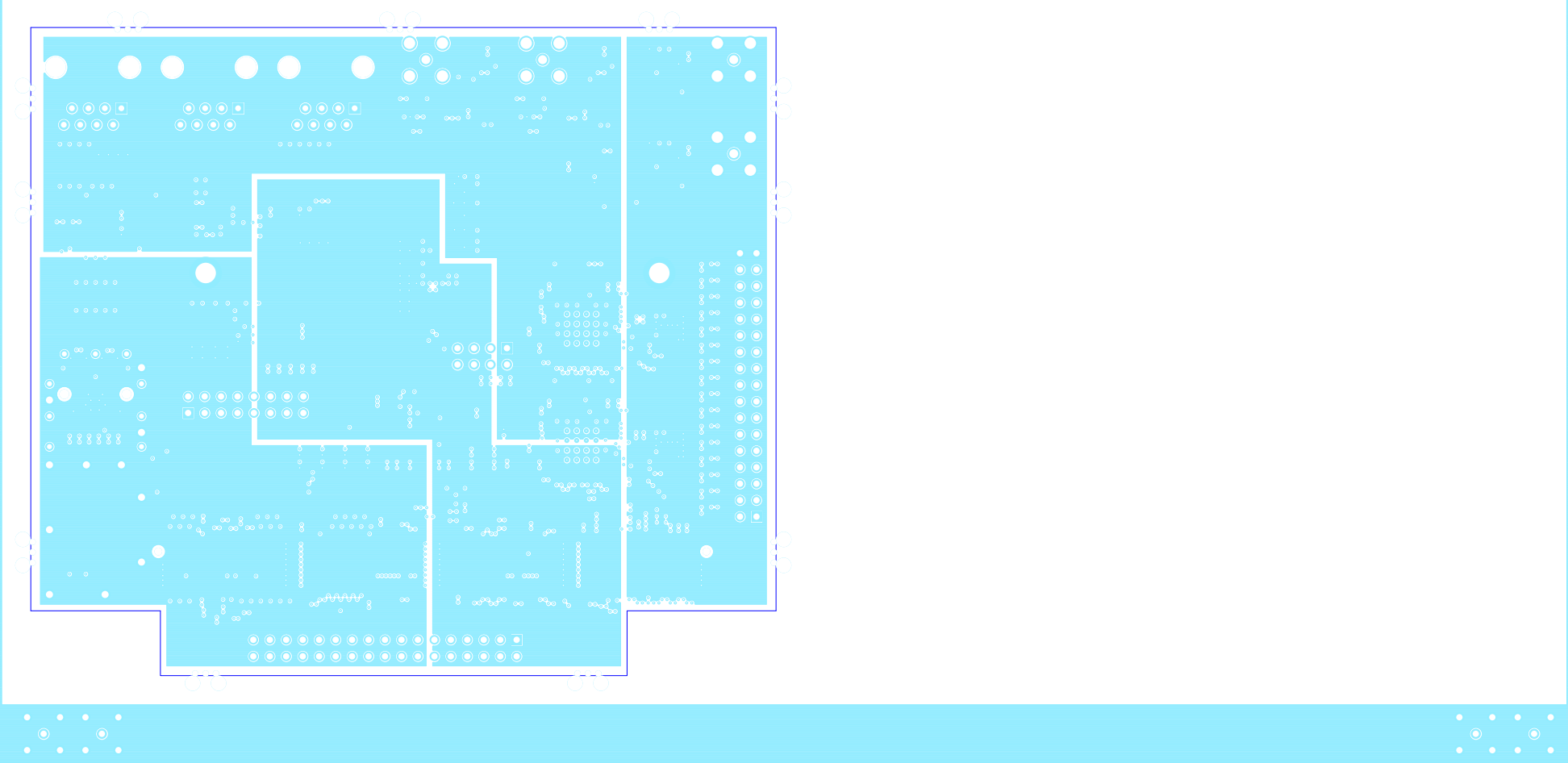


Jobname	Date	Designer	Layouter
MultiTestAddon1	01.2012	M.Kajetanowicz M.Traxler	S.Voltz

## IN2- Diff. Pairs

Layer Nickname

102

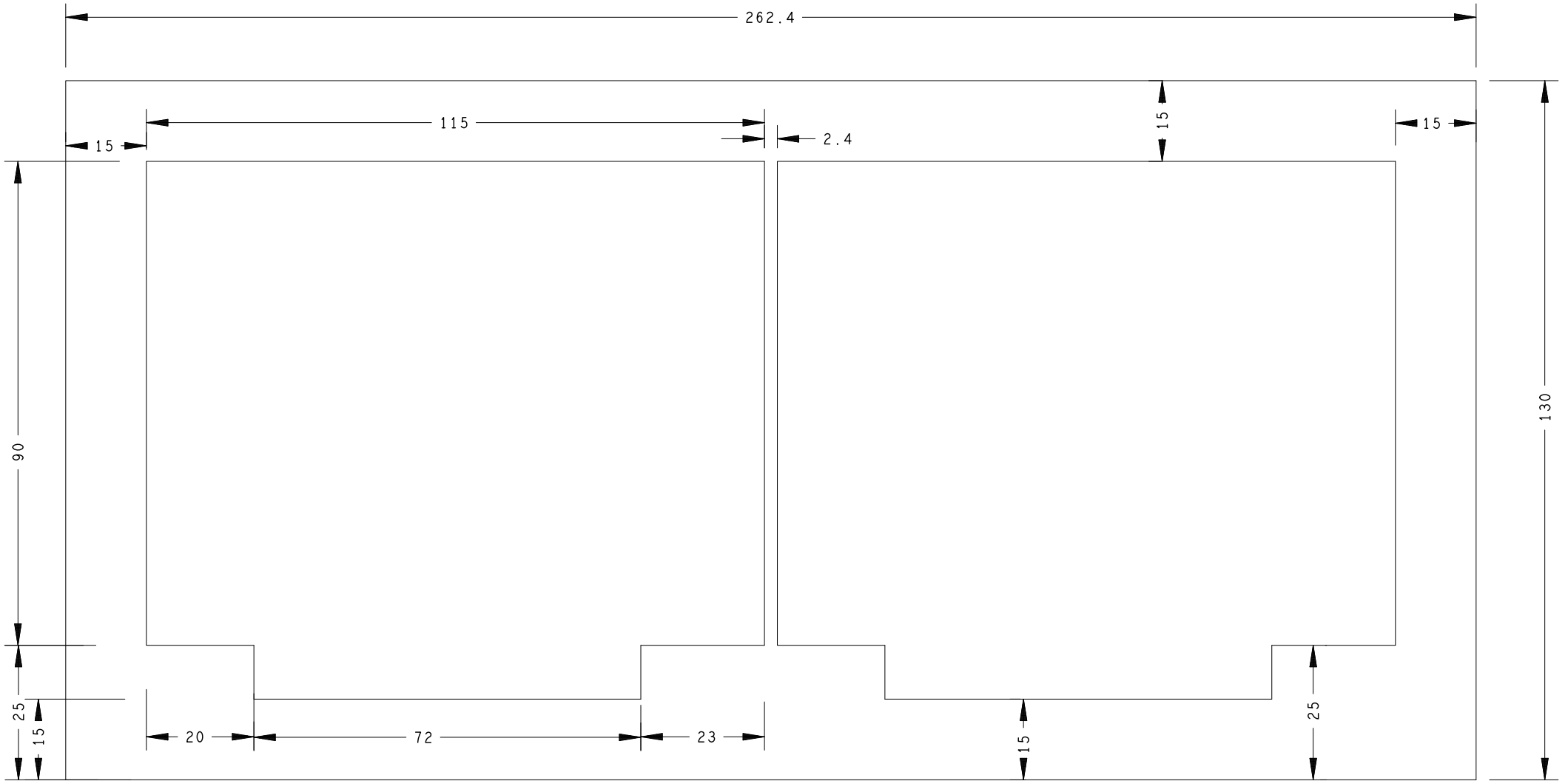


Jobname	Date	Designer	Layouter
MultiTestAddon1	01.2012	M.Kajetanowicz M.Traxler	S.Voltz

IN1- Planes: +6V, -5.5V, GND

Layer Nickname

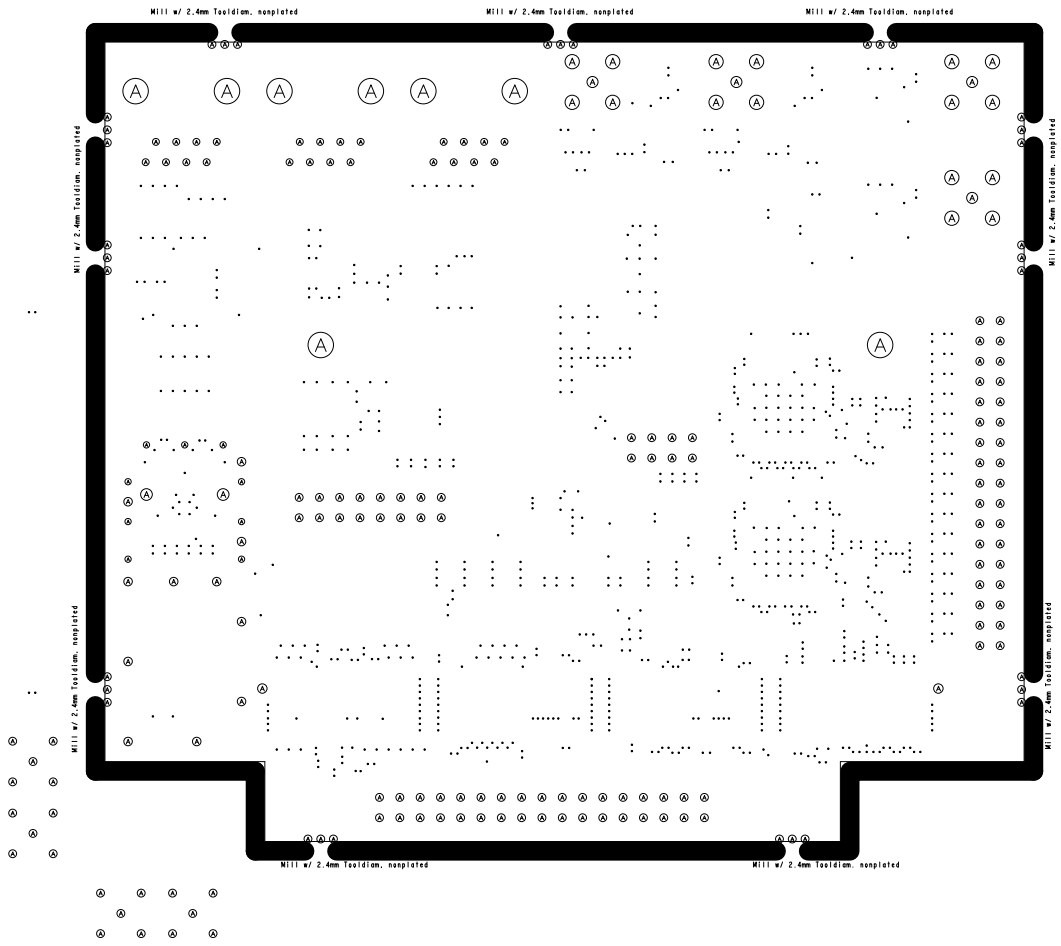
101



Jobname	Date	Designer	Layouter
MultiTestAddon1	01.2012	M.Kajetanowicz M.Traxler	S.Voltz

Layer Nickname

Fab



DRILL CHART: TOP to BOTTOM			
ALL UNITS ARE IN MILLIMETERS			
FIGURE	SIZE	PLATED	QTY
.	0.2	PLATED	902
.	0.4	PLATED	1
o	0.8	PLATED	9
o	0.9	PLATED	24
o	1.0	PLATED	132
o	1.1	PLATED	11
o	1.4	PLATED	4
o	1.8	PLATED	16
(A)	3.2	PLATED	2
o	1.0	NON-PLATED	33
o	1.2	NON-PLATED	2
o	1.5	NON-PLATED	2
o	2.4	NON-PLATED	22
(A)	3.2	NON-PLATED	6

TOTAL HOLES: 1166



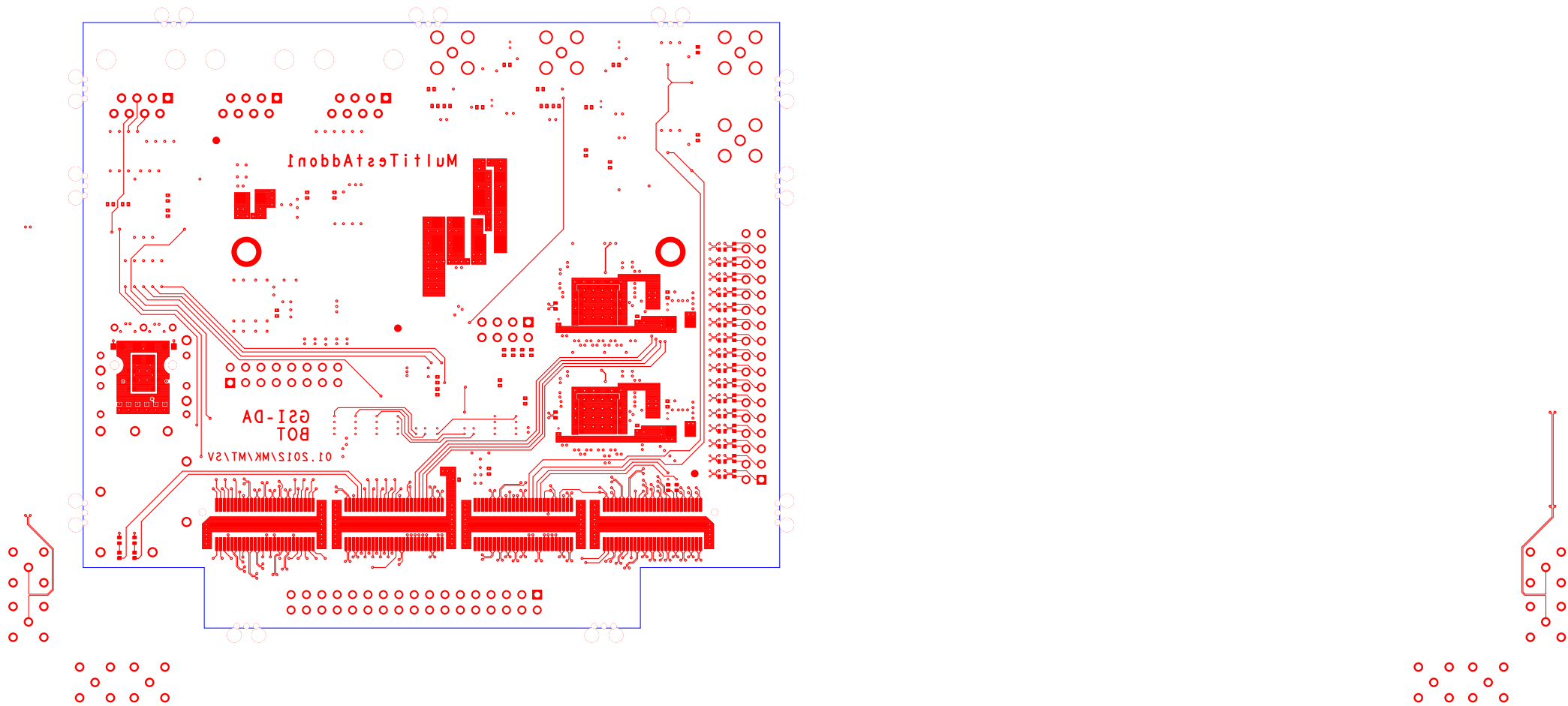
Jobname MultiTestAddon1 Date 01.2012 Designer M.Kajetanowicz M.Traxler Layouter S.Voltz

Layer Nickname

Drd

: : :

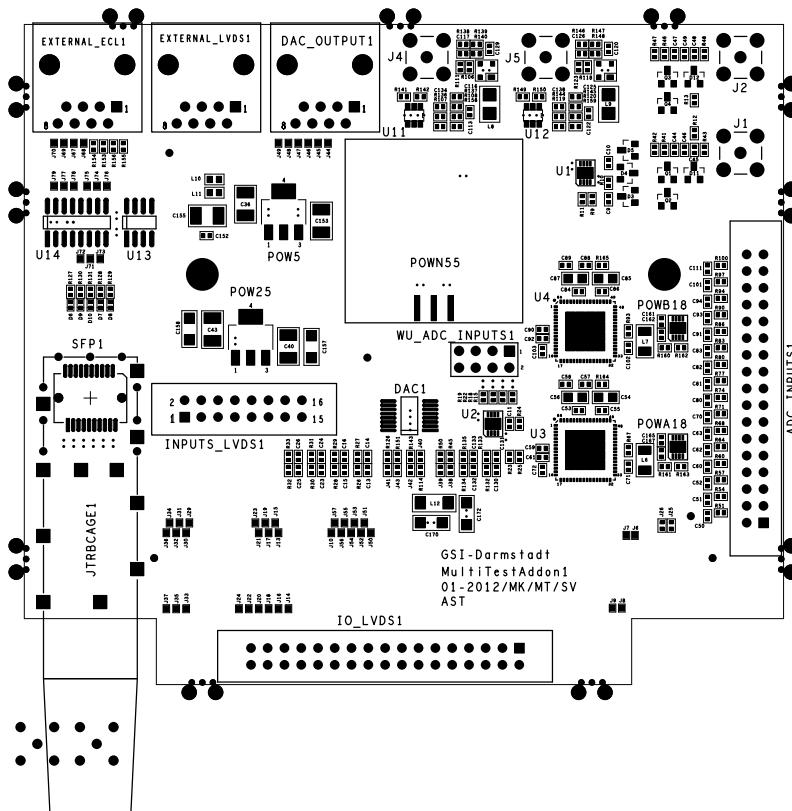
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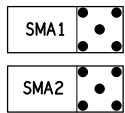
Jobname	Date	Designer	Layouter
MultiTestAddon1	01.2012	M.Kajetanowicz M.Traxler	S.Voltz

Layer Nickname      Bot

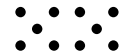
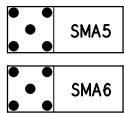
## BOT- Signals



SMA1+2 werden nicht bestueckt



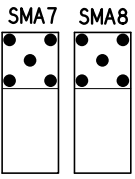
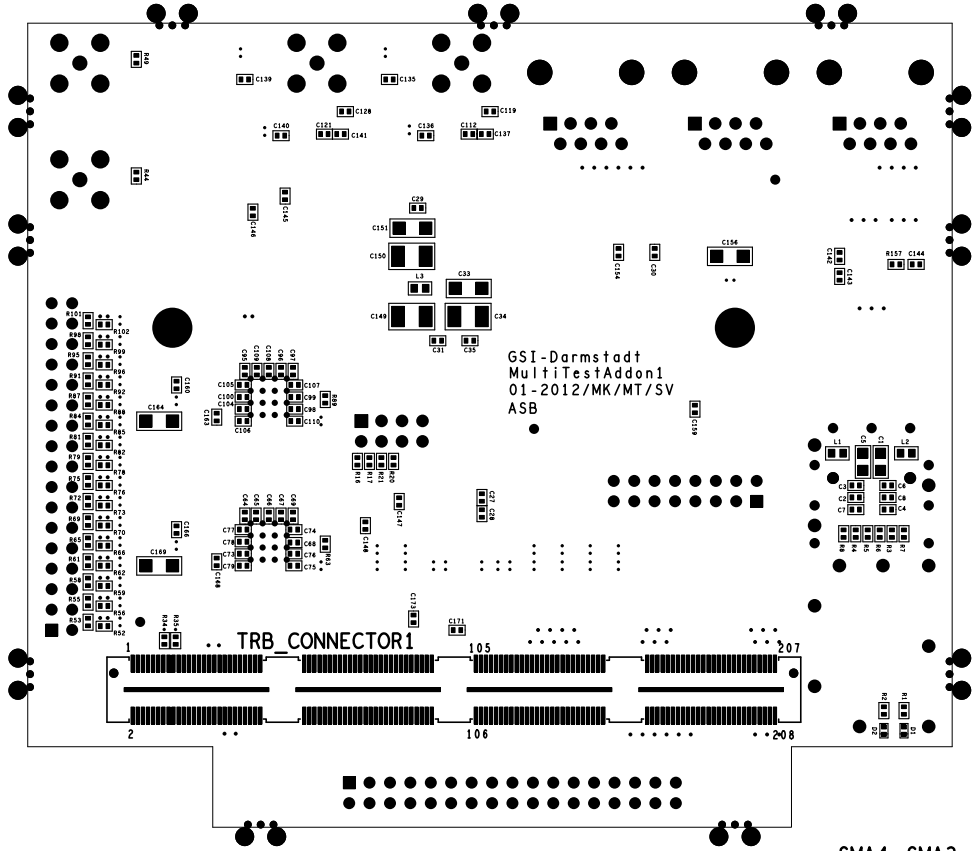
SMA5+6 werden nicht bestueckt



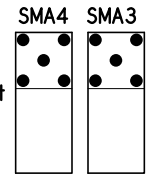
Jobname	Date	Designer	Layer	Nickname
MultiTestAddon1	01.2012	M.Kajetanowicz	S.Voltz	Ast

Layer Nickname

Ast



SMA7+8 werden nicht bestueckt



SMA3+4 werden nicht bestueckt

Jobname MultiTestAddon1  
 Date 01.2012  
 Designer M.Kajetanowicz  
 Layouter S.Volts  
 M.Trexler

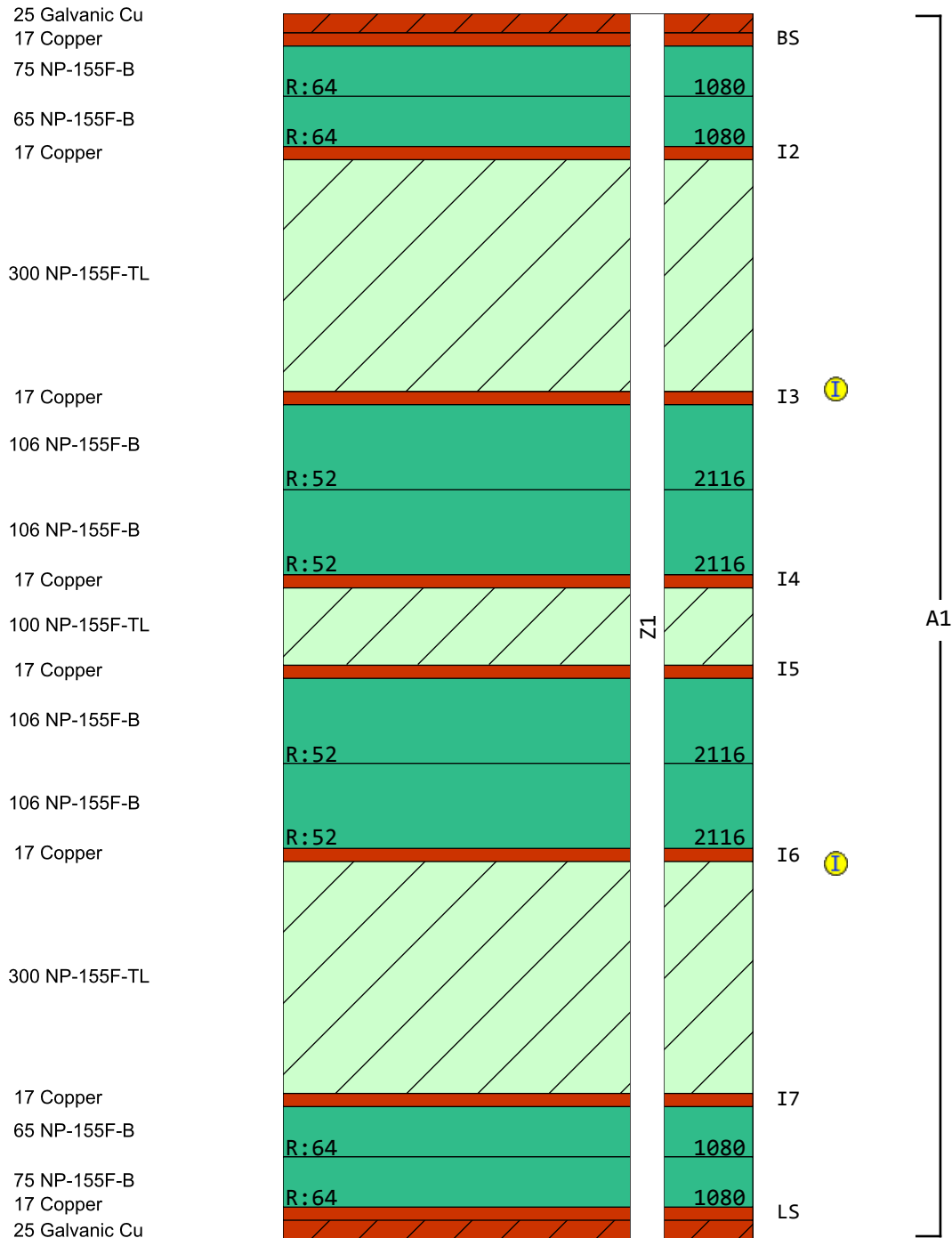


Material (µm)

Stack up

File

Assembly

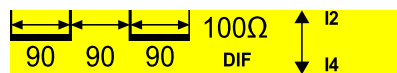


Thickness

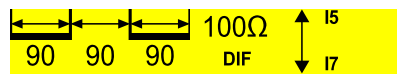
Bare Board	1.39 mm - 1.69 mm
Immersion Tin	1.39 mm - 1.70 mm
Hot-Air	1.41 mm - 1.71 mm
Immersion Gold	1.39 mm - 1.70 mm

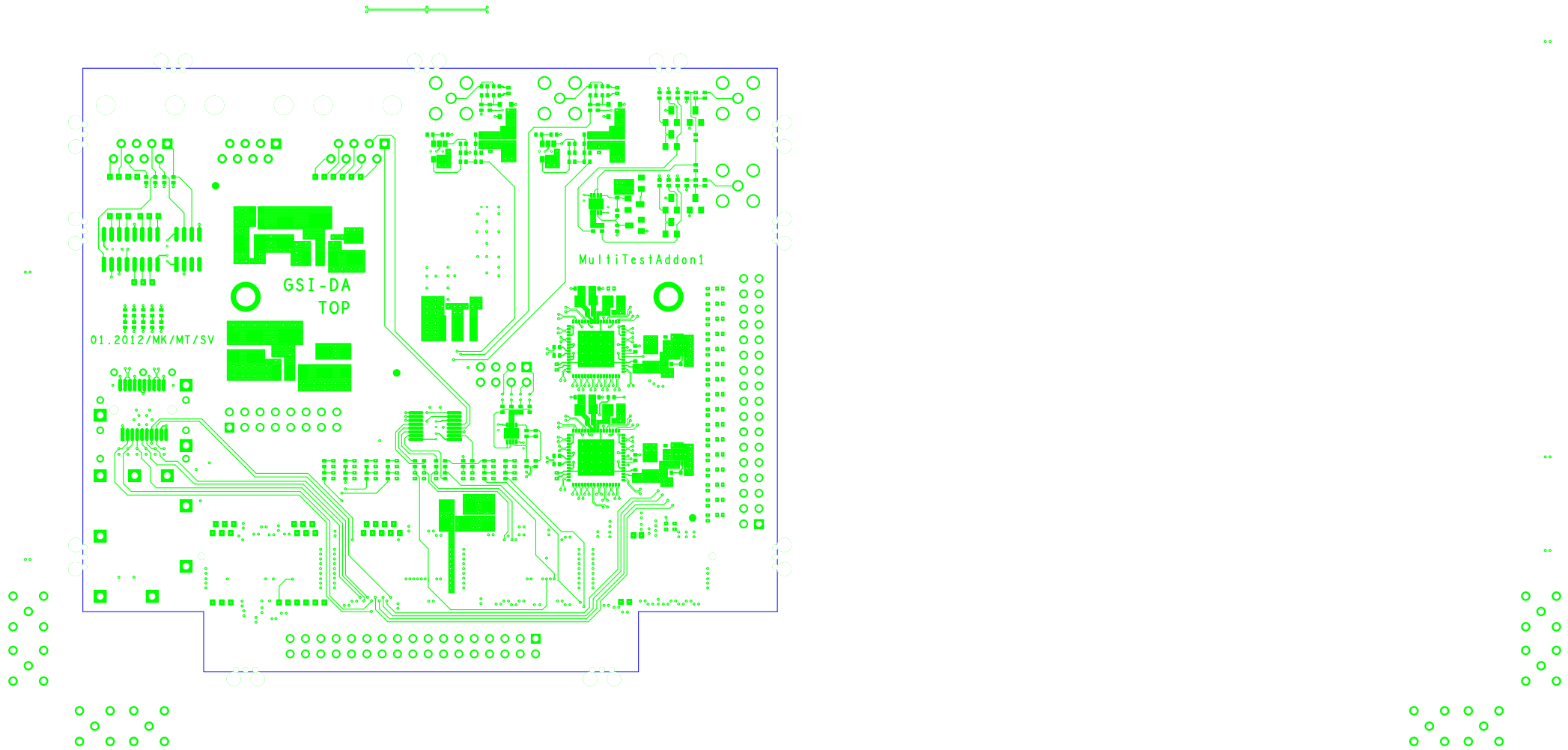
Date 14.01.2011  
Generated by gbiernat

**i3**



**i6**

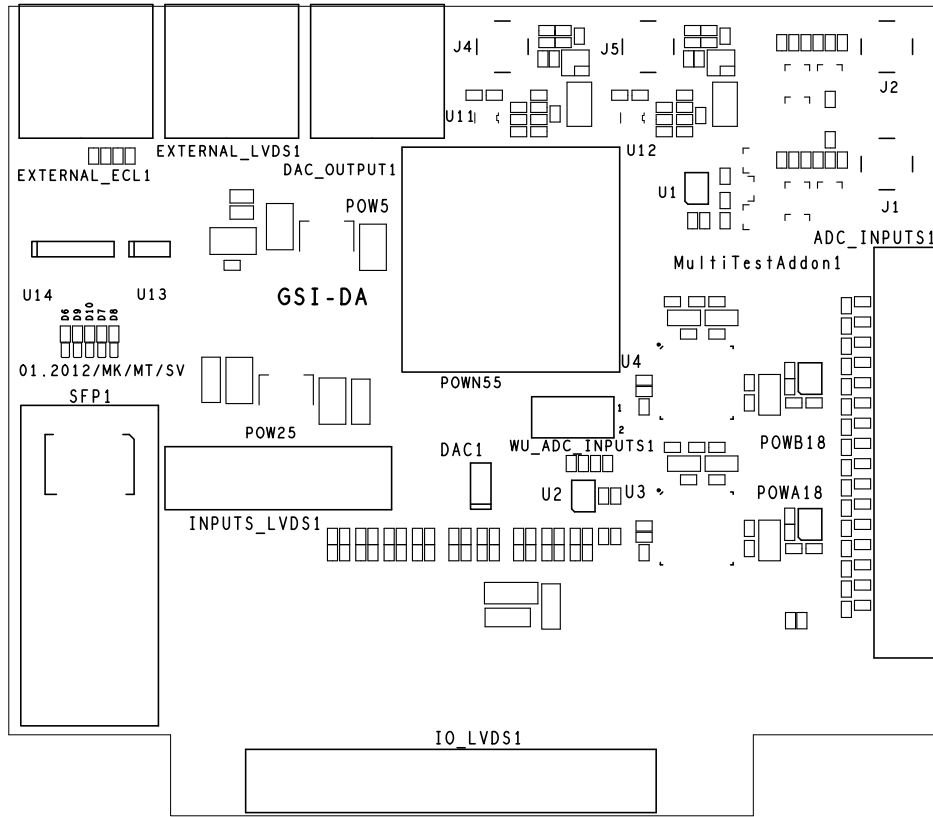




## TOP- Signals

Jobname	Date	Designer	Layouter
MultiTestAddon1	01.2012	M.Kajetanowicz M.Traxler	S.Voltz

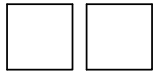
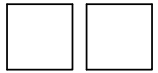
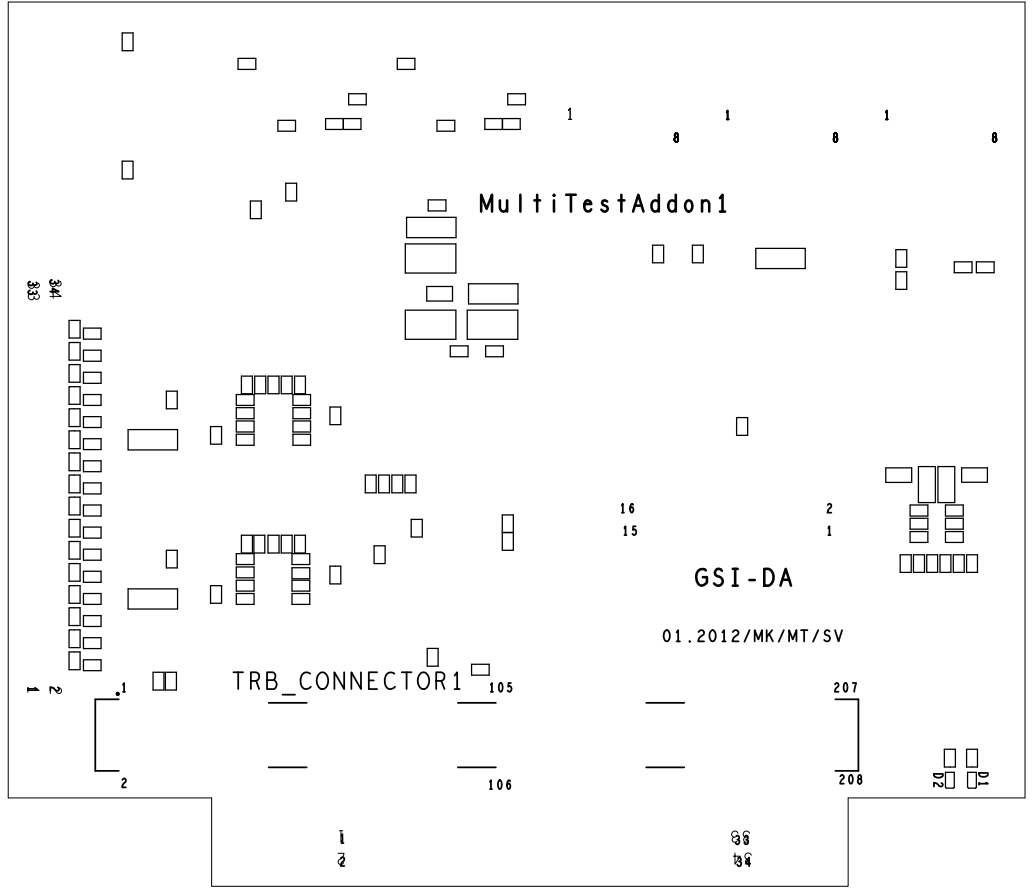
Layer Nickname  
Top



Jobname	Date	Designer	Layouter
MultiTestAddon1	01.2012	M.Kajetanowicz M.Traxler	S.Voltz

Layer Nickname

Sst



Jobname MultiTestAddon1  
 Date 01.2012  
 Designer M.Kajetanowicz  
 Layouter M. Traxler  
 2.Volts