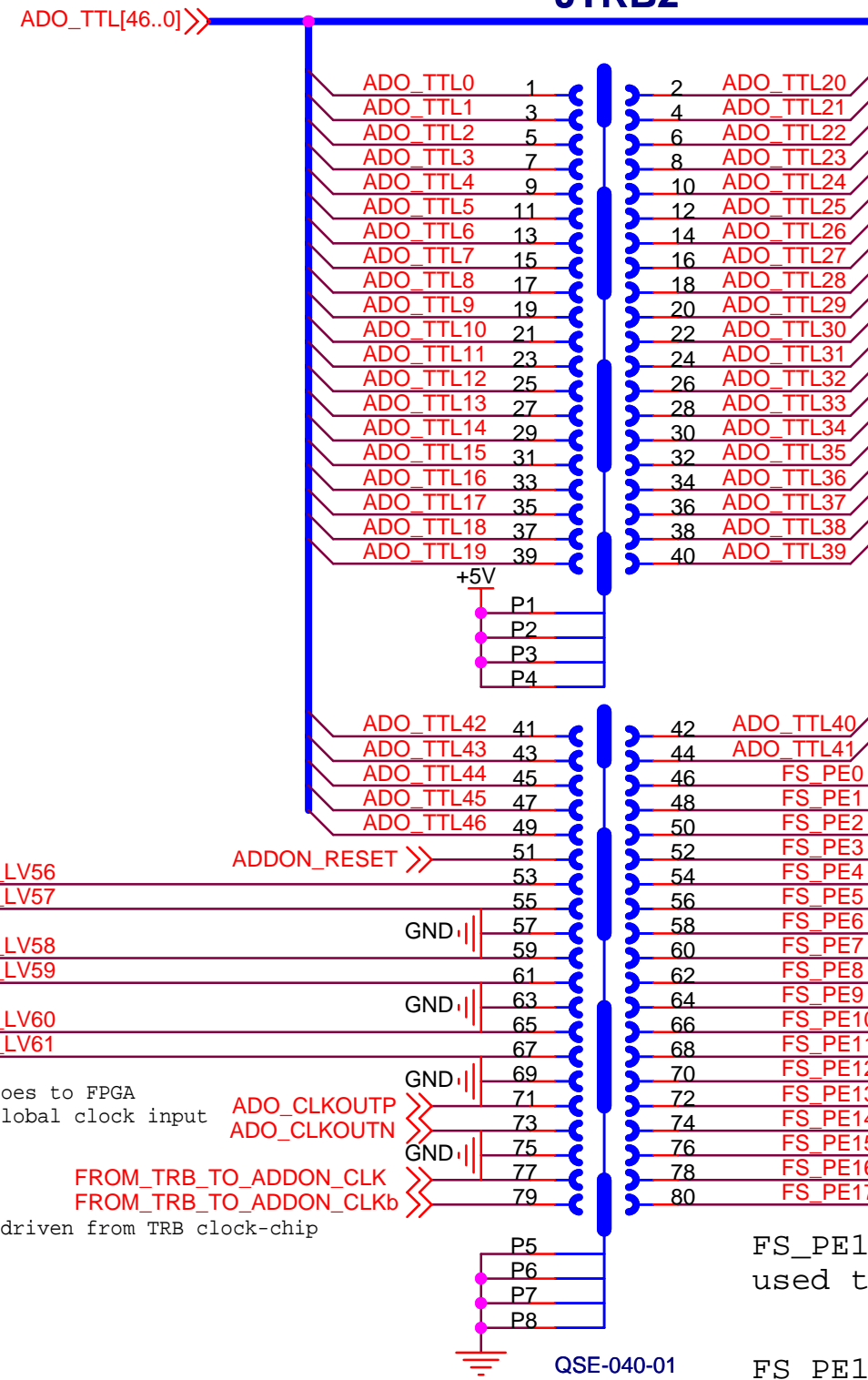
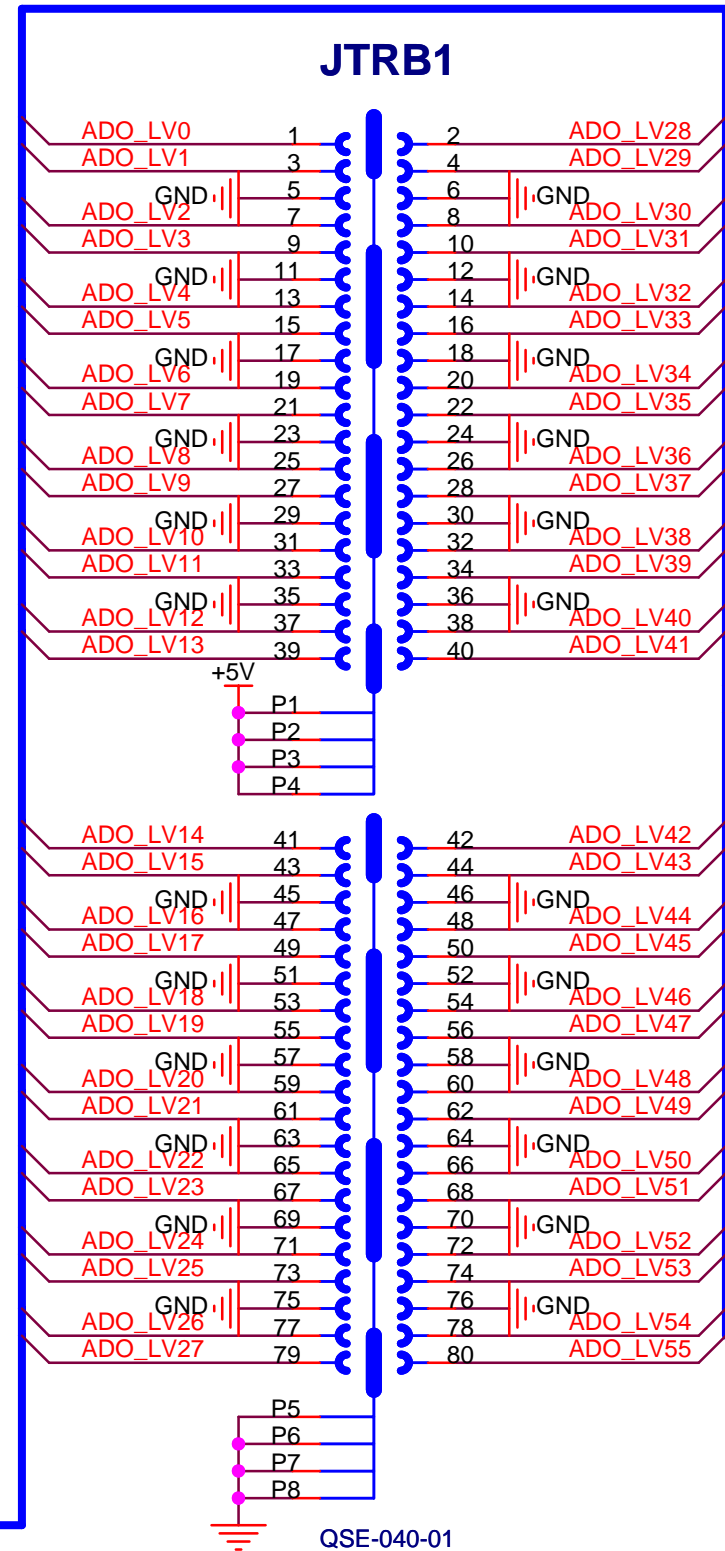


Even numbers: positive
 Odd numbers: negative



JTAG interface:
 (seen from TRB)
 TDI - TDO from FPGA on TRB (FS_PE0 high Z)
 TMS - FS_PE1
 TCK - FS_PE2
 TDO - FS_PE4

goes to FPGA
 global clock input

FROM_TRB_TO_ADDON_CLK
 FROM_TRB_TO_ADDON_CLKb
 driven from TRB clock-chip

FS_PE16 (SCL) and FS_PE17 (SDA)
 used to control ispPAC-POWER chip

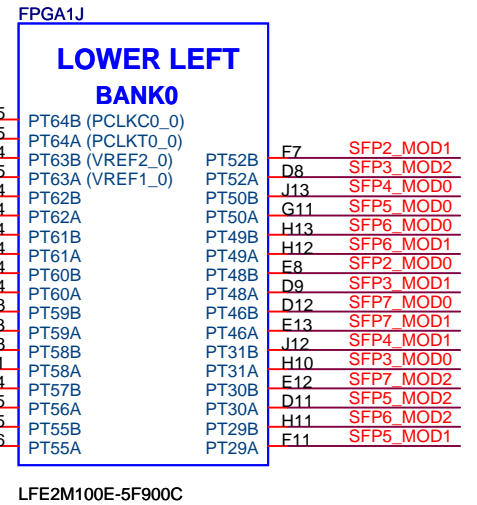
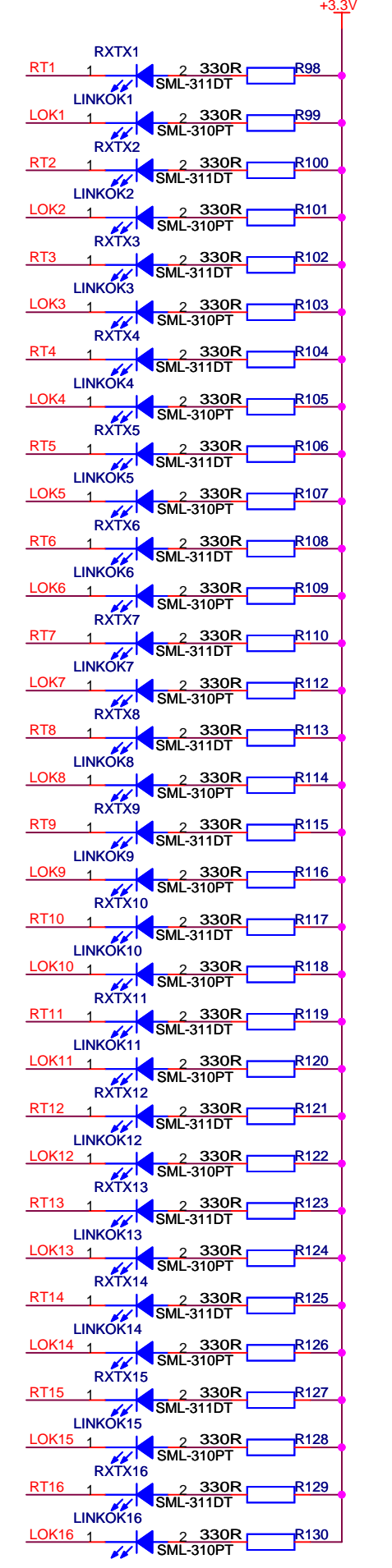
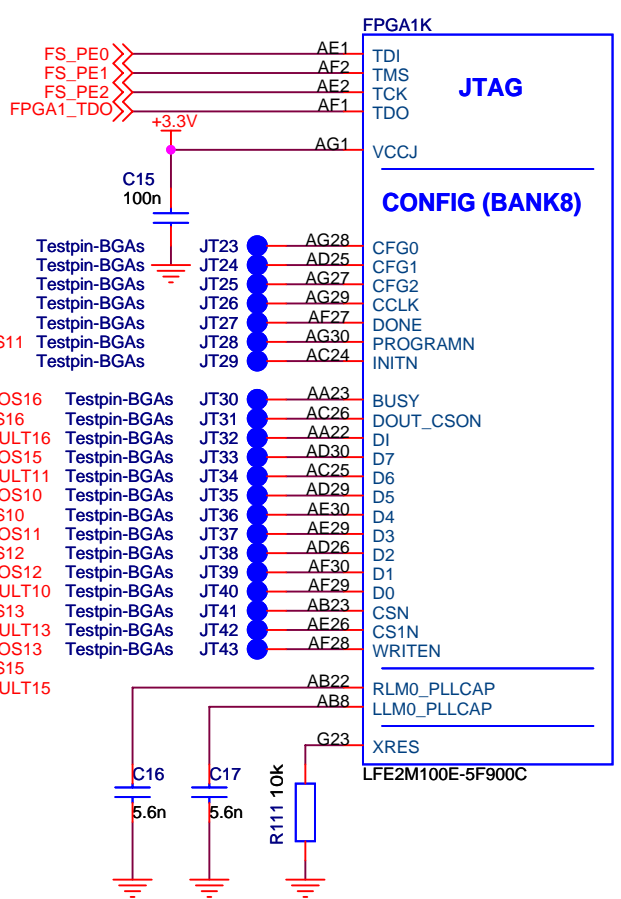
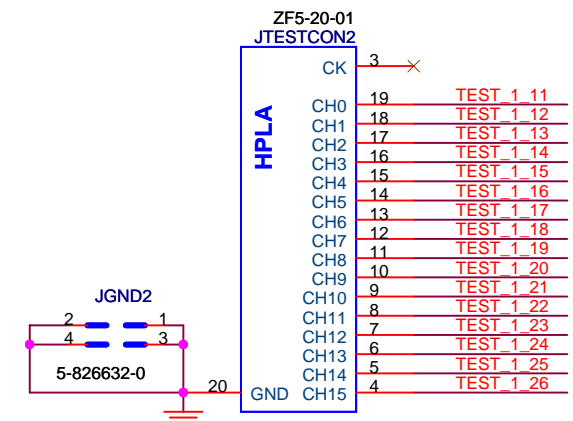
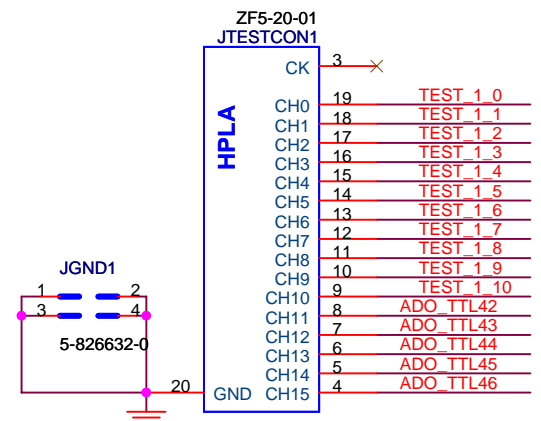
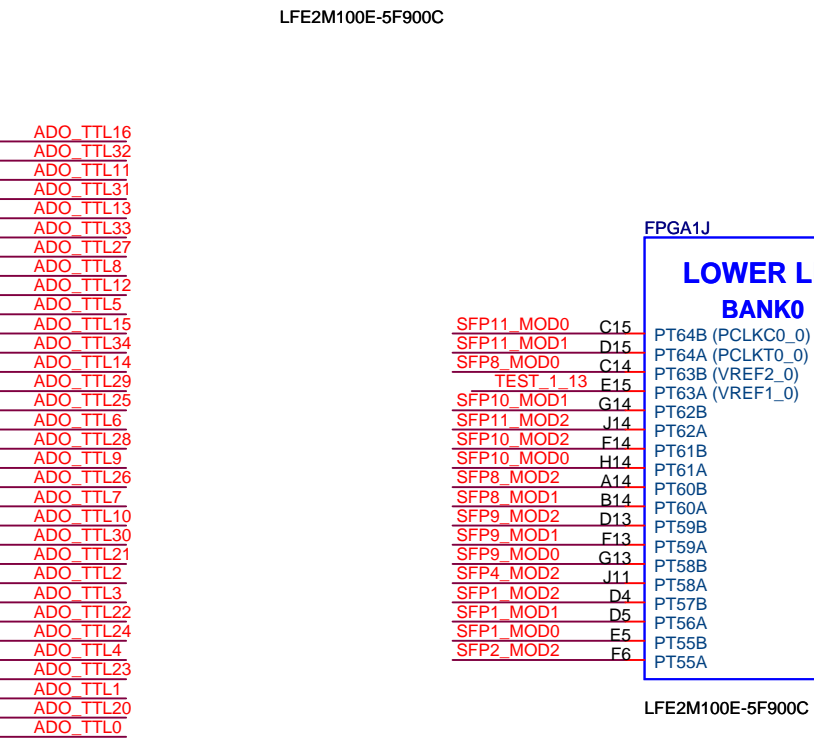
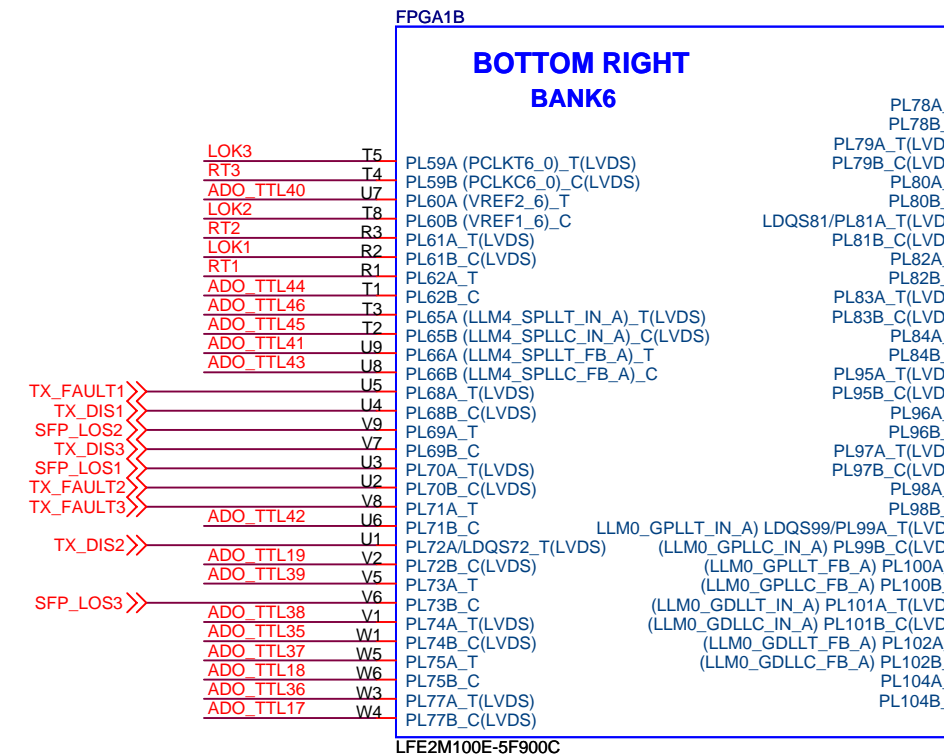
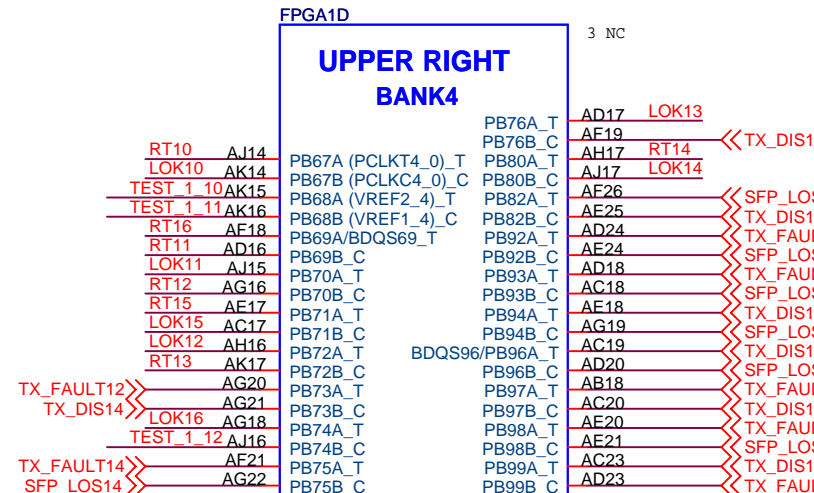
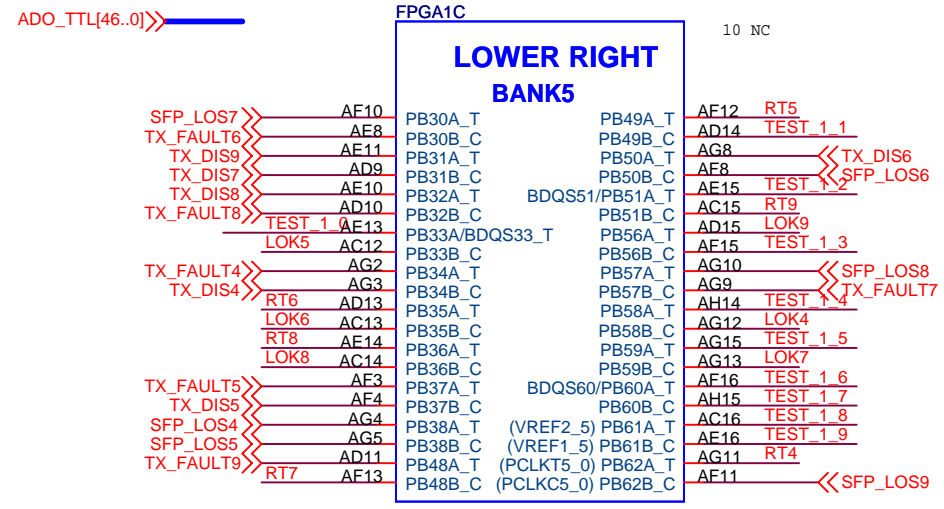
FS_PE12 - FS_PE15 connected to
 IN1 - IN4 in ispPAC-POWER chip
 general purpose inputs

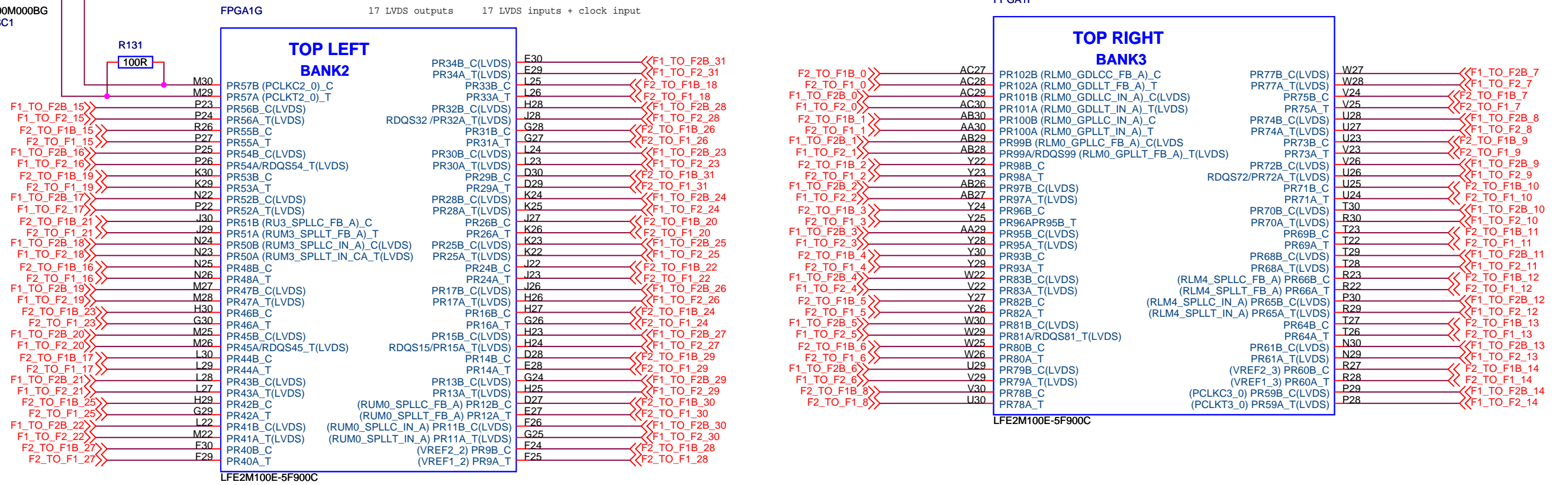
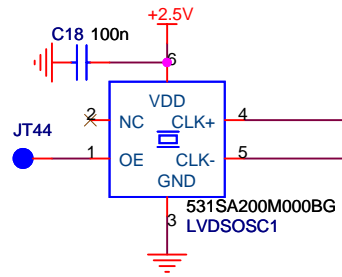
FS_PE11 - temperature control

ADO_LV[61..0]

QSE-040-01

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Size	Document Number				Rev
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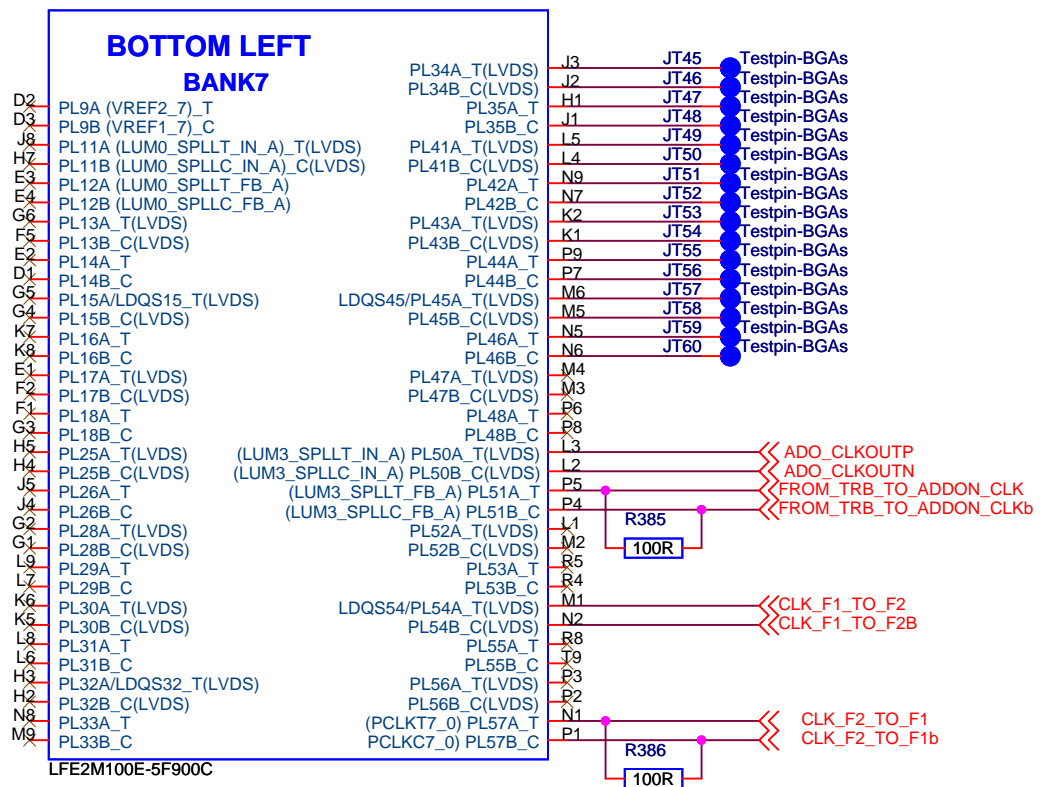
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F2_TO_F1_16	100R	R136	F2_TO_F1B_16
F2_TO_F1_17	100R	R140	F2_TO_F1B_17
F2_TO_F1_18	100R	R144	F2_TO_F1B_18
F2_TO_F1_19	100R	R148	F2_TO_F1B_19
F2_TO_F1_20	100R	R152	F2_TO_F1B_20
F2_TO_F1_21	100R	R156	F2_TO_F1B_21
F2_TO_F1_22	100R	R160	F2_TO_F1B_22

F2_TO_F1_23	100R	R133	F2_TO_F1B_23
F2_TO_F1_24	100R	R137	F2_TO_F1B_24
F2_TO_F1_25	100R	R141	F2_TO_F1B_25
F2_TO_F1_26	100R	R145	F2_TO_F1B_26
F2_TO_F1_27	100R	R149	F2_TO_F1B_27
F2_TO_F1_28	100R	R153	F2_TO_F1B_28
F2_TO_F1_29	100R	R157	F2_TO_F1B_29
F2_TO_F1_30	100R	R161	F2_TO_F1B_30
F2_TO_F1_31	100R	R163	F2_TO_F1B_31

F2_TO_F1_0	100R	R134	F2_TO_F1B_0
F2_TO_F1_1	100R	R138	F2_TO_F1B_1
F2_TO_F1_2	100R	R142	F2_TO_F1B_2
F2_TO_F1_3	100R	R146	F2_TO_F1B_3
F2_TO_F1_4	100R	R150	F2_TO_F1B_4
F2_TO_F1_5	100R	R154	F2_TO_F1B_5
F2_TO_F1_6	100R	R158	F2_TO_F1B_6

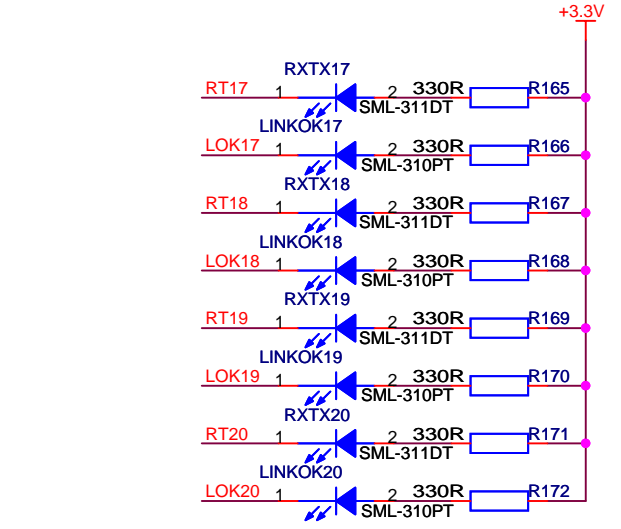
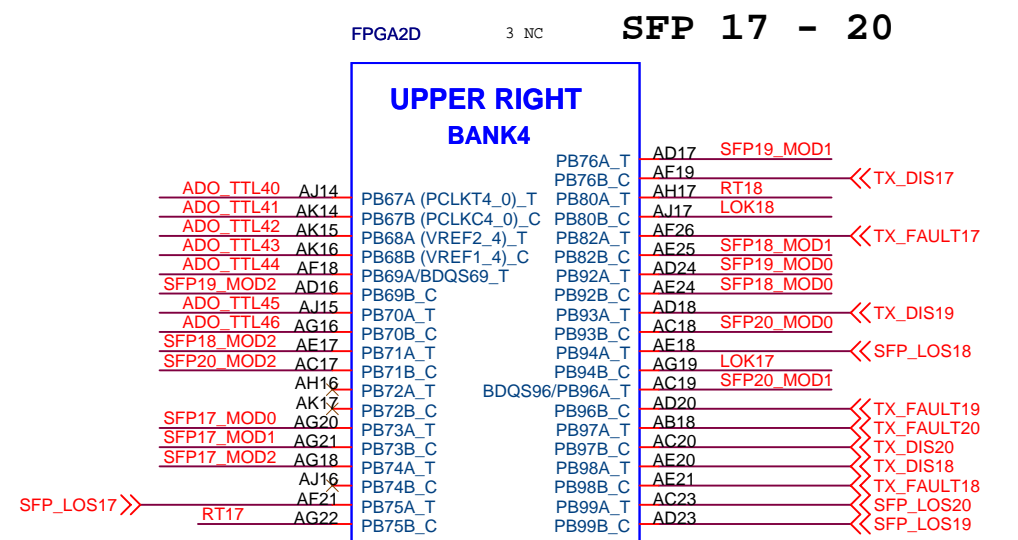
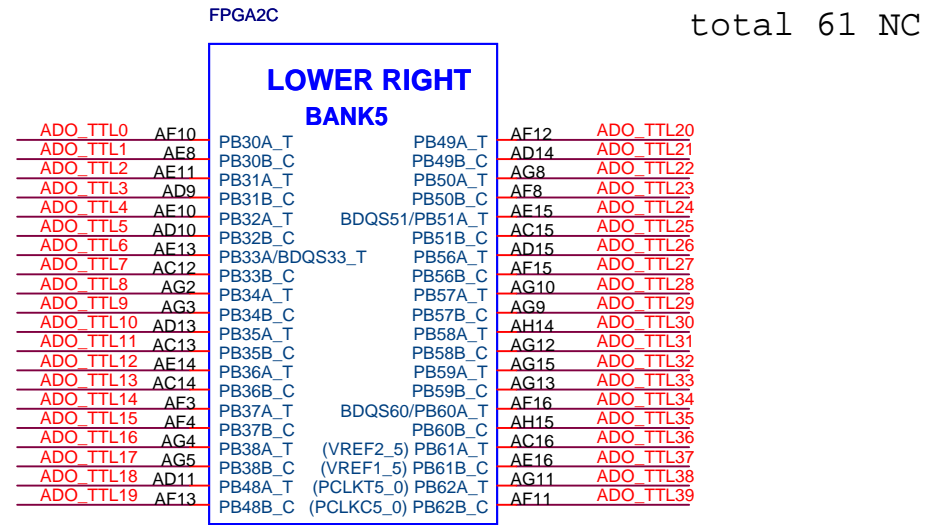
F2_TO_F1_7	100R	R135	F2_TO_F1B_7
F2_TO_F1_8	100R	R139	F2_TO_F1B_8
F2_TO_F1_9	100R	R143	F2_TO_F1B_9
F2_TO_F1_10	100R	R147	F2_TO_F1B_10
F2_TO_F1_11	100R	R151	F2_TO_F1B_11
F2_TO_F1_12	100R	R155	F2_TO_F1B_12
F2_TO_F1_13	100R	R159	F2_TO_F1B_13
F2_TO_F1_14	100R	R162	F2_TO_F1B_14

FPGA1A



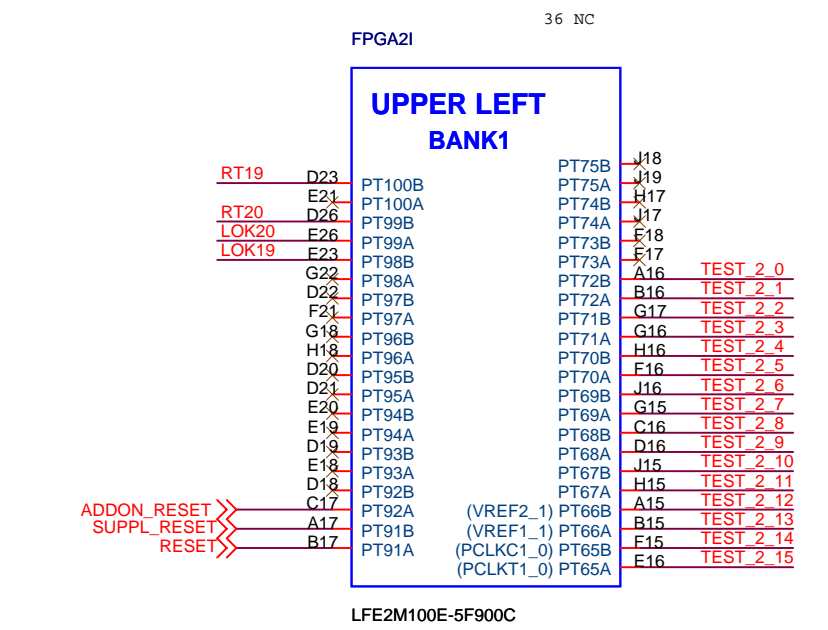
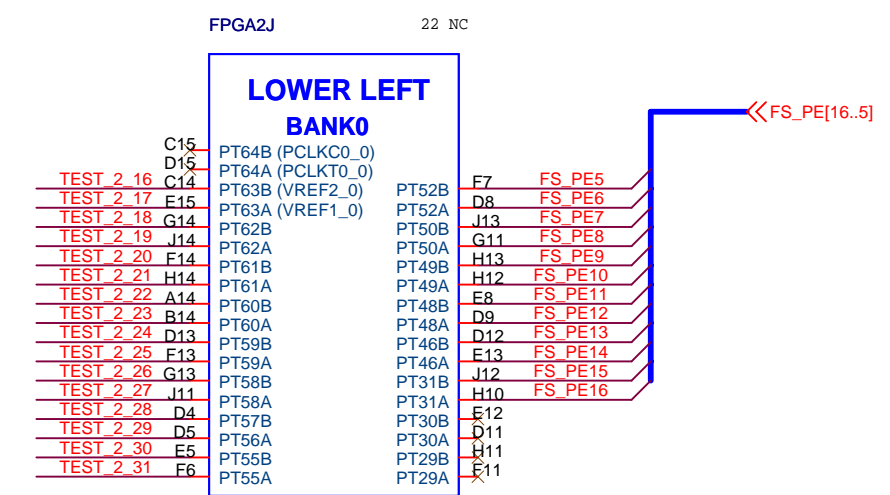
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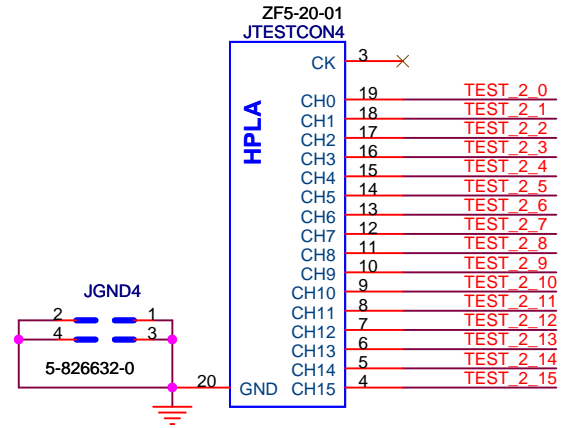
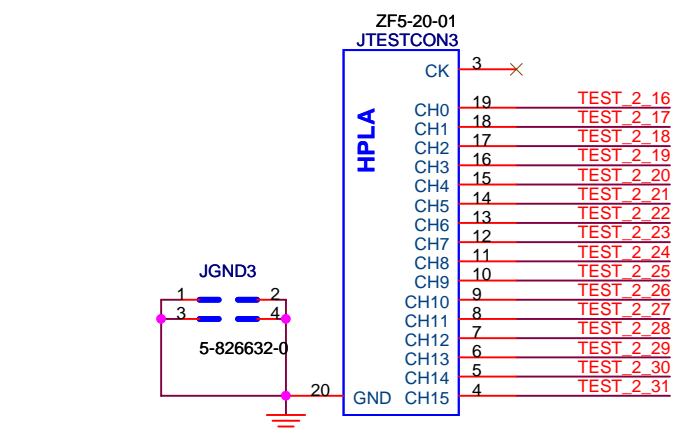
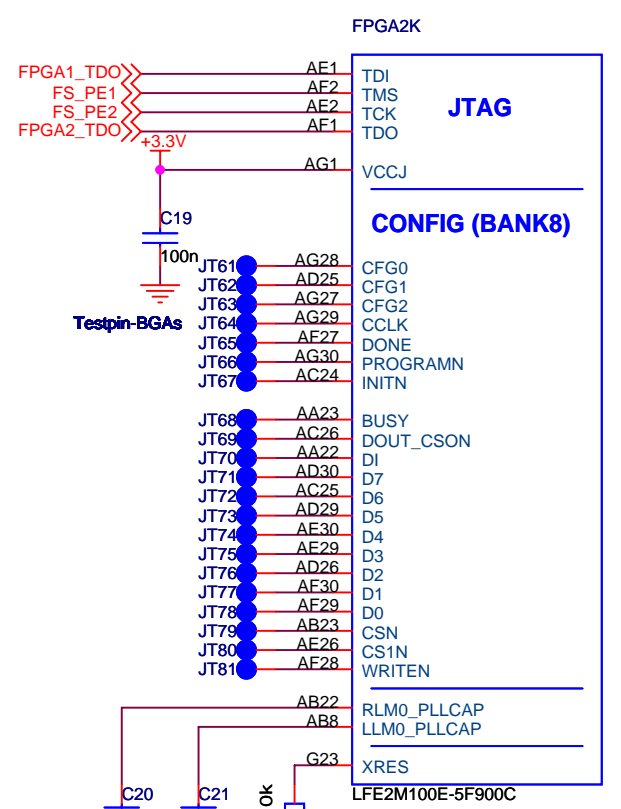


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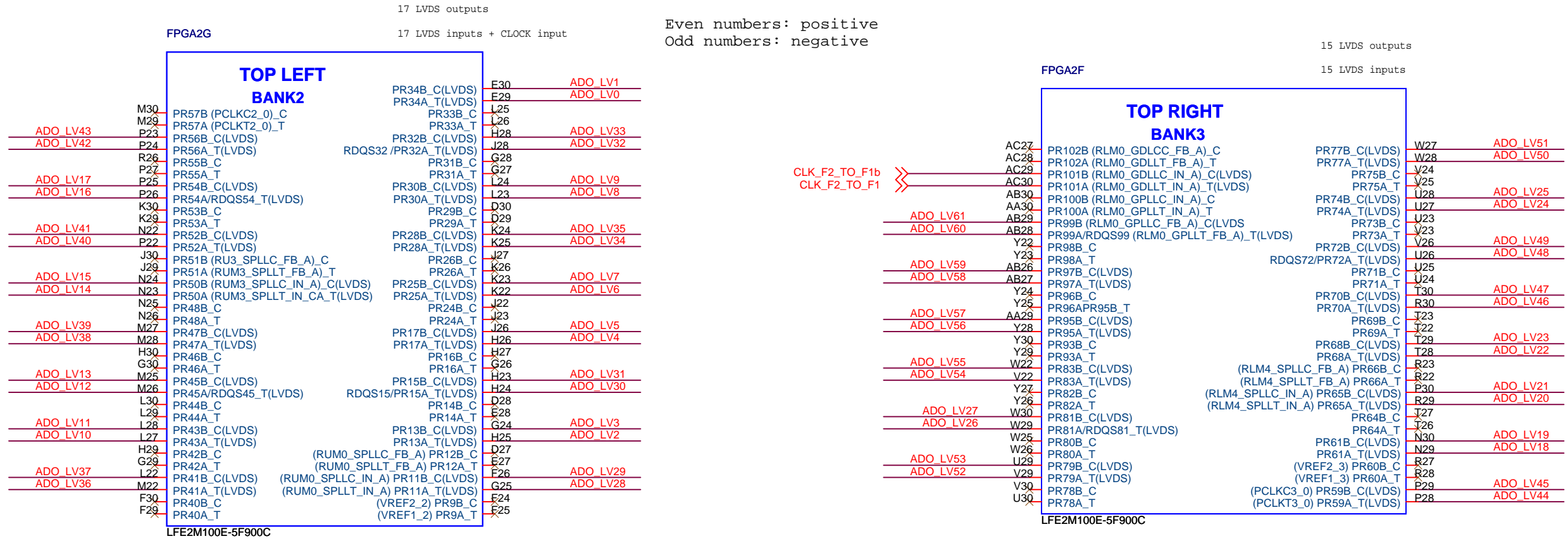
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LFE2M100E-5F900C



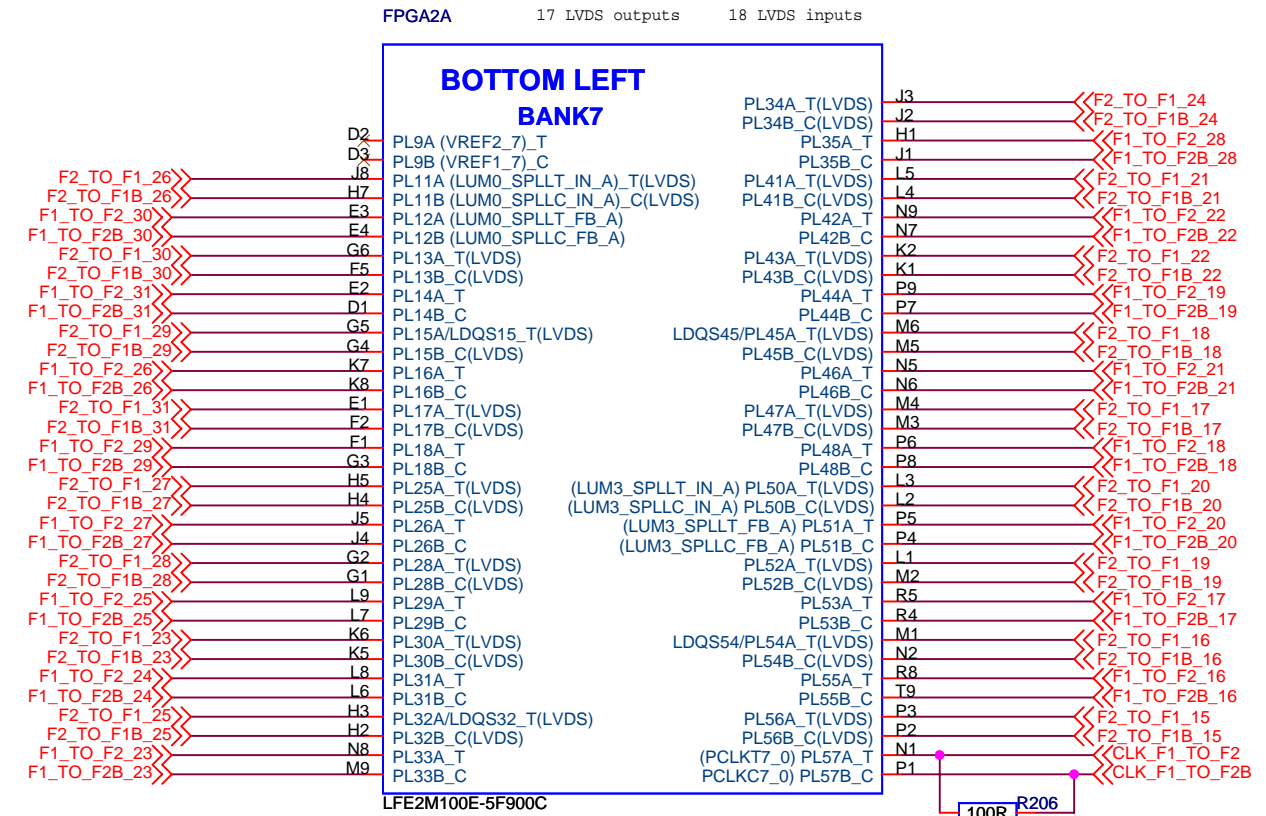
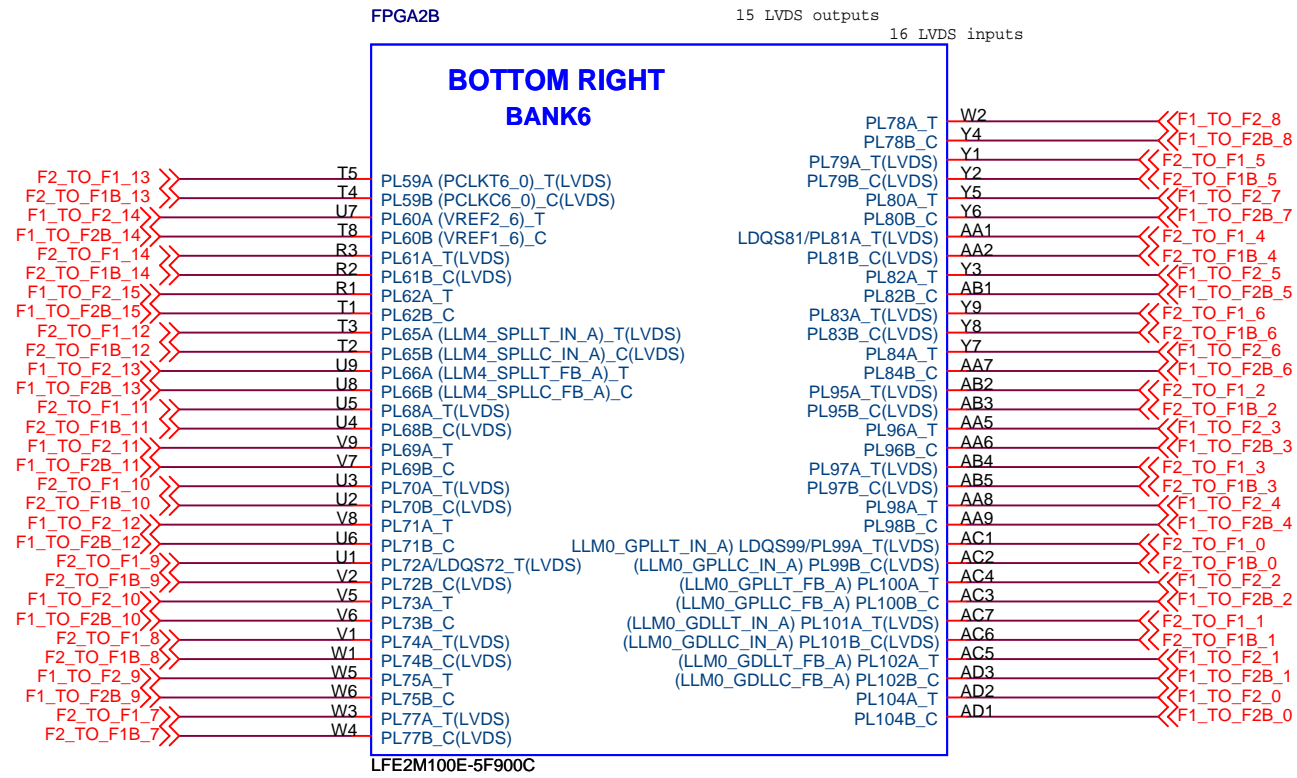
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ADO LV0	100R	R175	ADO LV1	ADO LV28	100R	R176	ADO LV29
ADO LV2	100R	R179	ADO LV3	ADO LV30	100R	R180	ADO LV31
ADO LV4	100R	R183	ADO LV5	ADO LV32	100R	R184	ADO LV33
ADO LV6	100R	R187	ADO LV7	ADO LV34	100R	R188	ADO LV35
ADO LV8	100R	R191	ADO LV9	ADO LV36	100R	R192	ADO LV37
ADO LV10	100R	R195	ADO LV11	ADO LV38	100R	R196	ADO LV39
ADO LV12	100R	R199	ADO LV13	ADO LV40	100R	R200	ADO LV41
ADO LV14	100R	R202	ADO LV15	ADO LV42	100R	R203	ADO LV43
ADO LV16	100R	R177	ADO LV17	ADO LV44	100R	R178	ADO LV45
ADO LV18	100R	R181	ADO LV19	ADO LV46	100R	R182	ADO LV47
ADO LV20	100R	R185	ADO LV21	ADO LV48	100R	R186	ADO LV49
ADO LV22	100R	R189	ADO LV23	ADO LV50	100R	R189	ADO LV25
ADO LV24	100R	R193	ADO LV25	ADO LV52	100R	R194	ADO LV53
ADO LV26	100R	R197	ADO LV27	ADO LV54	100R	R198	ADO LV55
				ADO LV56	100R	R201	ADO LV57
				ADO LV58	100R	R204	ADO LV59
				ADO LV60	100R	R205	ADO LV61

Soldering LVDS termination resistors depends on application (LVDS lines direction)

ADO_LV[61..0] >>

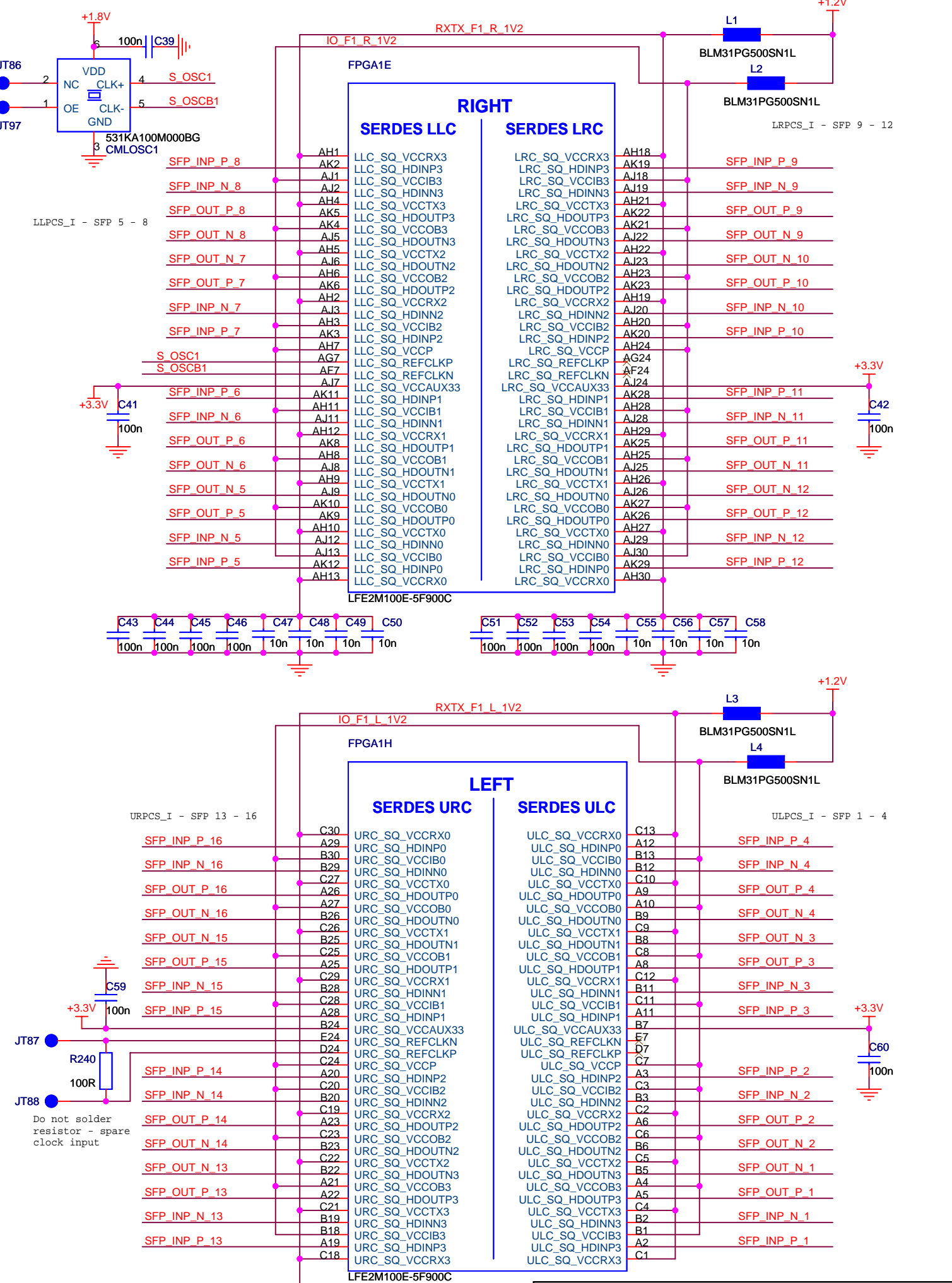
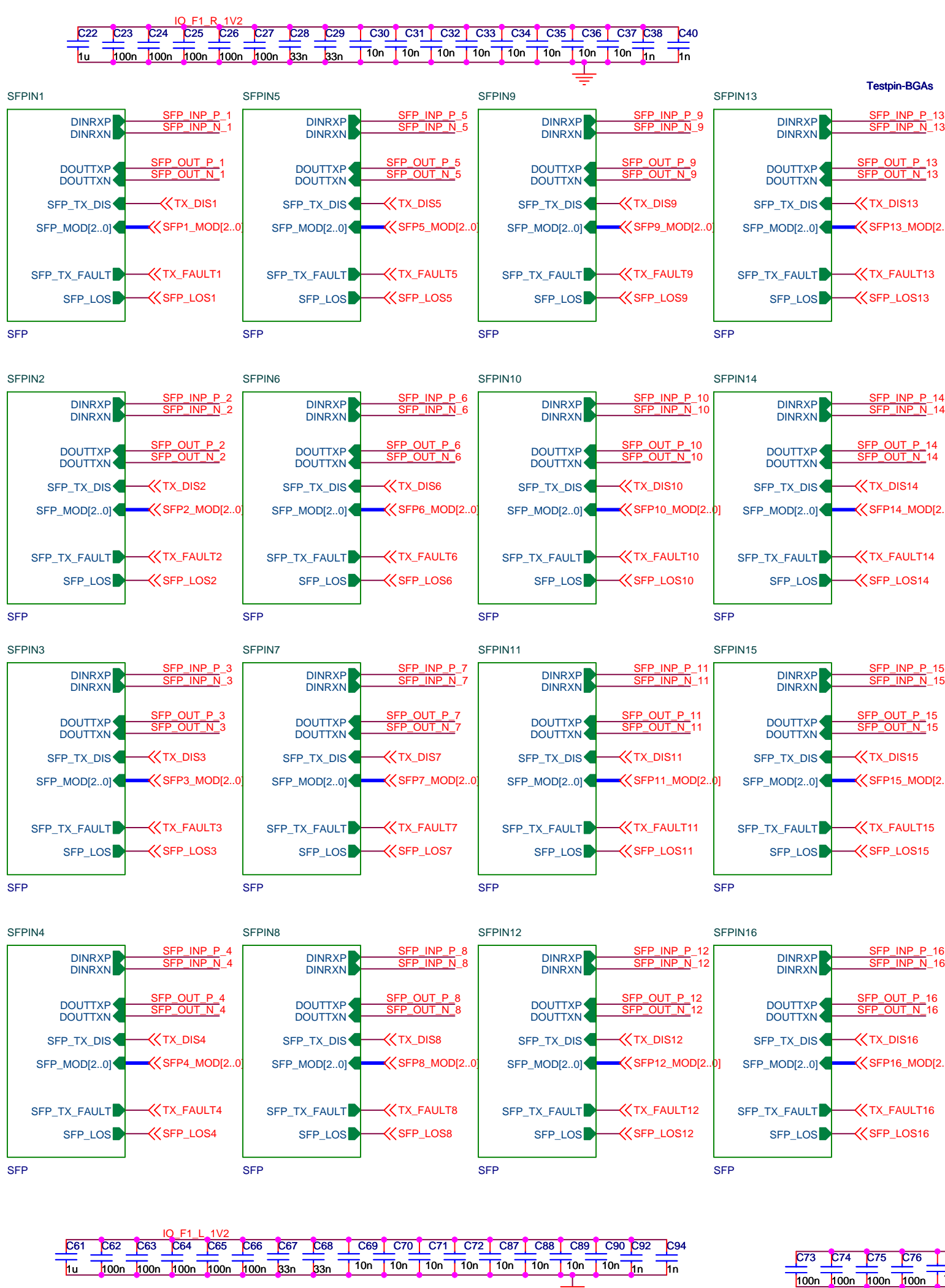


F1 TO F2B 15	100R	R207	F1 TO F2 15
F1 TO F2B 14	100R	R211	F1 TO F2 14
F1 TO F2B 13	100R	R215	F1 TO F2 13
F1 TO F2B 12	100R	R219	F1 TO F2 12
F1 TO F2B 11	100R	R223	F1 TO F2 11
F1 TO F2B 10	100R	R227	F1 TO F2 10
F1 TO F2B 9	100R	R231	F1 TO F2 9
F1 TO F2B 8	100R	R235	F1 TO F2 8

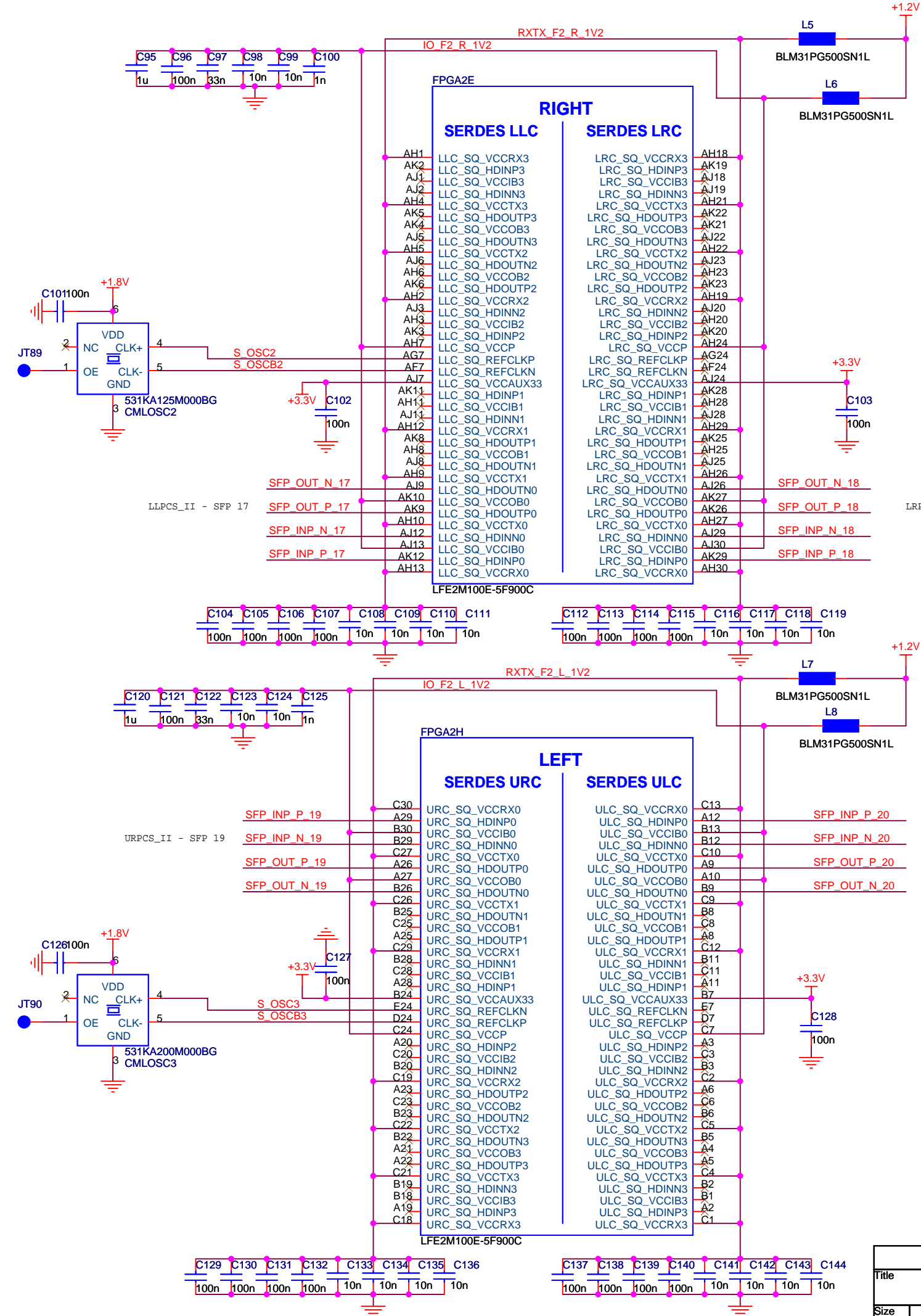
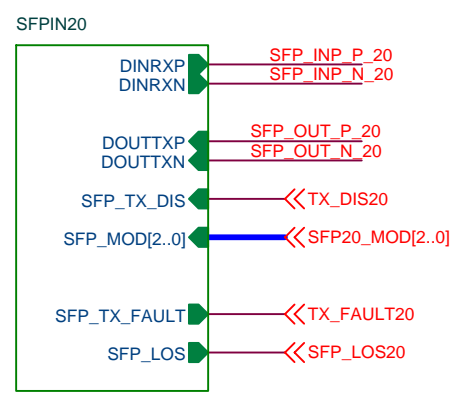
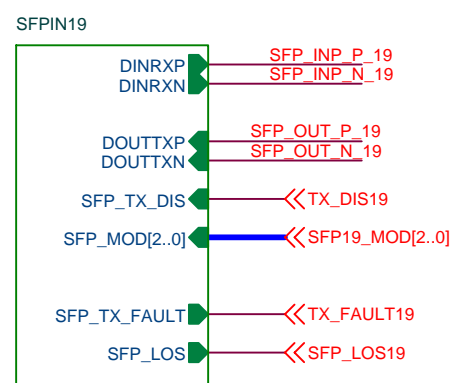
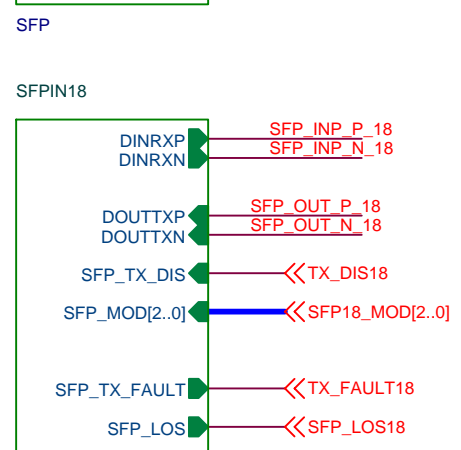
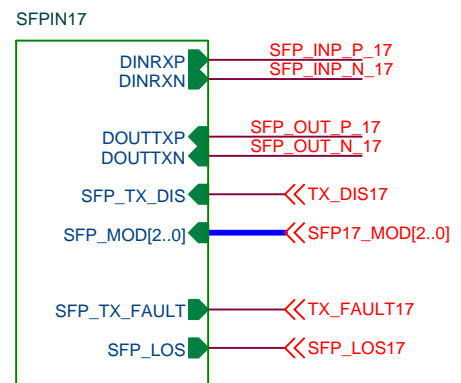
F1 TO F2B 7	100R	R208	F1 TO F2 7
F1 TO F2B 6	100R	R212	F1 TO F2 6
F1 TO F2B 5	100R	R216	F1 TO F2 5
F1 TO F2B 4	100R	R220	F1 TO F2 4
F1 TO F2B 3	100R	R224	F1 TO F2 3
F1 TO F2B 2	100R	R228	F1 TO F2 2
F1 TO F2B 1	100R	R232	F1 TO F2 1
F1 TO F2B 0	100R	R236	F1 TO F2 0

F1 TO F2B 31	100R	R209	F1 TO F2 31
F1 TO F2B 30	100R	R213	F1 TO F2 30
F1 TO F2B 29	100R	R217	F1 TO F2 29
F1 TO F2B 28	100R	R221	F1 TO F2 28
F1 TO F2B 27	100R	R225	F1 TO F2 27
F1 TO F2B 26	100R	R229	F1 TO F2 26
F1 TO F2B 25	100R	R233	F1 TO F2 25
F1 TO F2B 24	100R	R237	F1 TO F2 24

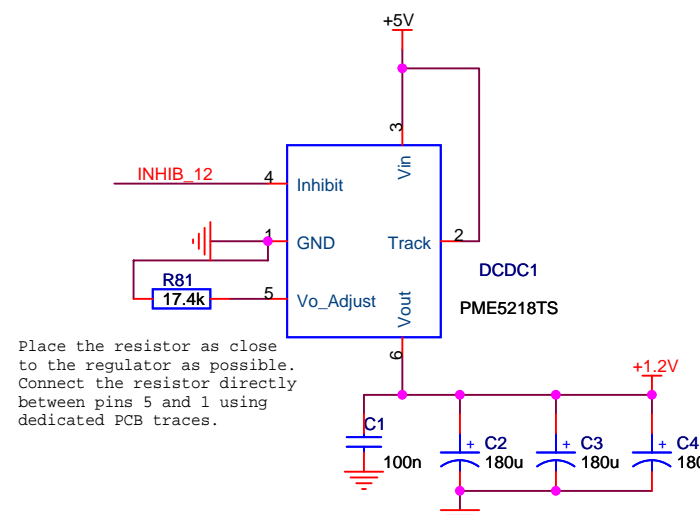
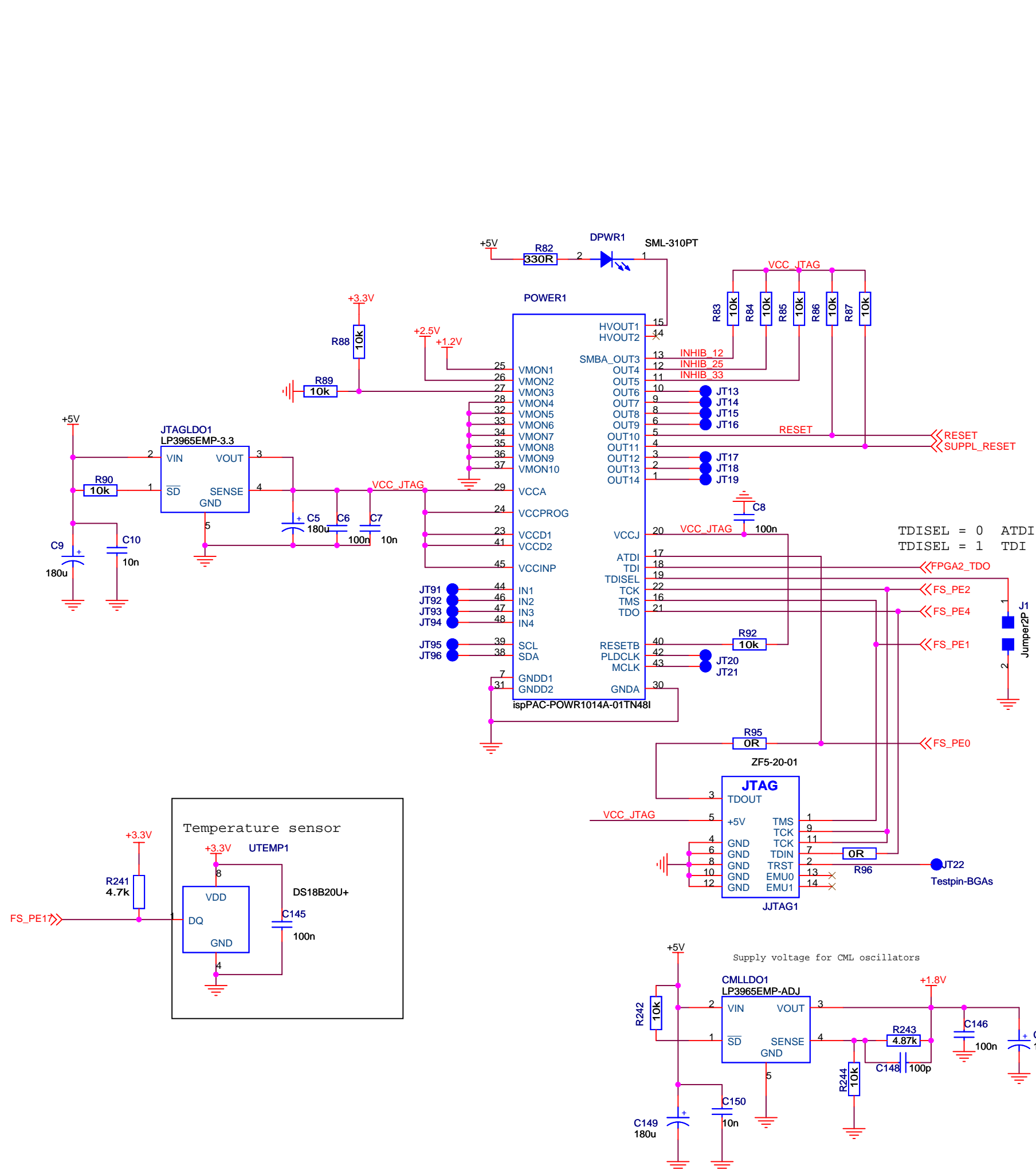
F1 TO F2B 23	100R	R210	F1 TO F2 23
F1 TO F2B 22	100R	R214	F1 TO F2 22
F1 TO F2B 21	100R	R218	F1 TO F2 21
F1 TO F2B 20	100R	R222	F1 TO F2 20
F1 TO F2B 19	100R	R226	F1 TO F2 19
F1 TO F2B 18	100R	R230	F1 TO F2 18
F1 TO F2B 17	100R	R234	F1 TO F2 17
F1 TO F2B 16	100R	R238	F1 TO F2 16



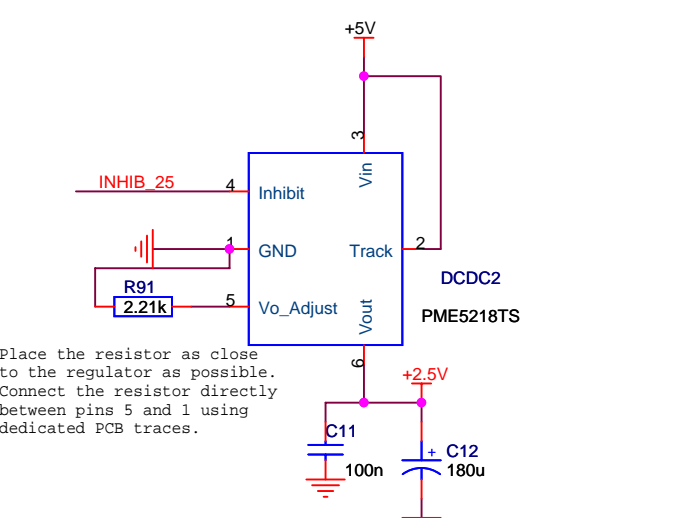
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Size	Document Number				Rev
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Date:	Wednesday, October 01, 2008	Sheet	9	of	33



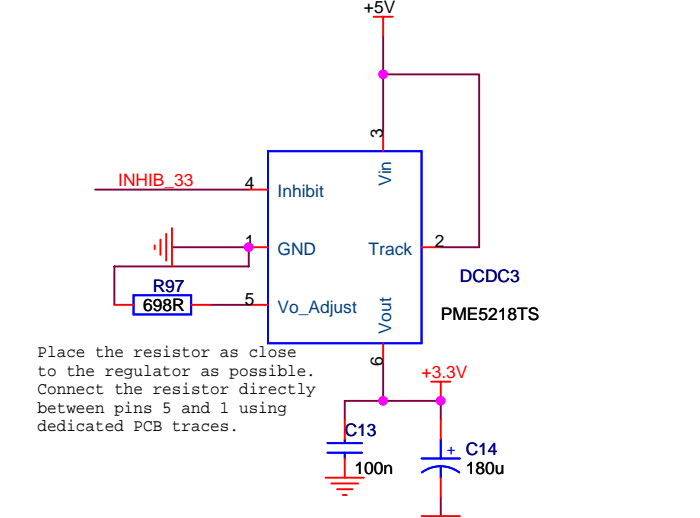
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Size	Document Number	Rev			
A3	<Doc>	<RevC>			
Date:	Wednesday, October 01, 2008	Sheet	10	of	33



Place the resistor as close to the regulator as possible. Connect the resistor directly between pins 5 and 1 using dedicated PCB traces.

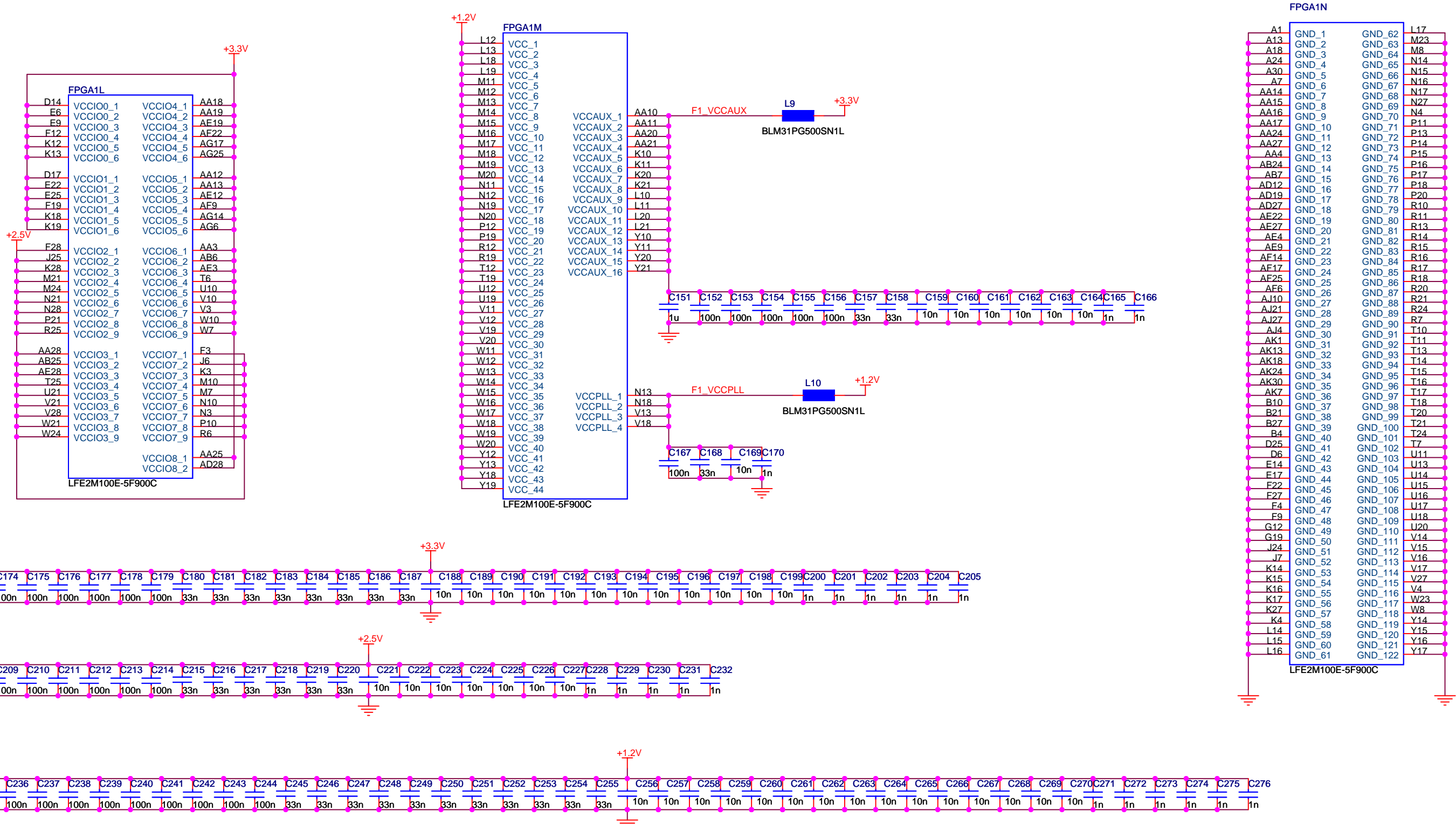


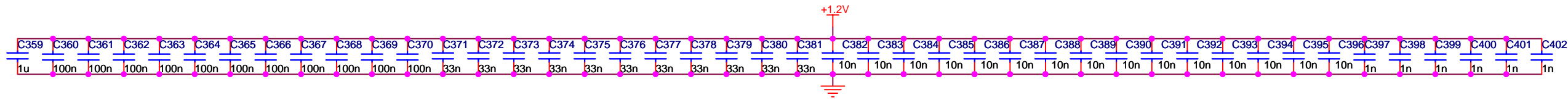
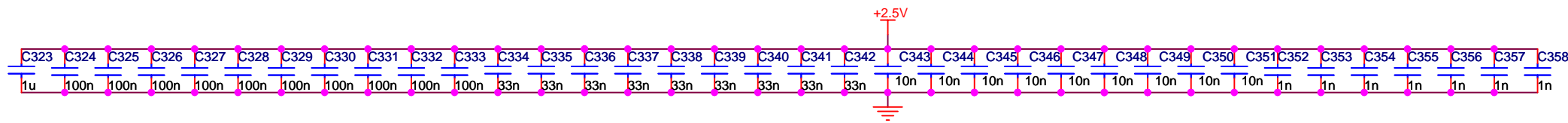
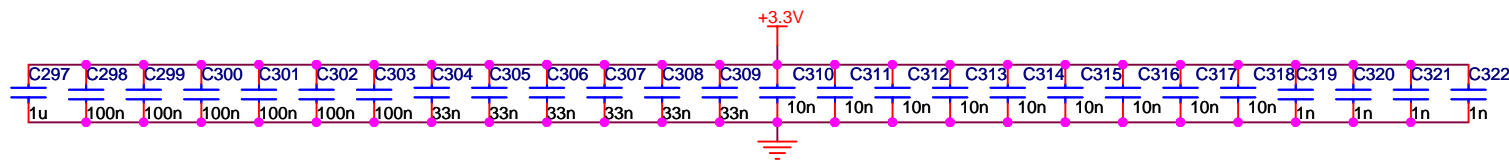
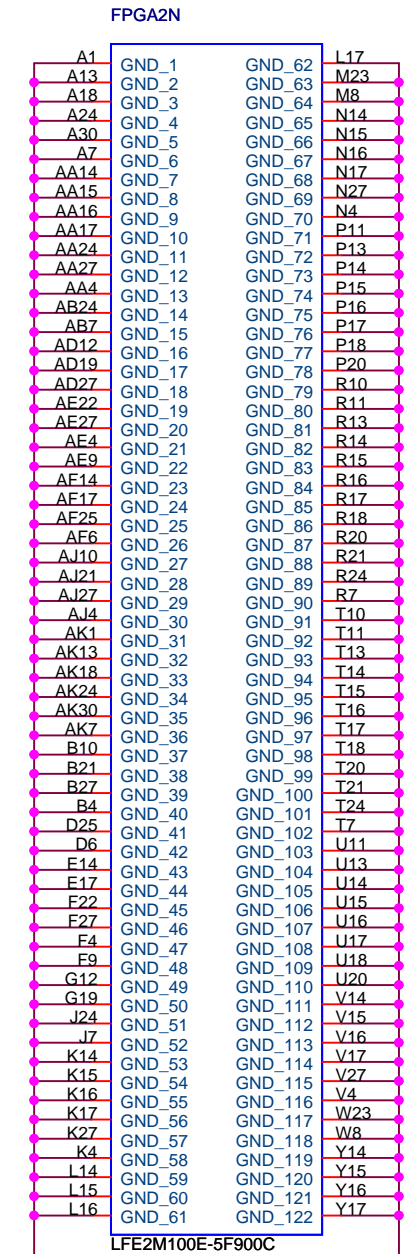
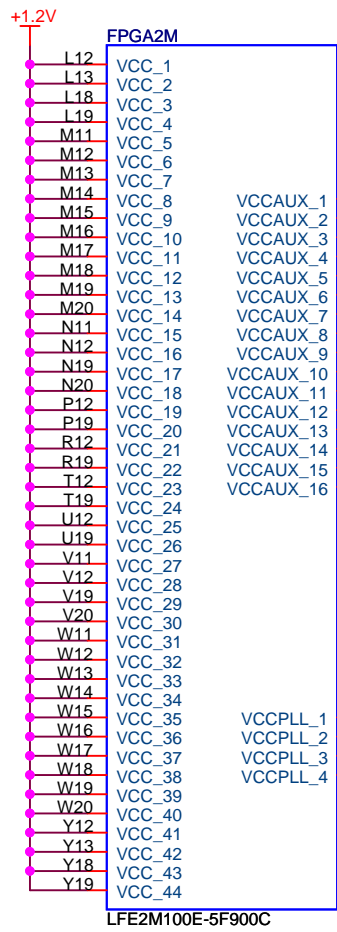
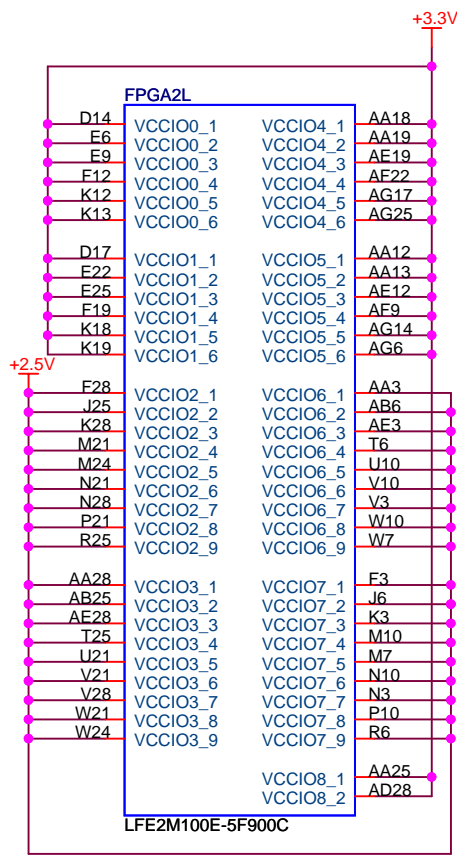
Place the resistor as close to the regulator as possible. Connect the resistor directly between pins 5 and 1 using dedicated PCB traces.

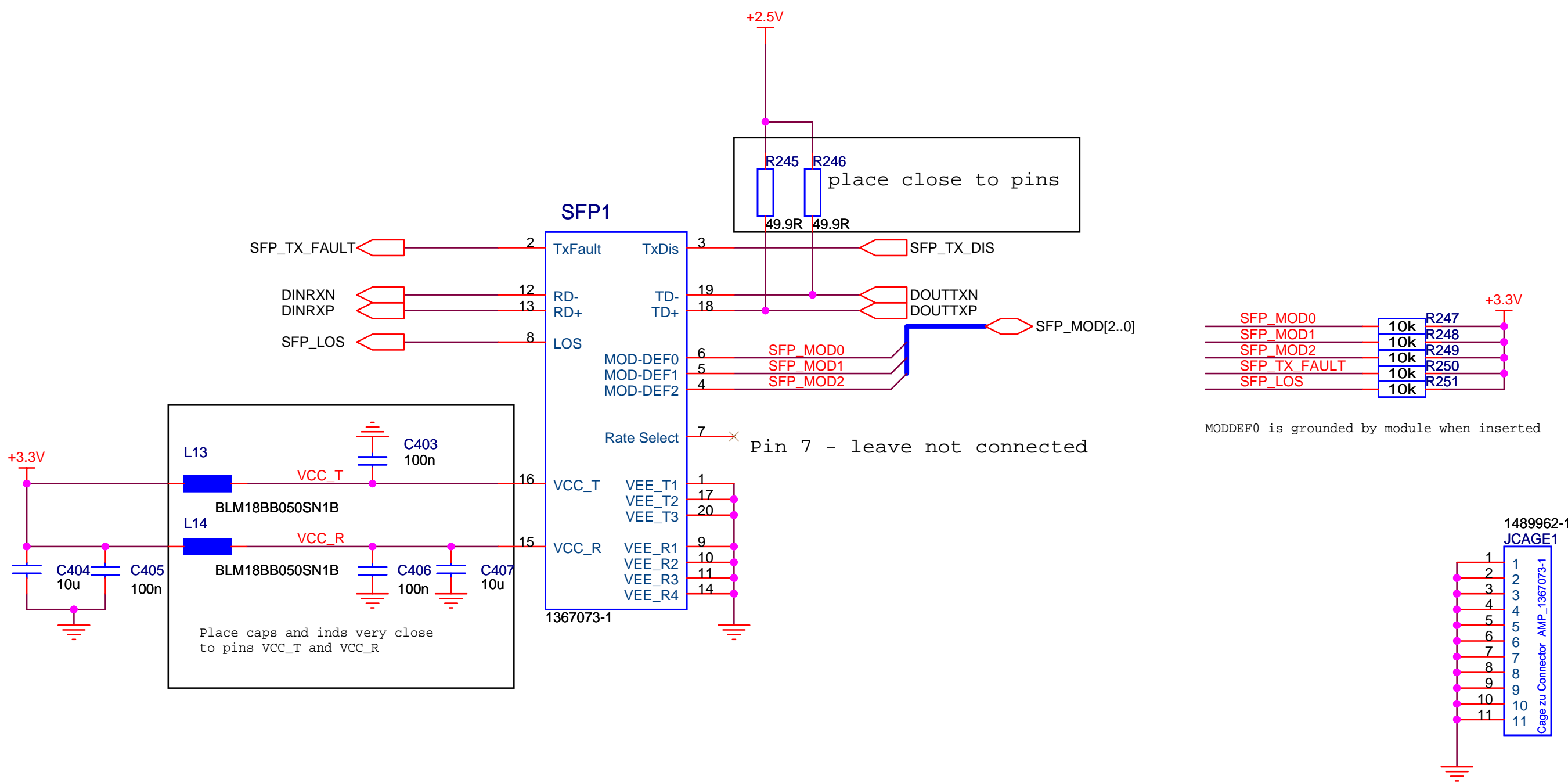


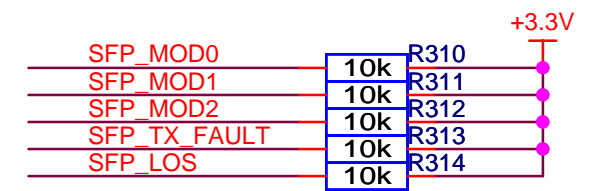
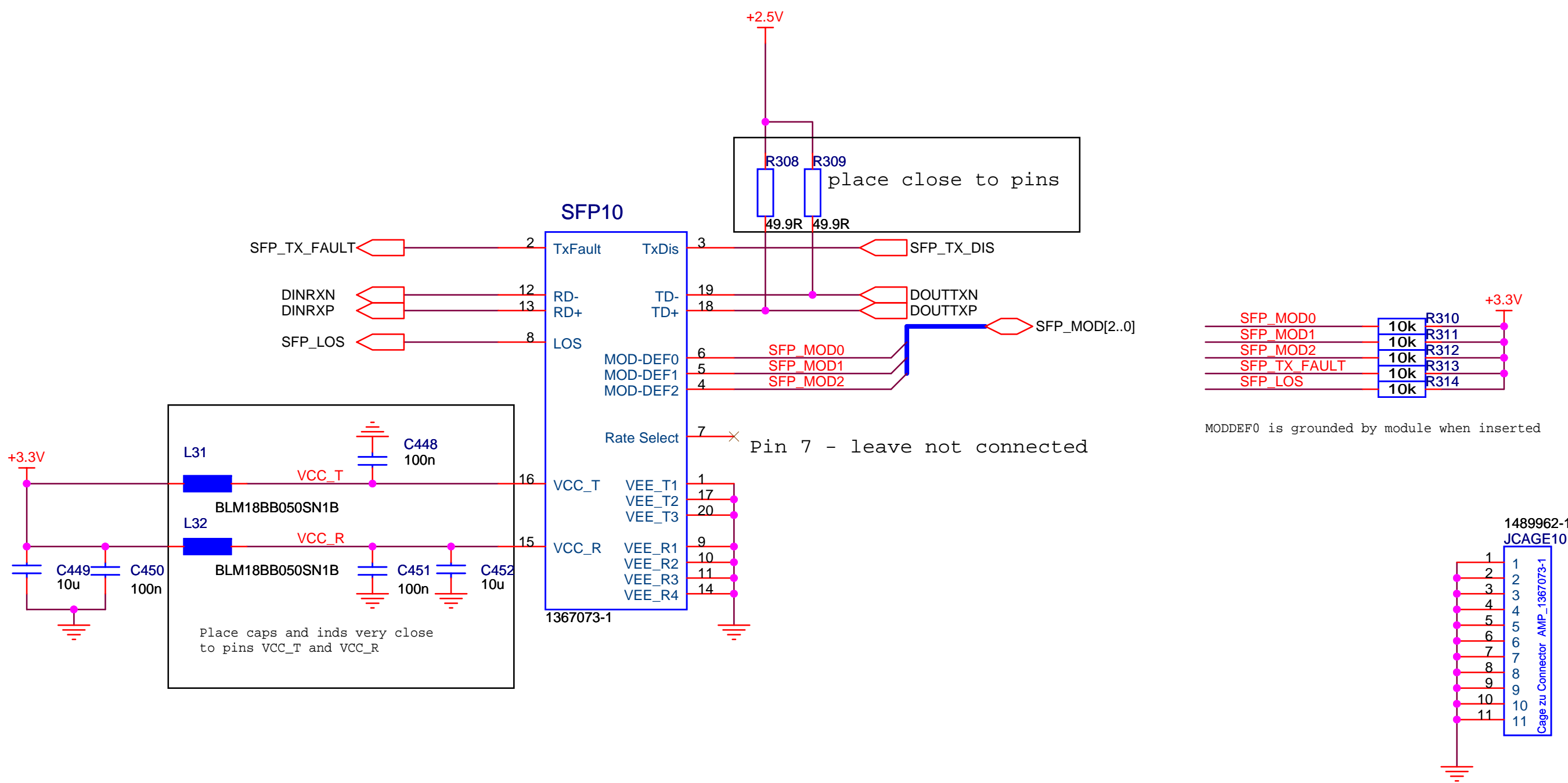
Place the resistor as close to the regulator as possible. Connect the resistor directly between pins 5 and 1 using dedicated PCB traces.

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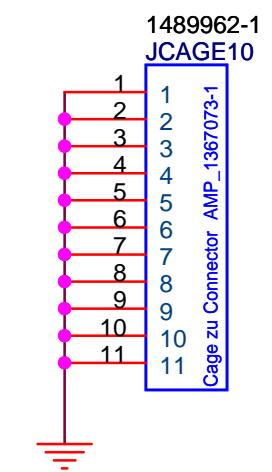




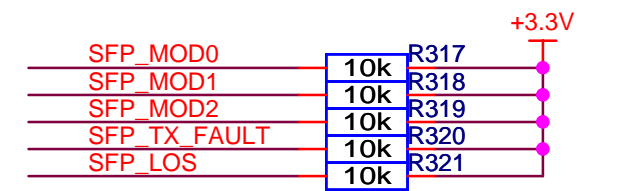
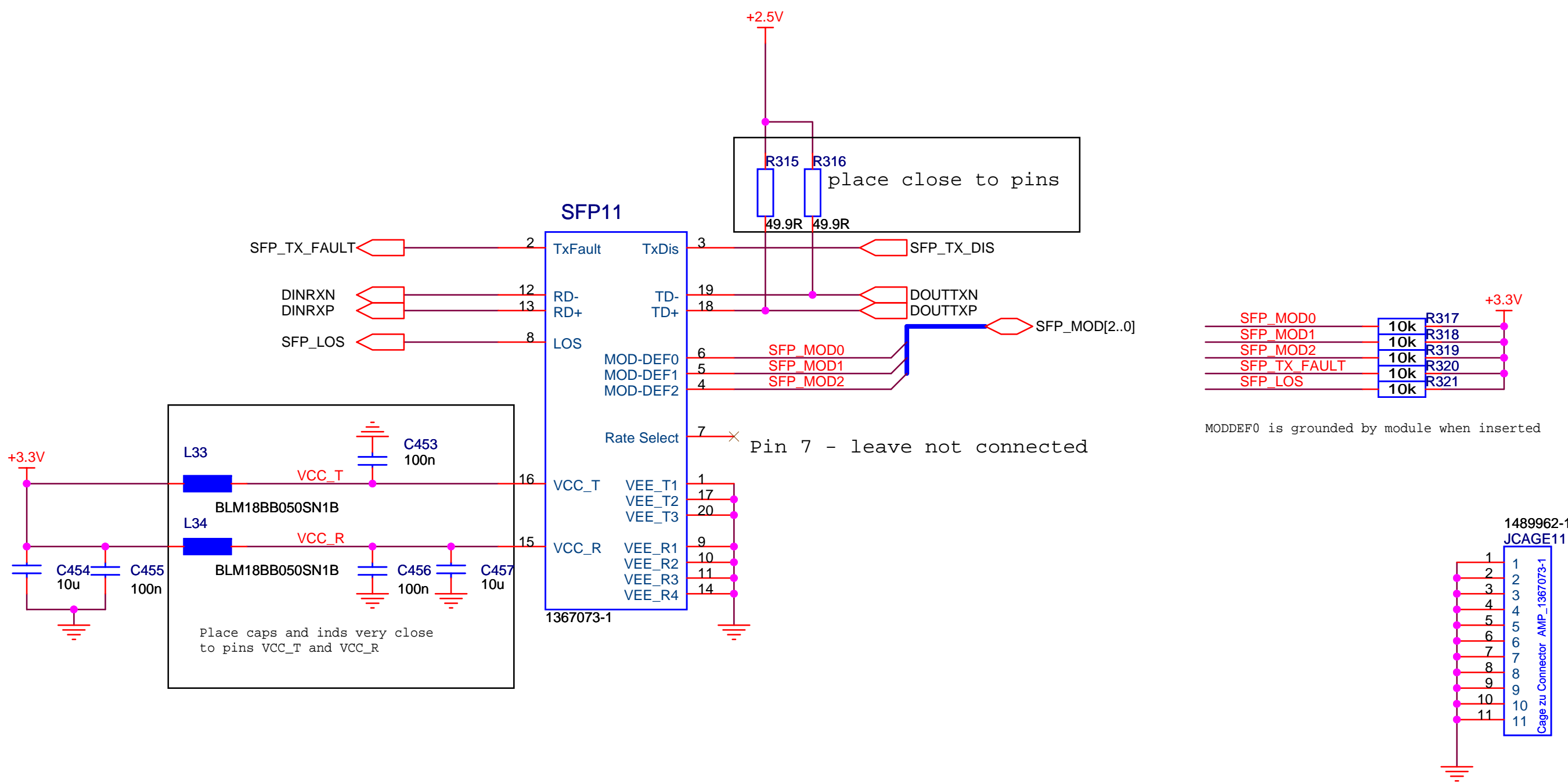




MODDEF0 is grounded by module when inserted

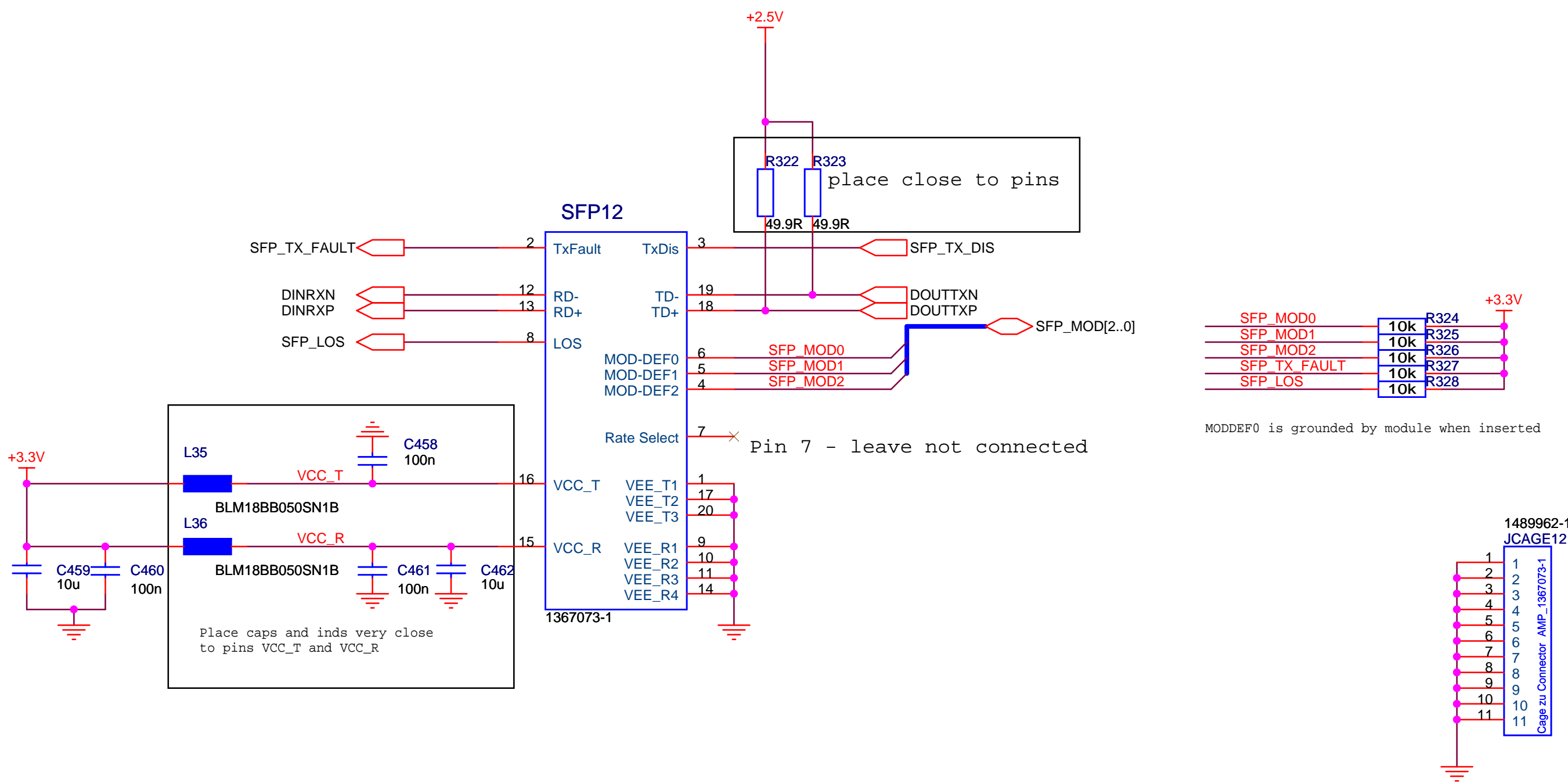


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Size	Document Number	Rev			
A4	<Doc>	<RevCo			
Date:	Monday, September 15, 2008	Sheet	15	of	33



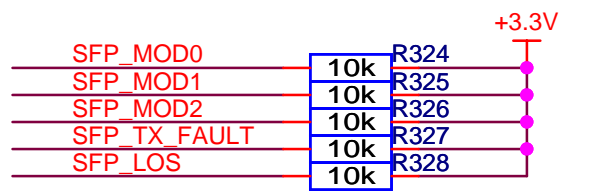
MODDEF0 is grounded by module when inserted

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Size	Document Number	Rev			
A4	<Doc>	<RevCo			
Date:	Monday, September 15, 2008	Sheet	16	of	33

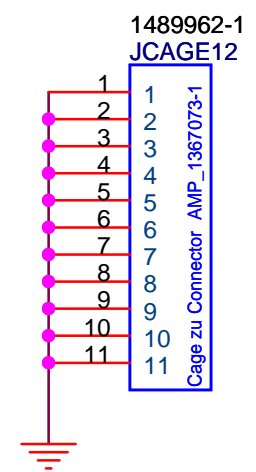


Place caps and inds very close to pins VCC_T and VCC_R

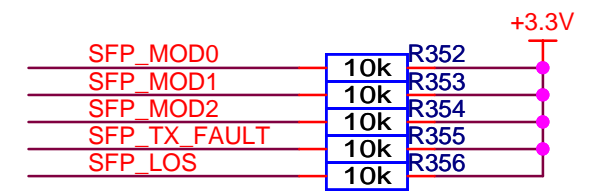
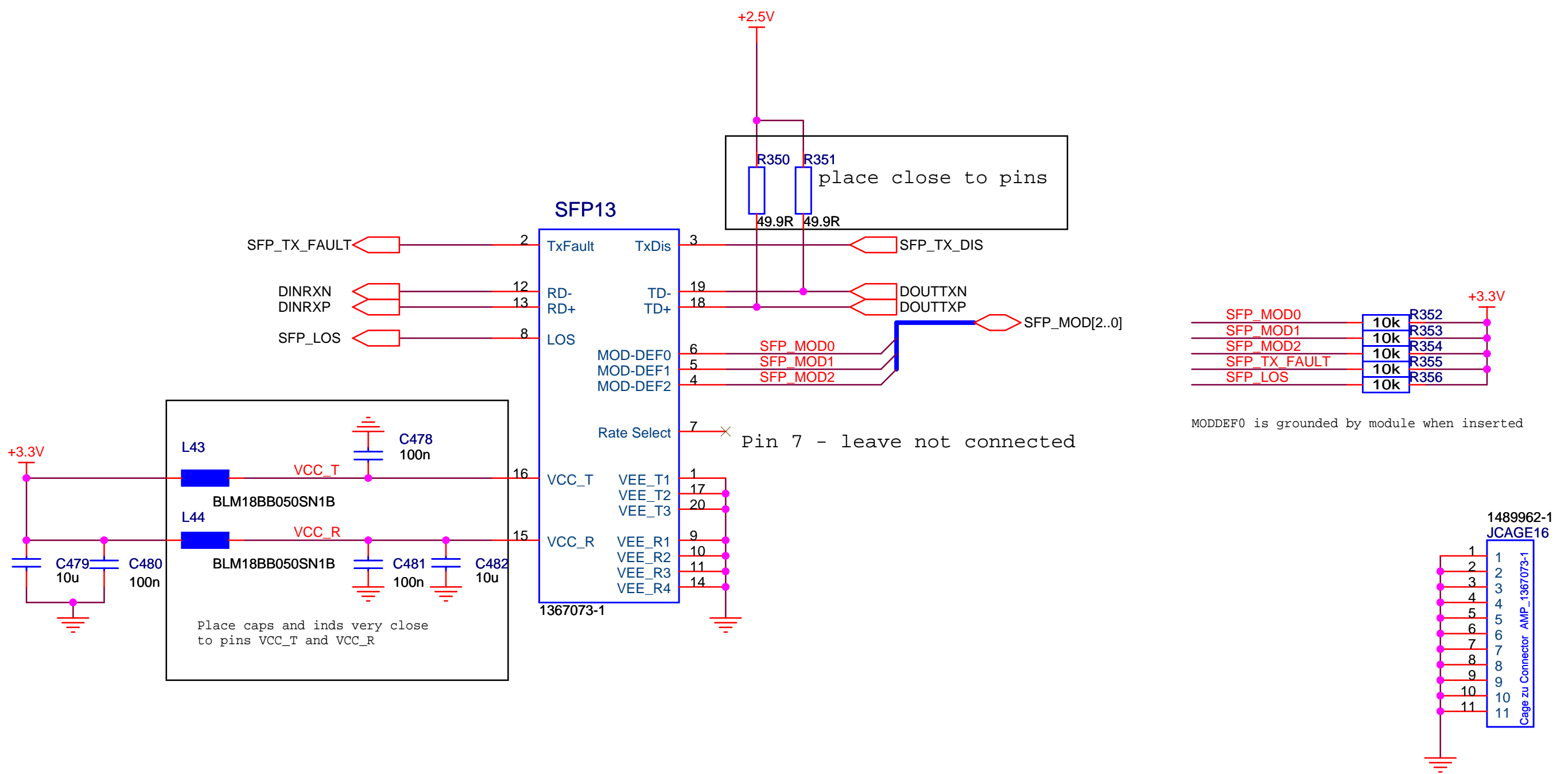
place close to pins



MODDEF0 is grounded by module when inserted

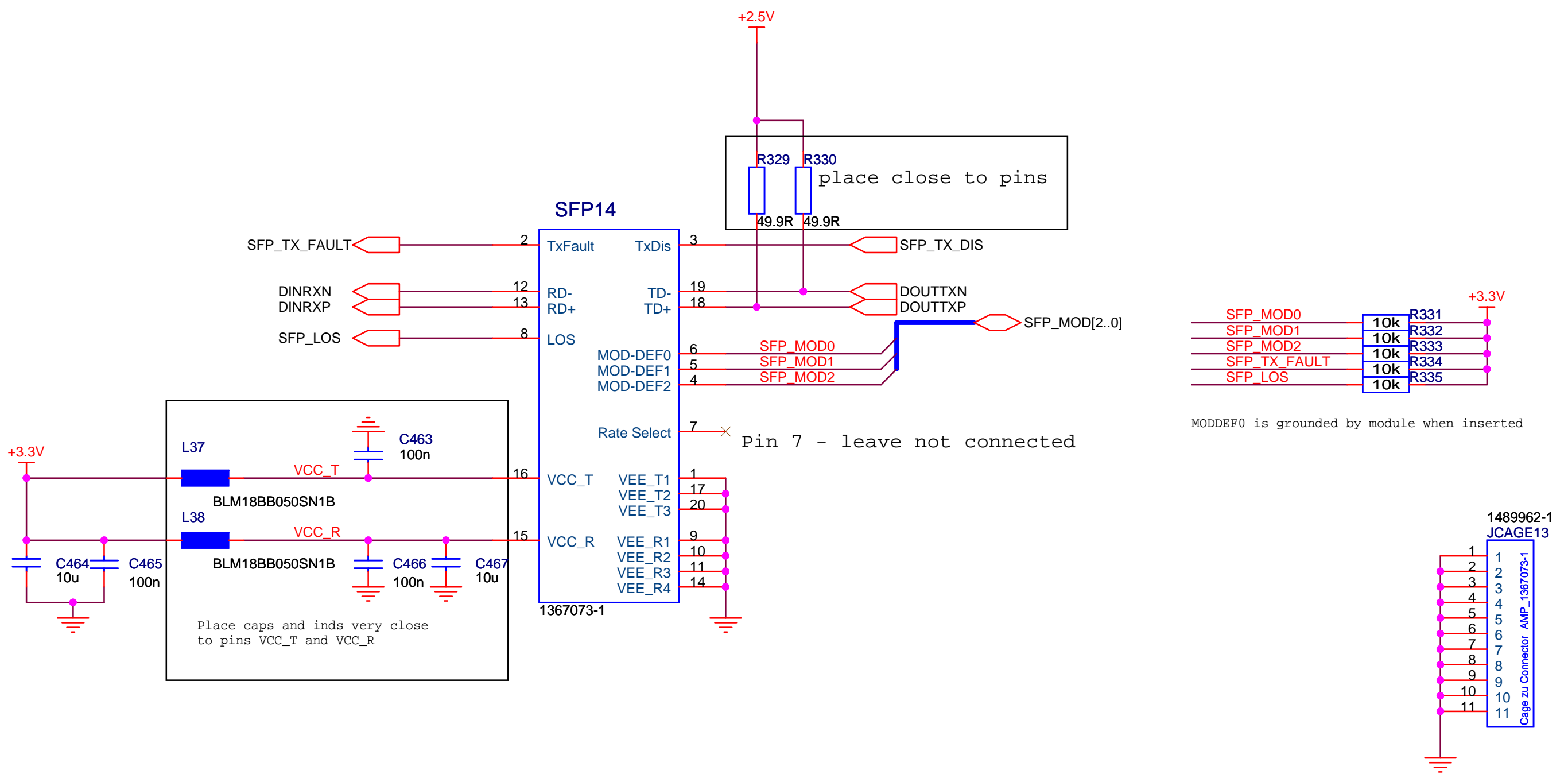


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Date:	Monday, September 15, 2008	Sheet	17	of	33

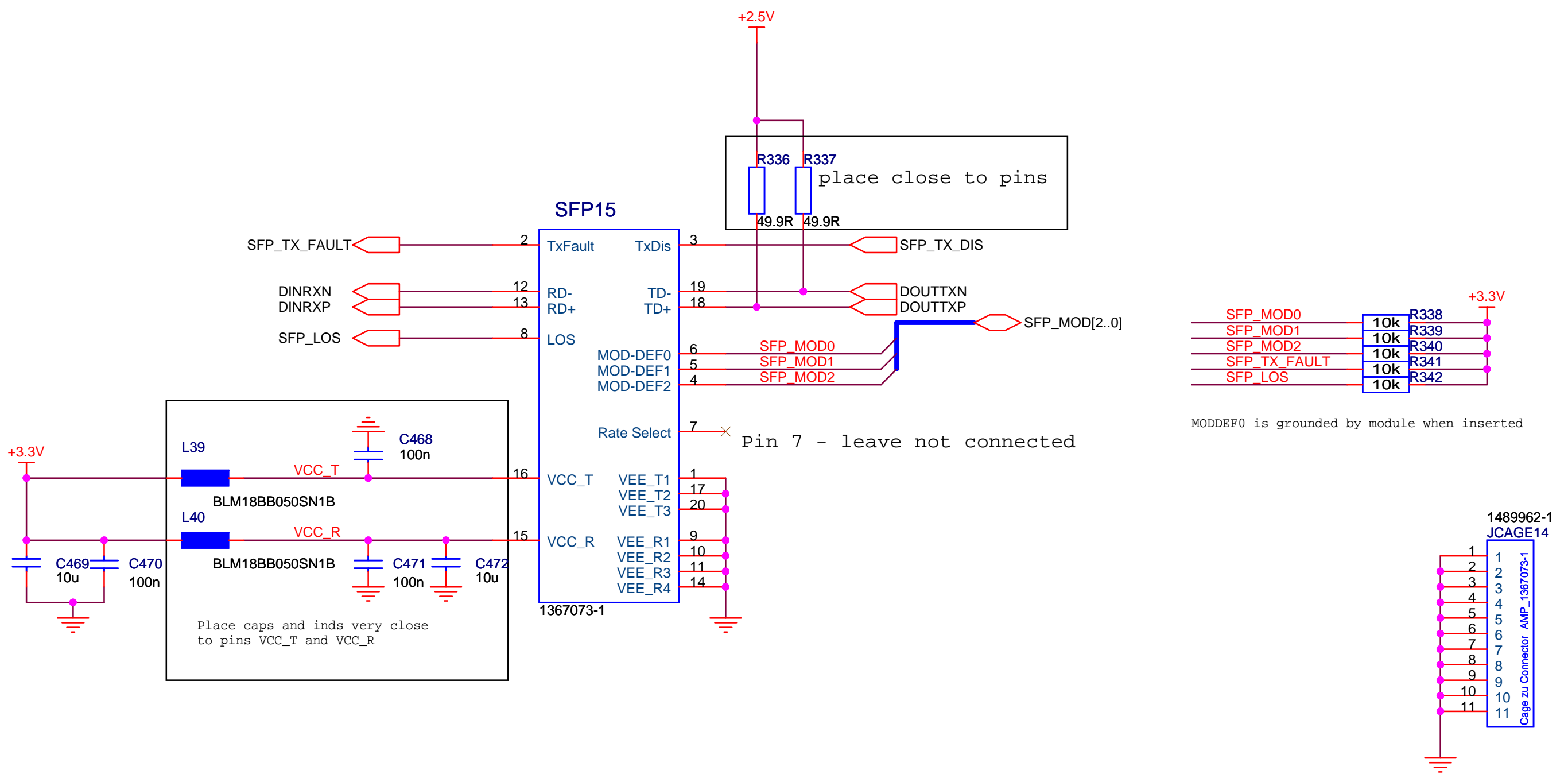


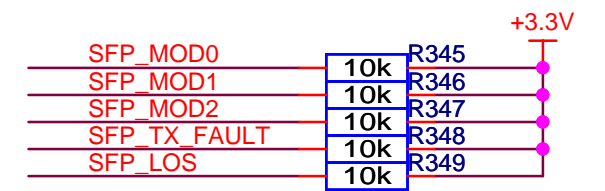
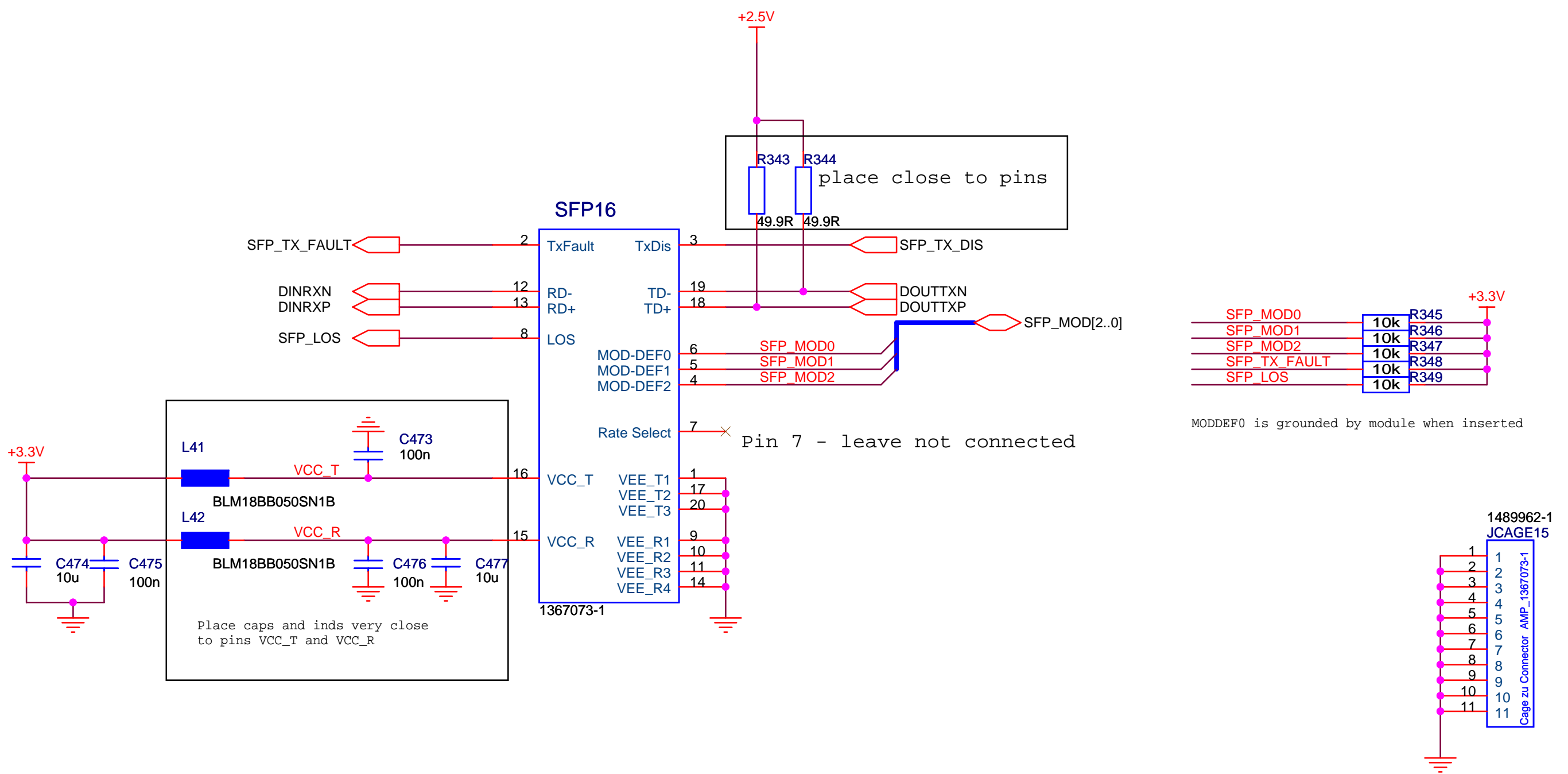
MODDEF0 is grounded by module when inserted

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Size	Document Number	Rev			
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Date:	Monday, September 15, 2008	Sheet	18	of	33



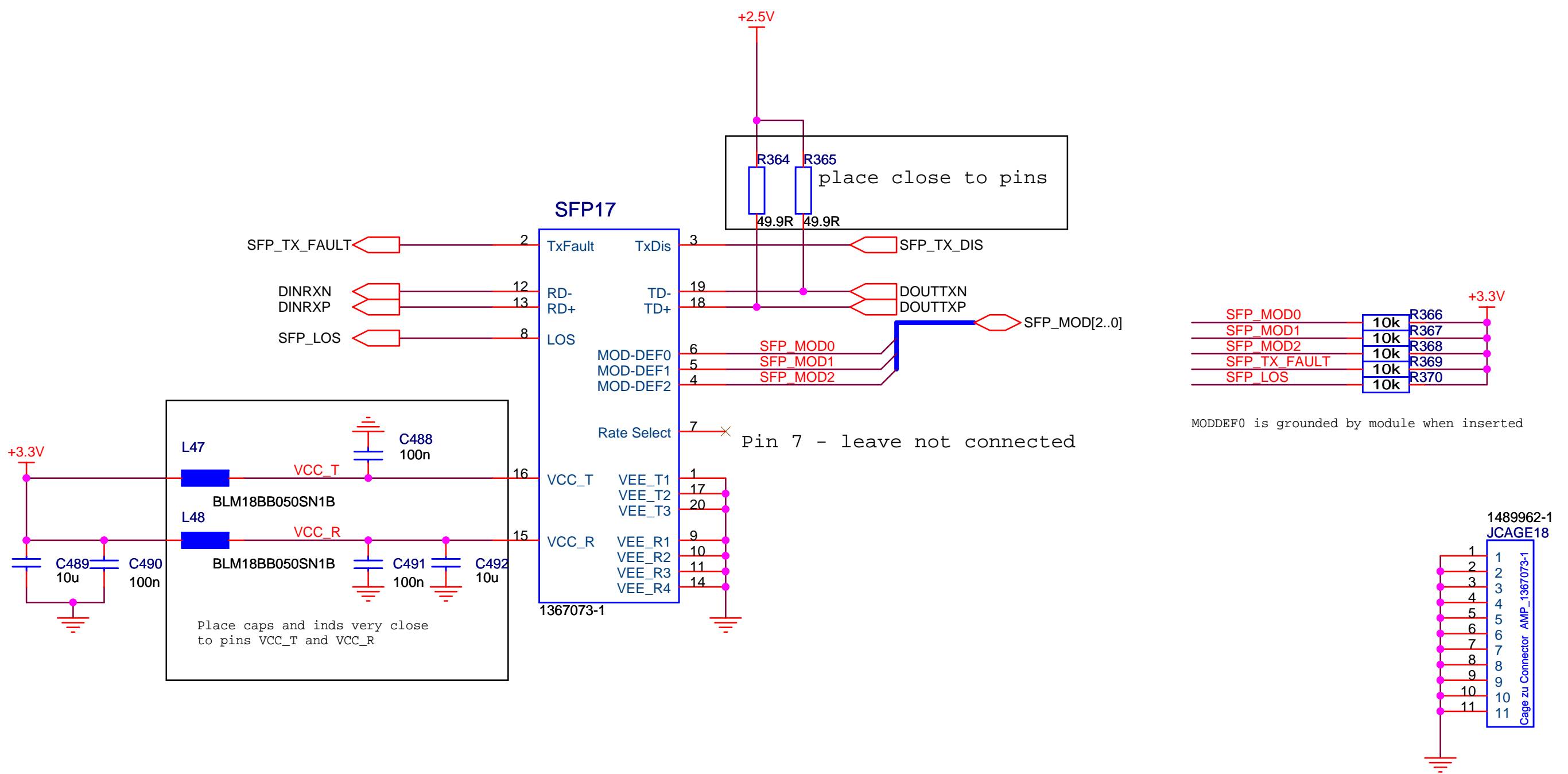
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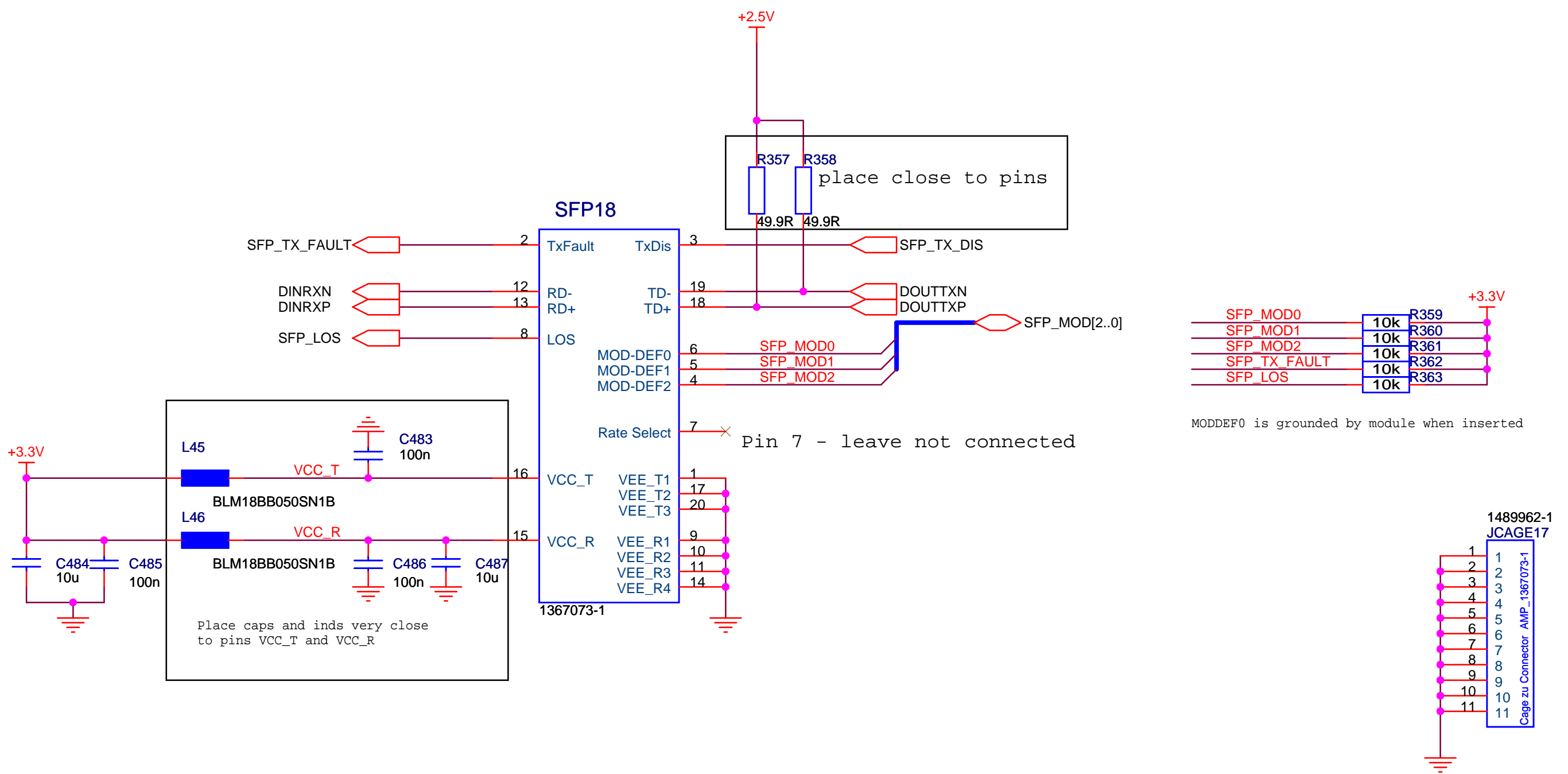


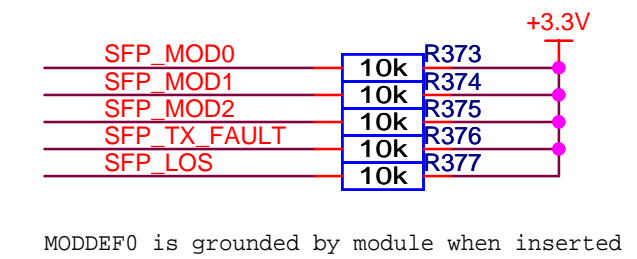
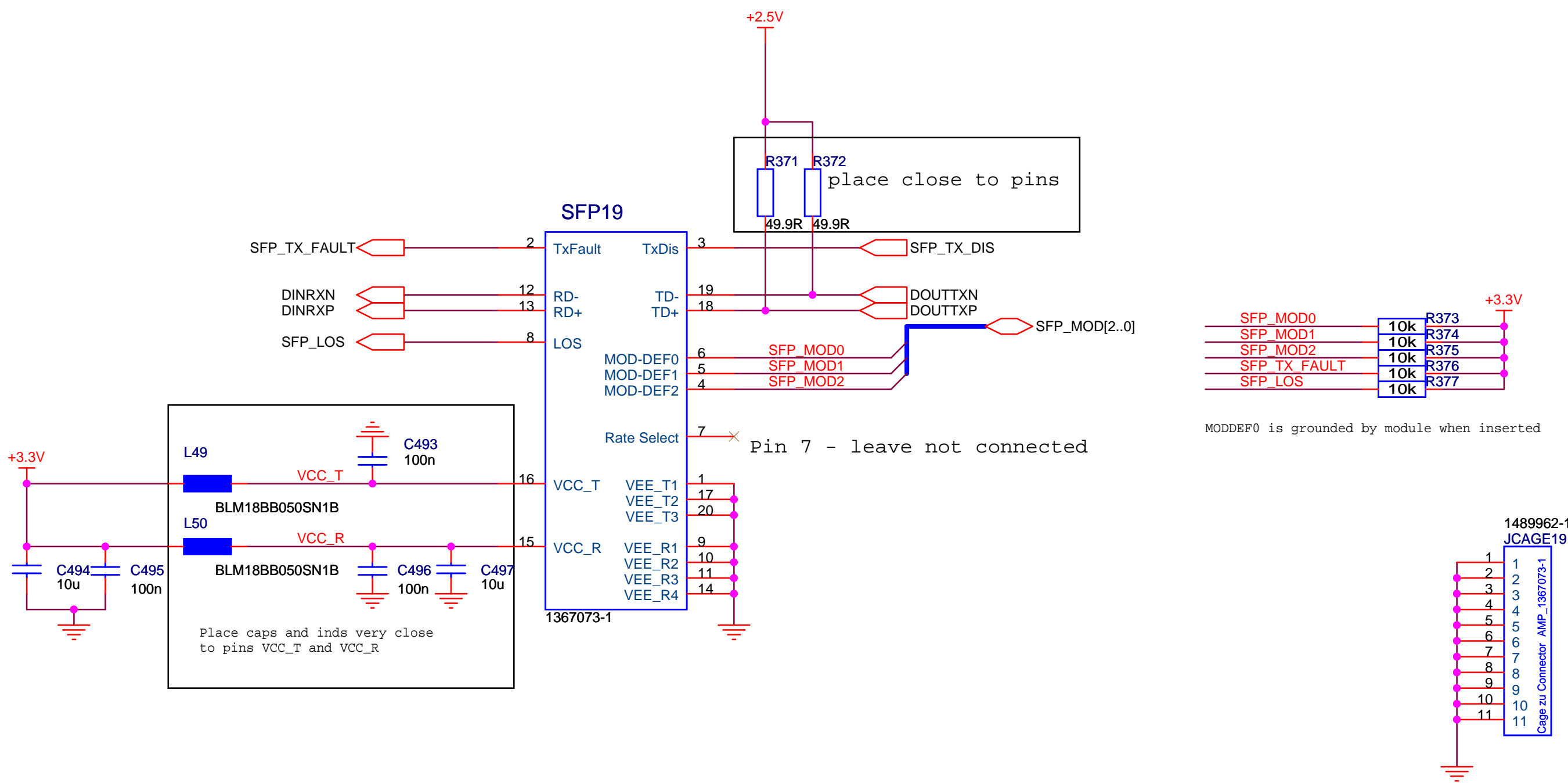
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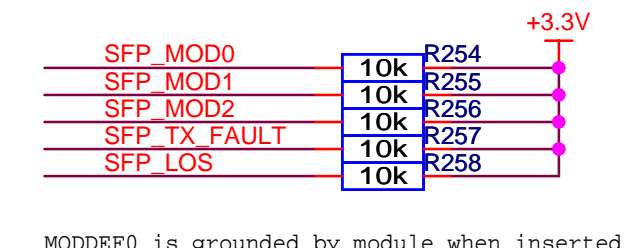
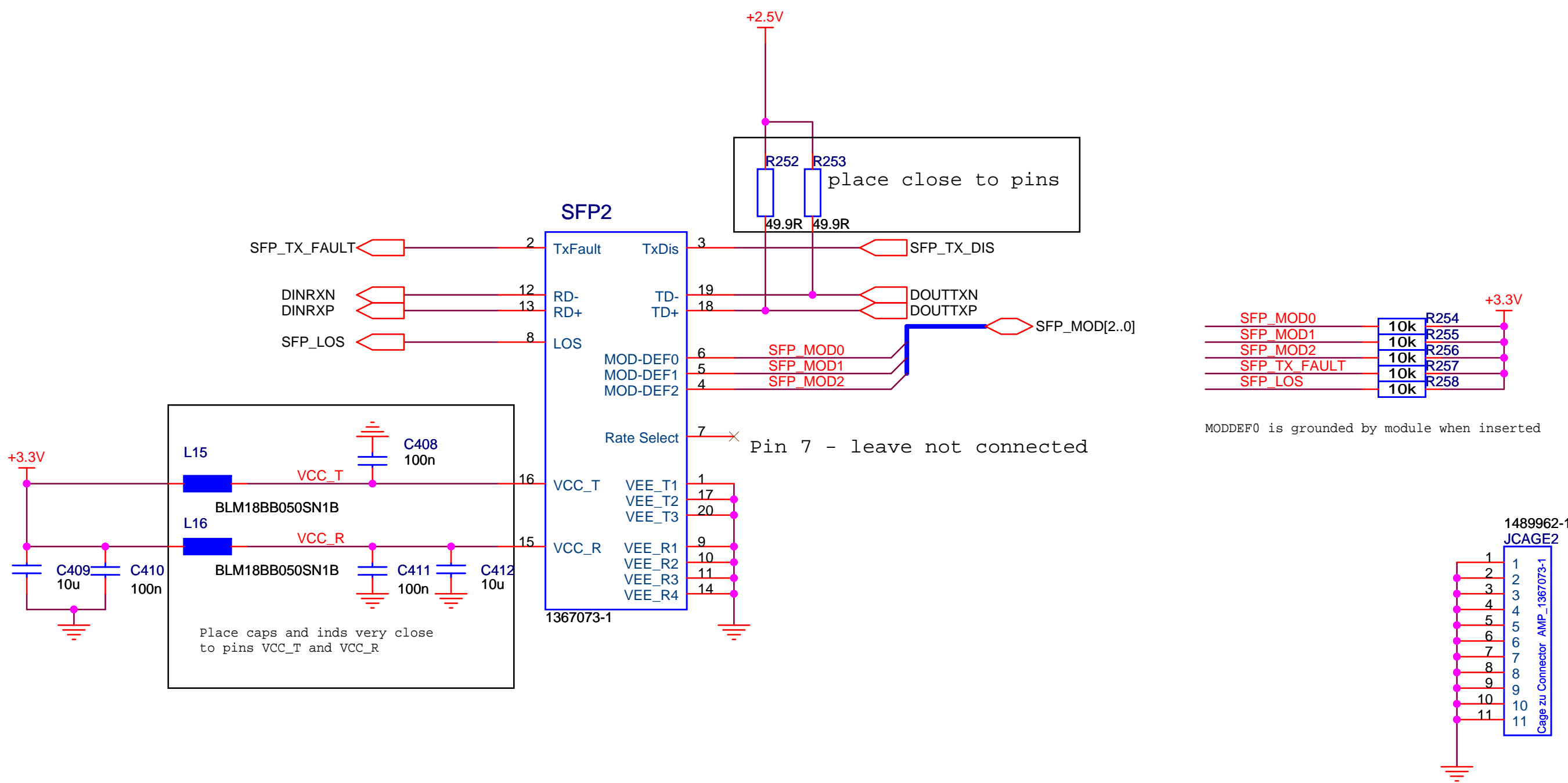
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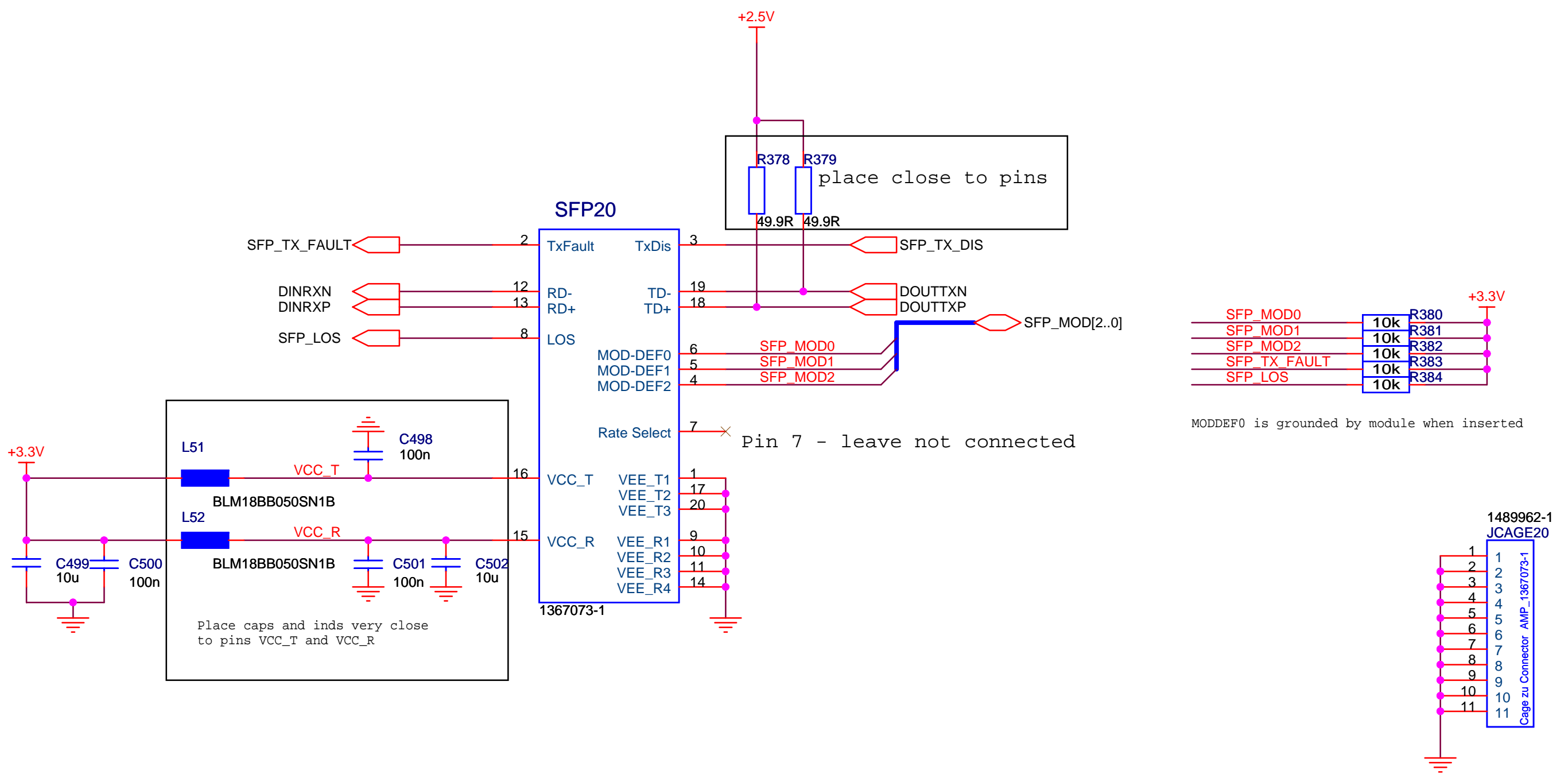


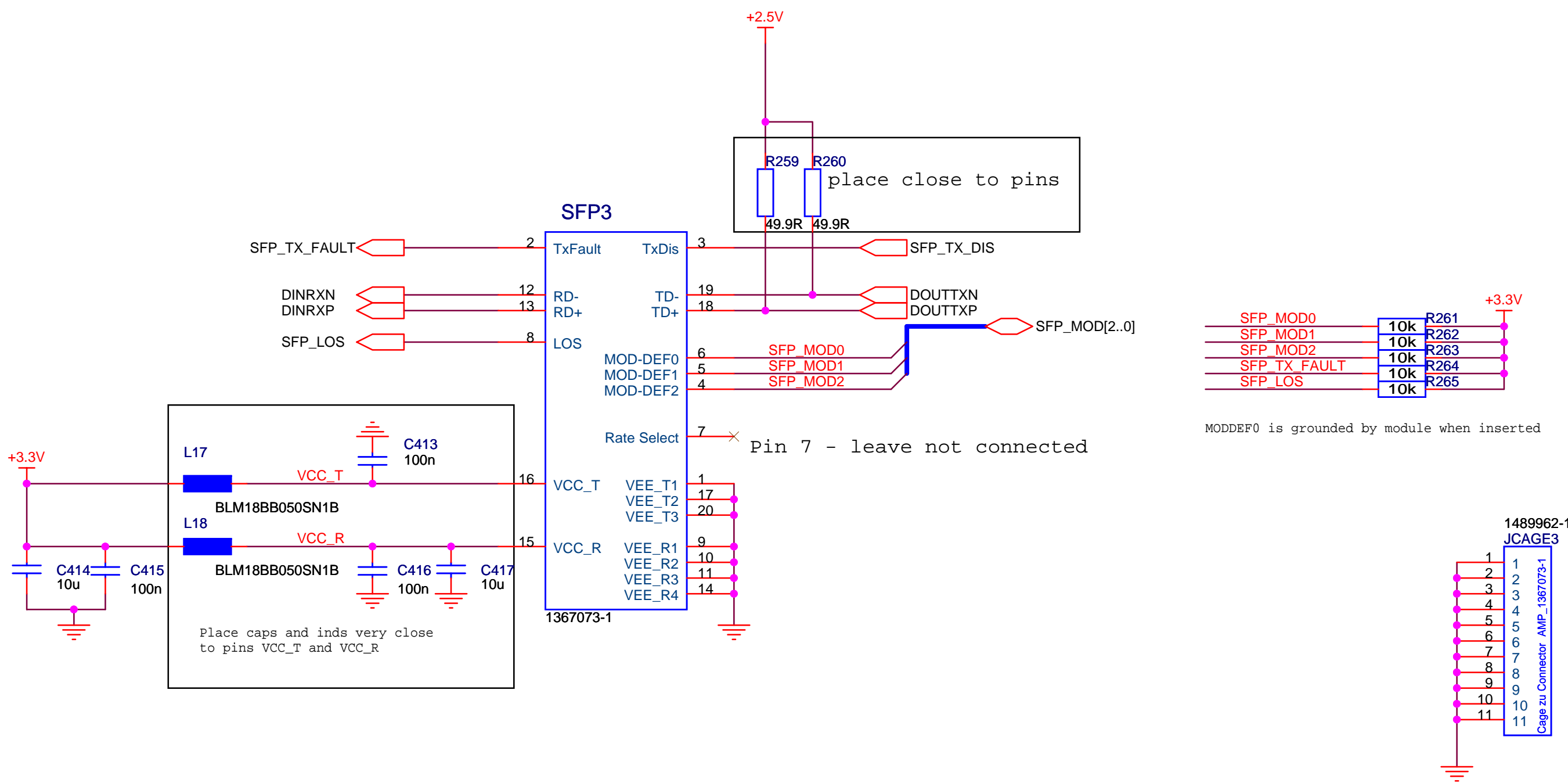
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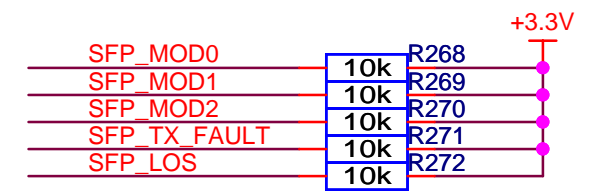
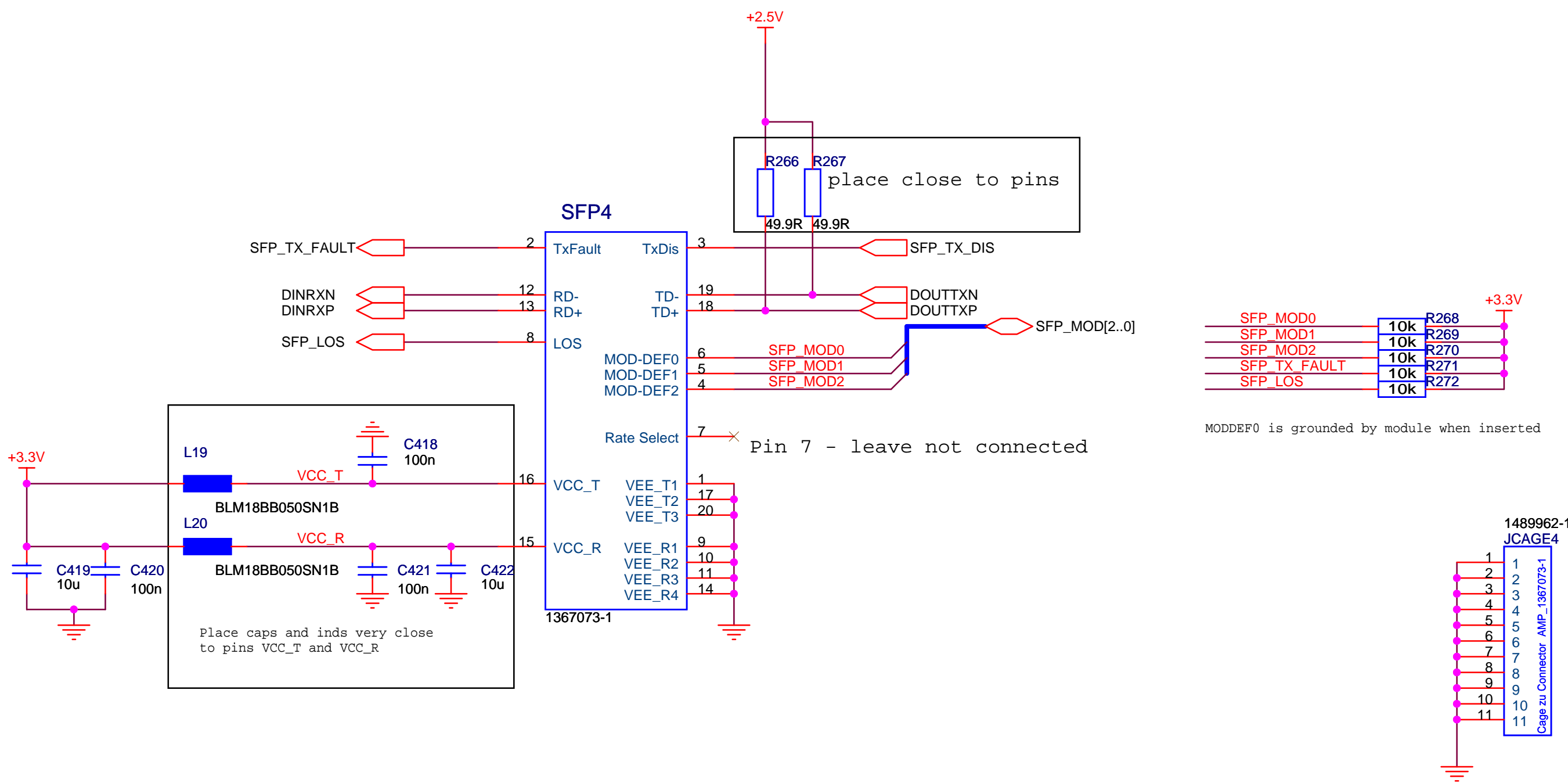




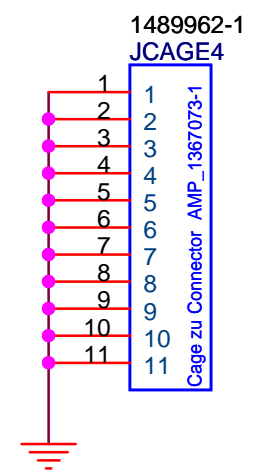




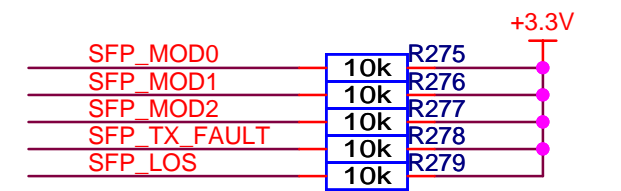
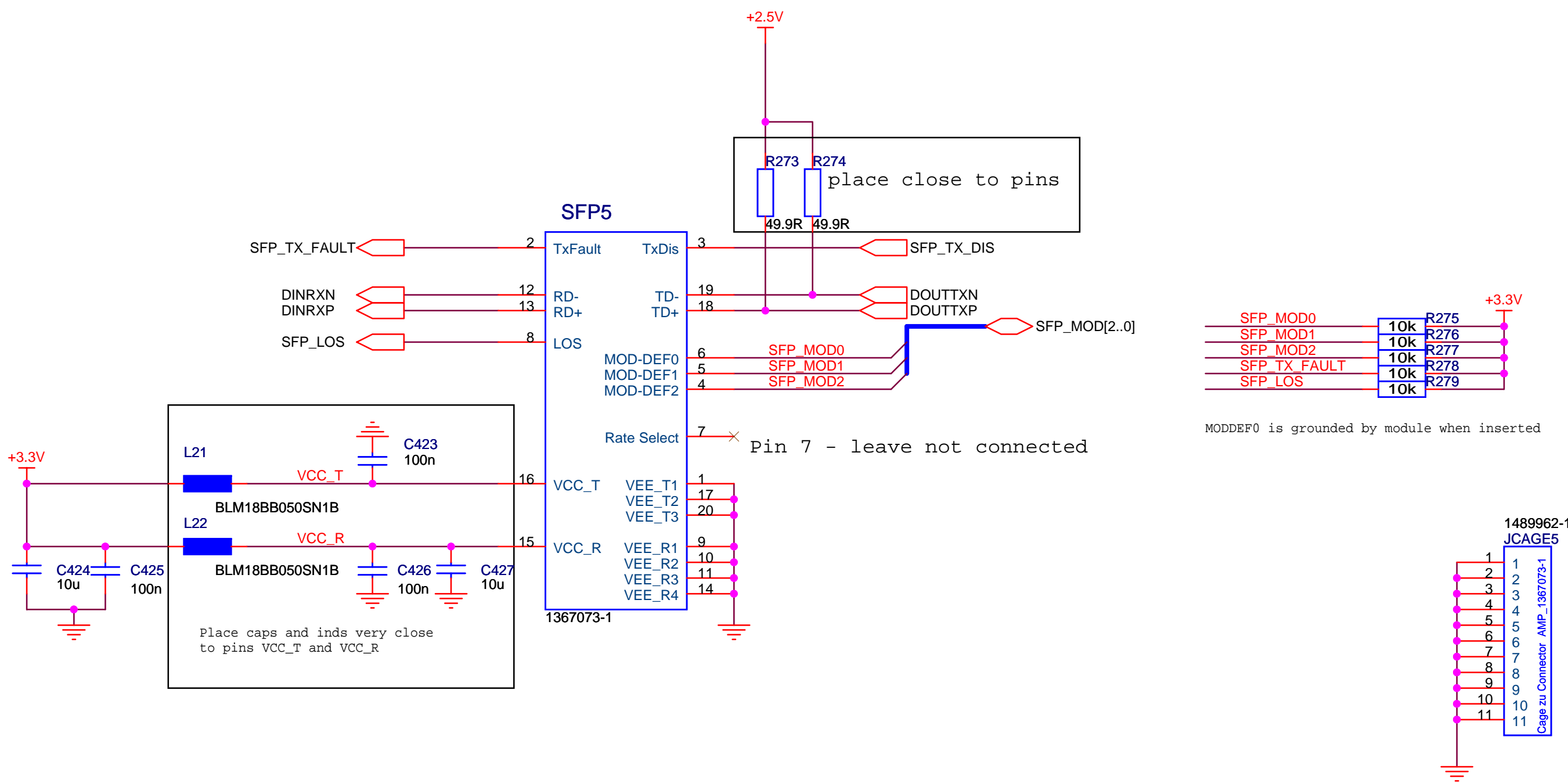
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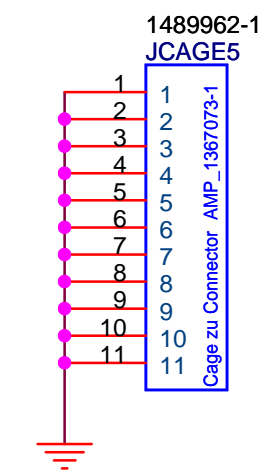
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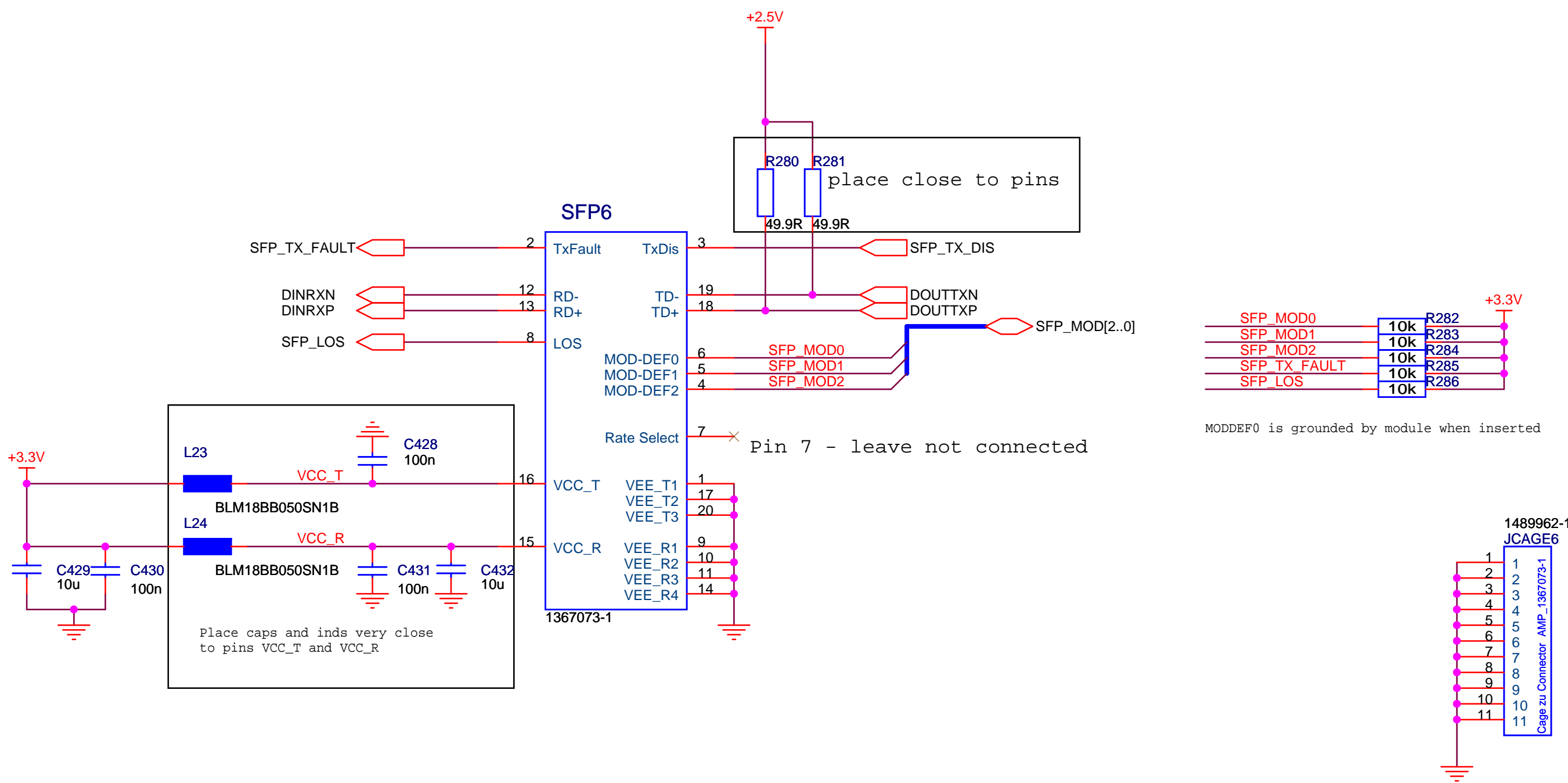
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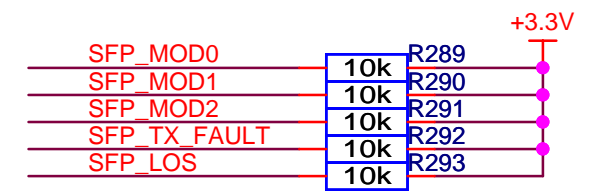
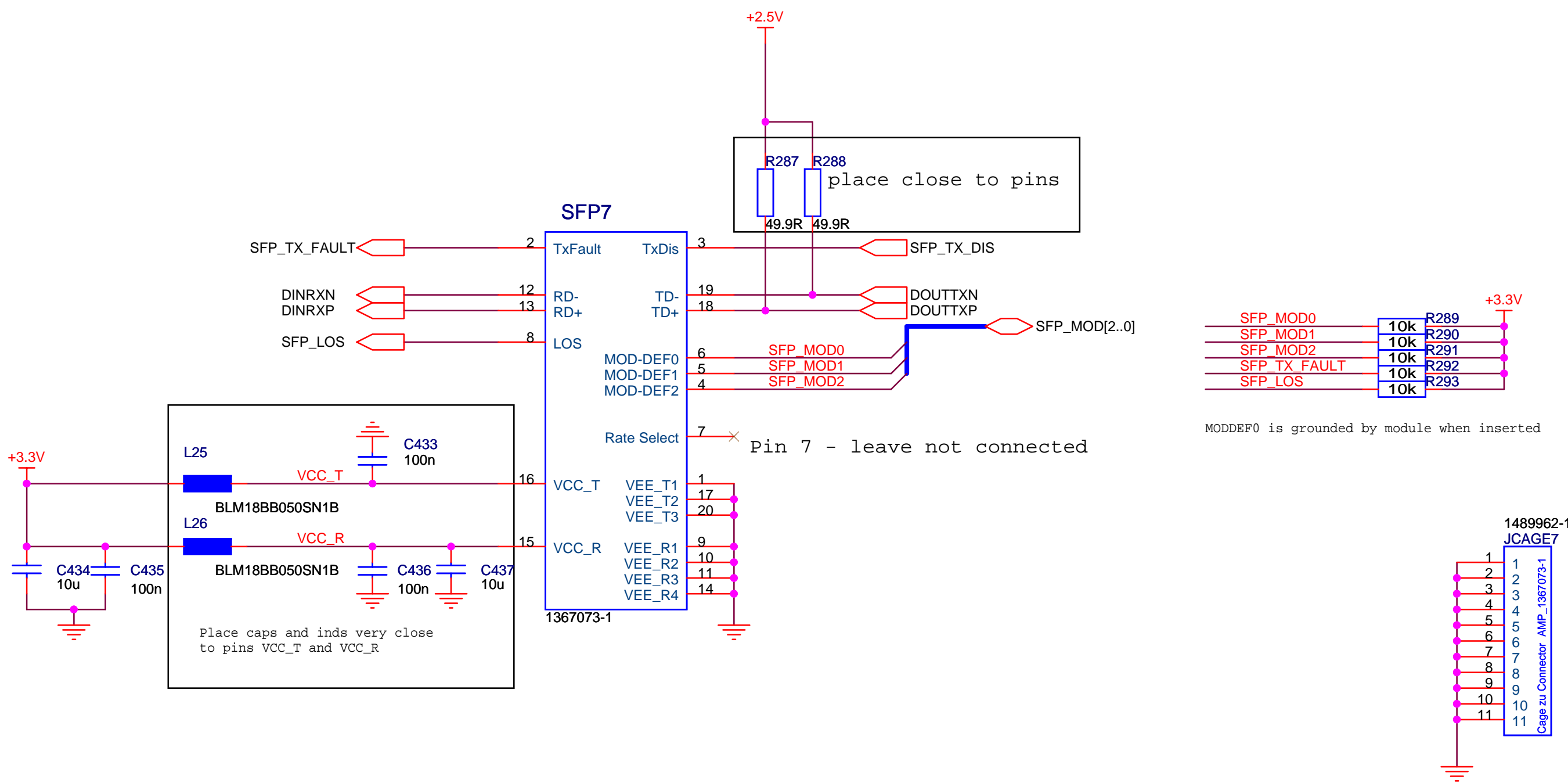


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