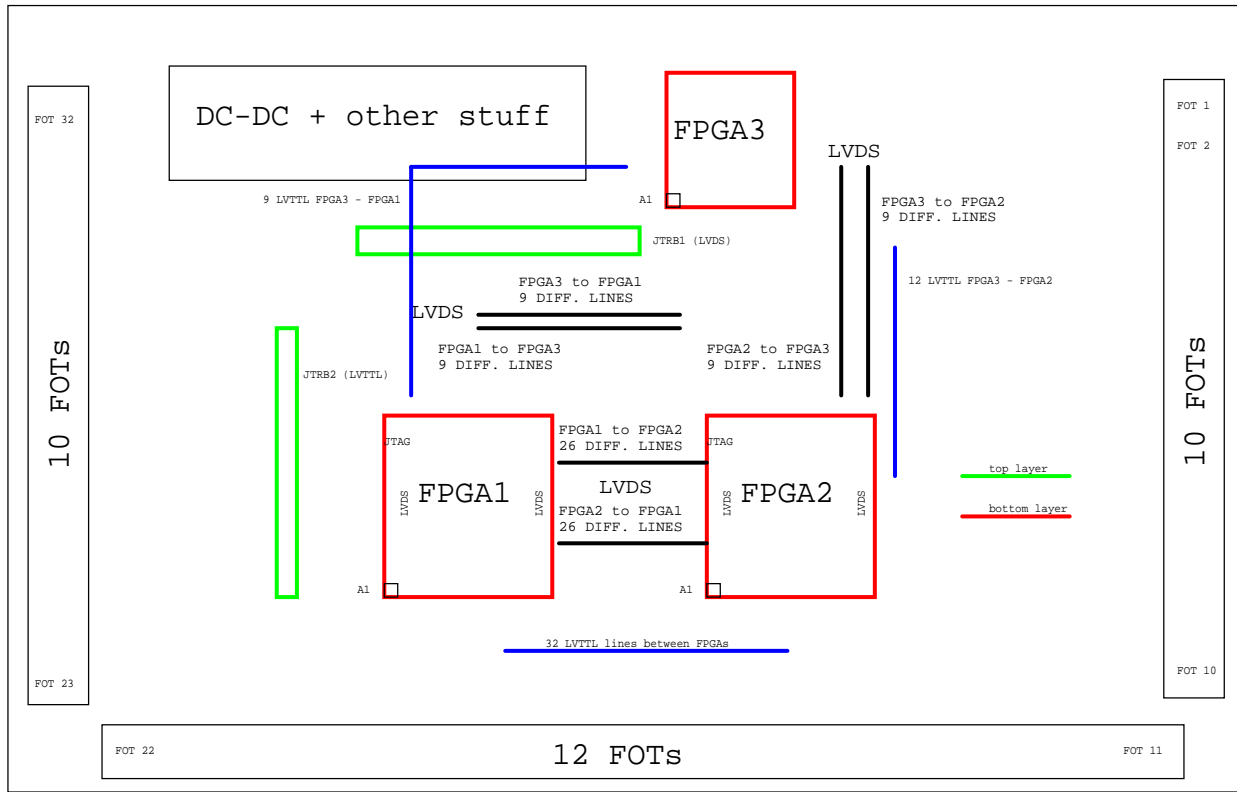
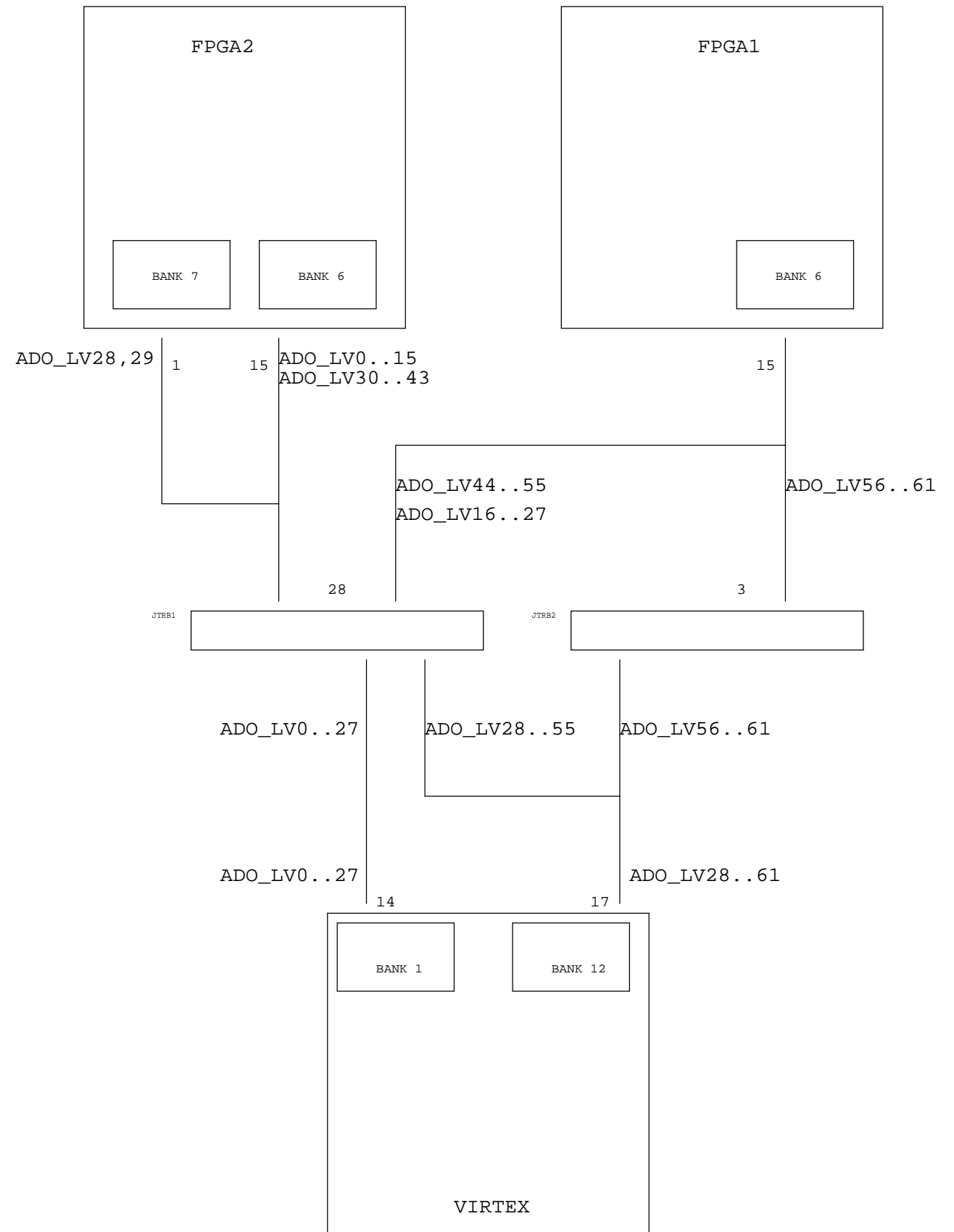
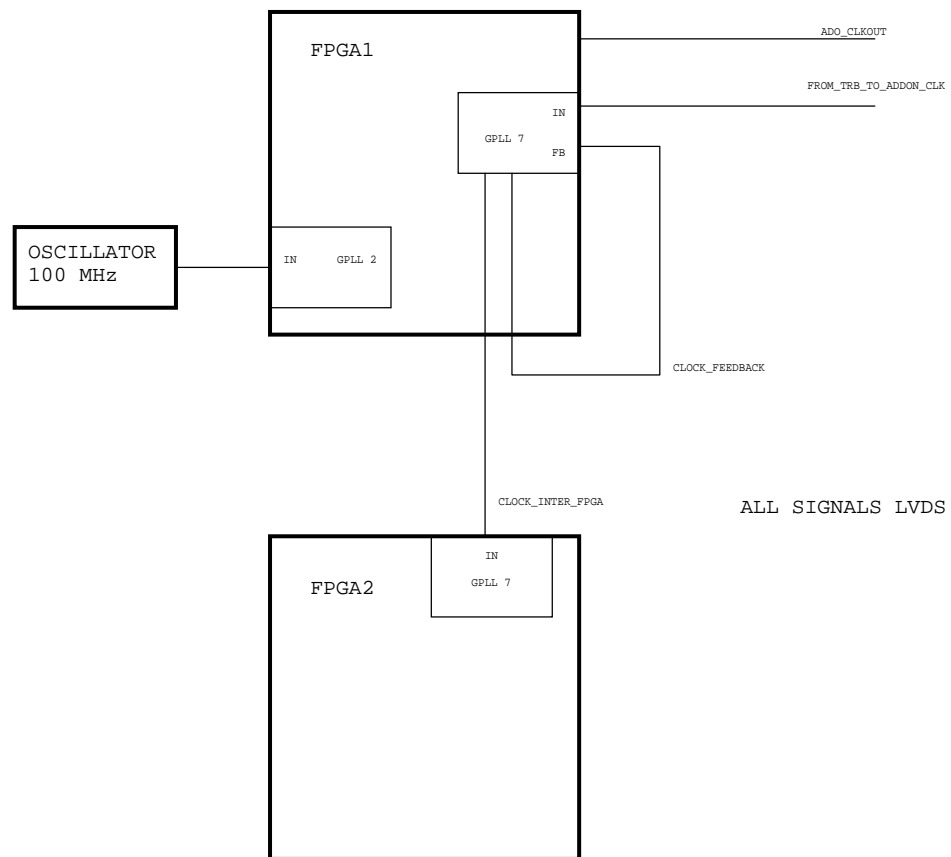


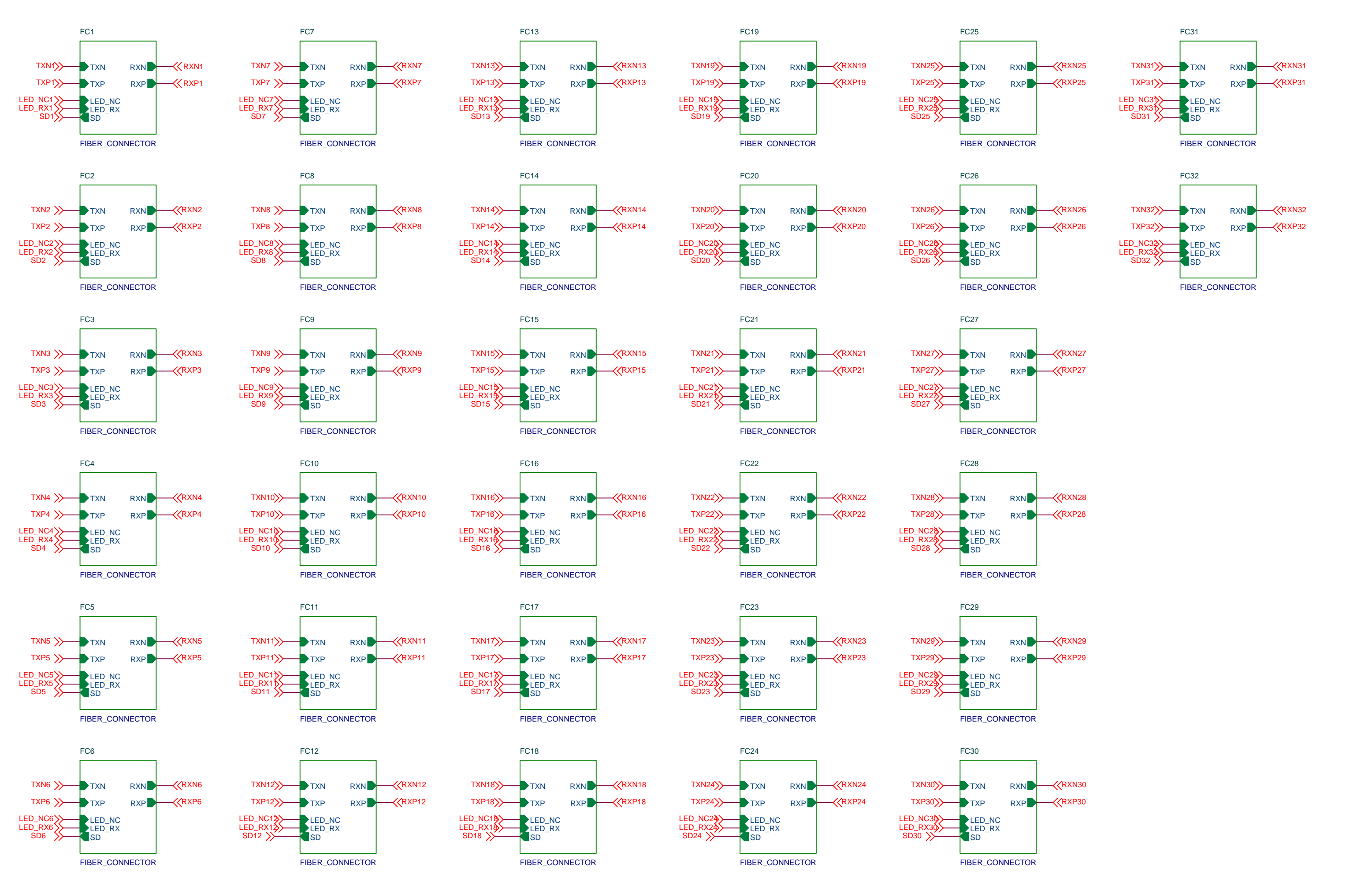
Proposed layout



Each FOT has a body of 1.6mm. If we get the FOTs for the optical AddOn without "wings", so with through-hole pins just for the fixture, then we can put them 1.7mm next to each other

CLOCK DISTRIBUTION:

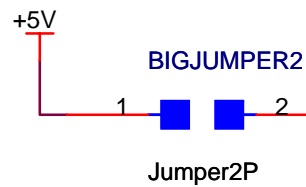




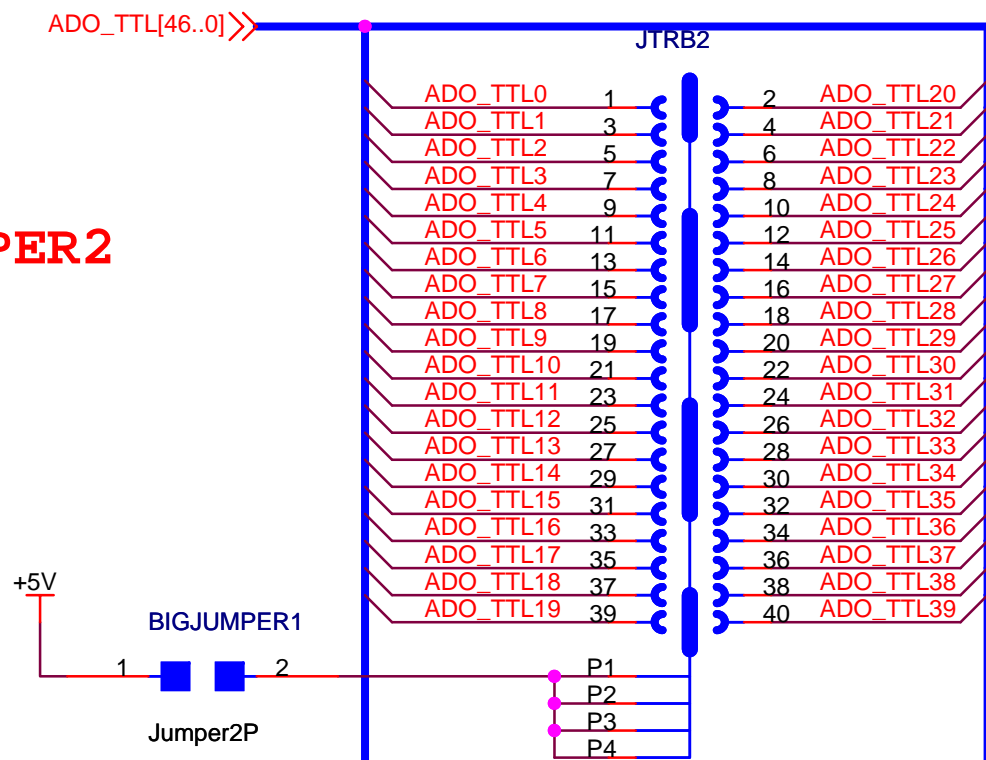
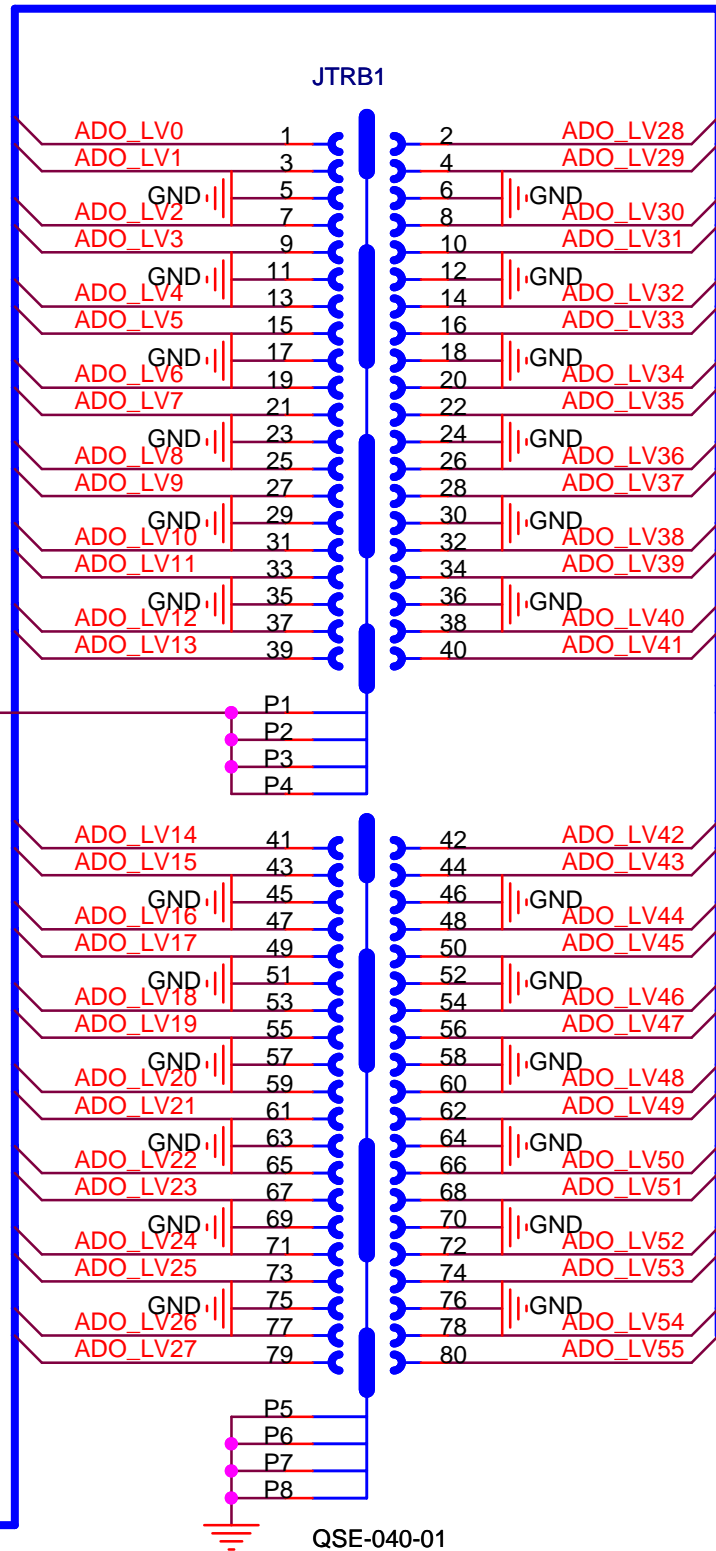
Title			01_FIBER_CONNECTS		
Size	Document Number				Rev
A3	<Doc>				<RevC
Date:	Friday, March 07, 2008	Sheet	2	of	47

**Either BIGJUMPER1 & BIGJUMPER2
are soldered or BIGJUMPER3**

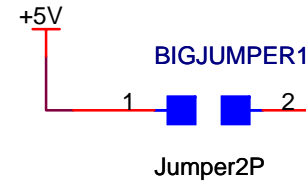
Even numbers: positive
Odd numbers: negative



**BIGJUMPER should stand
10A current**



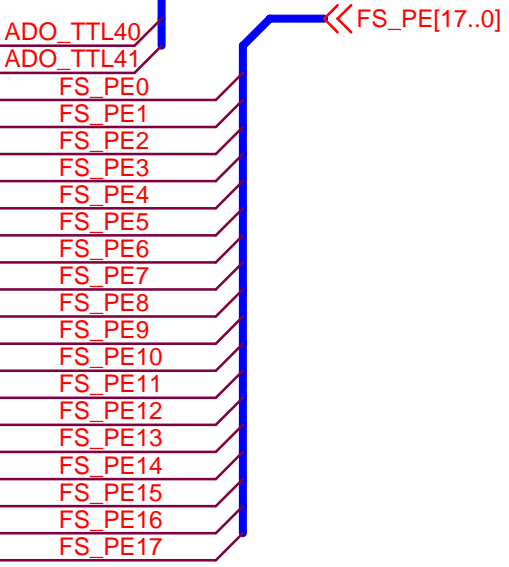
**BIGJUMPER should stand
10A current**



goes to FPGA
global clock input

FROM_TRB_TO_ADDON_CLK
FROM_TRB_TO_ADDON_CLKb
driven from TRB clock-chip

JTAG interface:
(seen from TRB)
TDI - TDO from FPGA on TRB (FS_PE0 high Z)
TMS - FS_PE1
TCK - FS_PE2
TDO - FS_PE4



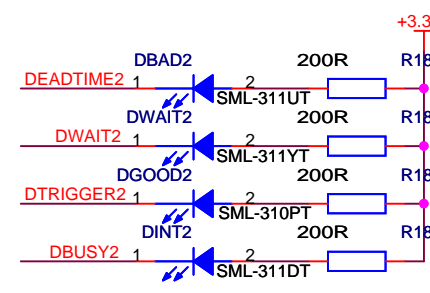
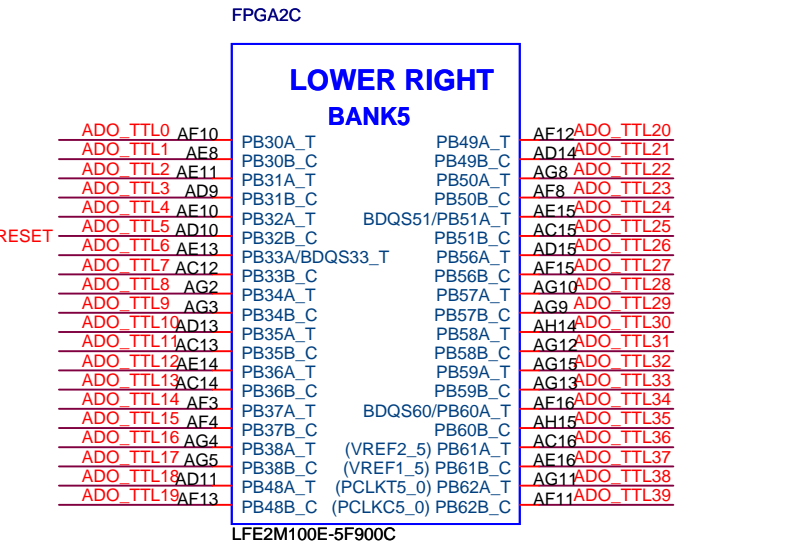
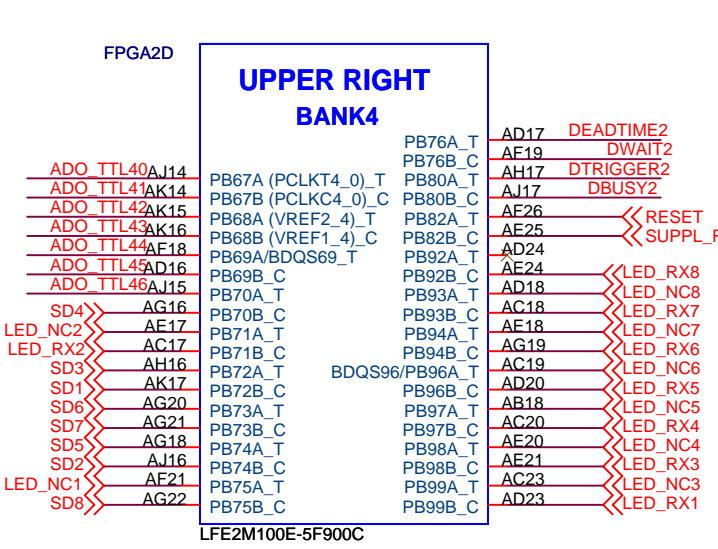
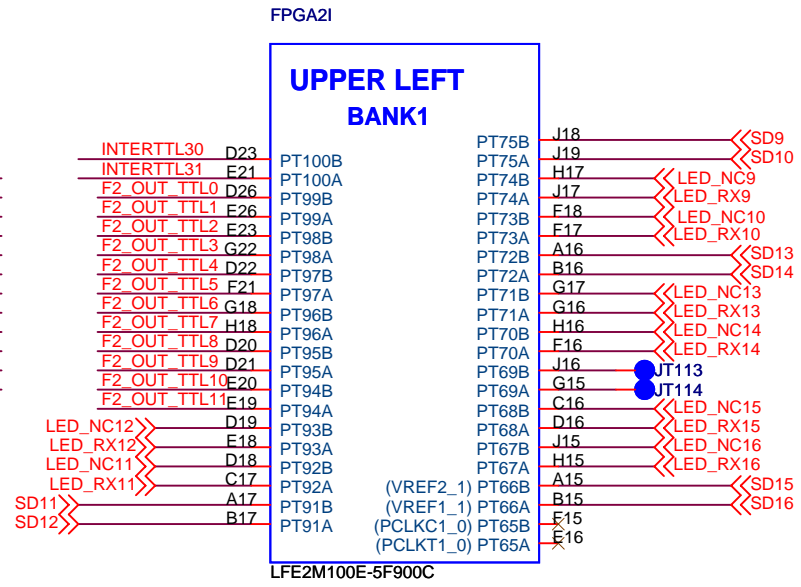
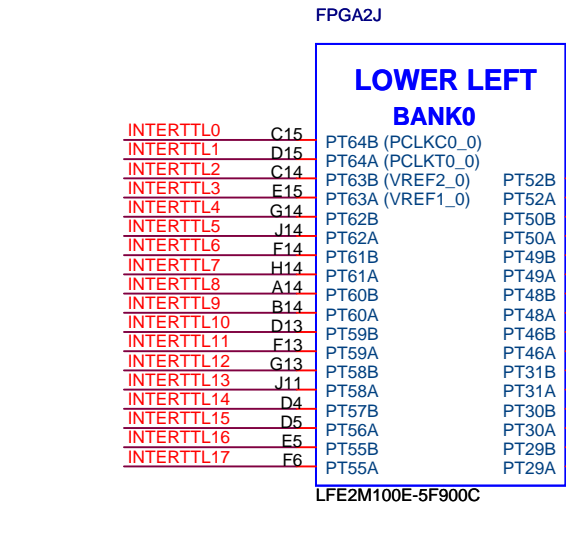
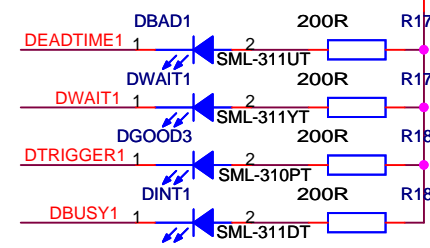
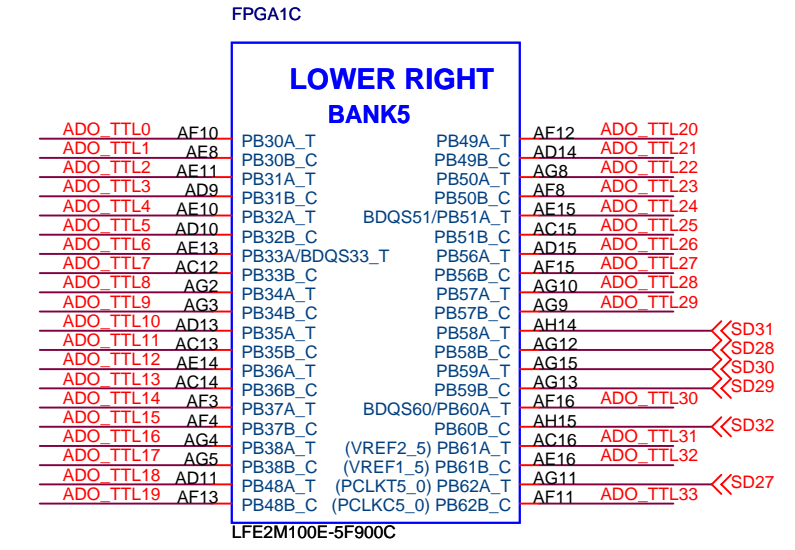
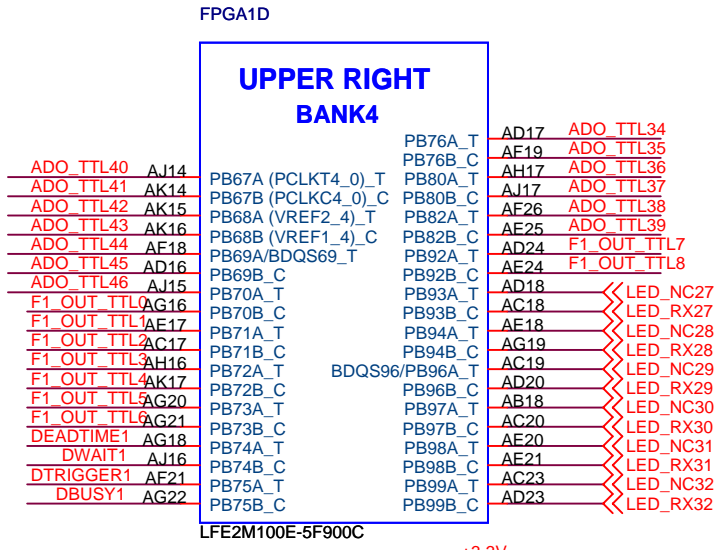
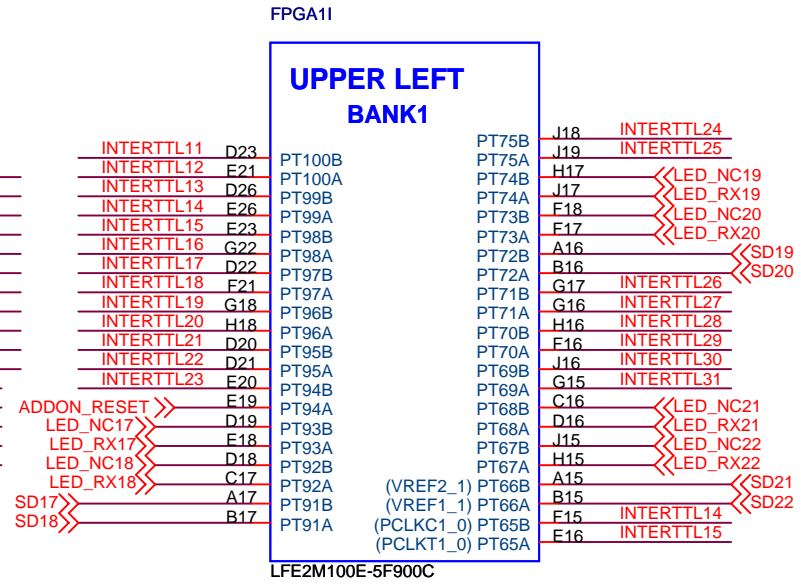
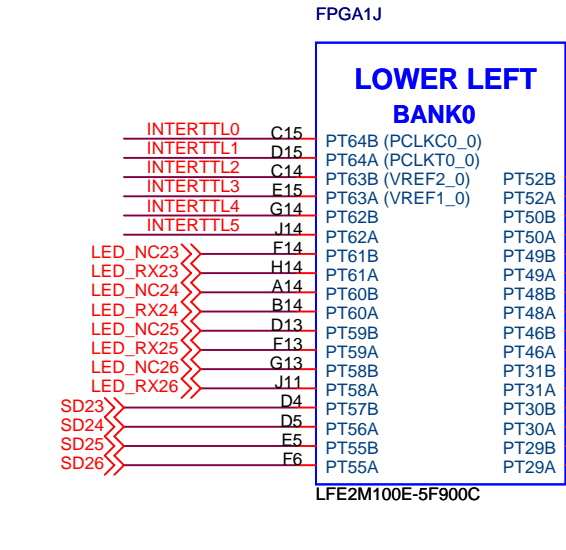
FS_PE16 (SCL) and FS_PE17 (SDA)
used to control ispPAC-POWER chip

FS_PE12 - FS_PE15 connected to
IN1 - IN4 in ispPAC-POWER chip
general purpose inputs

FS_PE11 - temperature control

Title			02_TRB_CONNECTORS		
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Date:	Wednesday, March 05, 2008		Sheet	3	of 47

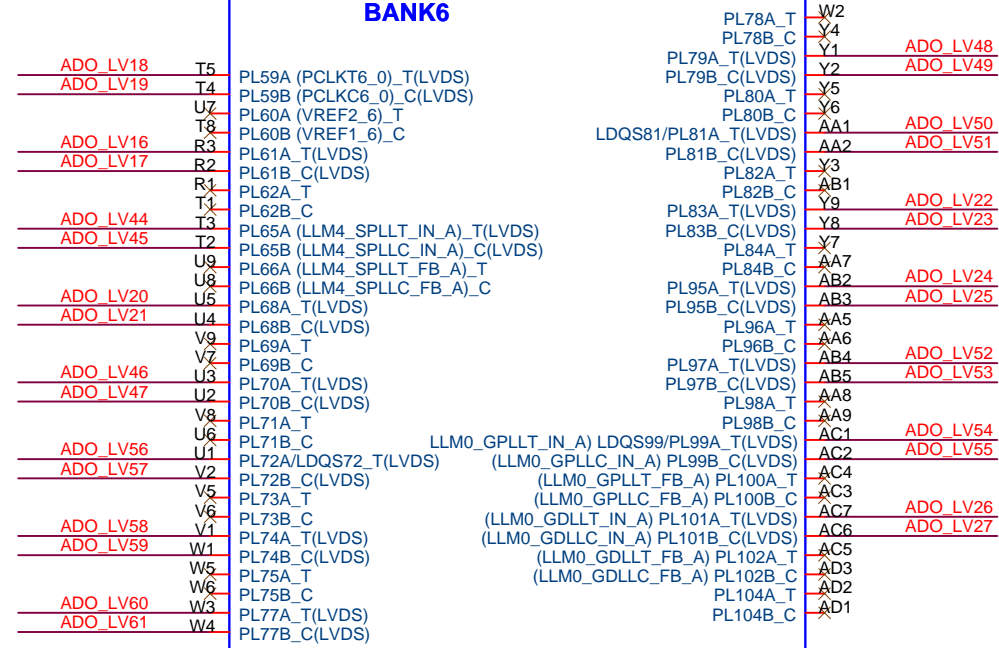
ADO_TTL[46..0] >>
 FS_PE[17..0] >>
 F1_OUT_TTL[8..] >>
 F2_OUT_TTL[11] >>



ADO_LV[61..0]

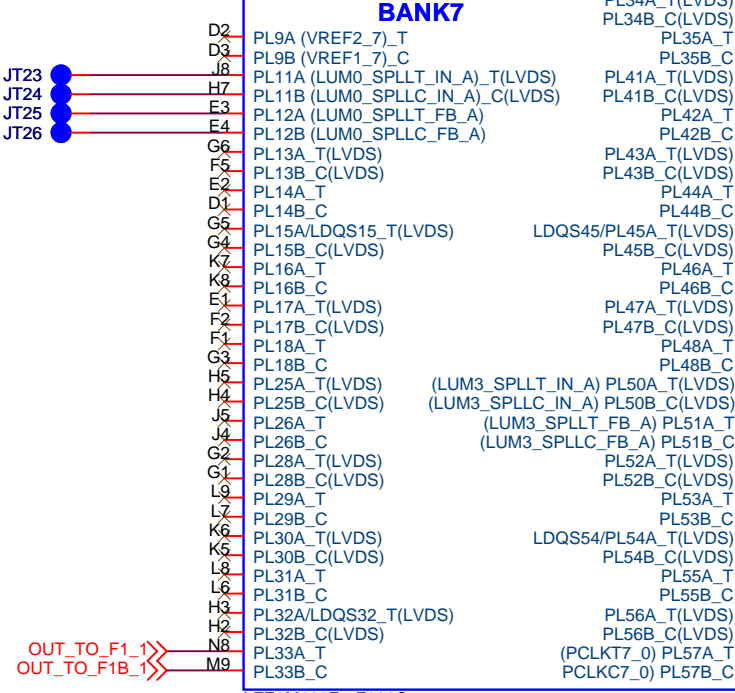
FPGA1B

BOTTOM RIGHT BANK6



FPGA1A

BOTTOM LEFT BANK7



OUT TO F1 0	100R	R357	OUT TO F1B 0
OUT TO F1 1	100R	R358	OUT TO F1B 1
OUT TO F1 2	100R	R359	OUT TO F1B 2
OUT TO F1 3	100R	R360	OUT TO F1B 3
OUT TO F1 4	100R	R361	OUT TO F1B 4
OUT TO F1 5	100R	R362	OUT TO F1B 5
OUT TO F1 6	100R	R363	OUT TO F1B 6
OUT TO F1 7	100R	R364	OUT TO F1B 7
OUT TO F1 8	100R	R365	OUT TO F1B 8

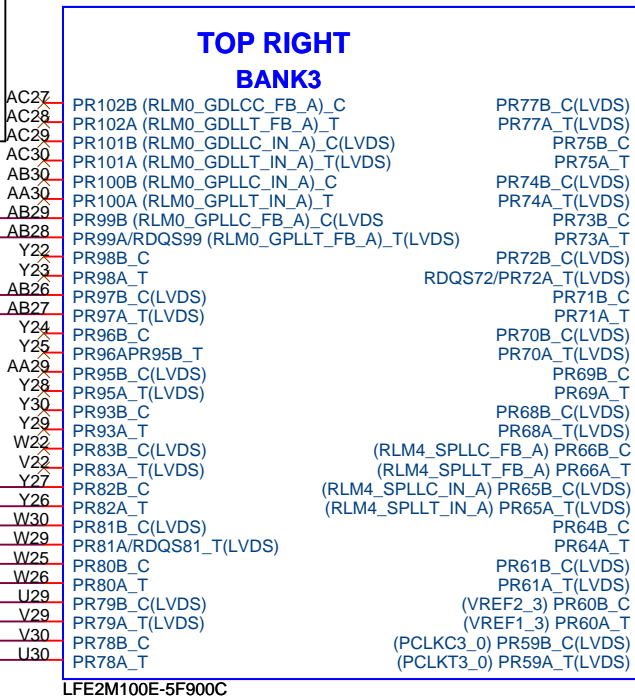
CK, SI, EN left open:
default state:
CLK0 - INPUT, all outputs active

ADO LV16	100R	R306	ADO LV17
ADO LV18	100R	R307	ADO LV19
ADO LV20	100R	R308	ADO LV21
ADO LV22	100R	R309	ADO LV23
ADO LV24	100R	R310	ADO LV25
ADO LV26	100R	R311	ADO LV27
ADO LV44	100R	R312	ADO LV45
ADO LV46	100R	R313	ADO LV47
ADO LV48	100R	R314	ADO LV49
ADO LV50	100R	R315	ADO LV51
ADO LV52	100R	R316	ADO LV53
ADO LV54	100R	R317	ADO LV55
ADO LV56	100R	R318	ADO LV57
ADO LV58	100R	R319	ADO LV59
ADO LV60	100R	R320	ADO LV61

Soldering LVDS termination resistors depends on application

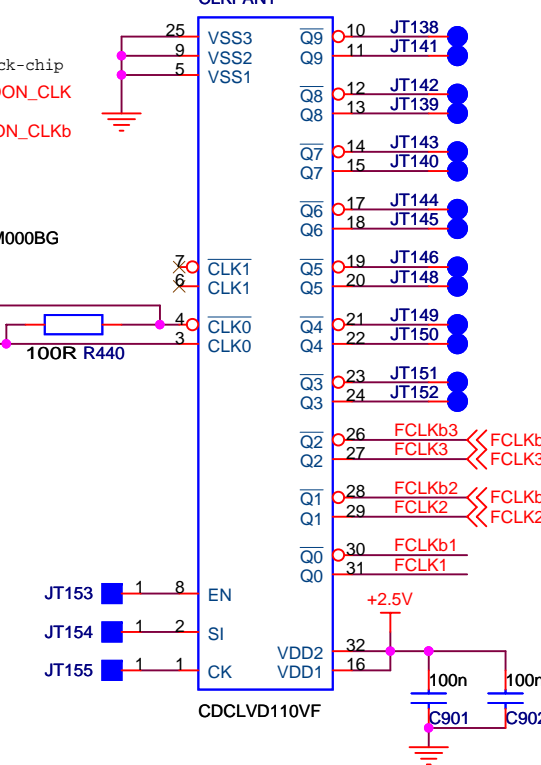
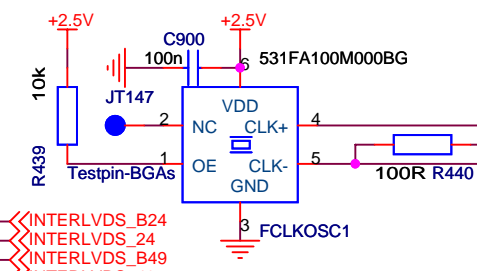
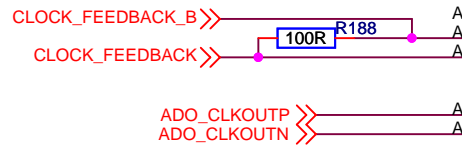
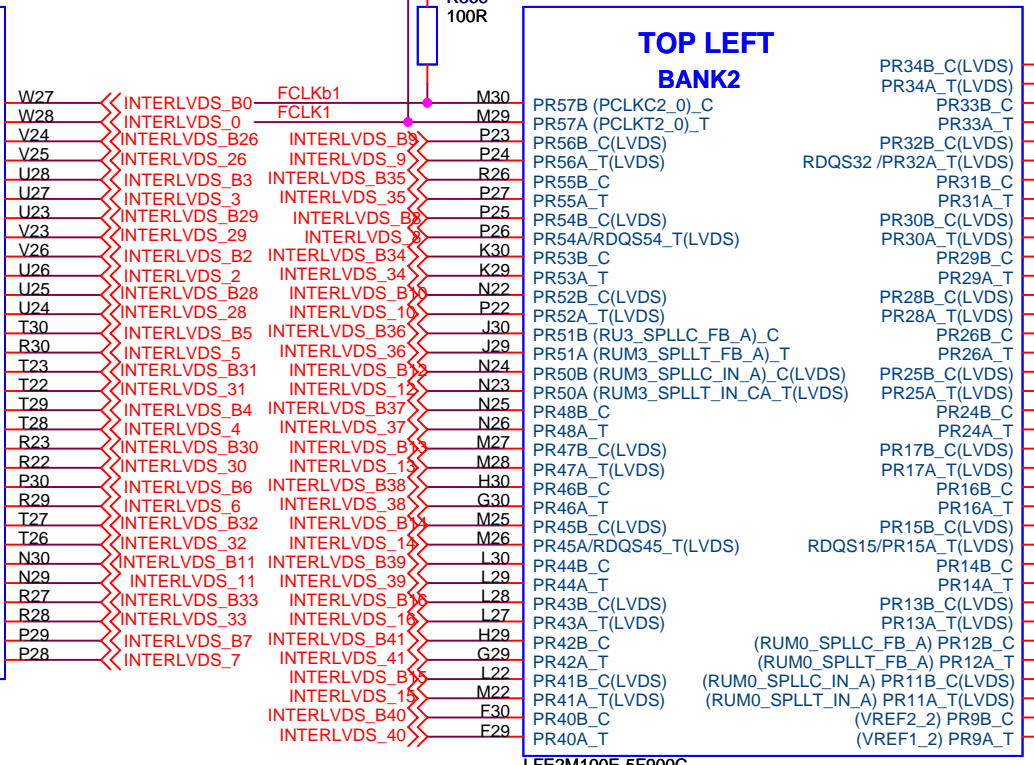
FPGA1F

TOP RIGHT BANK3

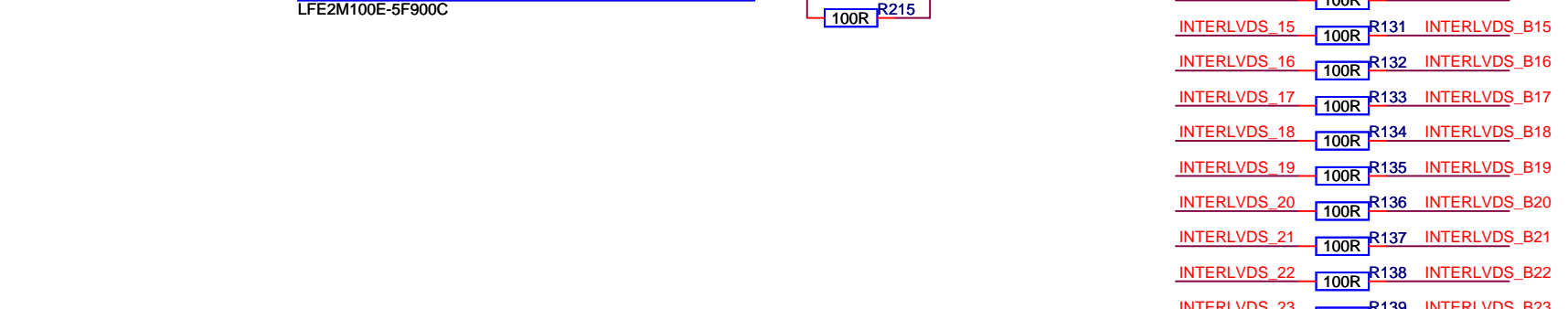
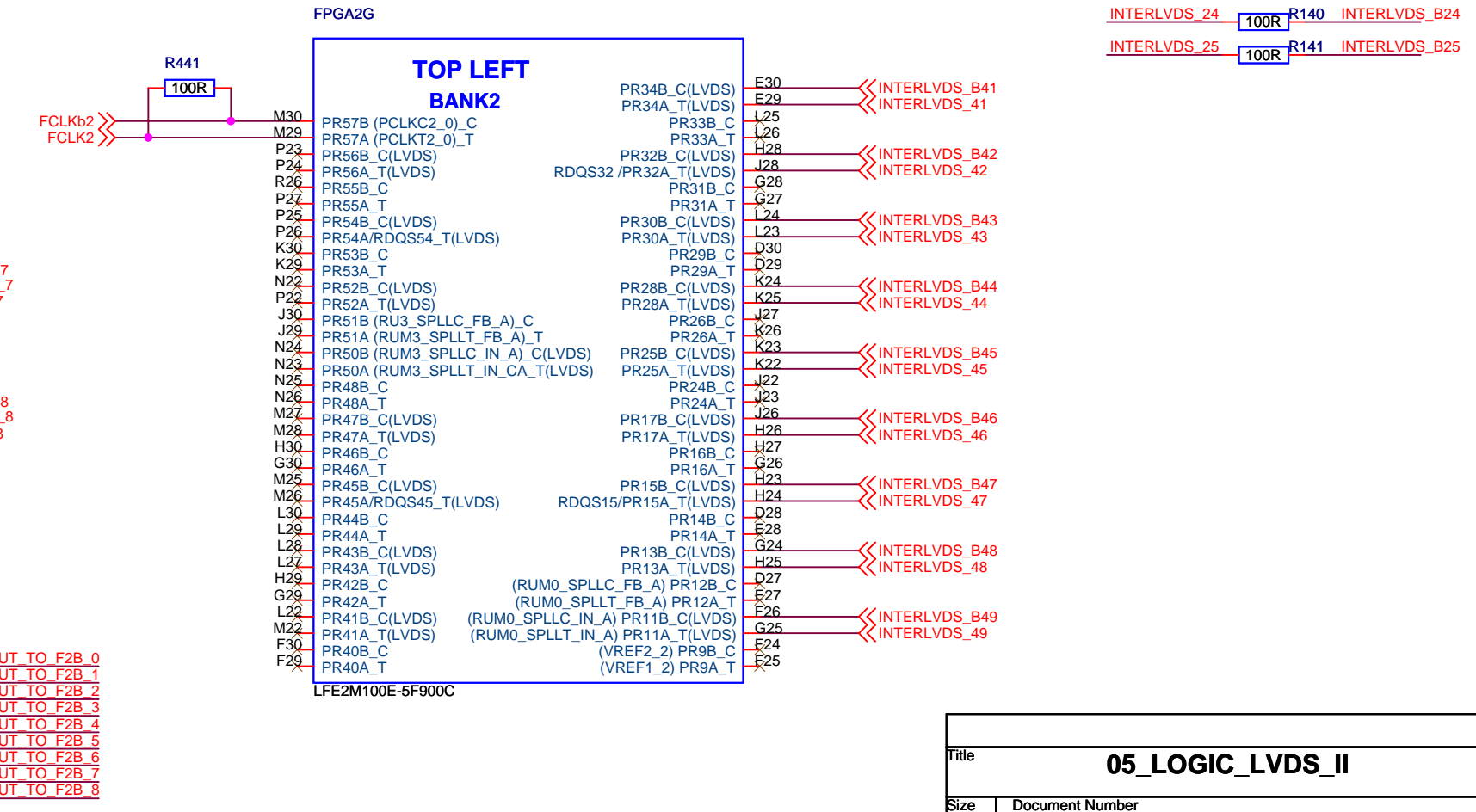
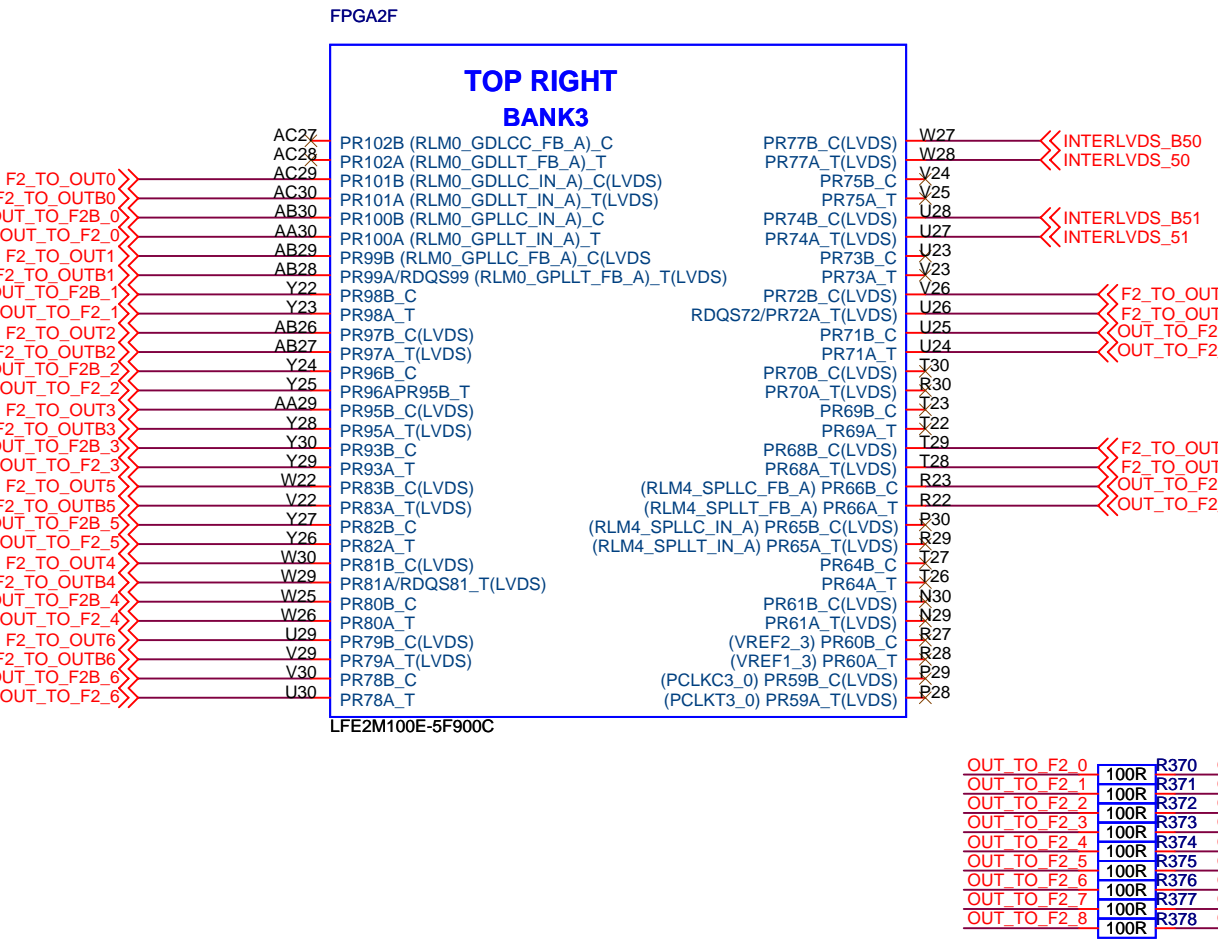
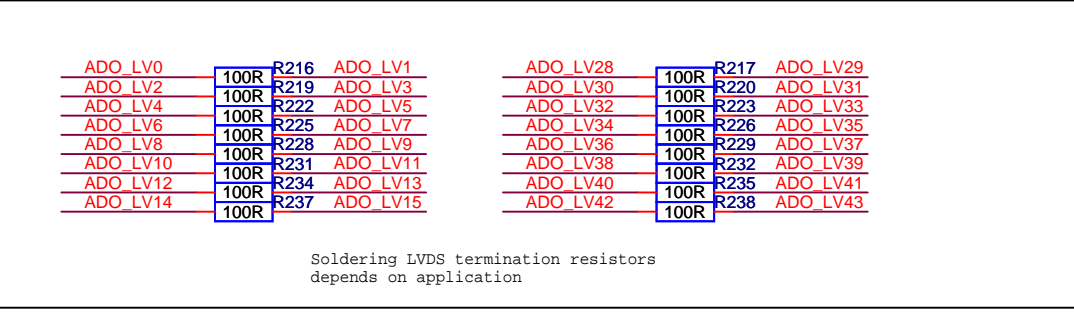
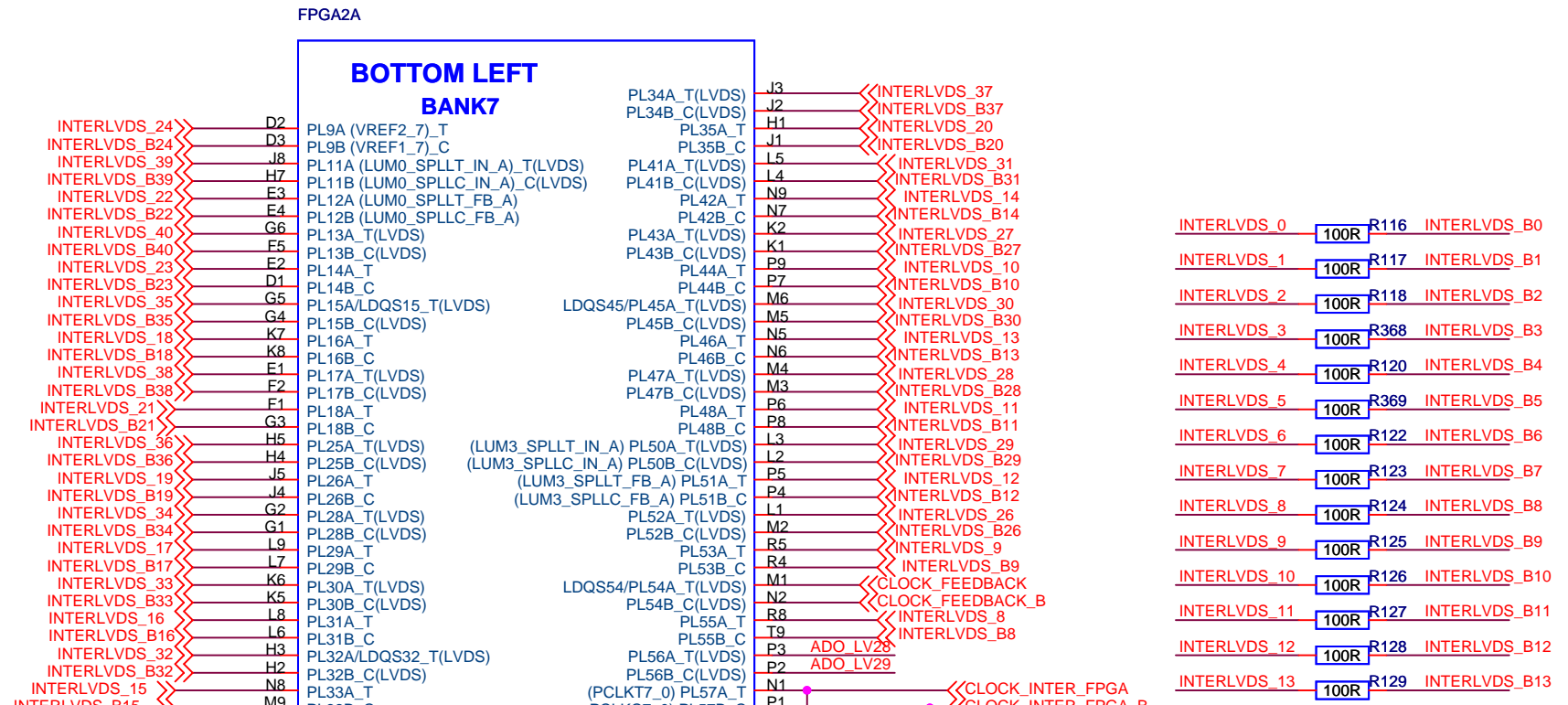
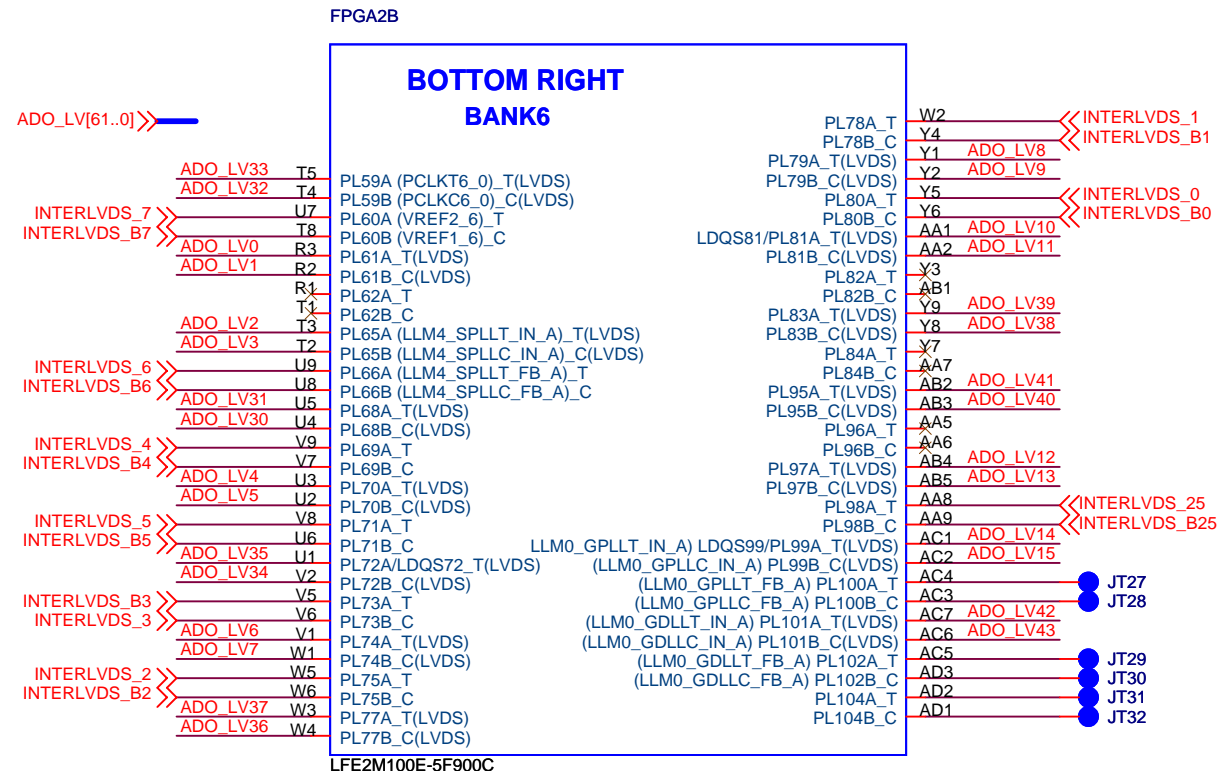


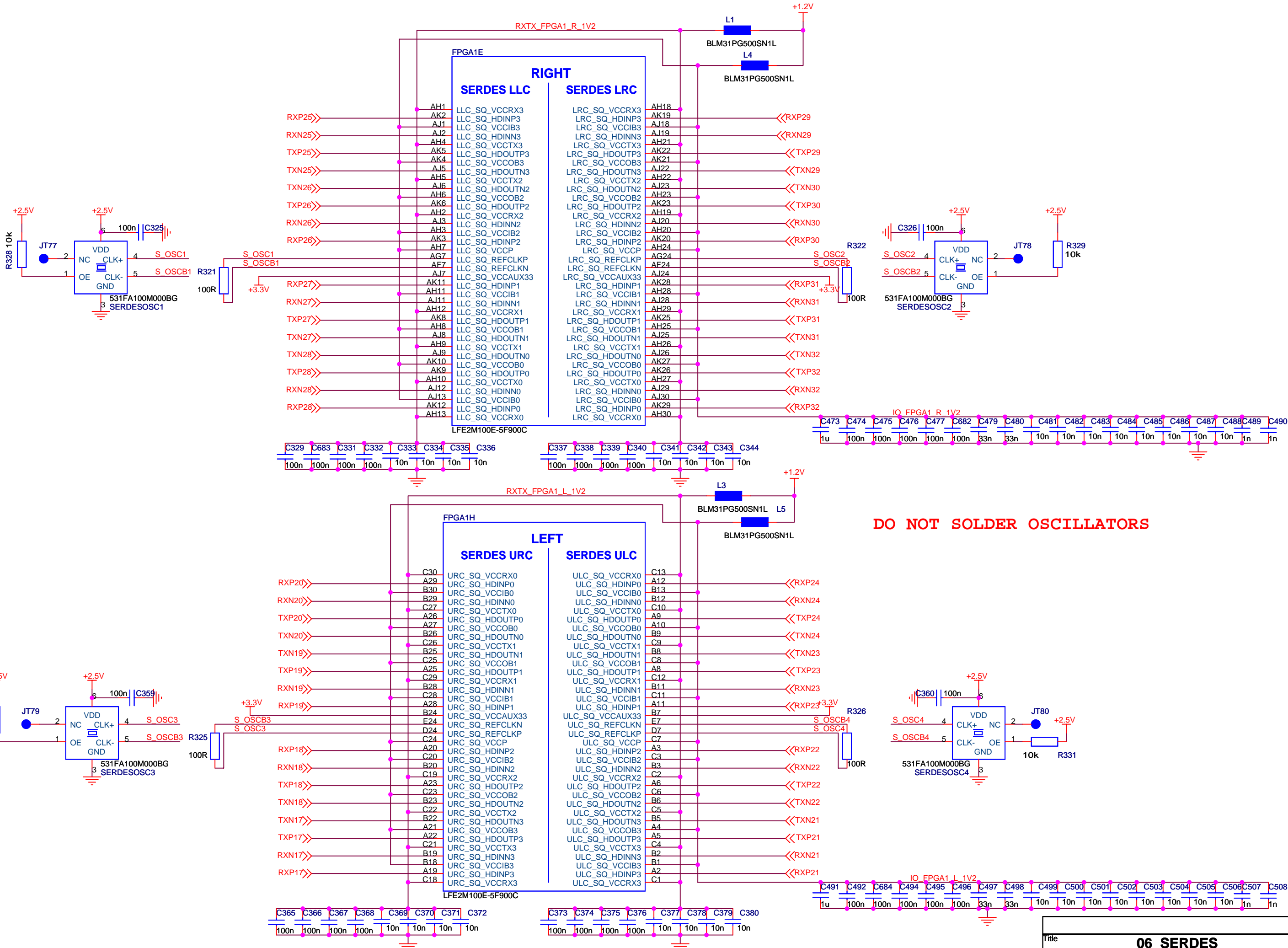
FPGA1G

TOP LEFT BANK2



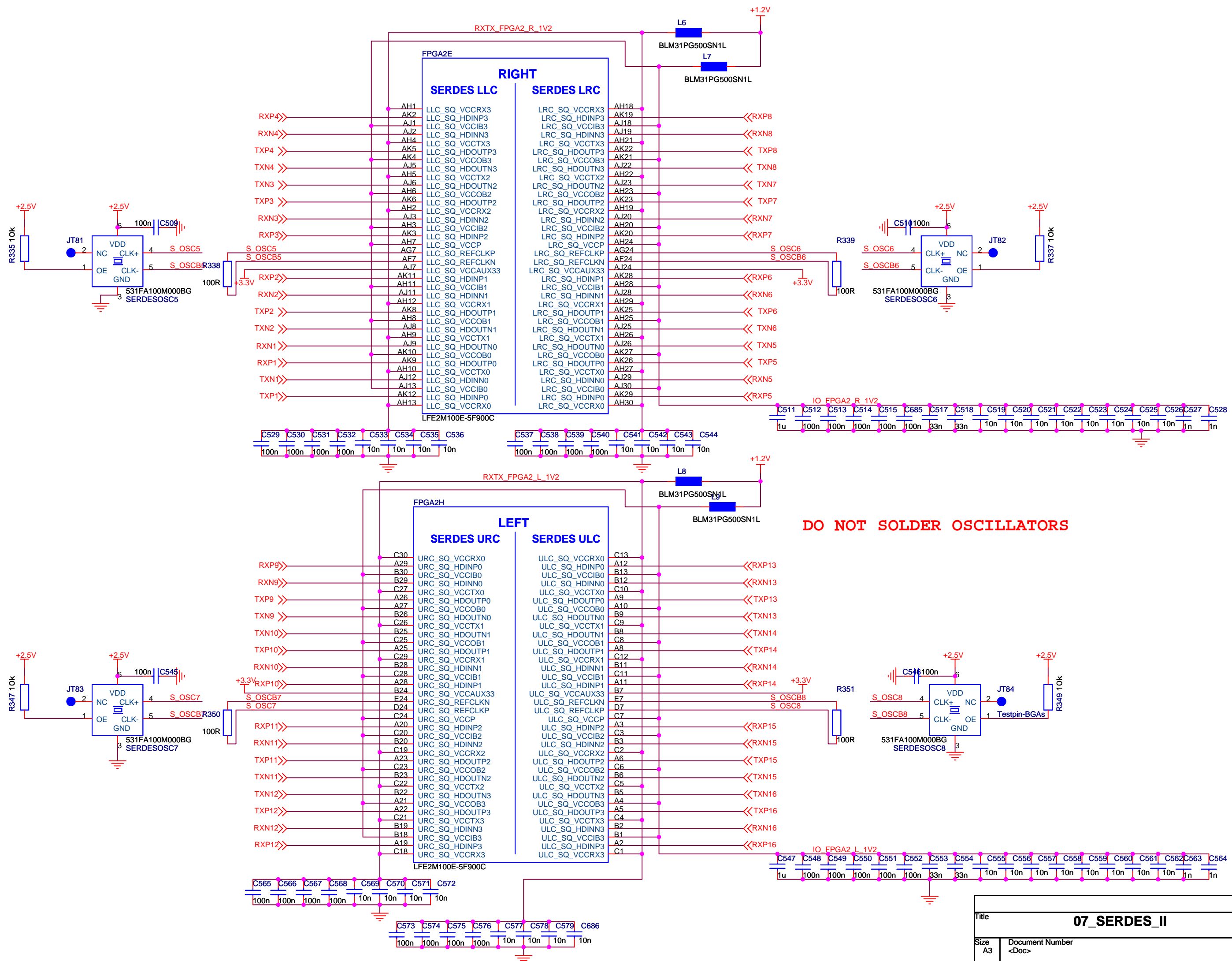
INTERLVDS_26	100R	R189	INTERLVDS_B26
INTERLVDS_27	100R	R192	INTERLVDS_B27
INTERLVDS_28	100R	R195	INTERLVDS_B28
INTERLVDS_29	100R	R198	INTERLVDS_B29
INTERLVDS_30	100R	R201	INTERLVDS_B30
INTERLVDS_31	100R	R204	INTERLVDS_B31
INTERLVDS_32	100R	R207	INTERLVDS_B32
INTERLVDS_33	100R	R210	INTERLVDS_B33
INTERLVDS_34	100R	R190	INTERLVDS_B34
INTERLVDS_35	100R	R193	INTERLVDS_B35
INTERLVDS_36	100R	R196	INTERLVDS_B36
INTERLVDS_37	100R	R199	INTERLVDS_B37
INTERLVDS_38	100R	R203	INTERLVDS_B38
INTERLVDS_39	100R	R205	INTERLVDS_B39
INTERLVDS_40	100R	R208	INTERLVDS_B40
INTERLVDS_41	100R	R211	INTERLVDS_B41
INTERLVDS_42	100R	R191	INTERLVDS_B42
INTERLVDS_43	100R	R194	INTERLVDS_B43
INTERLVDS_44	100R	R197	INTERLVDS_B44
INTERLVDS_45	100R	R200	INTERLVDS_B45
INTERLVDS_46	100R	R203	INTERLVDS_B46
INTERLVDS_47	100R	R206	INTERLVDS_B47
INTERLVDS_48	100R	R209	INTERLVDS_B48
INTERLVDS_49	100R	R212	INTERLVDS_B49
INTERLVDS_50	100R	R215	INTERLVDS_B50
INTERLVDS_51	100R	R218	INTERLVDS_B51





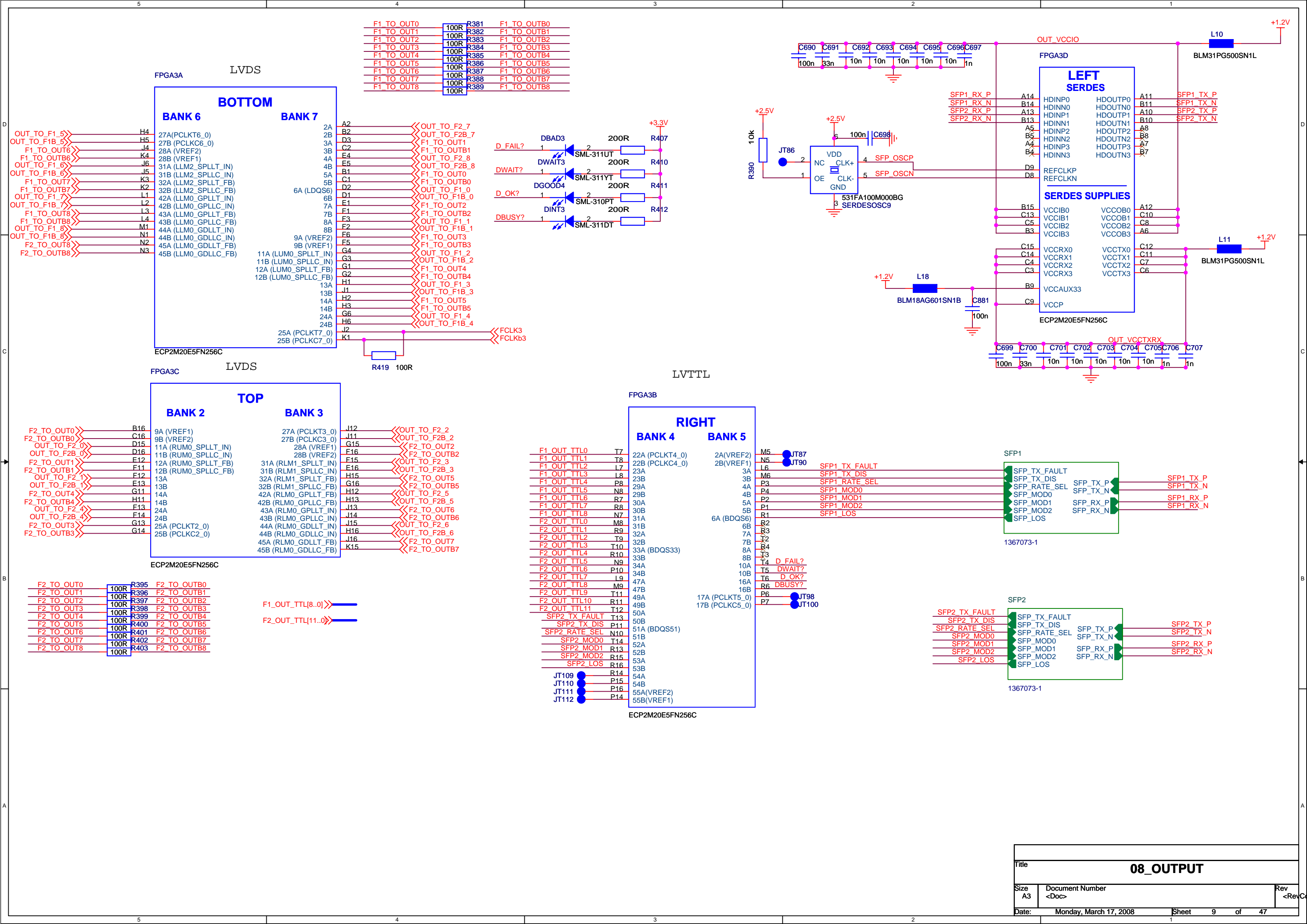
DO NOT SOLDER OSCILLATORS

Title			06_SERDES		
Size	Document Number		Rev		
A3	<Doc>		<RevC>		
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DO NOT SOLDER OSCILLATORS

Title			07_SERDES_II		
Size	Document Number		Rev		
A3	<Doc>		<RevC>		
Date:	Tuesday, March 11, 2008	Sheet	8	of	47



F1 TO OUT0	100R	R381	F1 TO OUTB0
F1 TO OUT1	100R	R382	F1 TO OUTB1
F1 TO OUT2	100R	R383	F1 TO OUTB2
F1 TO OUT3	100R	R384	F1 TO OUTB3
F1 TO OUT4	100R	R385	F1 TO OUTB4
F1 TO OUT5	100R	R386	F1 TO OUTB5
F1 TO OUT6	100R	R387	F1 TO OUTB6
F1 TO OUT7	100R	R388	F1 TO OUTB7
F1 TO OUT8	100R	R389	F1 TO OUTB8

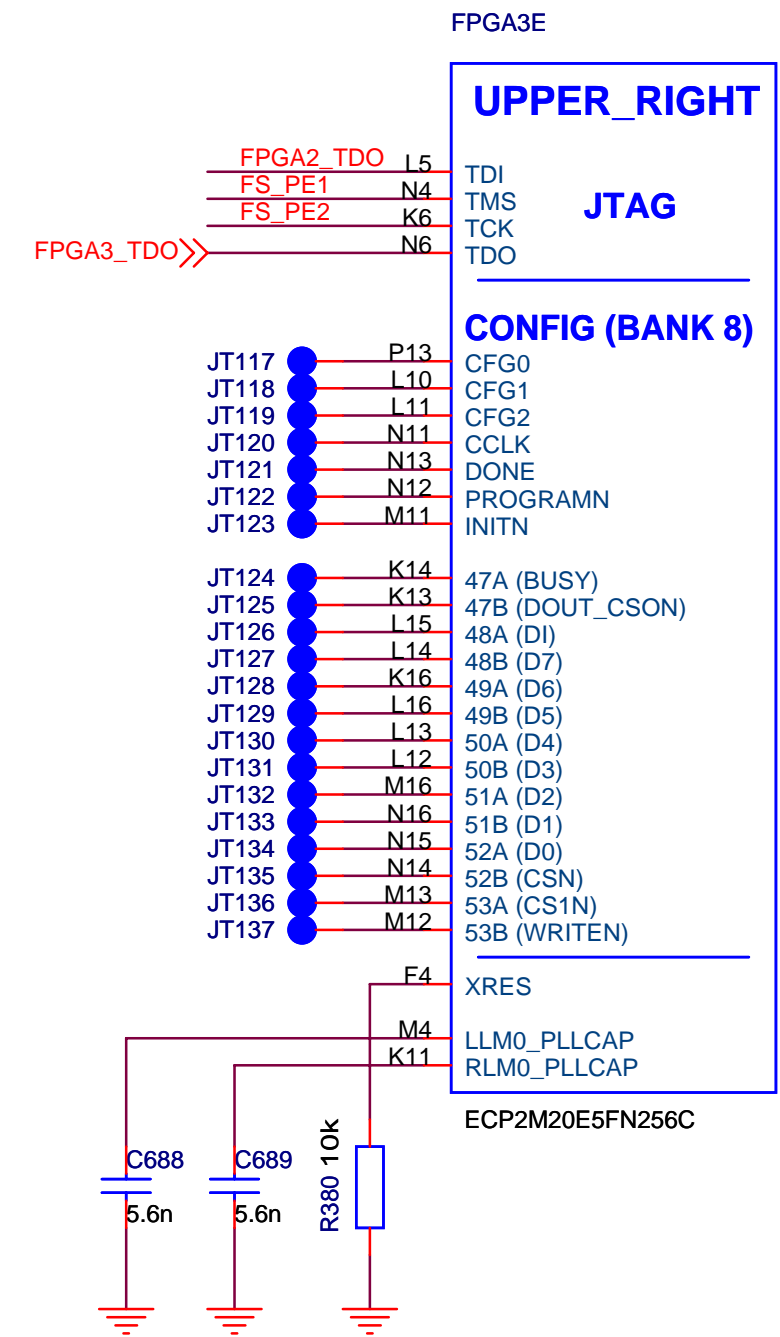
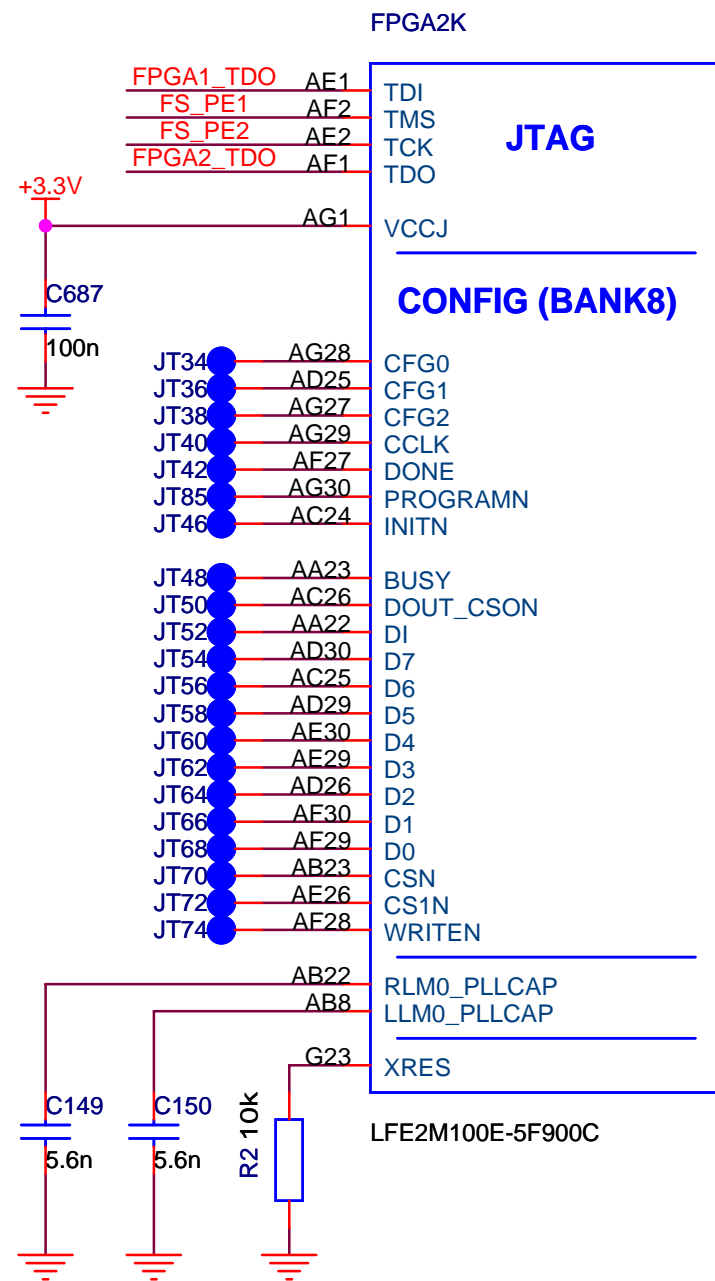
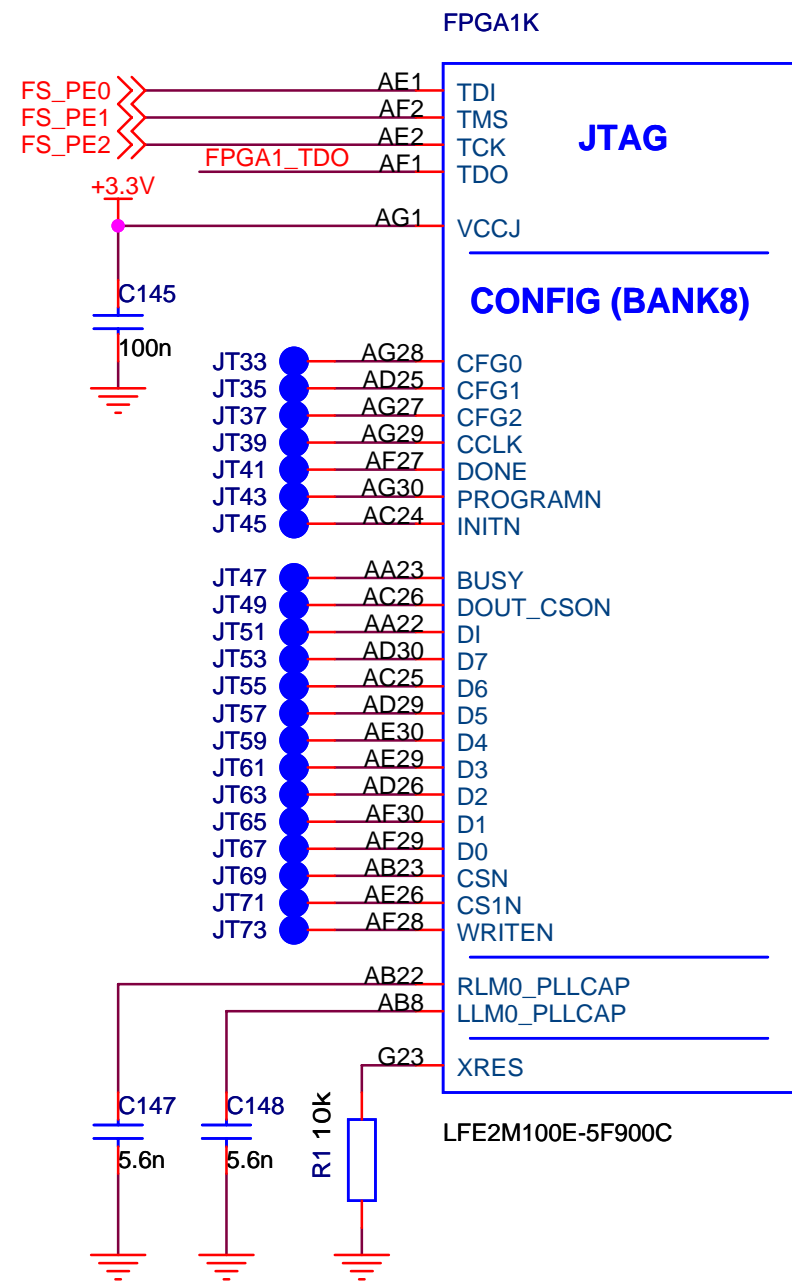
OUT_TO_F1_5	H4	27A (PCLKT6_0)	2A	OUT_TO_F2_7
OUT_TO_F1B_5	H5	27B (PCLKC6_0)	2B	OUT_TO_F2B_7
F1_TO_OUT6	J4	28A (VREF2)	3A	F1_TO_OUT1
F1_TO_OUTB6	K4	28B (VREF1)	3B	F1_TO_OUTB1
OUT_TO_F1_6	J6	31A (LLM2_SPLLT_IN)	4A	OUT_TO_F2_8
OUT_TO_F1B_6	J5	31B (LLM2_SPLLC_IN)	4B	OUT_TO_F2B_8
F1_TO_OUT7	K3	32A (LLM2_SPLLT_FB)	5A	F1_TO_OUT0
F1_TO_OUTB7	K2	32B (LLM2_SPLLC_FB)	5B	F1_TO_OUTB0
OUT_TO_F1_7	L1	42A (LLM0_GPLLT_IN)	6A (LDQS6)	OUT_TO_F1_0
OUT_TO_F1B_7	L2	42B (LLM0_GPLLC_IN)	6B	OUT_TO_F1B_0
F1_TO_OUT8	L3	43A (LLM0_GPLLT_FB)	7A	F1_TO_OUT2
F1_TO_OUTB8	L4	43B (LLM0_GPLLC_FB)	7B	F1_TO_OUTB2
OUT_TO_F1_8	M1	44A (LLM0_GDLLT_IN)	8A	OUT_TO_F1B_1
OUT_TO_F1B_8	N1	44B (LLM0_GDLLC_IN)	8B	OUT_TO_F1B_1
F2_TO_OUT8	N2	45A (LLM0_GDLLT_FB)	9A (VREF2)	F1_TO_OUT3
F2_TO_OUTB8	N3	45B (LLM0_GDLLC_FB)	9B (VREF1)	F1_TO_OUTB3
			11A (LUM0_SPLLT_IN)	OUT_TO_F1_2
			11B (LUM0_SPLLC_IN)	OUT_TO_F1B_2
			12A (LUM0_SPLLT_FB)	F1_TO_OUT4
			12B (LUM0_SPLLC_FB)	F1_TO_OUTB4
			13A	OUT_TO_F1_3
			13B	OUT_TO_F1B_3
			14A	F1_TO_OUT5
			14B	F1_TO_OUTB5
			24A	OUT_TO_F1_4
			24B	OUT_TO_F1B_4
			J2	
			K1	FCLK3
				FCLKb3

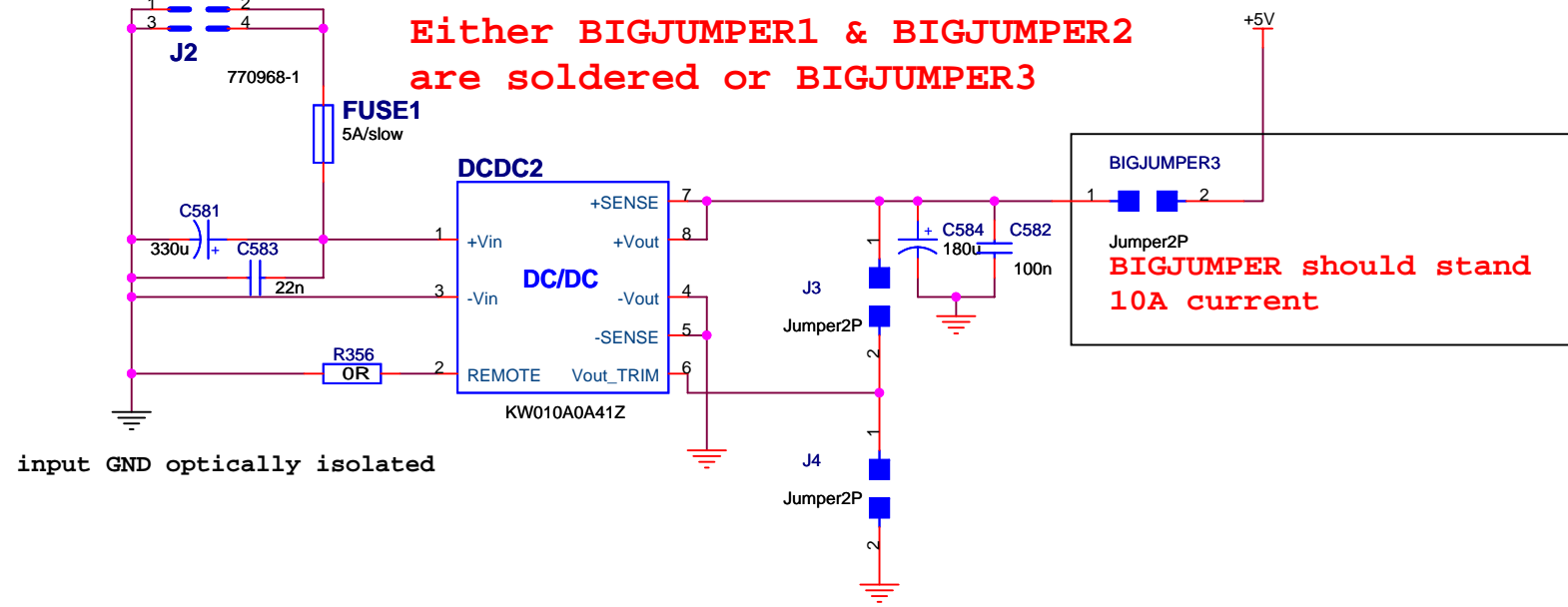
F2_TO_OUT0	B16	9A (VREF1)	J12	OUT_TO_F2_2
F2_TO_OUTB0	C16	9B (VREF2)	J11	OUT_TO_F2B_2
OUT_TO_F2_0	D15	11A (RUM0_SPLLT_IN)	G15	F2_TO_OUT2
OUT_TO_F2B_0	D16	11B (RUM0_SPLLC_IN)	E16	F2_TO_OUTB2
F2_TO_OUT1	E11	12A (RUM0_SPLLT_FB)	E15	OUT_TO_F2_3
F2_TO_OUTB1	E12	12B (RUM0_SPLLC_FB)	H15	OUT_TO_F2B_3
OUT_TO_F2_1	E13	13A	G16	F2_TO_OUT5
OUT_TO_F2B_1	E14	13B	H15	F2_TO_OUTB5
F2_TO_OUT4	G11	14A	H12	OUT_TO_F2_5
F2_TO_OUTB4	H11	14B	H13	OUT_TO_F2B_5
OUT_TO_F2_4	F13	24A	J13	F2_TO_OUT6
OUT_TO_F2B_4	F14	24B	J14	F2_TO_OUTB6
F2_TO_OUT3	G13	25A (PCLKT2_0)	J15	OUT_TO_F2_6
F2_TO_OUTB3	G14	25B (PCLKC2_0)	H16	OUT_TO_F2B_6
			J16	F2_TO_OUT7
			K15	F2_TO_OUTB7

F2_TO_OUT0	100R	R395	F2_TO_OUTB0
F2_TO_OUT1	100R	R396	F2_TO_OUTB1
F2_TO_OUT2	100R	R397	F2_TO_OUTB2
F2_TO_OUT3	100R	R398	F2_TO_OUTB3
F2_TO_OUT4	100R	R399	F2_TO_OUTB4
F2_TO_OUT5	100R	R400	F2_TO_OUTB5
F2_TO_OUT6	100R	R401	F2_TO_OUTB6
F2_TO_OUT7	100R	R402	F2_TO_OUTB7
F2_TO_OUT8	100R	R403	F2_TO_OUTB8

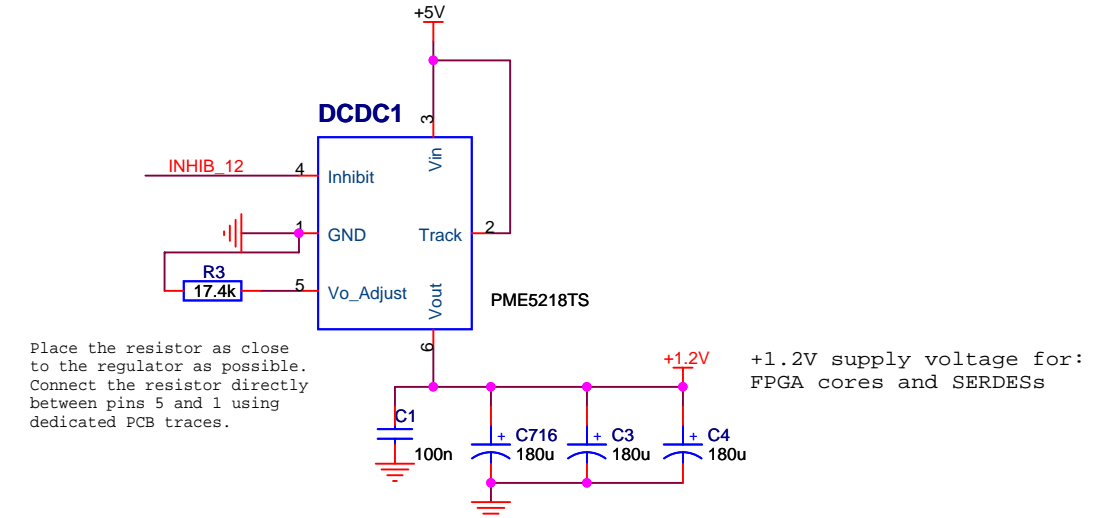
F1_OUT_TTL[8..0] >>>
F2_OUT_TTL[11..0] >>>

F1_OUT_TTL0	T7	22A (PCLKT4_0)	M5	JT87
F1_OUT_TTL1	T8	22B (PCLKC4_0)	N5	JT90
F1_OUT_TTL2	L7	23A	L6	
F1_OUT_TTL3	L8	23B	M6	SFP1_TX_FAULT
F1_OUT_TTL4	P8	29A	P3	SFP1_TX_DIS
F1_OUT_TTL5	N8	29B	P6	SFP1_RATE_SEL
F1_OUT_TTL6	R7	30A	P4	SFP1_MOD0
F1_OUT_TTL7	R8	30B	P2	SFP1_MOD1
F1_OUT_TTL8	N7	31A	P1	SFP1_MOD2
F2_OUT_TTL0	M8	31B	R1	SFP1_LOS
F2_OUT_TTL1	R9	32A	R2	
F2_OUT_TTL2	T9	32B	R3	
F2_OUT_TTL3	T10	33A (BDQS33)	T2	
F2_OUT_TTL4	R10	33B	R4	
F2_OUT_TTL5	N9	34A	T3	
F2_OUT_TTL6	P10	34B	T4	D_FAIL?
F2_OUT_TTL7	L9	47A	T5	DWAIT?
F2_OUT_TTL8	M9	47B	T6	D_OK?
F2_OUT_TTL9	R11	49A	R6	DBUSY?
F2_OUT_TTL10	R11	49B	P6	
F2_OUT_TTL11	T12	50A	P7	JT98
SFP2_TX_FAULT	T13	50B	JT100	
SFP2_TX_DIS	P11	51A (BDQS51)		
SFP2_RATE_SEL	N10	51B		
SFP2_MOD0	T14	52A		
SFP2_MOD1	R13	52B		
SFP2_MOD2	R15	53A		
SFP2_LOS	R16	53B		
	R14	54A		
	P15	54B		
	P16	55A (VREF2)		
	P14	55B (VREF1)		

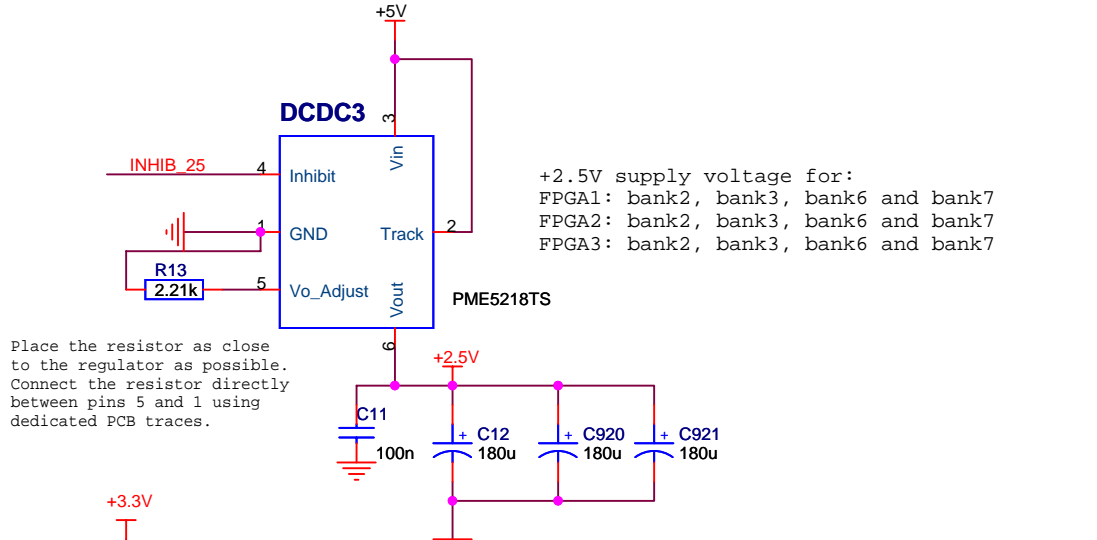




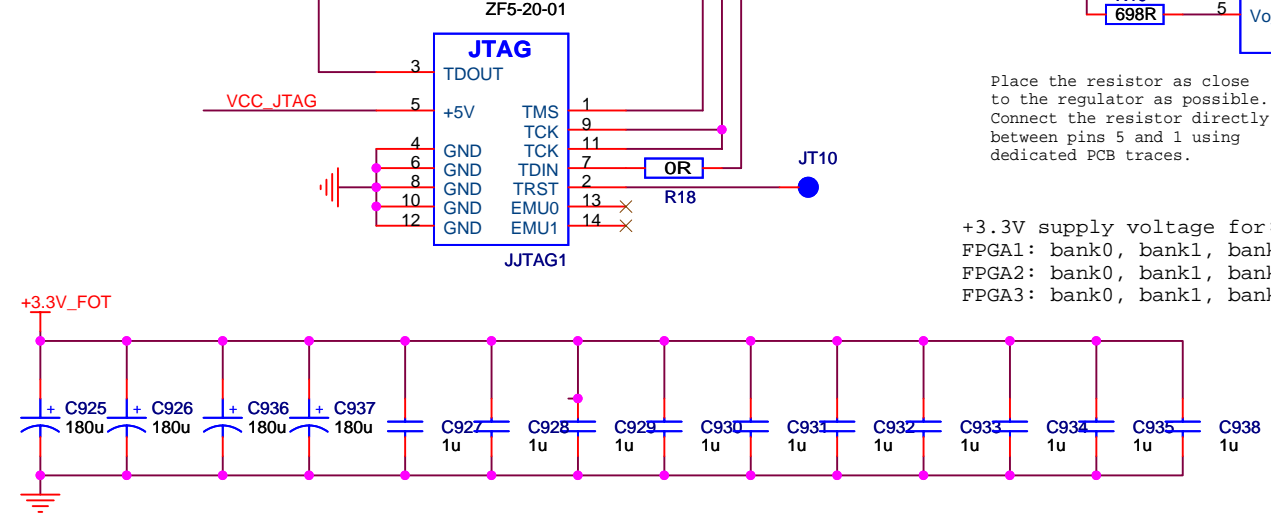
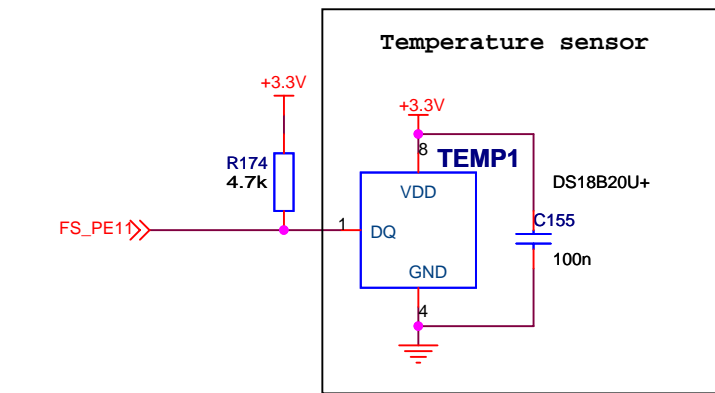
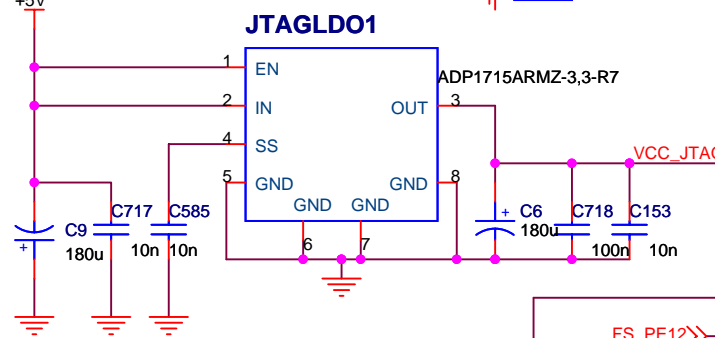
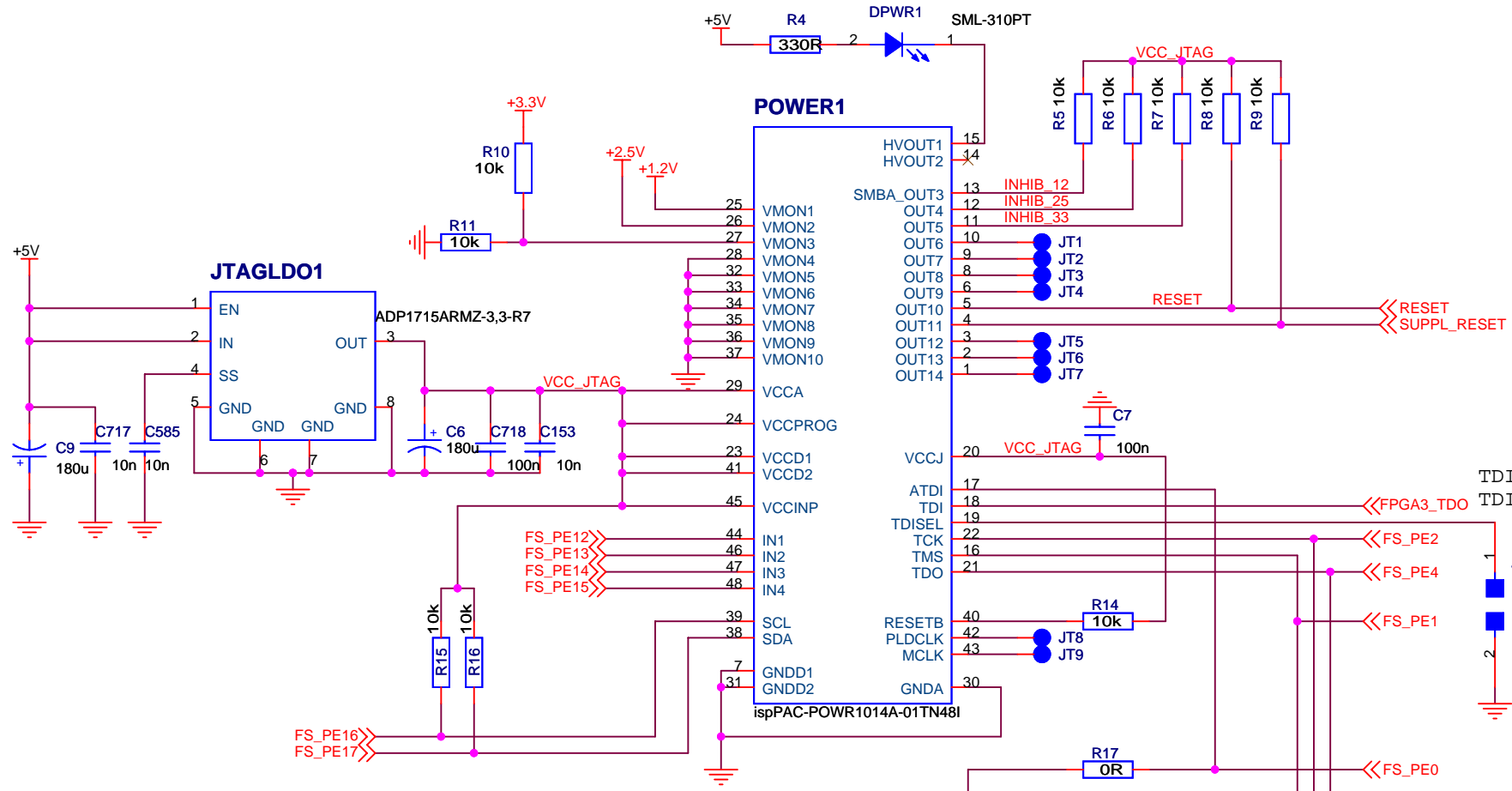
input GND optically isolated



Place the resistor as close to the regulator as possible. Connect the resistor directly between pins 5 and 1 using dedicated PCB traces.



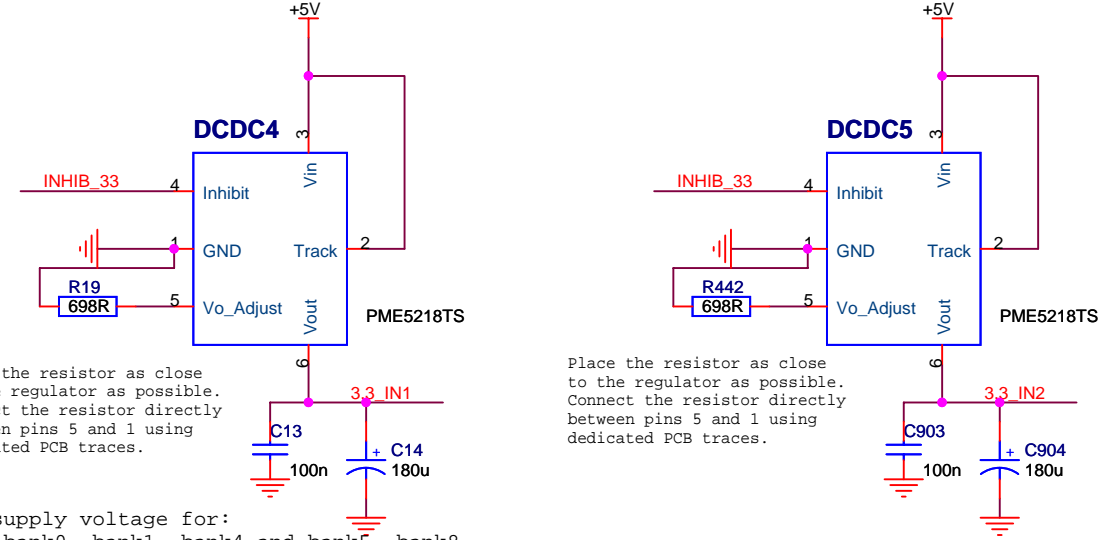
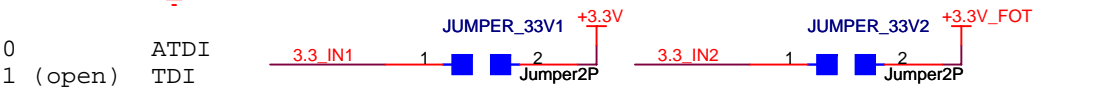
Place the resistor as close to the regulator as possible. Connect the resistor directly between pins 5 and 1 using dedicated PCB traces.



TDISEL = 0; TDISEL = 1 (open)

Place the resistor as close to the regulator as possible. Connect the resistor directly between pins 5 and 1 using dedicated PCB traces.

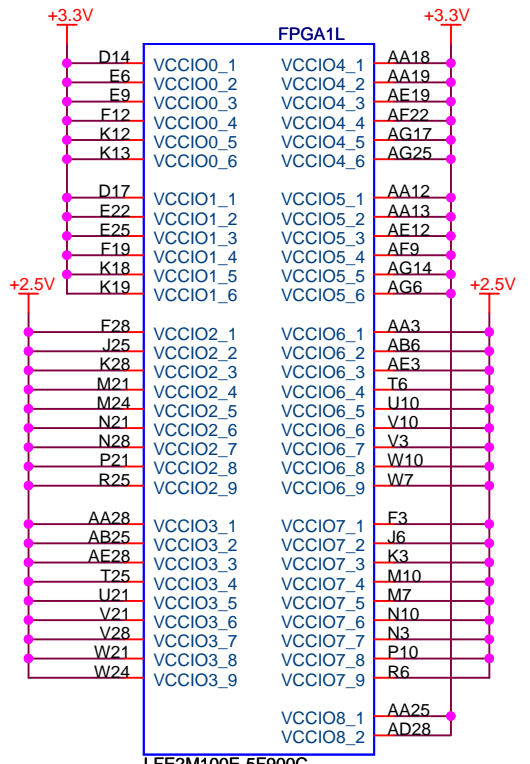
+3.3V supply voltage for: FPGA1: bank0, bank1, bank4 and bank5, bank8; FPGA2: bank0, bank1, bank4 and bank5, bank8; FPGA3: bank0, bank1, bank4 and bank5, bank8



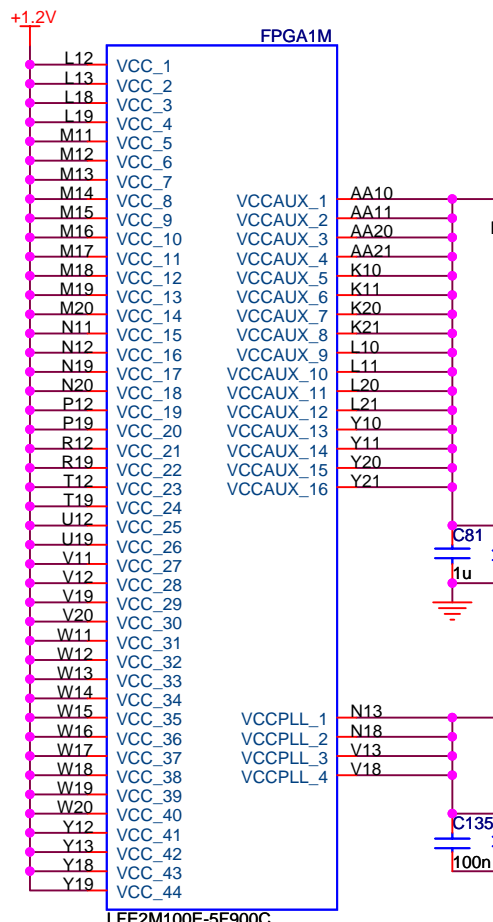
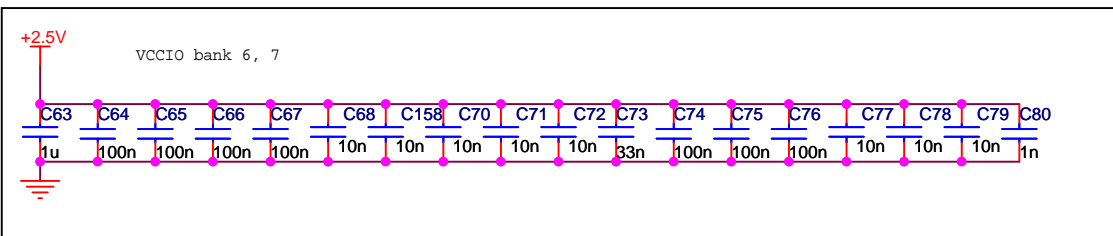
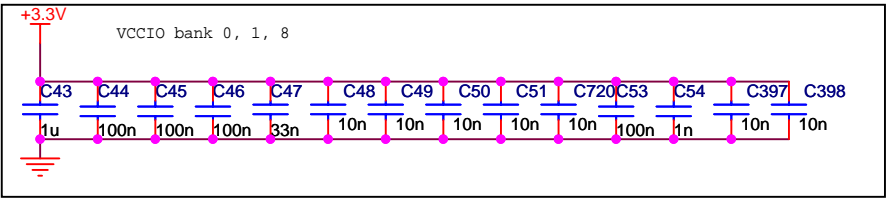
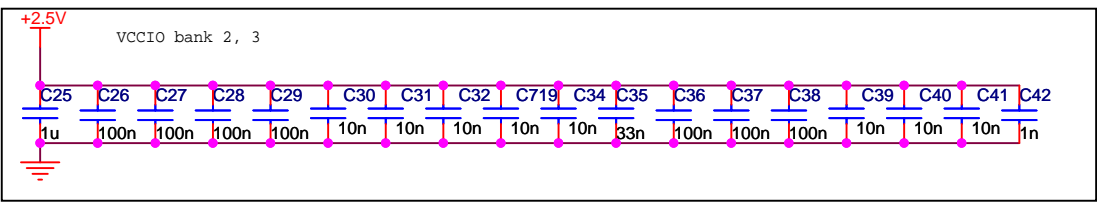
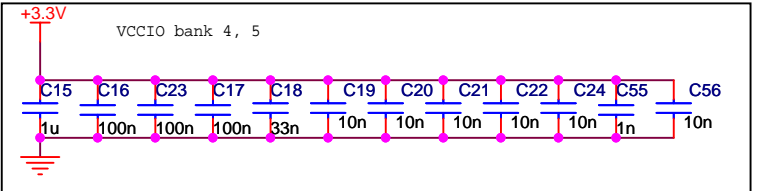
Place the resistor as close to the regulator as possible. Connect the resistor directly between pins 5 and 1 using dedicated PCB traces.

+3.3V_FOT supply voltage for: all FOTs

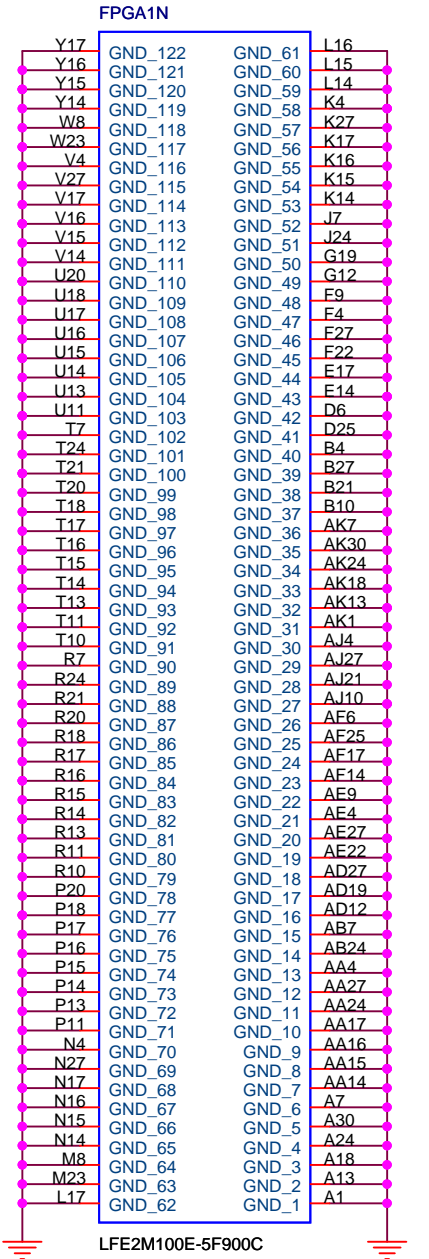
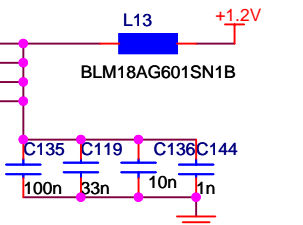
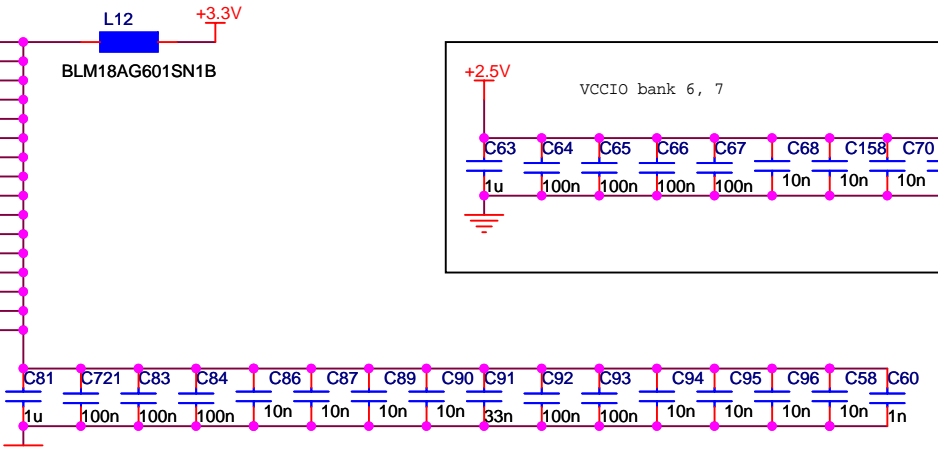
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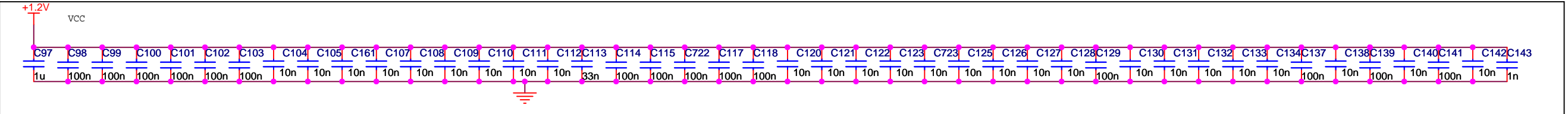
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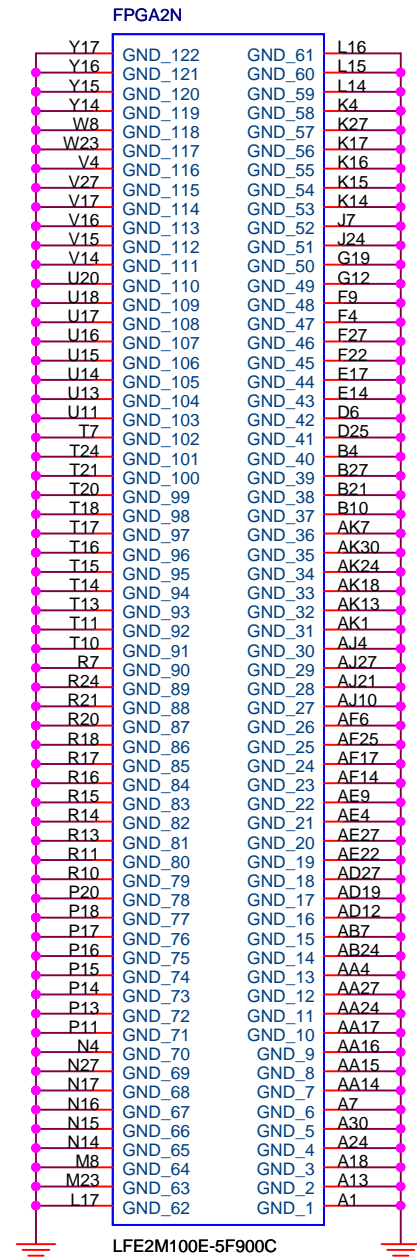
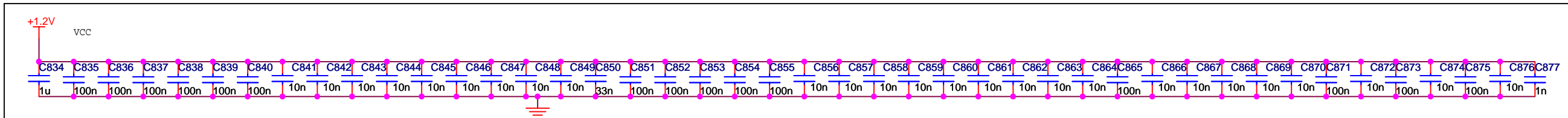
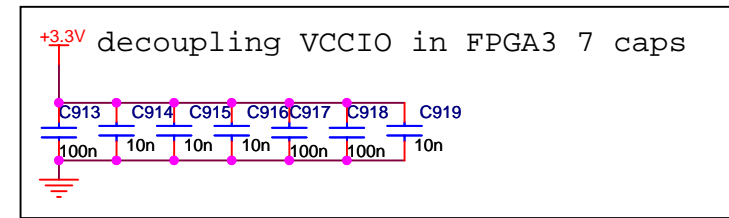
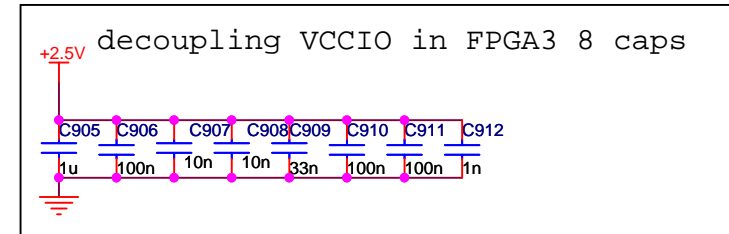
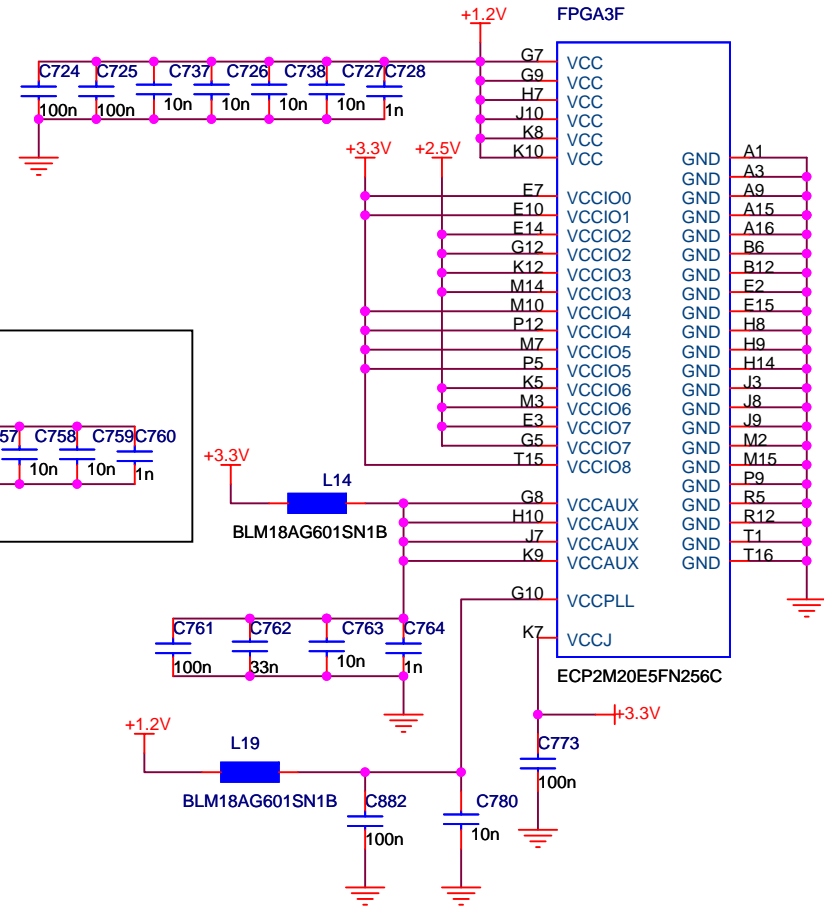
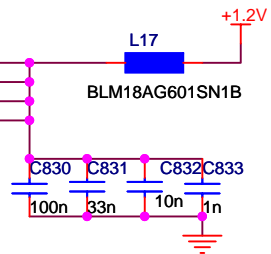
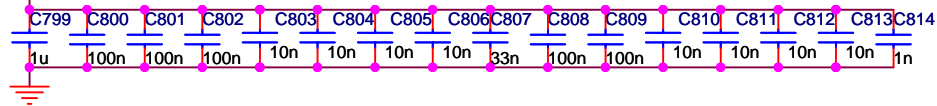
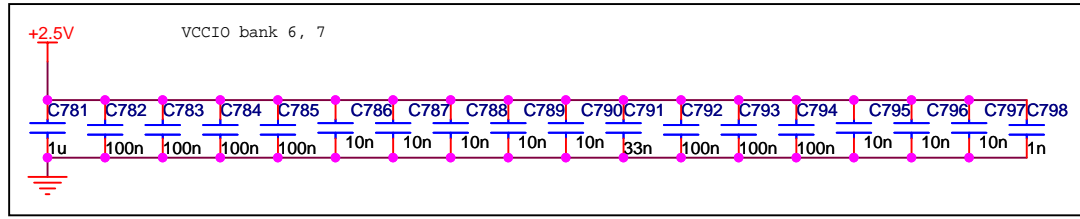
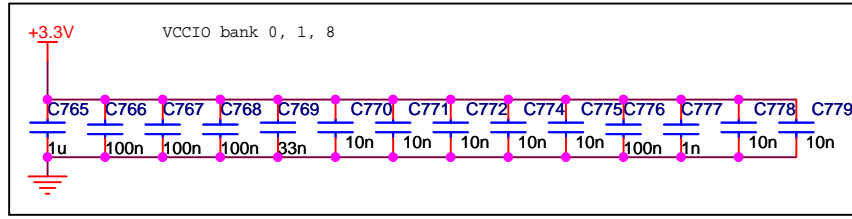
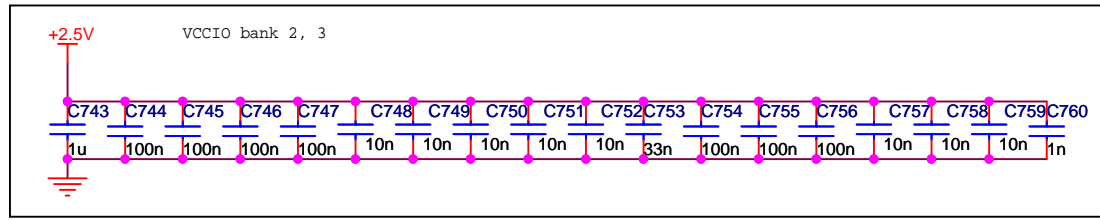
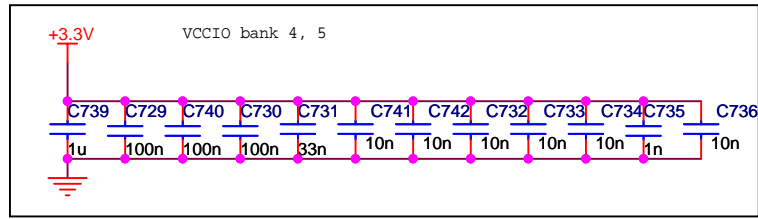
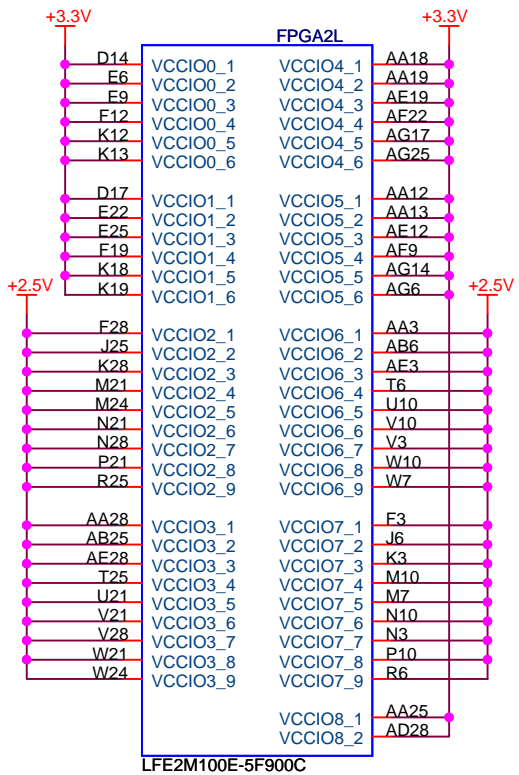


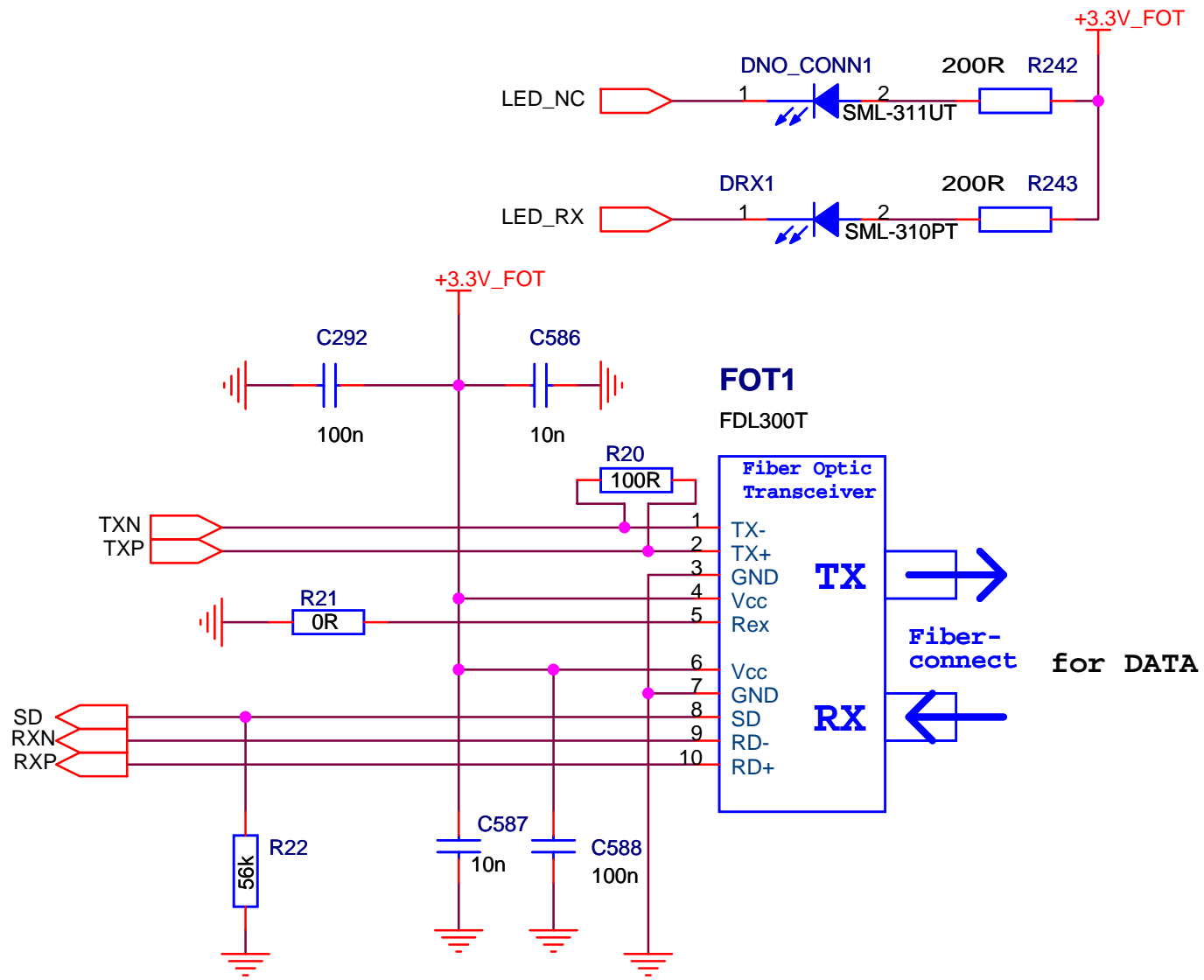
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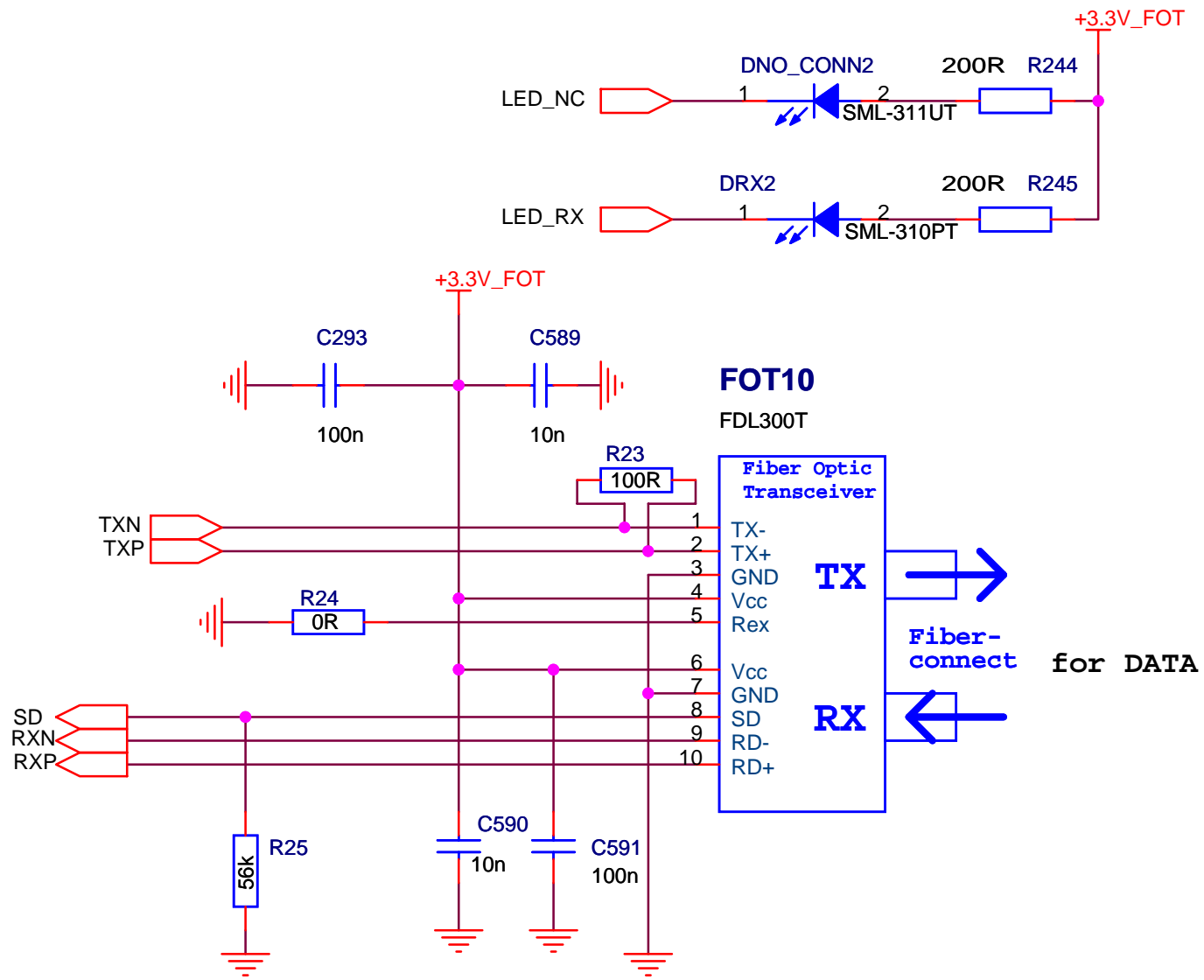
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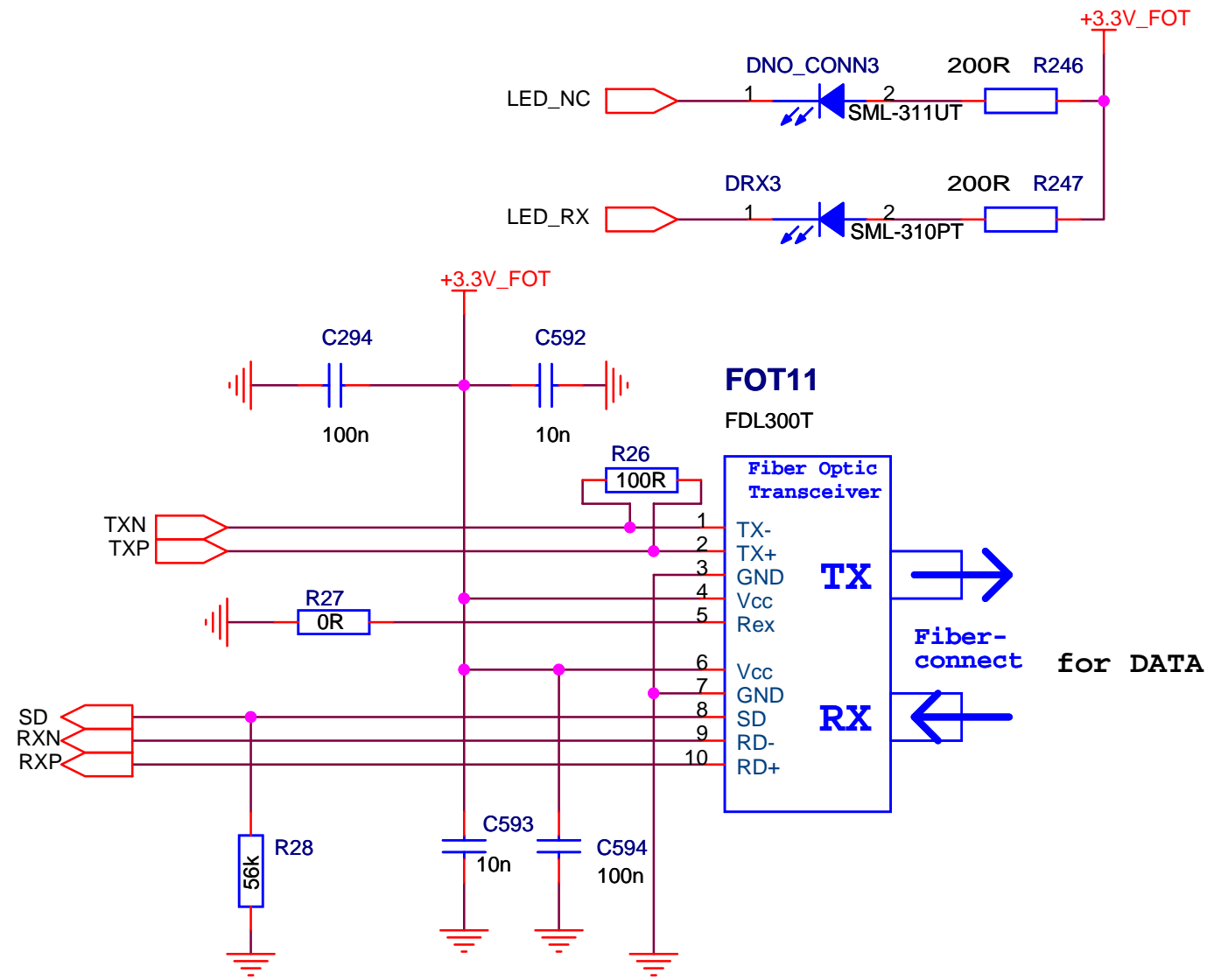




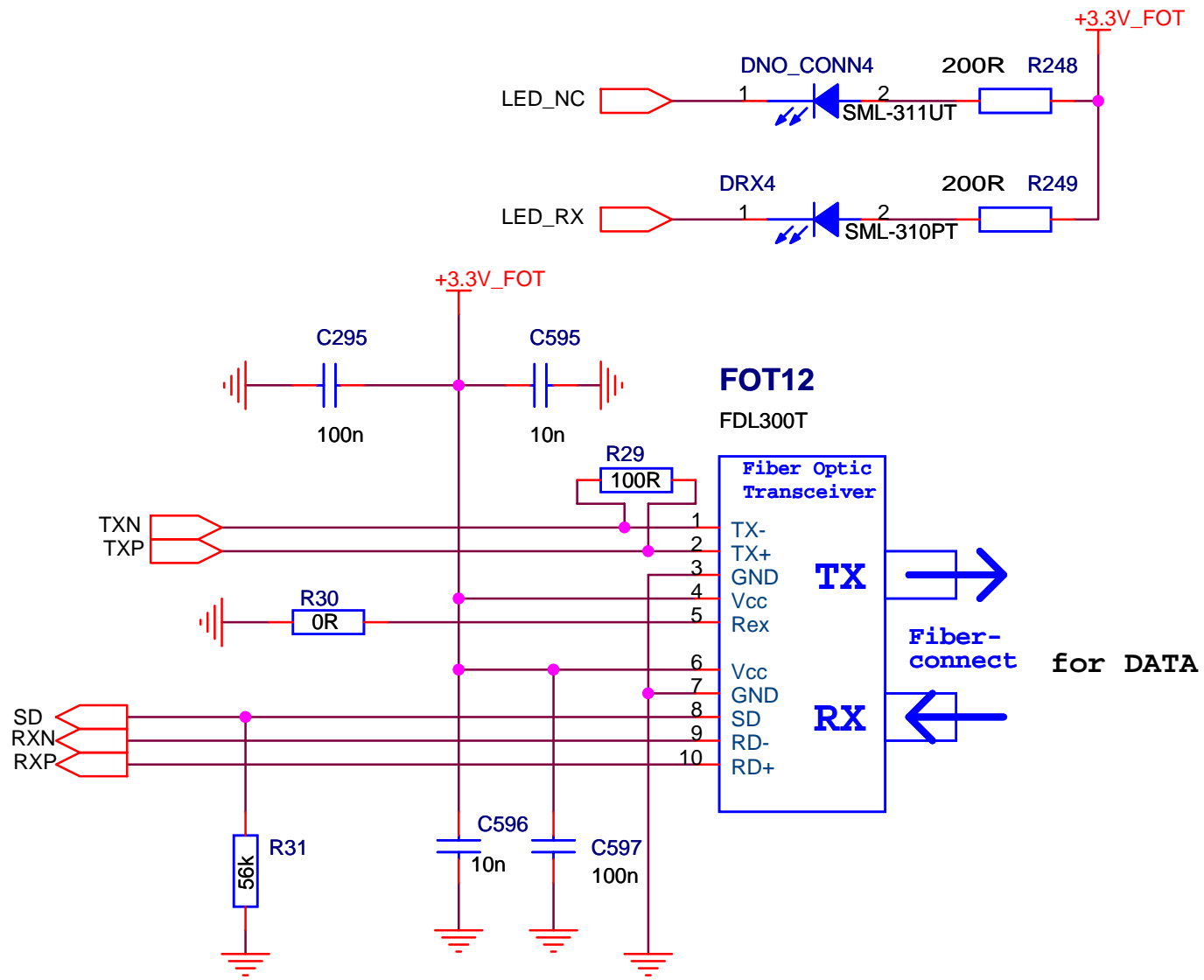
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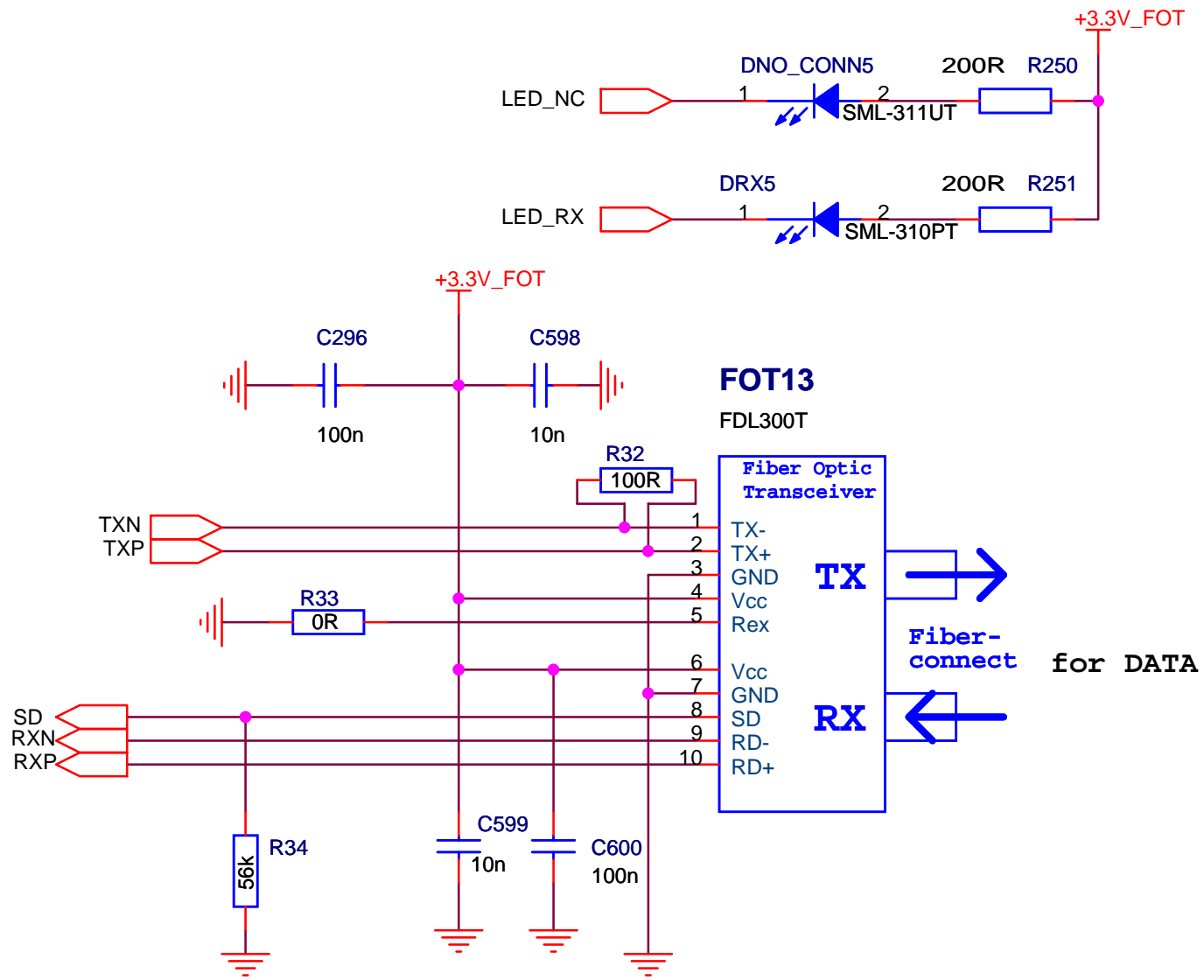
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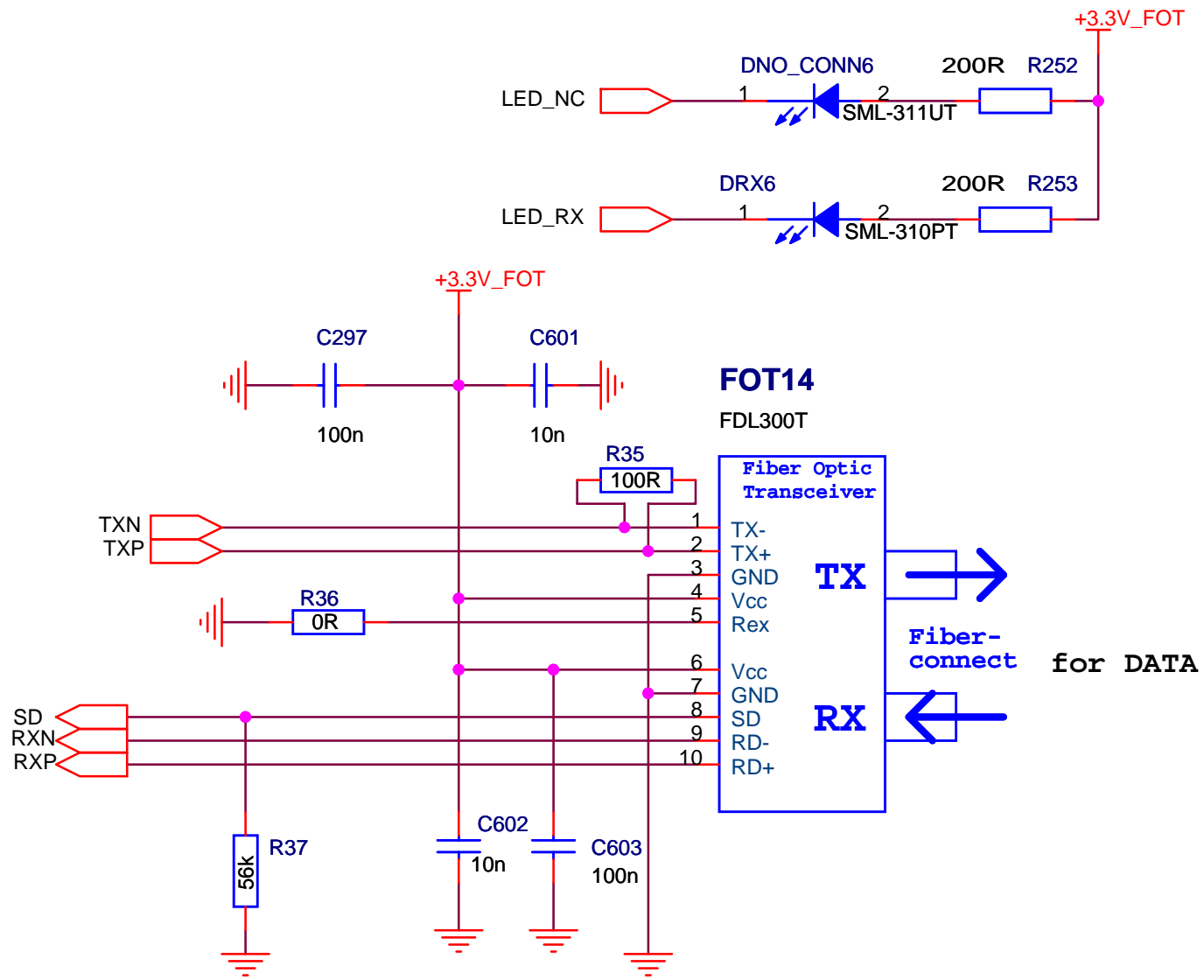
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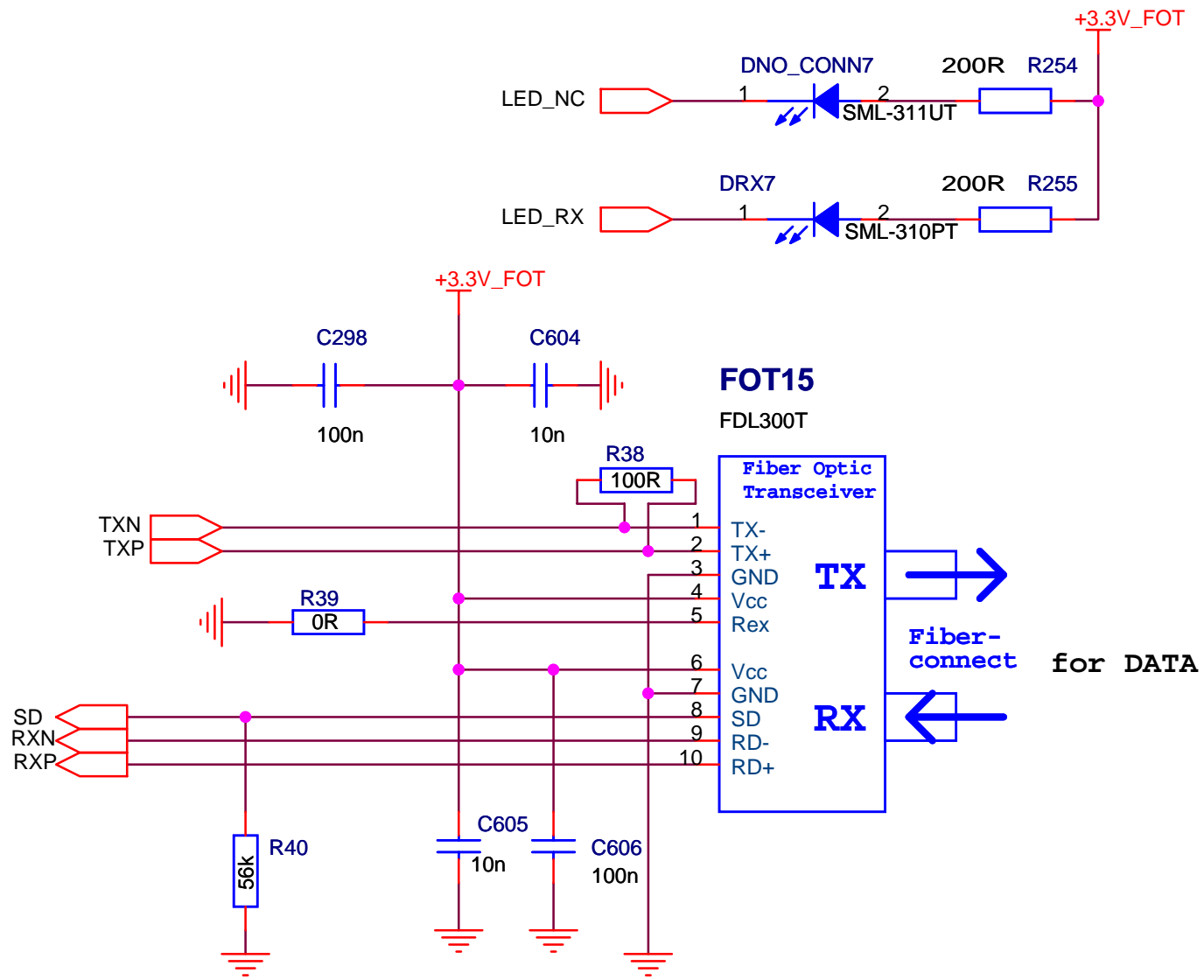
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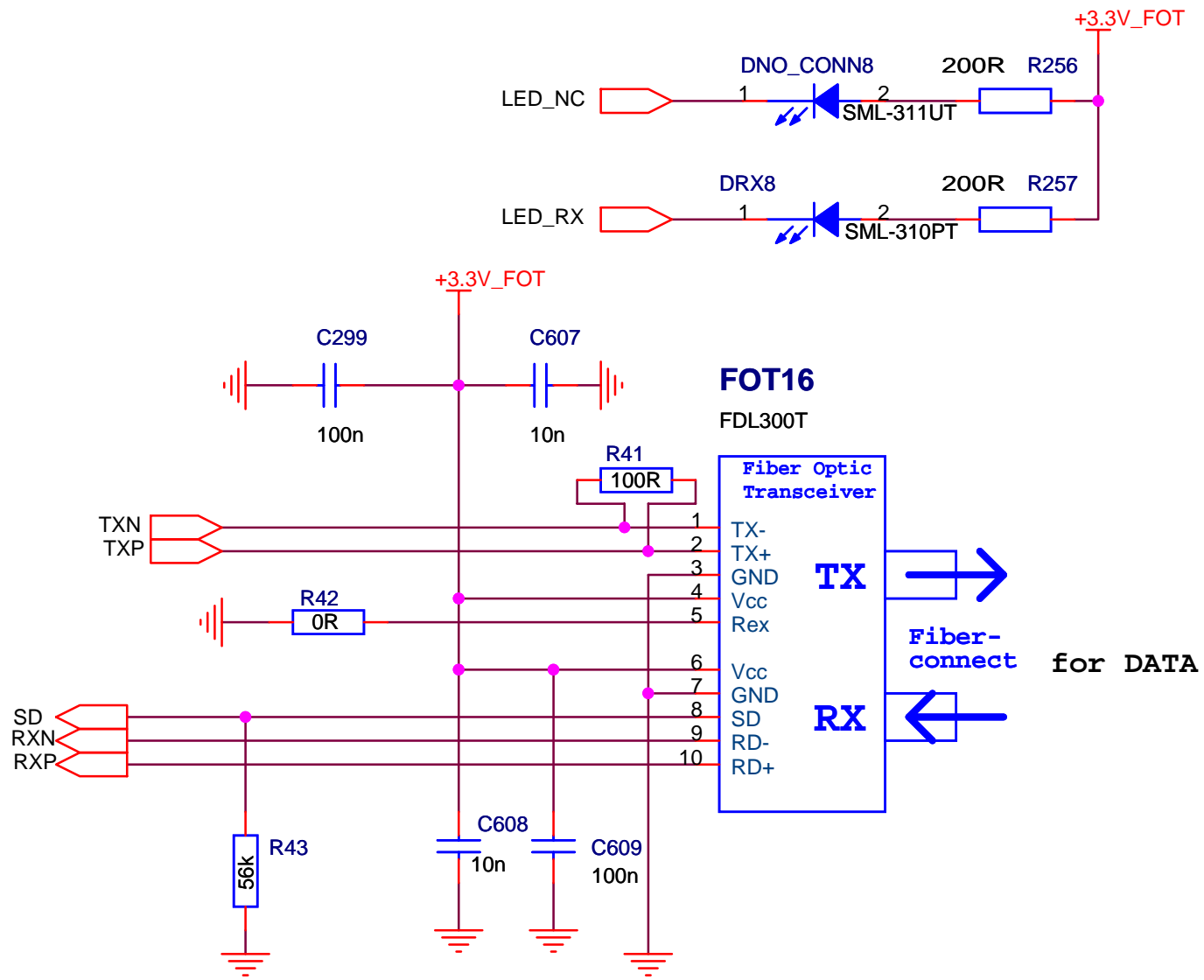
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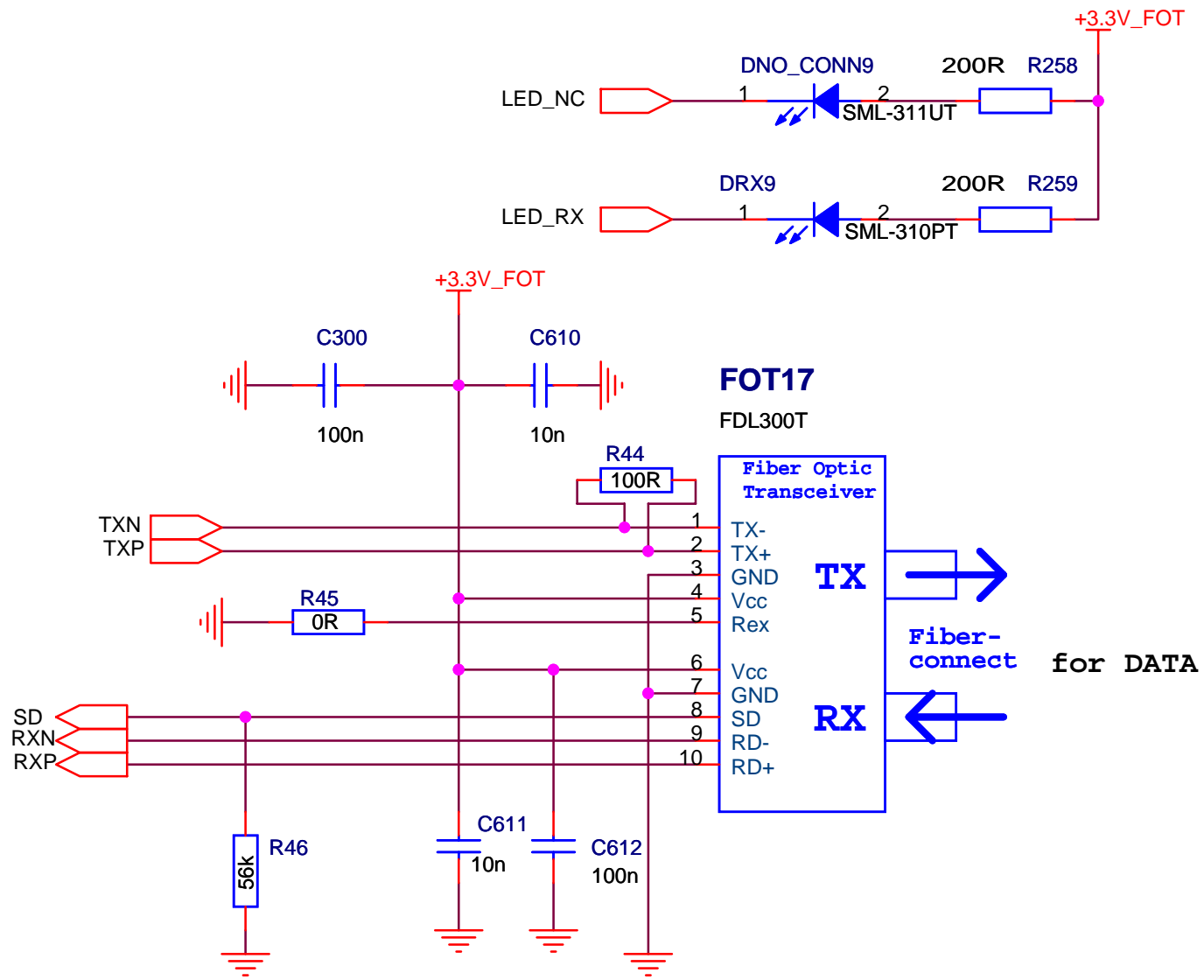
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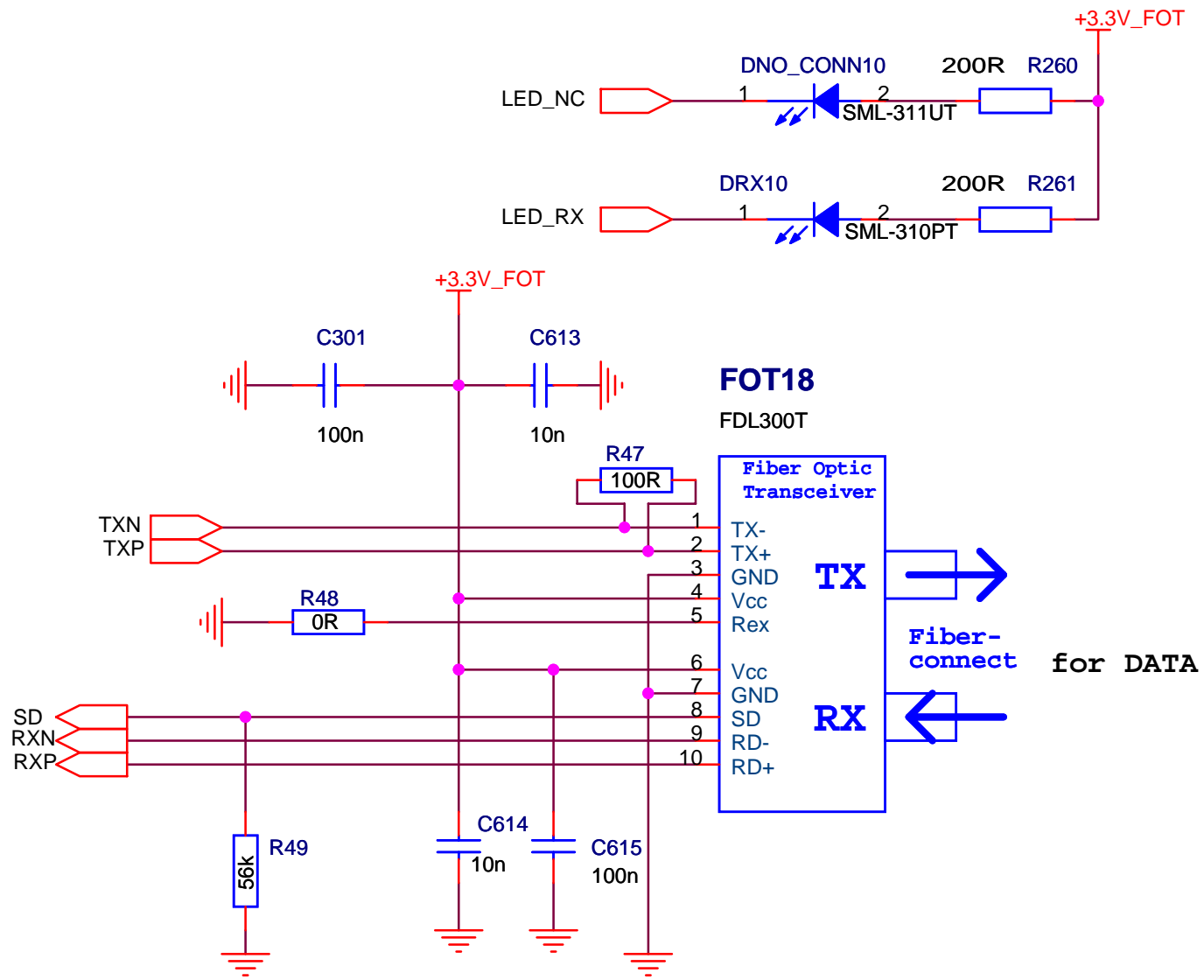
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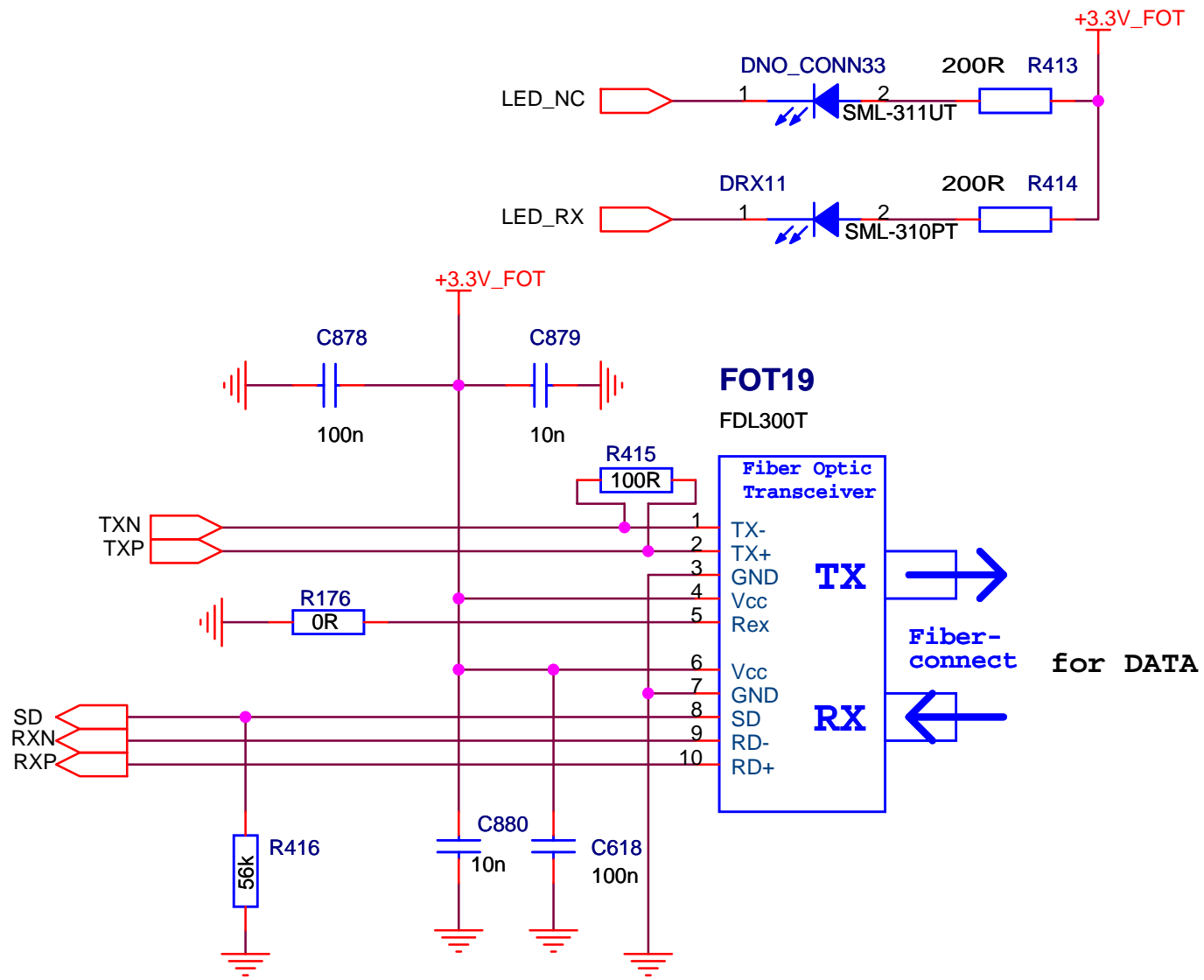
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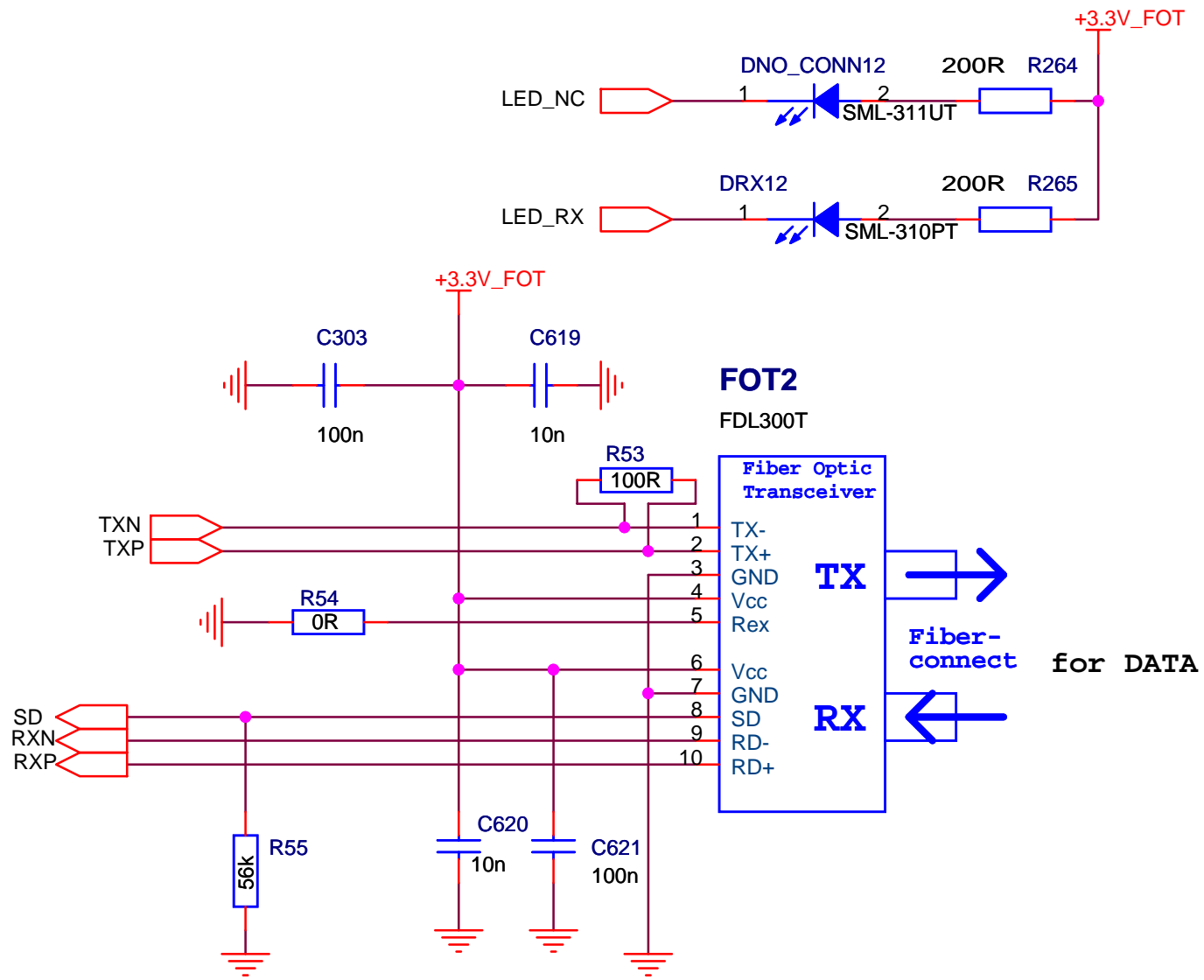
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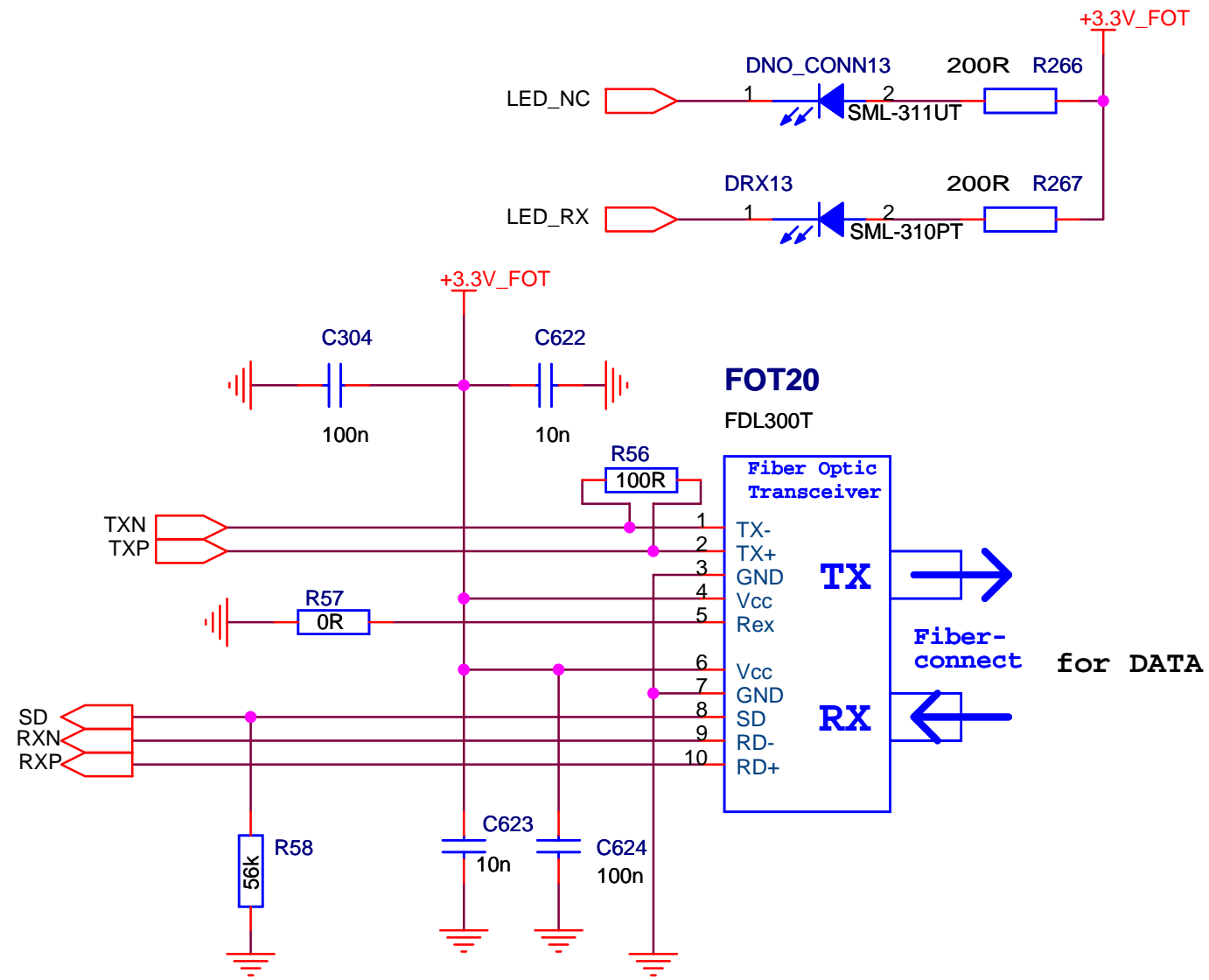
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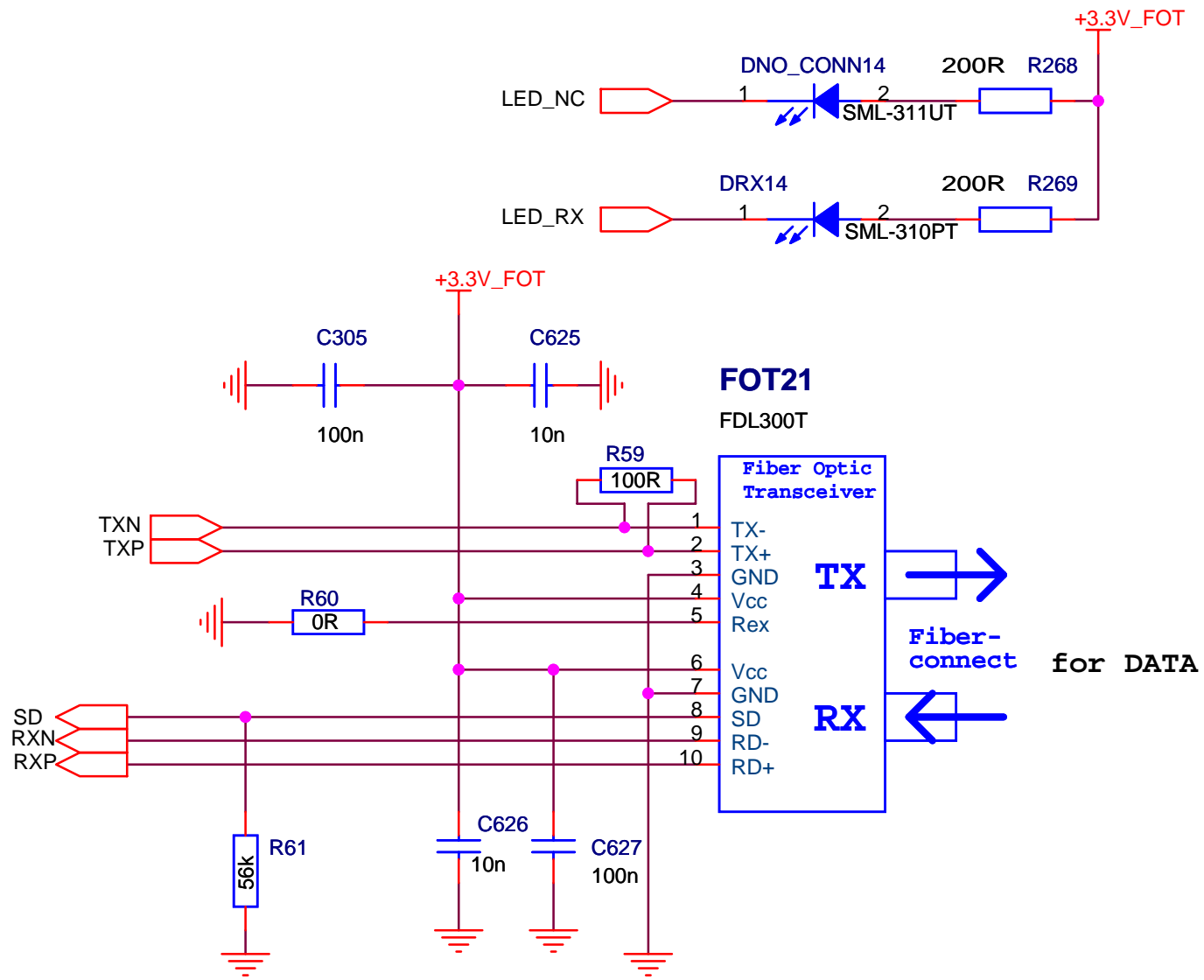
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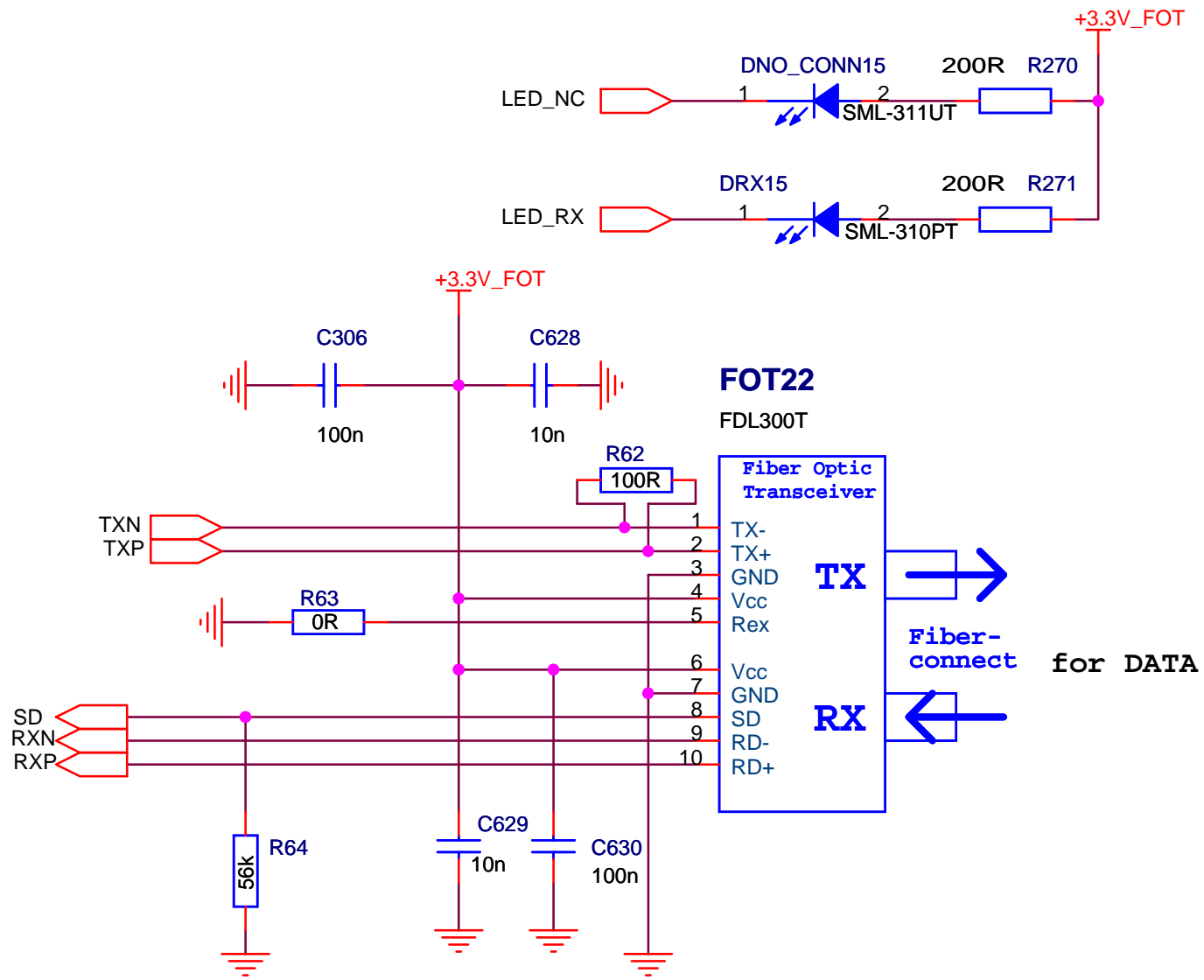
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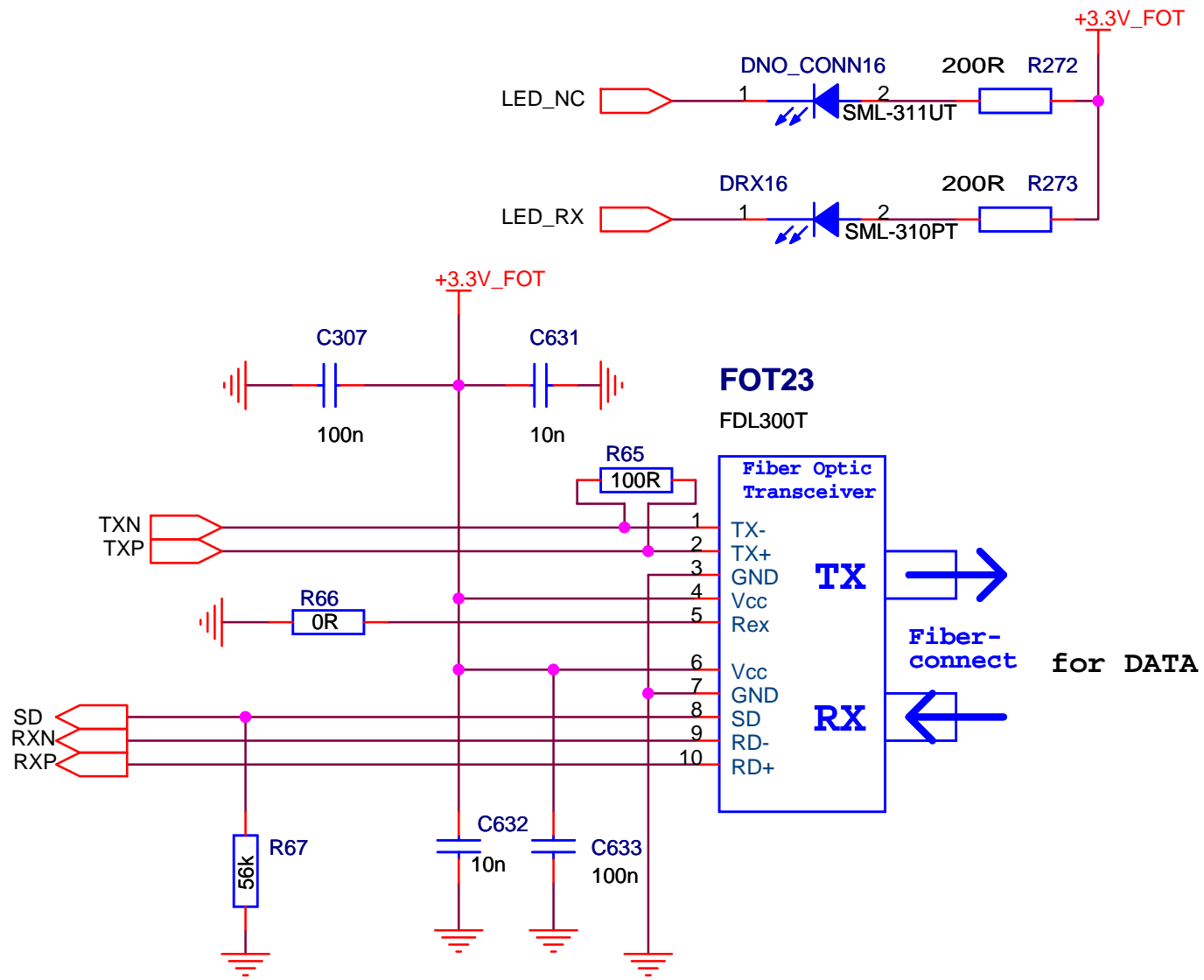
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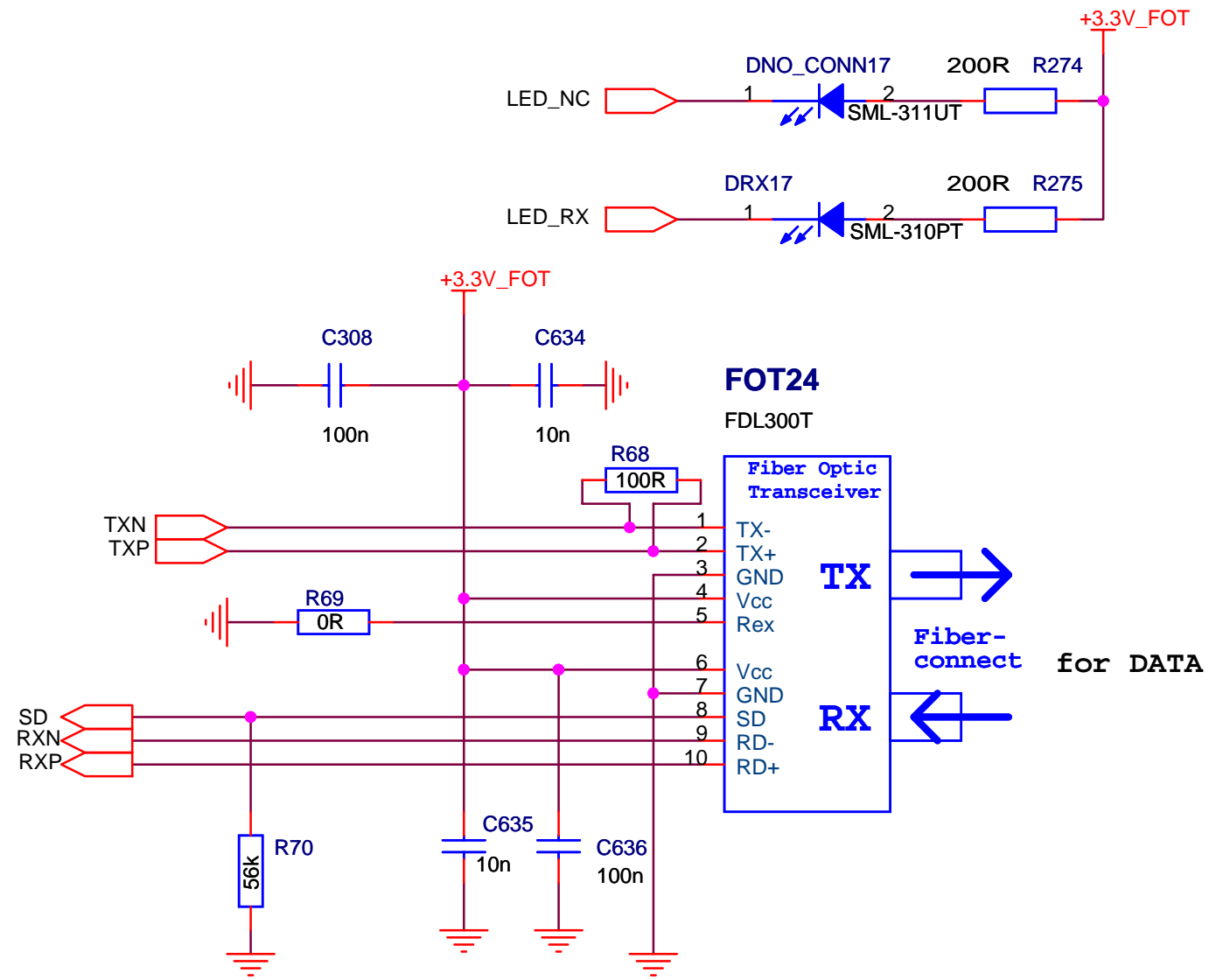
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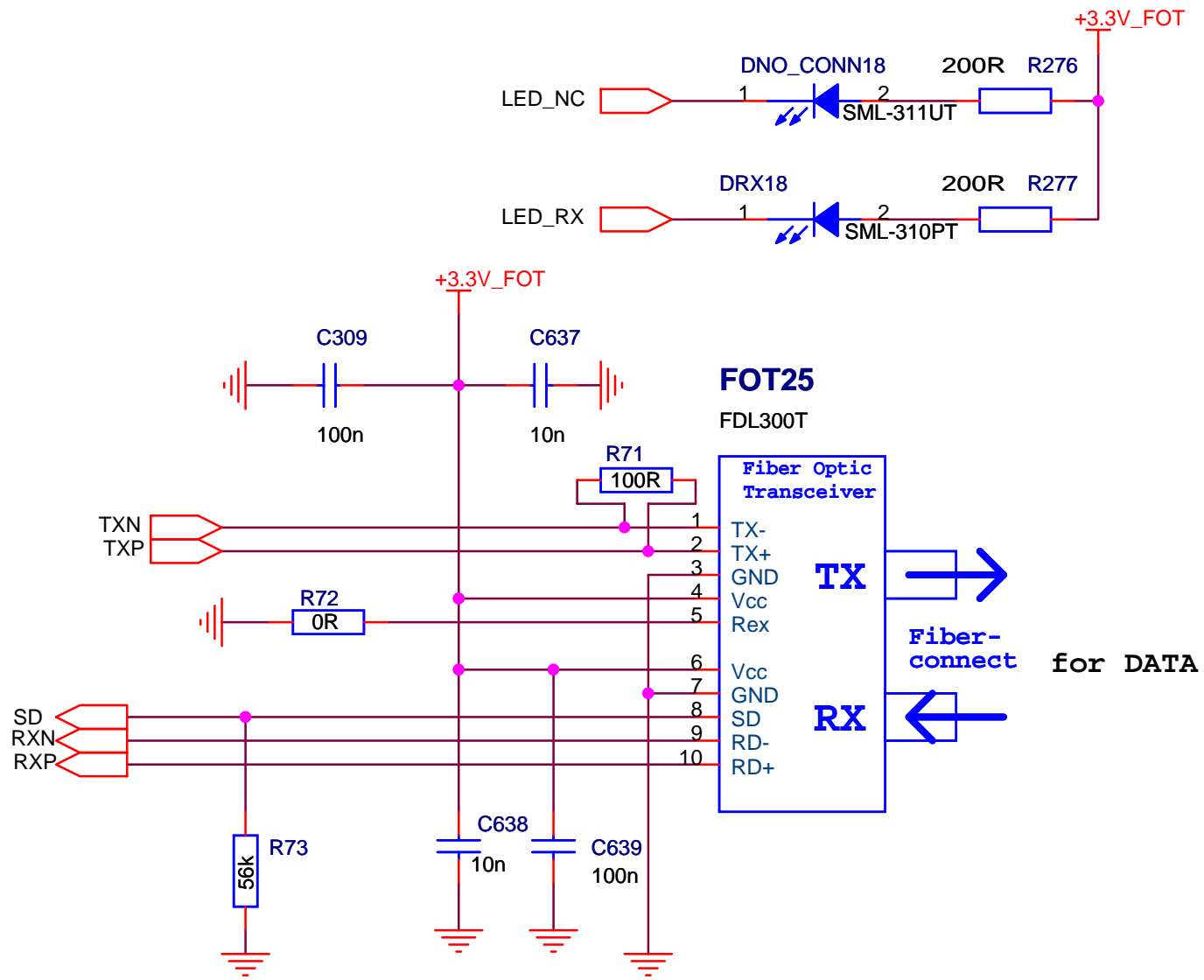
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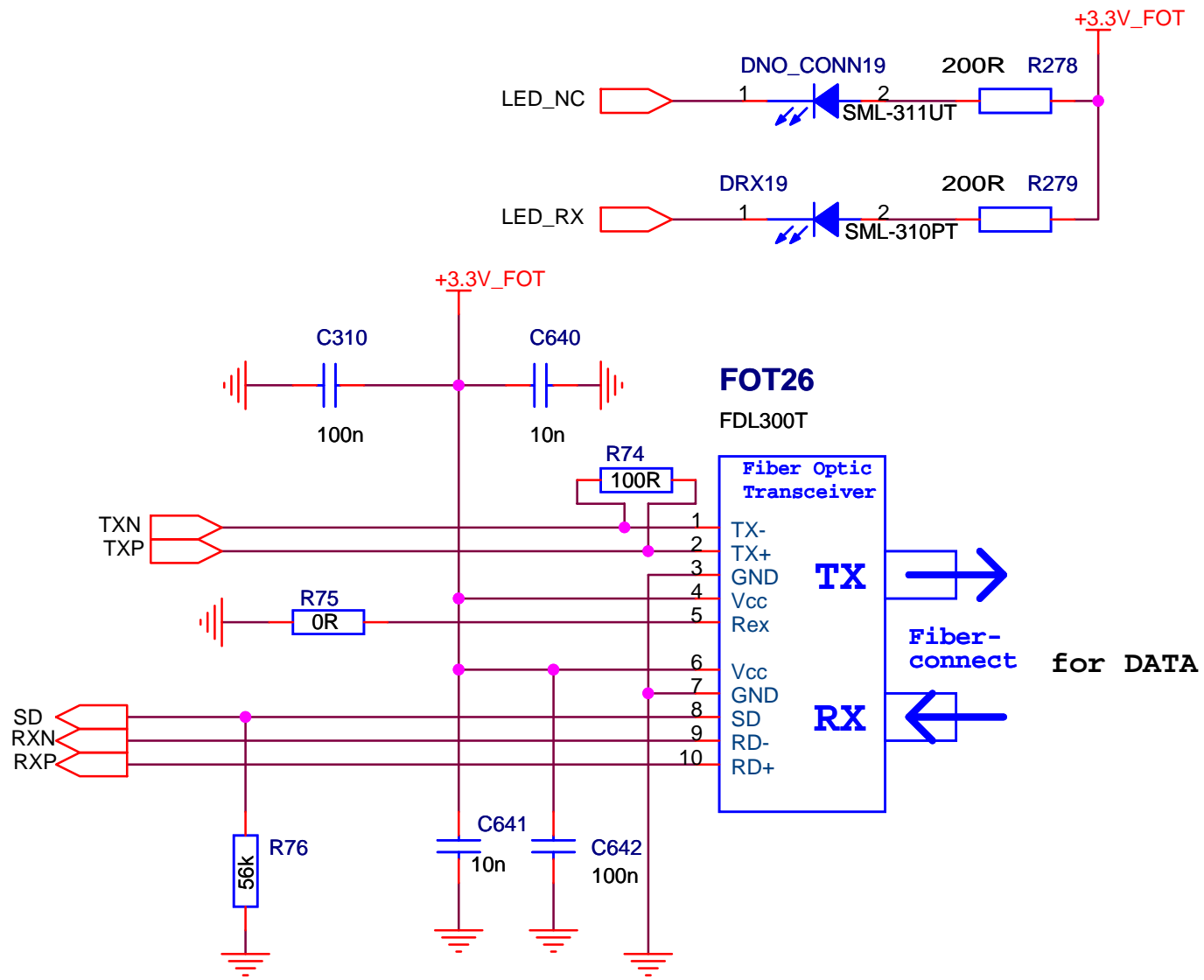
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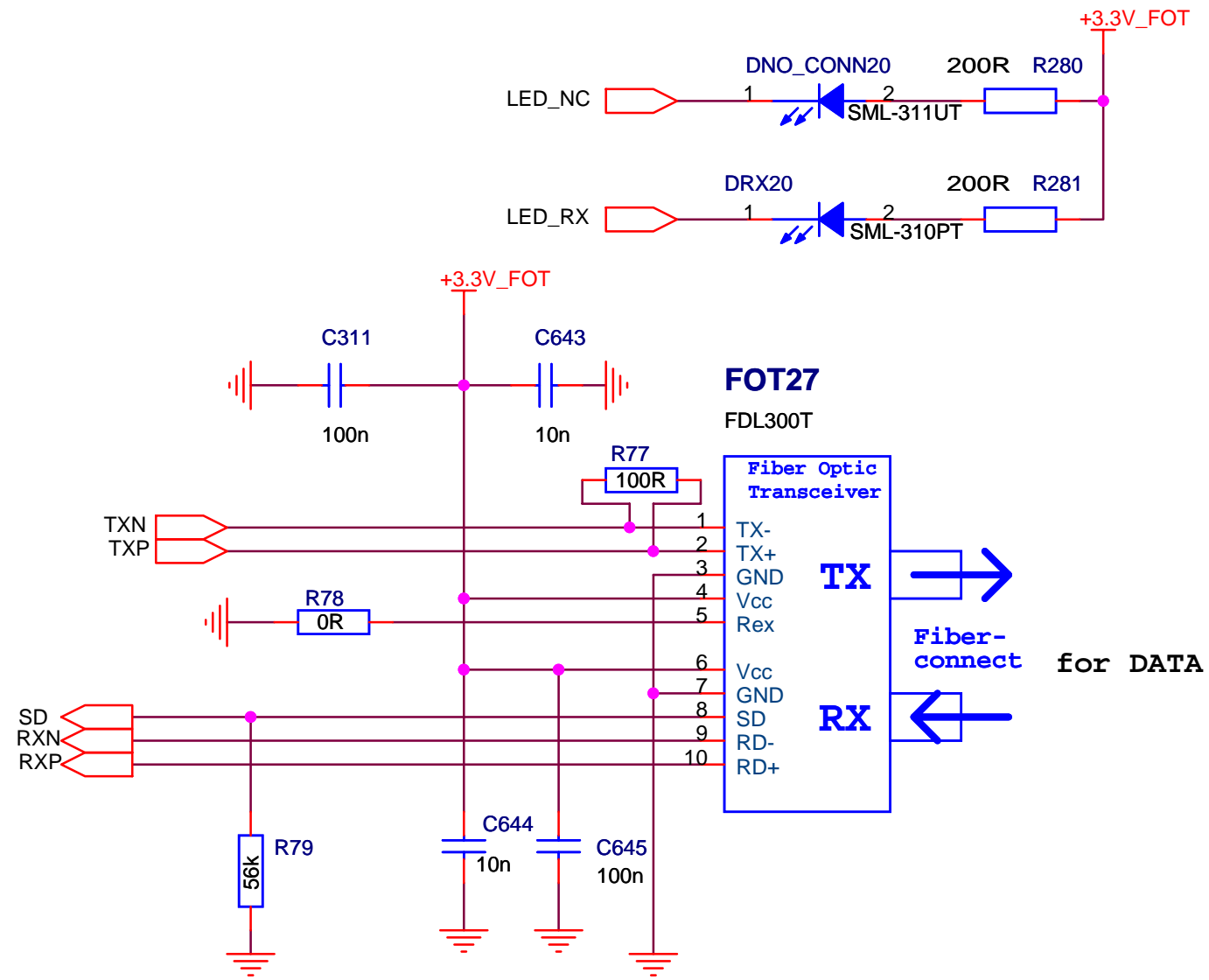
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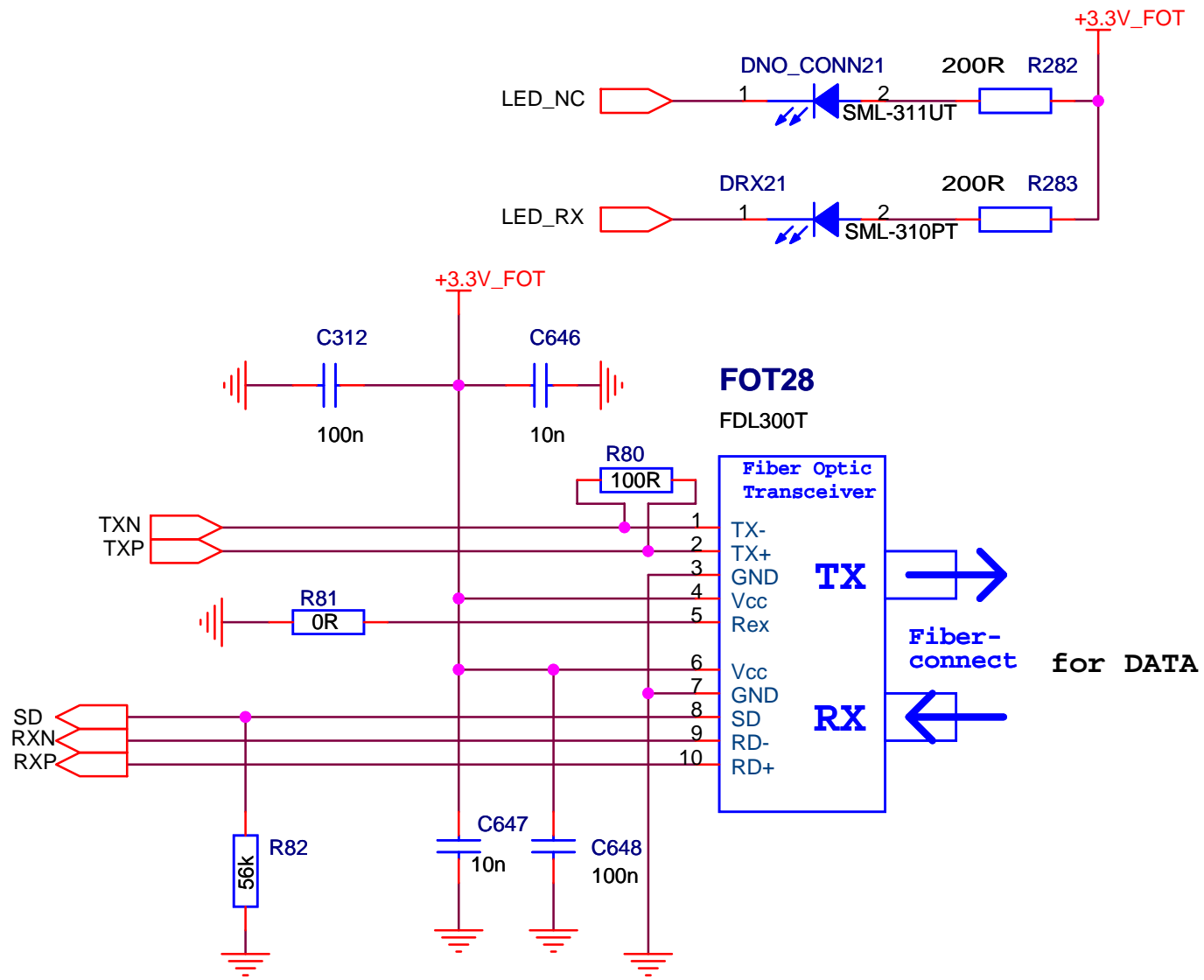
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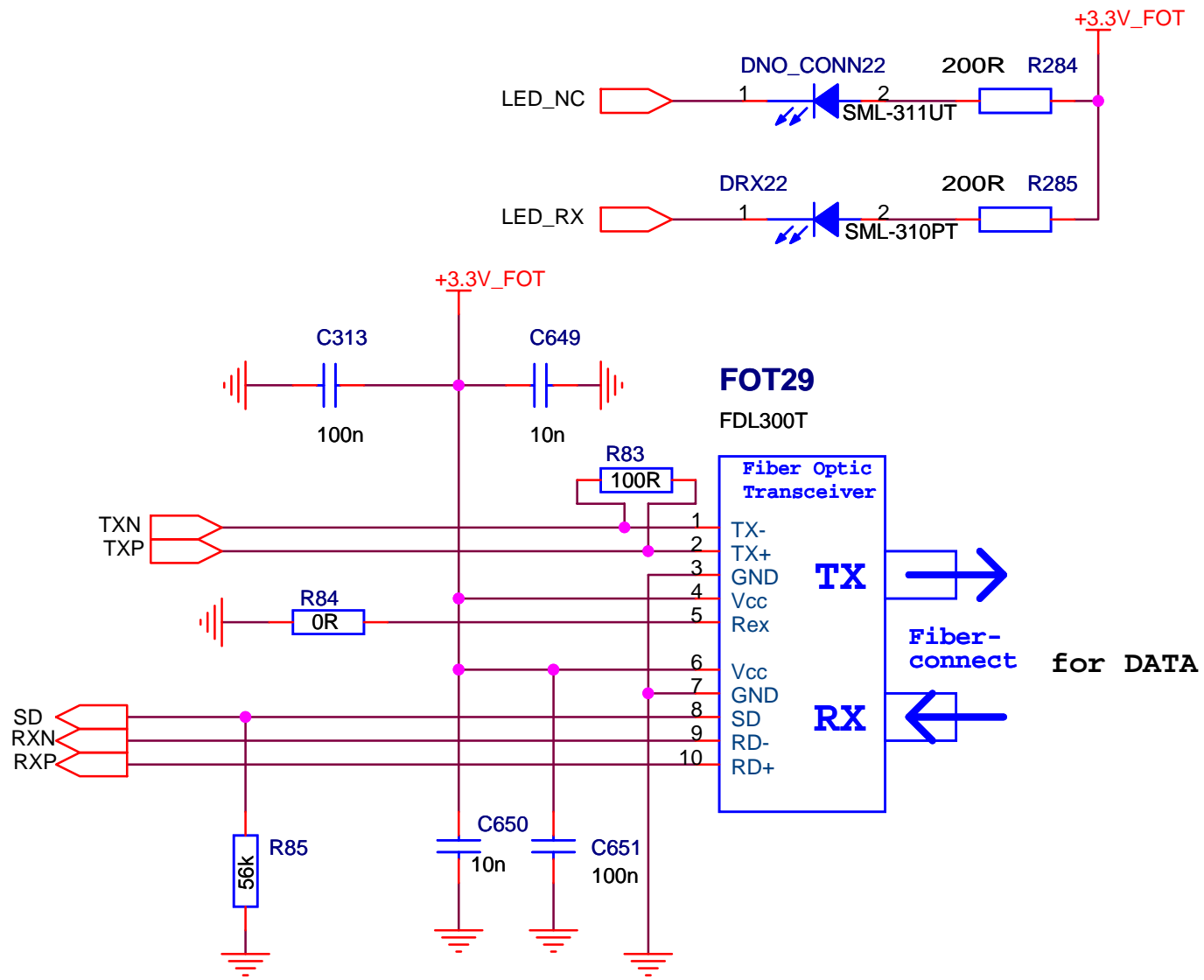
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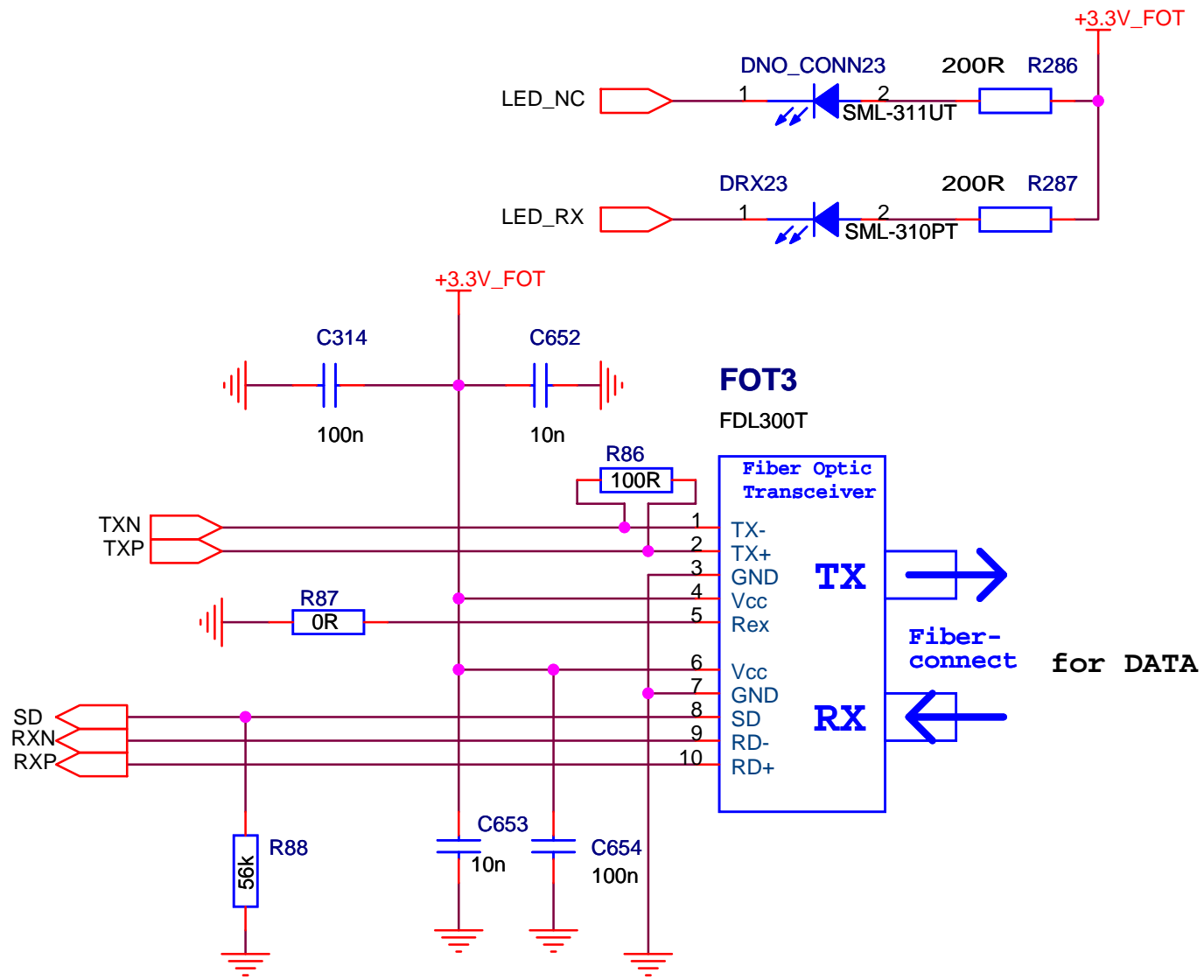
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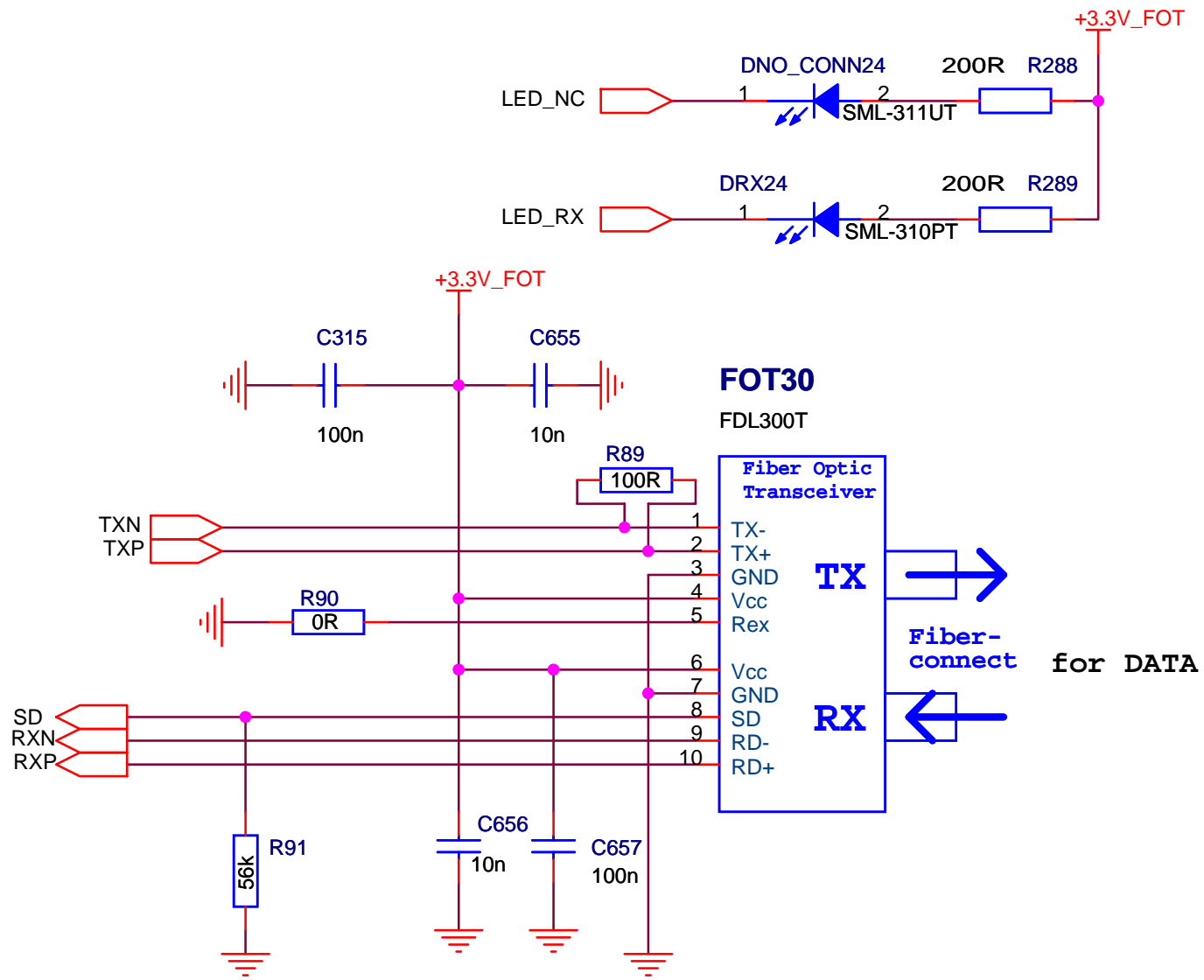
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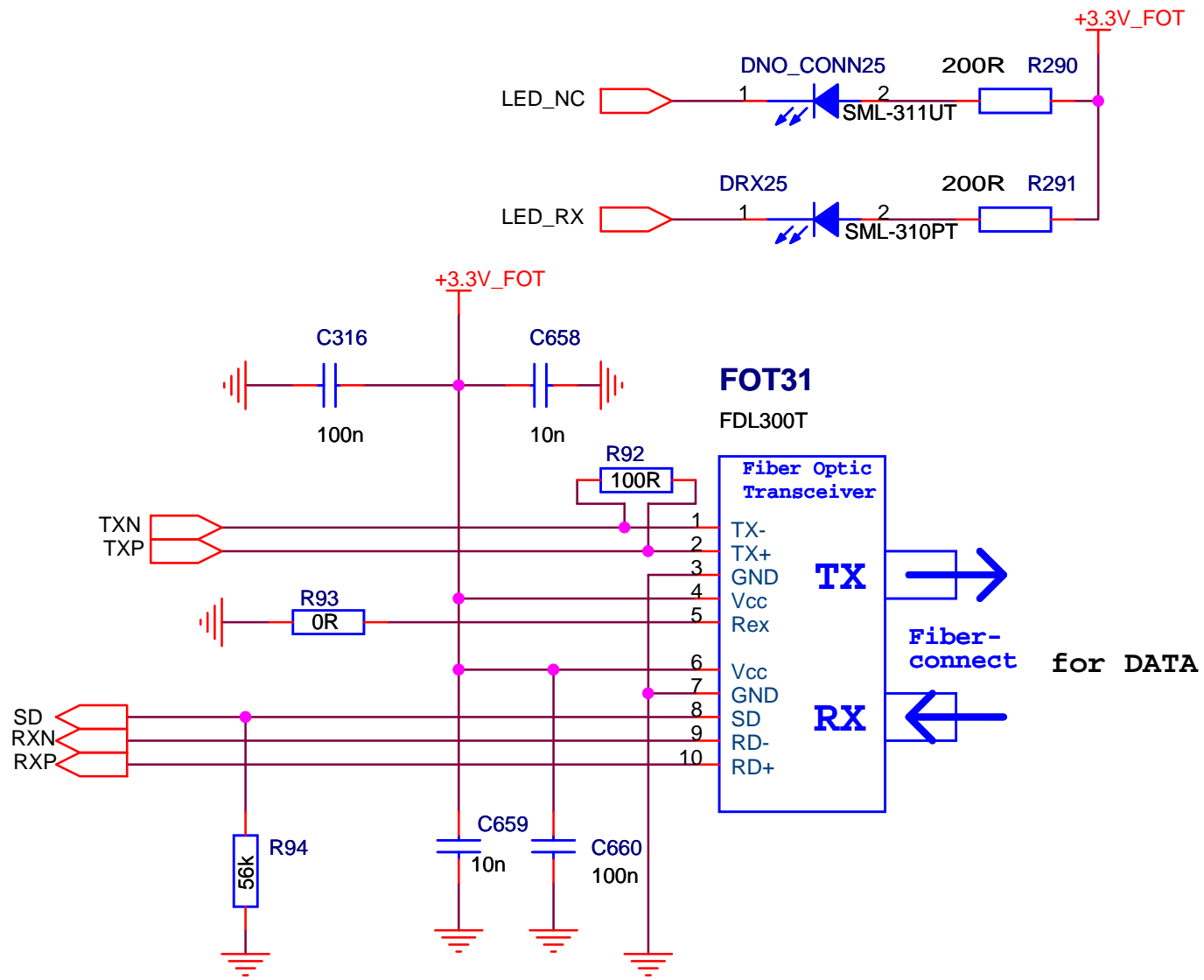
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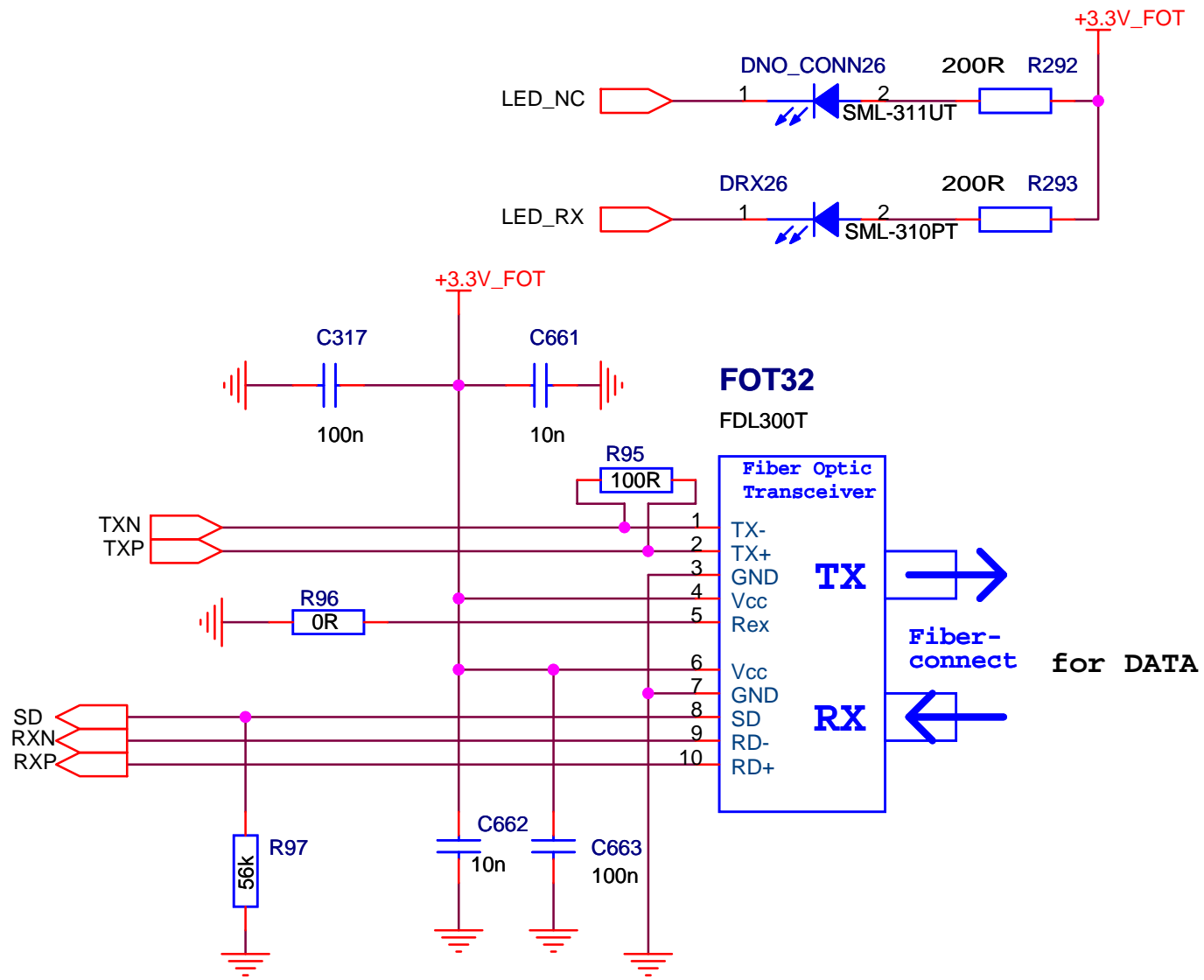
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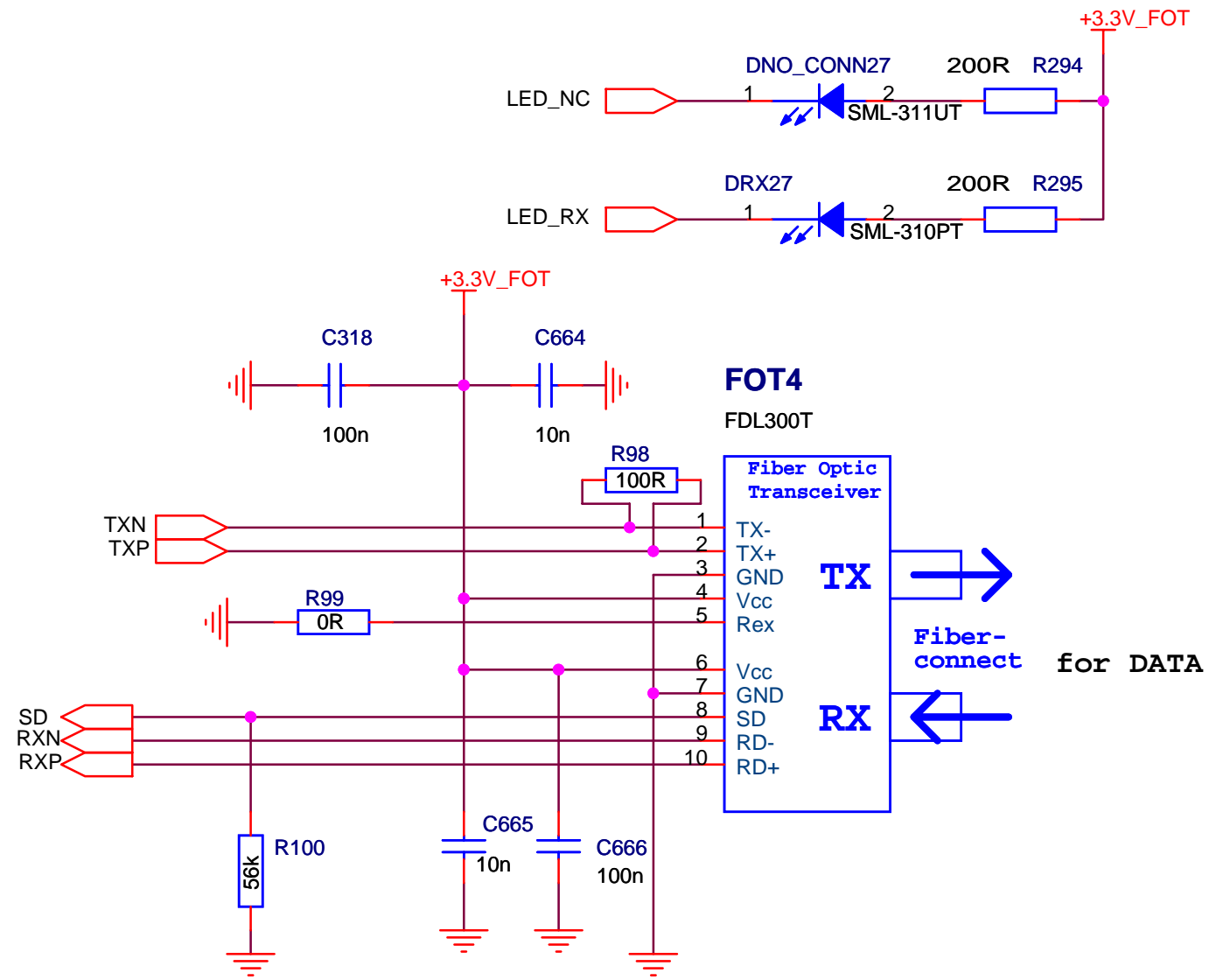
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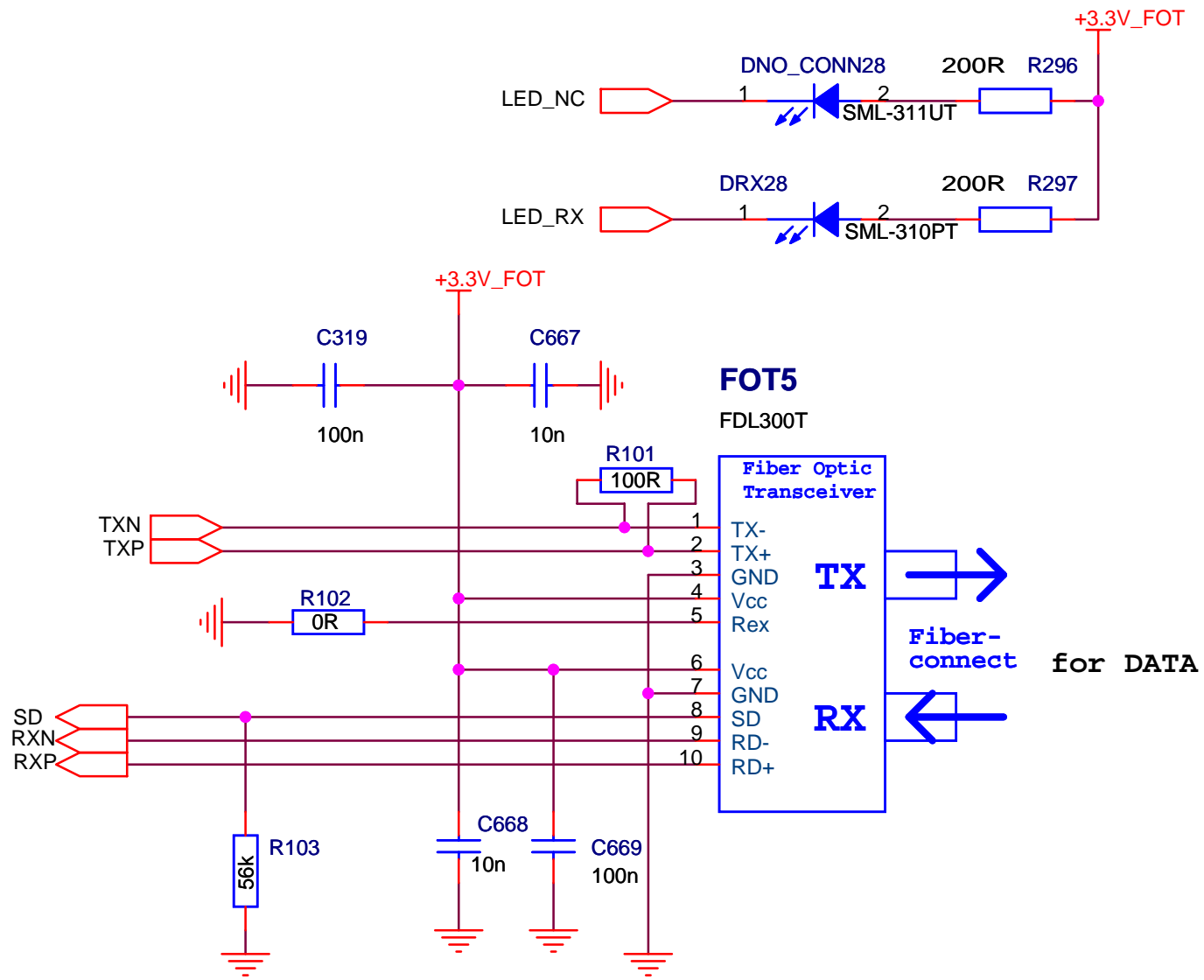
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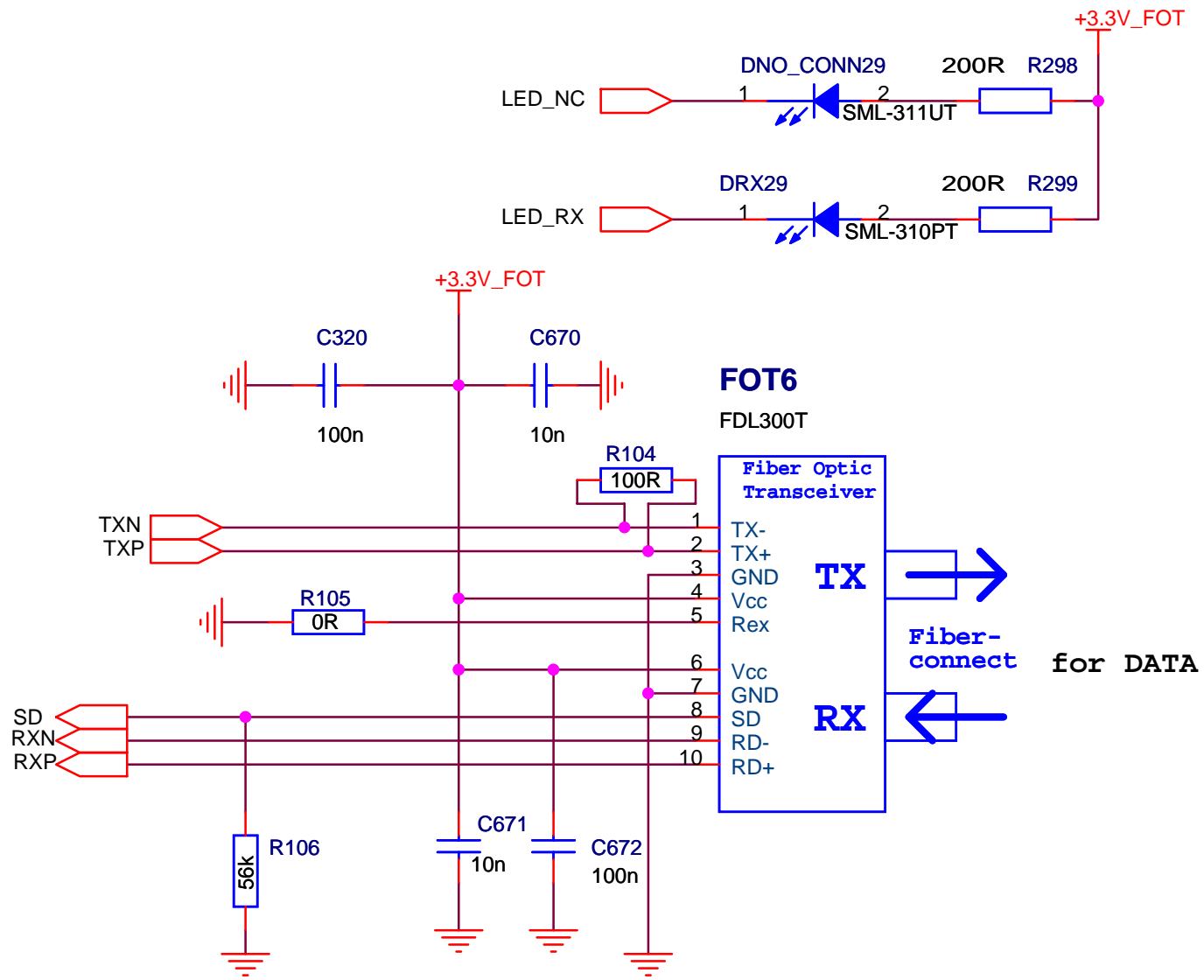
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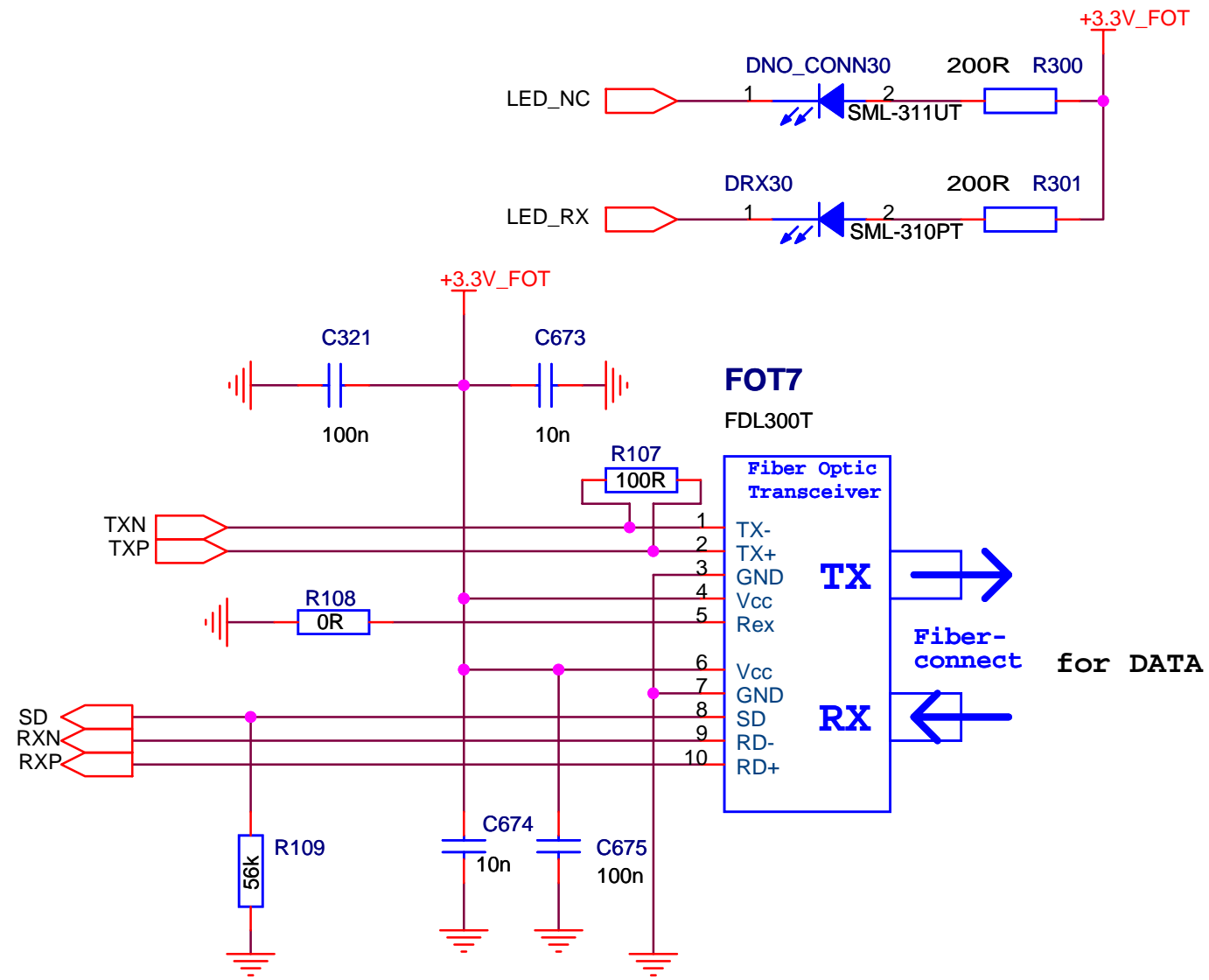
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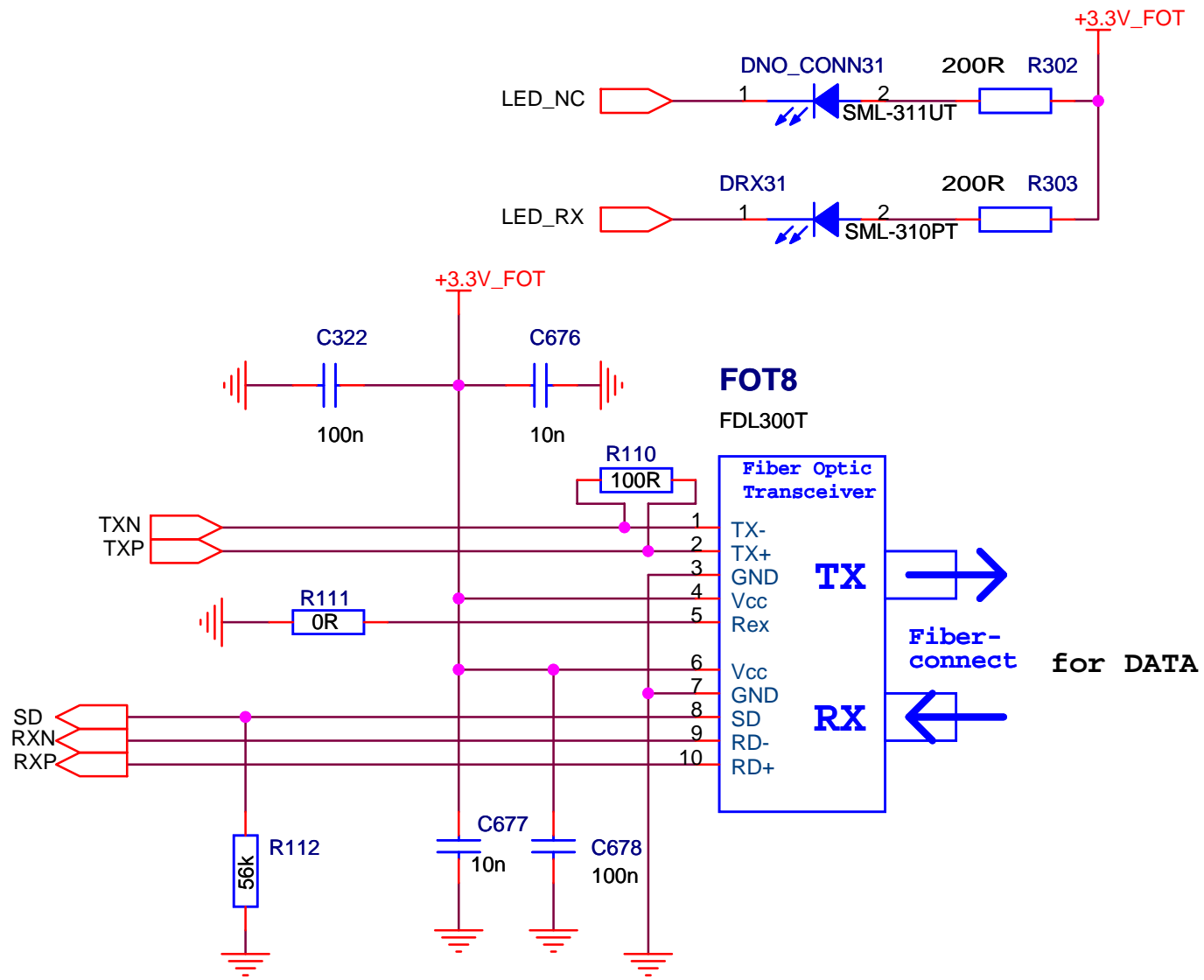
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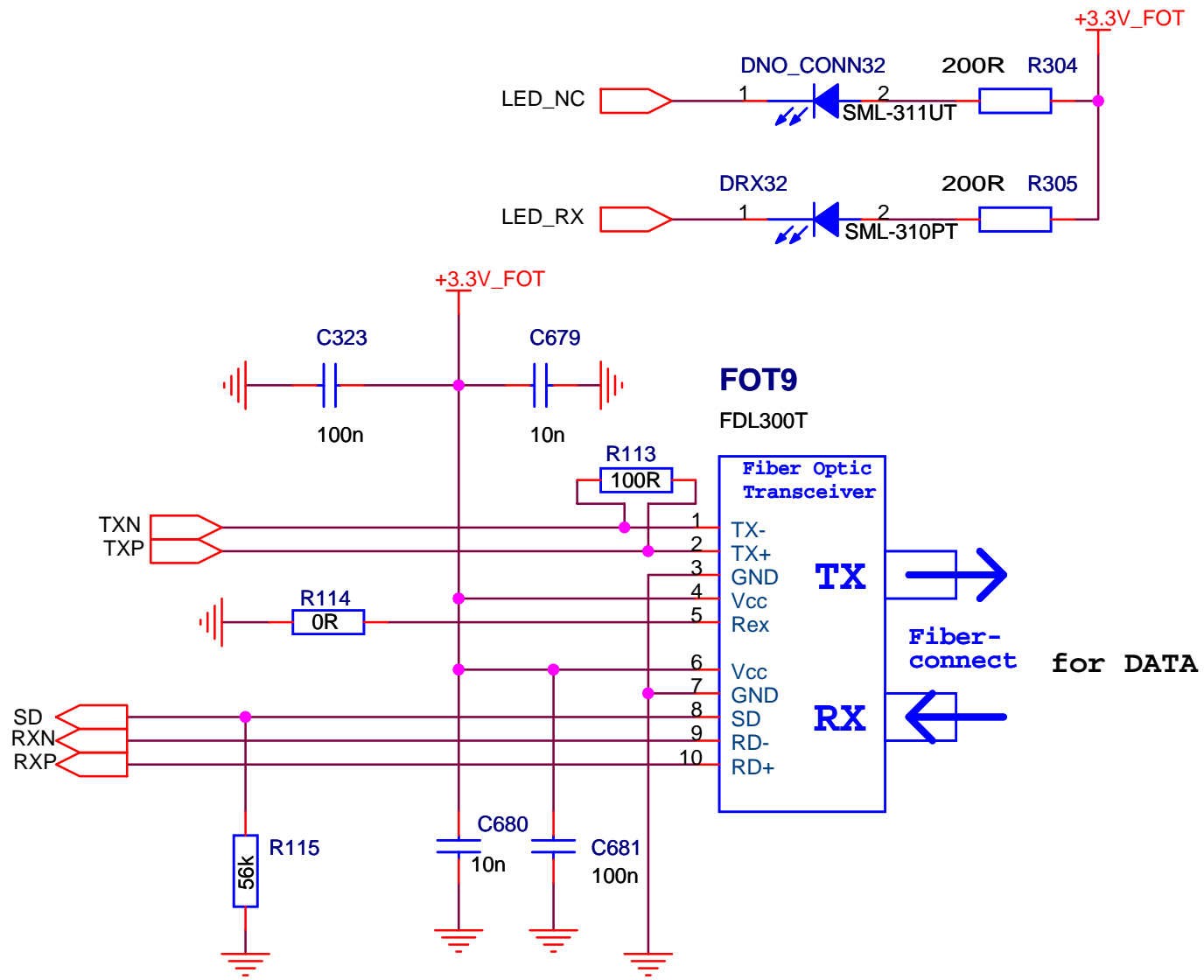
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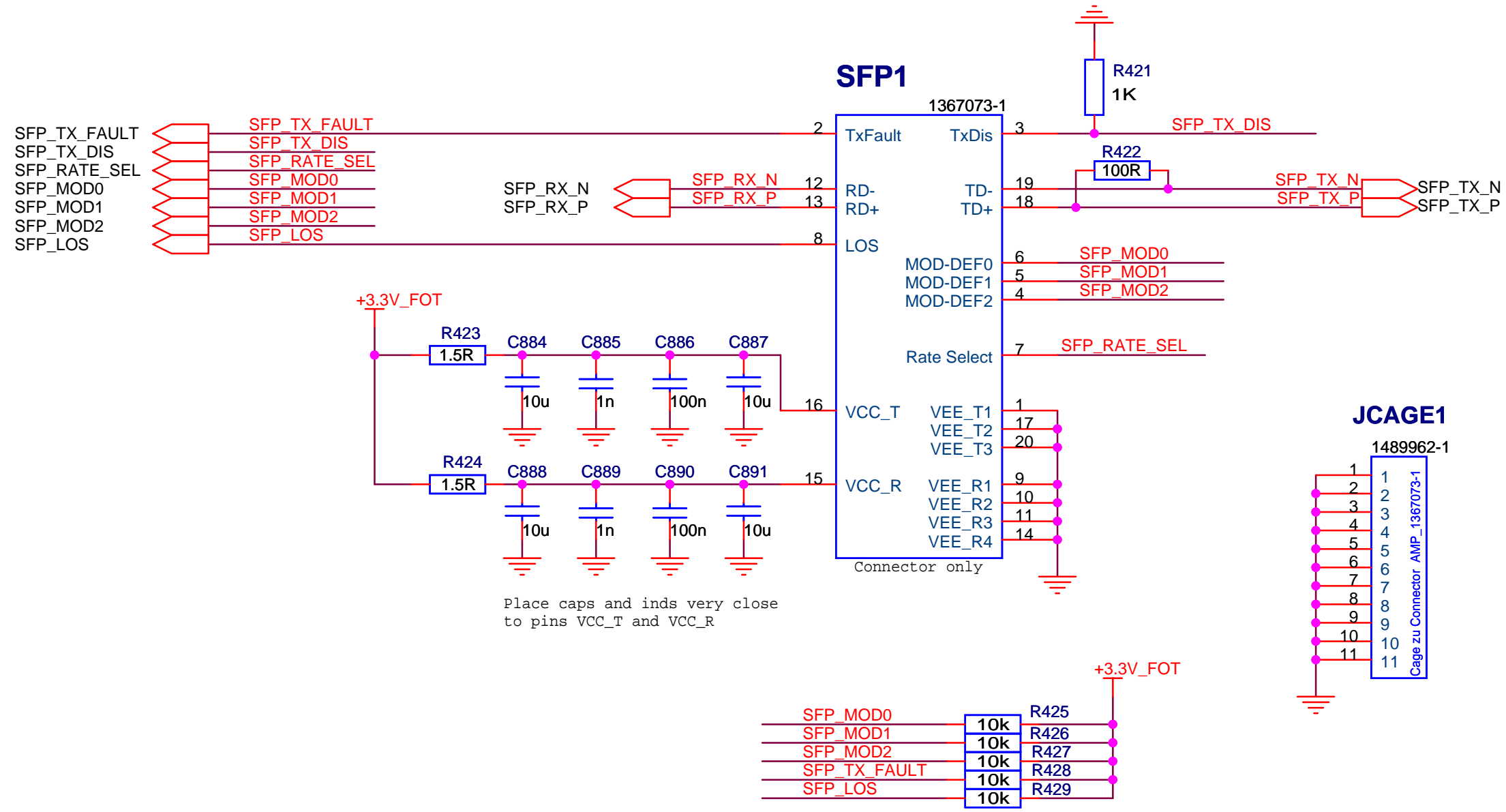
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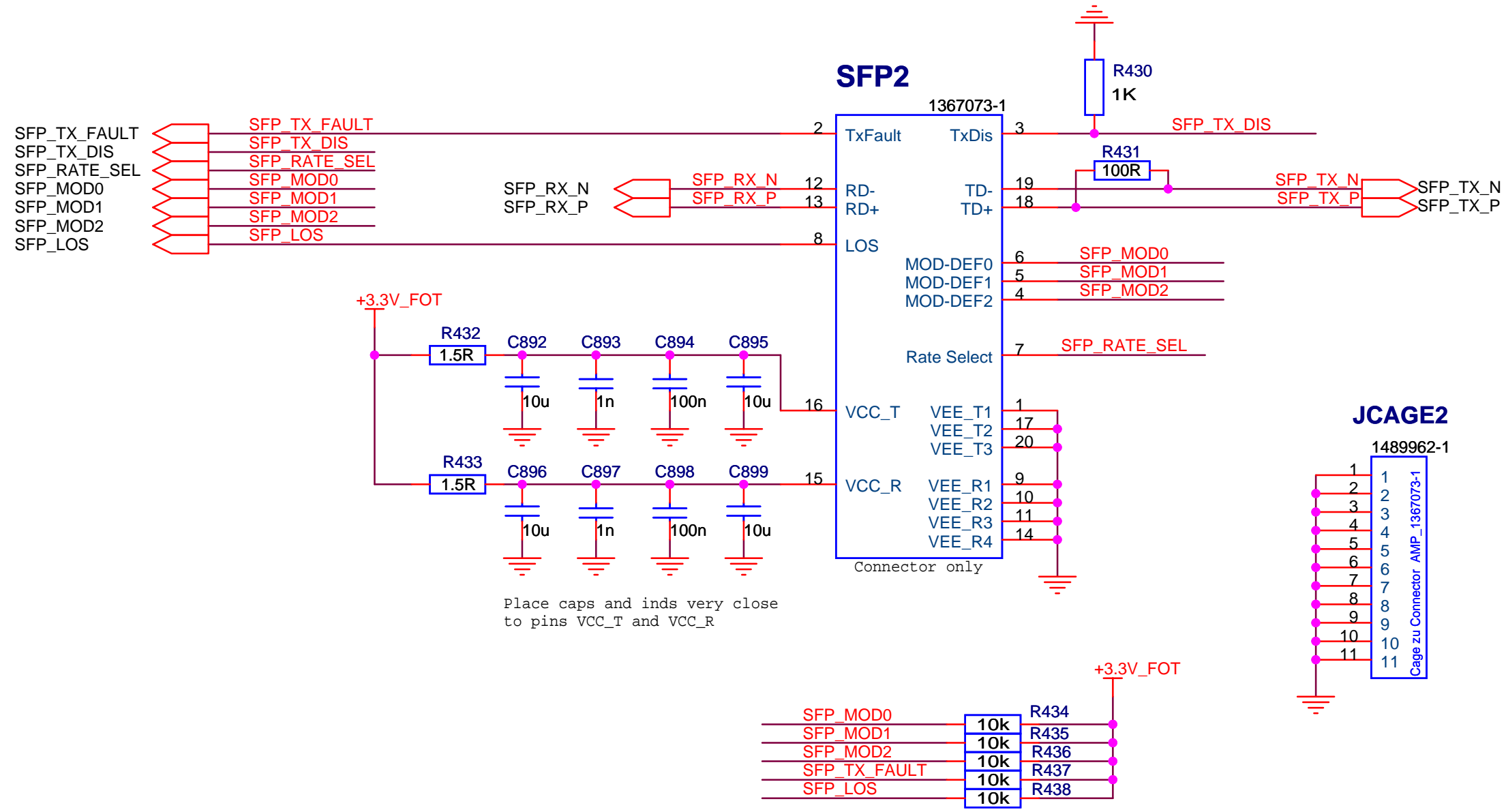
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Place caps and inds very close to pins VCC_T and VCC_R

MODDEF0 is grounded by module when inserted

GSi Gesellschaft für Schwerionenforschung mbH
 Planckstrasse 1
 D-64291 Darmstadt
 GERMANY
 www.gsi.de



Place caps and inds very close to pins VCC_T and VCC_R

MODDEF0 is grounded by module when inserted

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 GERMANY
 www.gsi.de

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