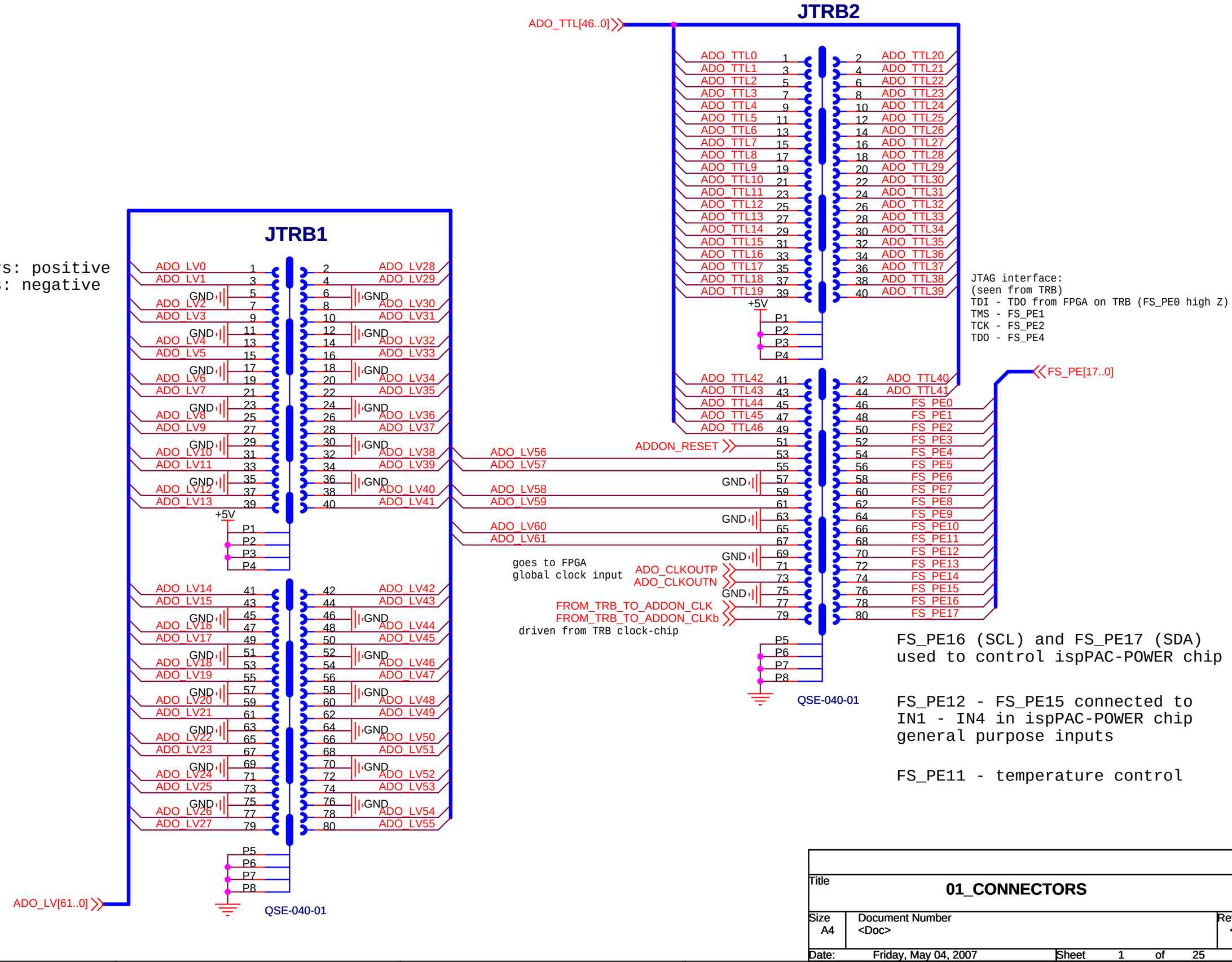
Even numbers: positive
Odd numbers: negative



JTAG interface:
(seen from TRB)
TDI - TDO from FPGA on TRB (FS_PE0 high Z)
TMS - FS_PE1
TCK - FS_PE2
TDO - FS_PE4

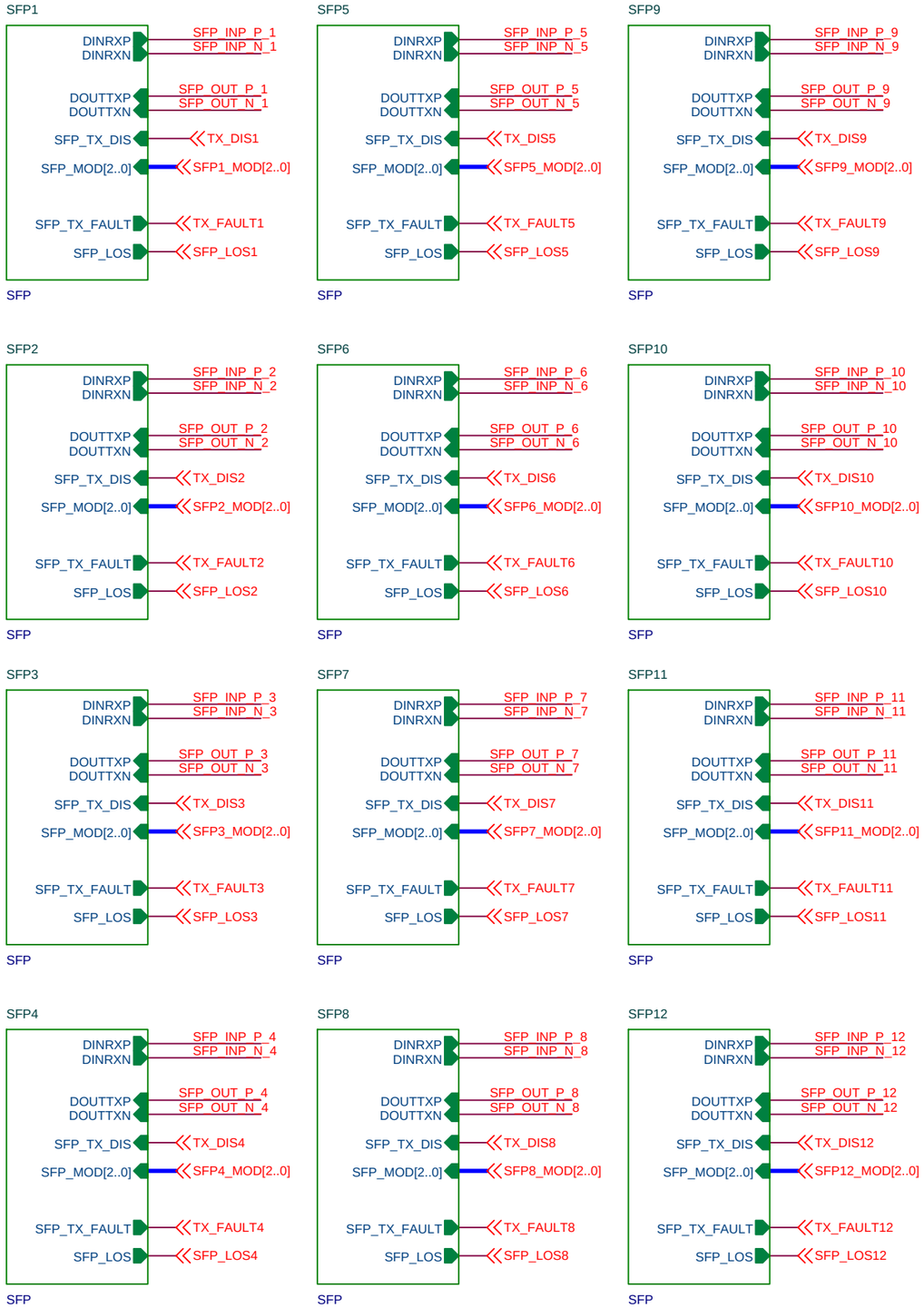
FS_PE16 (SCL) and FS_PE17 (SDA) used to control ispPAC-POWER chip

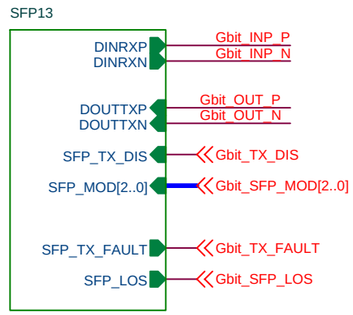
FS_PE12 - FS_PE15 connected to IN1 - IN4 in ispPAC-POWER chip general purpose inputs

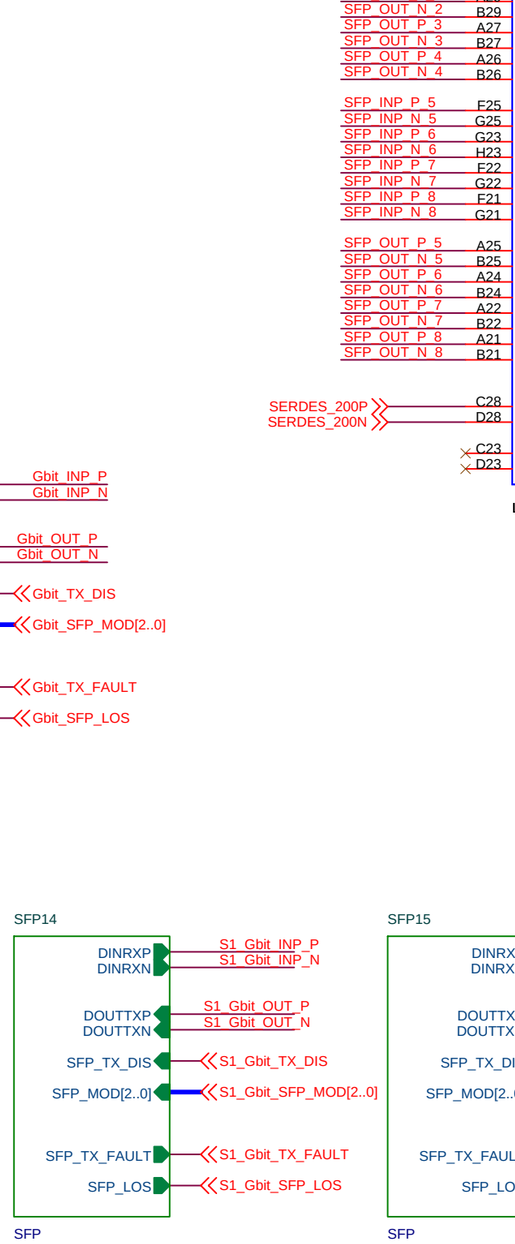
FS_PE11 - temperature control

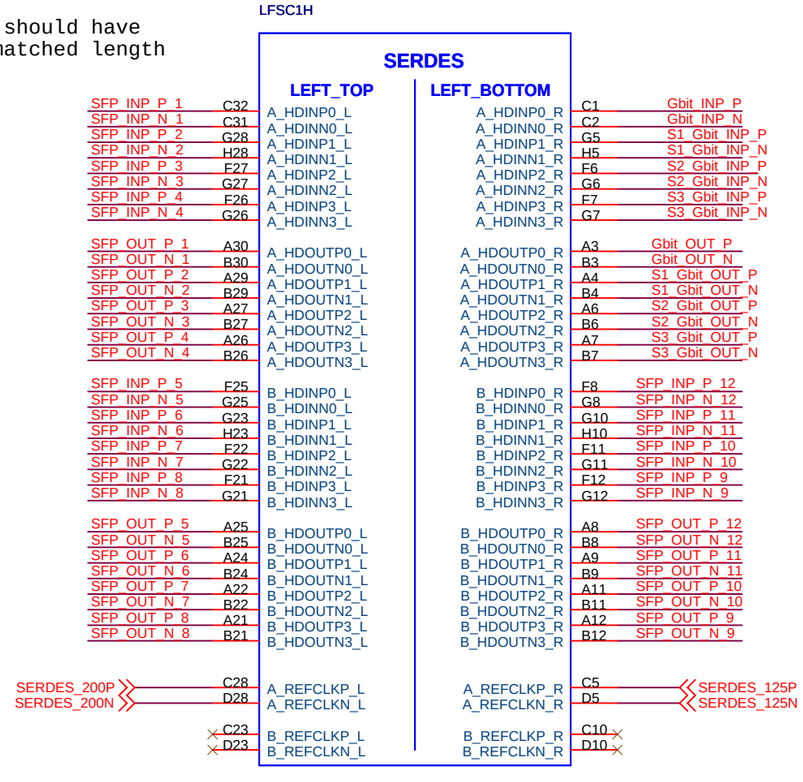
Title	**01_CONNECTORS**	
Size A4	Document Number <Doc>	Rev <RevCo
Date: Friday, May 04, 2007	Sheet 1 of 25	

All diff signal paths should have
50 Ohm impedance and matched length









Title	02_SERDES_SFP		
Size A3	Document Number <Doc>		Rev <RevCo
Date: Wednesday, May 09, 2007	Sheet 2 of 25		

SFP1_MOD[2..0]
SFP2_MOD[2..0]
SFP3_MOD[2..0]
SFP4_MOD[2..0]
SFP5_MOD[2..0]
SFP6_MOD[2..0]
SFP11_MOD[2..0]
SFP12_MOD[2..0]
Gbit_SFP_MOD[2..0]

LVTTL BANK

LFSC1A

LEFT_CENTER

BANK 1

SFP1_MOD0	E20	PT23A/D15/MPI_DATA15
SFP1_MOD1	E20	PT23B/A21/MPI_BURST
SFP1_MOD2	K18	PT23C/DP1/MPI_PAR1
SFP2_MOD0	J18	PT23D/D14/MPI_DATA14
SFP2_MOD1	F19	PT24A/MPI_TEA
SFP2_MOD2	E19	PT24B/A18MPI_TSIZ0
SFP3_MOD0	G20	PT24C/A20/MPI_BDIP
SFP3_MOD1	H20	PT24D/A19/MPI_TSIZ1
SFP3_MOD2	D19	PT25A/A17MPI_ADDR31
SFP4_MOD0	D20	PT25B/A15MPI_ADDR29
SFP4_MOD1	G19	PT25C/D13/MPI_DATA13
SFP4_MOD2	H19	PT25D/A16/MPI_ADDR30
SFP5_MOD0	C19	PT27A/A14MPI_ADDR28
SFP5_MOD1	C20	PT27B/A13/MPI_ADDR27
SFP5_MOD2	E18	PT27C/D12/MPI_DATA12
SFP6_MOD0	E17	PT27D/D11/MPI_DATA11
SFP6_MOD1	B20	PT28A/A12/MPI_ADDR26
SFP6_MOD2	B19	PT28B/A11/MPI_ADDR25
SFP11_MOD0	D18	PT29A/A10/MPI_ADDR24
SFP11_MOD1	C18	PT29B/A9/MPI_ADDR23
SFP11_MOD2	K17	PT31A/A8/MPI_ADDR22
SFP12_MOD0	J17	PT31B/A7/MPI_ADDR21
SFP12_MOD1	L20	PT31C/VREF1_1
SFP12_MOD2	A20	PT32A/A6/MPI_ADDR20
Gbit_SFP_MOD0	A19	PT32B/A5MPI_ADDR19
Gbit_SFP_MOD1	H18	PT32C/D26/PCLKT1_5/MPI_DATA26
Gbit_SFP_MOD2	H17	PT32D/D25/PCLKC1_5/MPI_DATA25
SUPPL_RESET	B18	PT33A/A4/MPI_ADDR18
	B17	PT33B/A3/MPI_ADDR17
TX_DIS1	G17	PT33C/A2/MPI_ADDR16
TX_FAULT1	F17	PT33D/A1/MPI_ADDR15
SFP_LOS1	A18	PT35A/A0/MPI_ADDR14
TX_DIS2	A17	PT35B/MPI_RETRY
TX_FAULT2	L17	PT35C/D24/PCLKT1_4/MPI_DATA24
SFP_LOS2	A15	PT37A/PCLKT1_0/MPI_CLK
TX_DIS3	A16	PT37B/PCLKC1_0
TX_FAULT3	L16	PT37C/DP2/MPI_PAR2
SFP_LOS3	B15	PT38A/MPI_TA
TX_DIS4	B16	PT38B/DP0/MPI_PAR0
TX_FAULT4	F16	PT38C/BUSY/RCLK
SFP_LOS4	G16	PT38D/MCA_DONE_OUT
TX_DIS5	A13	PT39A/MCA_CLK_P1_IN
TX_FAULT5	A14	PT39B/MCA_CLK_P2_OUT
SFP_LOS5	H16	PT39C/D22/PCLKT1_1/MPI_DATA22
TX_DIS6	H15	PT39D/D21/PCLKC1_1/MPI_DATA21
TX_FAULT6	K16	PT41A/MCA_CLK_P1_IN
SFP_LOS6	J16	PT41B/MCA_CLK_P1_OUT
TX_DIS7	D15	PT42A/MCA_DONE_IN
TX_FAULT7	C15	PT42B/DOUT
SFP_LOS7	L13	PT42D/VREF2_1
TX_DIS8	B13	PT43A/QOUTCEON
TX_FAULT8	B14	PT43B/D0/MPI_DATA0
SFP_LOS8	C14	PT45A/D1/MPI_DATA1
TX_DIS9	C13	PT45B/D2MPI_DATA2
TX_FAULT9	E16	PT45C/D3/MPI_DATA3
SFP_LOS9	E15	PT45D/D4/MPI_DATA4
TX_DIS10	D14	PT46A/D5/MPI_DATA5
TX_FAULT10	D13	PT46B/D6/MPI_DATA6
SFP_LOS10	G14	PT46C/D7/MPI_DATA7
TX_DIS11	H14	PT46D/WRN/MPI_WR_N
TX_FAULT11	F14	PT47A/RDN/MPI_STRB_N
SFP_LOS11	E14	PT47B/CS0N/MPI_CS0N
TX_DIS12	G13	PT47C/D10/MPI_DATA10
TX_FAULT12	H13	PT47D/D9/MPI_DATA9
SFP_LOS12	F13	PT49A/CS1/MPI_CS1
Gbit_TX_DIS	E13	PT49B/D8/MPI_DATA8
Gbit_TX_FAULT	K15	PT49C/LDCN
Gbit_SFP_LOS	J15	PT49D/HDC

LFSCM3GA25EP1-5FFN1020C

Temperature sensor

+3.3V
R1
4.7k
FS_PE11
+3.3V
TEMPSENS1
8
VDD
DQ
GND
4
1
DS18B20U+
C1
100n

JTAG interface:
(seen from TRB)
TDI - TDO from FPGA on TRB (FS_PE0 high Z)
TMS - FS_PE1
TCK - FS_PE2
TDO - FS_PE4

LFSC1J

FS_PE0	J13	TDI
FS_PE1	K9	TMS
FS_PE2	J12	TCK
SC_TDO	J9	TDO
		JTAG
	K23	M0
	J23	M1
	J24	M2
	K24	M3
		CONF
	K10	CCLK
	K20	DONE
	K21	INITN
	K12	PROGRAMN
	K13	MPIIRQN
ADDON_RESET	J21	RESETN
	J20	RDCFGN
	F28	RESP_ULC
	F5	RESP_URC

+3.3V
R198 10k
4.02k R2
4.02k R3

LFSCM3GA25EP1-5FFN1020C

Title	03_BANK_1_JTAG		
Size A3	Document Number <Doc>		Rev <RevCo
Date: Friday, May 04, 2007		Sheet 3 of 25	

LVDS bank

LFSC1G

TOP_LEFT
BANK 7

ADO_LV0	K25	PL16A/ULC_PLLT_IN_A/ULC_PLLT_FB_B
ADO_LV1	J25	PL16B/ULC_PLLC_IN_A/ULC_PLLC_FB_B
	K26	PL16C
	K27	PL16D
	D32	PL17A/ULC_DLLT_IN_C/ULC_DLLT_FB_D
	D31	PL17B/ULC_DLLC_IN_C/ULC_DLLC_FB_D
	M23	PL17C/ULC_PLLT_IN_B/ULC_PLLT_FB_A
	N23	PL17D/ULC_PLLC_IN_B/ULC_PLLC_FB_A
ADO_LV28	E32	PL18A/ULC_DLLT_IN_D/ULC_DLLT_FB_C
ADO_LV29	E31	PL18B/ULC_DLLC_IN_D/ULC_DLLC_FB_C
	J28	PL18C
	K28	PL18D/VREF2_7
ADO_LV2	F32	PL20A
ADO_LV3	F31	PL20B
	L25	PL20C
	L26	PL20D
ADO_LV30	G31	PL21A
ADO_LV31	G32	PL21B
ADO_LV4	J29	PL22A
ADO_LV5	H29	PL22B
	M25	PL22C
	N25	PL22D
ADO_LV32	H31	PL25A
ADO_LV33	H32	PL25B
	M24	PL25C/VREF1_7
	N24	PL25D/DIFFR_7
ADO_LV6	L32	PL26A/PCLKT7_1
ADO_LV7	M32	PL26B/PCLKC7_1
	R25	PL26C/PCLKT7_3
	R24	PL26D/PCLKC7_3
ADO_LV34	N31	PL27A/PCLKT7_0
ADO_LV35	N32	PL27B/PCLKC7_0
	P27	PL27C/PCLKT7_2
	P28	PL27D/PCLKC7_2

LFSCM3GA25EP1-5FFN1020C

1k R4

LVDS bank (not used)

LFSC1B

BOTTOM_LEFT
BANK 2

	K8	PR16A/URC_PLLT_IN_A/URC_PLLT_FB_B
	J8	PR16B/URC_PLLC_IN_A/URC_PLLC_FB_B
	K7	PR16C
	K6	PR16D
	D1	PR17A/URC_DLLT_IN_C/URC_DLLT_FB_D
	D2	PR17B/URC_DLLC_IN_C/URC_DLLC_FB_D
	M10	PR17C/URC_PLLT_IN_B/URC_PLLT_FB_A
	N10	PR17D/URC_PLLC_IN_B/URC_PLLC_FB_A
	E1	PR18A/URC_DLLT_IN_D/URC_DLLT_FB_C
	E2	PR18B/URC_DLLC_IN_D/URC_DLLC_FB_C
	J5	PR18C
	K5	PR18D/VREF2_2
	F1	PR20A
	F2	PR20B
	L8	PR20C
	L7	PR20D
	G2	PR21A
	G1	PR21B
	J4	PR22A
	H4	PR22B
	M8	PR22C
	N8	PR22D
	H2	PR25A
	H1	PR25B
	M9	PR25C/VREF1_2
	N9	PR25D/DIFFR_2
	L1	PR26A/PCLKT2_1
	M1	PR26B/PCLKC2_1
	R8	PR26C/PCLKT2_3
	R9	PR26D/PCLKC2_3
	N2	PR27A/PCLKT2_0
	N1	PR27B/PCLKC2_0
	P6	PR27C/PCLKT2_2
	P5	PR27D/PCLKC2_2

LFSCM3GA25EP1-5FFN1020C

1k R5

LVDS bank

LFSC1F

TOP_RIGHT
BANK 6

ADO_LV8	P30	PL29A/PCLKT6_0	W31	ADO_LV44
ADO_LV9	P29	PL29B/PCLKC6_0	Y31	ADO_LV45
	T23	PL29C/PCLKT6_1	W27	
	T24	PL29D/PCLKC6_1	Y27	PL42D/DIFFR_6
ADO_LV36	P32	PL30A	W28	ADO_LV18
ADO_LV37	P31	PL30B	Y28	ADO_LV19
	R28	PL30C/PCLKT6_3	Y26	
	T28	PL30D/PCLKC6_3	W25	
ADO_LV10	R30	PL31A	W32	ADO_LV46
ADO_LV11	R29	PL31B	Y32	ADO_LV47
	T25	PL31C/PCLKT6_2	AB28	
	T26	PL31D/PCLKC6_2	AA28	
ADO_LV38	R31	PL34A	AB32	ADO_LV20
ADO_LV39	R32	PL34B	AA32	ADO_LV21
	U23	PL34C/VREF1_6	AB27	
	U24	PL34D	AC27	
ADO_LV12	T31	PL35A	AD31	ADO_LV48
ADO_LV13	T32	PL35B	AC31	ADO_LV49
	T27	PL35C	Y24	
	U28	PL35D	Y23	
ADO_LV40	U32	PL36A	AD29	ADO_LV22
ADO_LV41	U31	PL36B	AD30	ADO_LV23
	U26	PL36C	AE28	
	U25	PL36D	AE28	
ADO_LV14	V32	PL38A	AC28	ADO_LV50
ADO_LV15	V31	PL38B	AD28	ADO_LV51
	V24	PL38C	AB26	
	V23	PL38D	AC26	PL51D/VREF2_6
ADO_LV42	V29	PL39A	AC32	ADO_LV24
ADO_LV43	V30	PL39B	AD32	ADO_LV25
	U27	PL39C	AA24	
	V28	PL39D	AA23	
ADO_LV16	W30	PL40A	AE30	ADO_LV52
ADO_LV17	W29	PL40B	AE29	ADO_LV53
	V25	PL40C	AC25	
	W26	PL40D	AB25	
			AE31	ADO_LV26
			AE32	ADO_LV27
		PL55C/LLC_DLLT_IN_E/LLC_DLLT_FB_F	AE26	
		PL55D/LLC_DLLC_IN_E/LLC_DLLC_FB_F	AE27	
			AF32	ADO_LV54
		PL56A	AF31	ADO_LV55
		PL56B	AC24	
		PL56C	AD25	
		PL56D	AG32	
		PL57A/LLC_DLLT_IN_F/LLC_DLLT_FB_E	AG31	
		PL57B/LLC_DLLC_IN_F/LLC_DLLC_FB_E	AC23	
		PL57C/LLC_PLLT_IN_B/LLC_PLLT_FB_A	AD24	
		PL57D/LLC_PLLC_IN_B/LLC_PLLC_FB_A		

LFSCM3GA25EP1-5FFN1020C

R6
1k

ADO_LV[61..0]

driven from TRB clock-chip

LVDS bank

LFSC1C

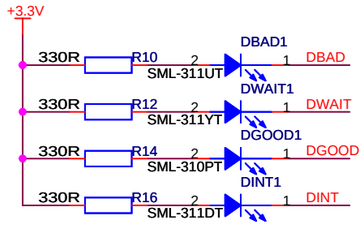
BOTTOM_RIGHT
BANK 3

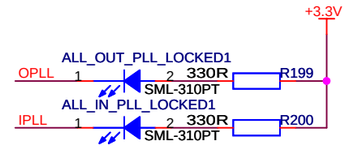
LVDS_CLK_200P	P3	PR29A/PCLKT3_0	W2	
LVDS_CLK_200N	P4	PR29B/PCLKC3_0	Y2	
FROM_TRB_TO_ADDON_CLK	T10	PR29C/PCLKT3_1	W6	
FROM_TRB_TO_ADDON_CLKb	T9	PR29D/PCLKC3_1	Y6	PR42D/DIFFR_3
	P1	PR30A	W5	
	P2	PR30B	Y5	
	R5	PR30C/PCLKT3_3	Y7	
	T5	PR30D/PCLKC3_3	W8	
	R3	PR31A	W1	
	R4	PR31B	Y1	
	T8	PR31C/PCLKT3_2	AB5	
	T7	PR31D/PCLKC3_2	AA5	
	R2	PR34A	AB1	
	R1	PR34B	AA1	
	U10	PR34C/VREF1_3	AB6	
	U9	PR34D	AC6	
	T2	PR35A	AD2	
	T1	PR35B	AC2	
	T6	PR35C	Y9	
	U5	PR35D	Y10	
	U1	PR36A	AD4	
	U2	PR36B	AD3	
	U7	PR36C	AE5	
	U8	PR36D	AE5	
	V1	PR38A	AC5	
	V2	PR38B	AD5	
	V9	PR38C	AB7	
	V10	PR38D	AC7	PR51D/VREF2_3
	V4	PR39A	AC1	
	V3	PR39B	AD1	
	U6	PR39C	AA9	
	V5	PR39D	AA10	
	W3	PR40A	AE3	ADO_CLKOUTP
	W4	PR40B	AE4	ADO_CLKOUTN
	V8	PR40C	AC8	
	W7	PR40D	AB8	
			AE2	ADO_LV58
			AE1	ADO_LV59
		PR55C/LRC_DLLT_IN_E/LRC_DLLT_FB_F	AE7	
		PR55D/LRC_DLLC_IN_E/LRC_DLLC_FB_F	AE6	
			AF1	ADO_LV60
		PR56A	AF2	ADO_LV61
		PR56B	AC9	
		PR56C	AD8	
		PR56D	AG1	ADO_LV56
		PR57A/LRC_DLLT_IN_F/LRC_DLLT_FB_E	AG2	ADO_LV57
		PR57B/LRC_DLLC_IN_F/LRC_DLLC_FB_E	AC10	
		PR57C/LRC_PLLT_IN_B/LRC_PLLT_FB_A	AD9	
		PR57D/LRC_PLLC_IN_B/LRC_PLLC_FB_A		

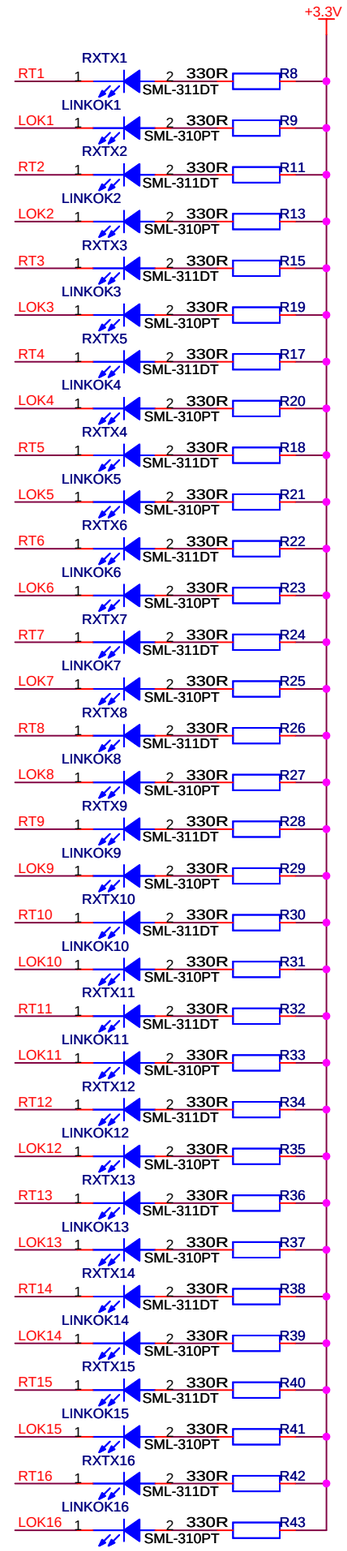
LFSCM3GA25EP1-5FFN1020C

1k
R7

Title	04_BANKS_2_3_6_7		
Size A3	Document Number <Doc>		Rev <RevCo
Date: Friday, May 04, 2007	Sheet 4 of 25		







LVTTL BANK

LFSC1E

ADO_TTL[46..0]

RIGHT_TOP
BANK 5

ADO_TTL0	AJ32	PB3A/LLC_PLLT_IN_A/LLC_PLLT_FB_B
ADO_TTL20	AK32	PB3B/LLC_PLLC_IN_A/LLC_PLLC_FB_B
ADO_TTL1	AE27	PB3C/LLC_DLLT_IN_C/LLC_DLLT_FB_D
ADO_TTL21	AG28	PB3D/LLC_DLLC_IN_C/LLC_DLLC_FB_D
ADO_TTL2	AK31	PB4A/LLC_DLLT_IN_D/LLC_DLLT_FB_C
ADO_TTL22	AL31	PB4B/LLC_DLLC_IN_D/LLC_DLLC_FB_C
ADO_TTL3	AE25	PB4C
ADO_TTL23	AE24	PB4D
ADO_TTL4	AK30	PB5A
ADO_TTL24	AL30	PB5B
ADO_TTL5	AD23	PB5C
ADO_TTL25	AE23	PB5D/VREF1_5
ADO_TTL6	AK29	PB7A
ADO_TTL26	AL29	PB7B
ADO_TTL7	AE26	PB7C
ADO_TTL27	AE25	PB7D
ADO_TTL8	AJ28	PB8A
ADO_TTL28	AK28	PB8B
ADO_TTL9	AJ31	PB9A
ADO_TTL29	AH30	PB9B
ADO_TTL10	AM30	PB11A
ADO_TTL30	AM29	PB11B
ADO_TTL11	AH29	PB11C
ADO_TTL31	AH28	PB11D
ADO_TTL12	AJ27	PB12A
ADO_TTL32	AK27	PB12B
ADO_TTL13	AE22	PB12C
ADO_TTL33	AE23	PB12D
ADO_TTL14	AL28	PB13A
ADO_TTL34	AL27	PB13B
ADO_TTL15	AC21	PB13C
ADO_TTL35	AD21	PB13D
ADO_TTL16	AM28	PB15A
ADO_TTL36	AM27	PB15B
ADO_TTL17	AG23	PB15C
ADO_TTL37	AE22	PB15D
ADO_TTL18	AG26	PB16A
ADO_TTL38	AG25	PB16B
ADO_TTL19	AL26	PB17A
ADO_TTL39	AM26	PB17B
ADO_TTL42	AJ24	PB19A
ADO_TTL40	AK24	PB19B
ADO_TTL43	AE21	PB19C
ADO_TTL41	AE20	PB19D
ADO_TTL44	AJ22	PB20A/PCLKT5_3
ADO_TTL45	AK22	PB20B/PCLKC5_3
ADO_TTL46	AG22	PB20C/PCLKT5_4
	AH22	PB20D/PCLKC5_4

PB21A/PCLKT5_5	AL23	RESET
PB21B/PCLKC5_5	AL22	
PB21C	AH23	
PB21D	AH24	
PB23A/PCLKT5_0	AJ21	S1_Gbit_TX_DIS
PB23B/PCLKC5_0	AK21	S1_Gbit_TX_FAULT
PB23C	AE19	S1_Gbit_SFP_LOS
PB23D/VREF2_5	AF19	S2_Gbit_TX_DIS
PB24A/PCLKT5_1	AM23	S2_Gbit_TX_FAULT
PB24B/PCLKC5_1	AM22	S2_Gbit_SFP_LOS
PB24C/PCLKT5_6	AH25	S3_Gbit_TX_DIS
PB24D/PCLKC5_6	AH26	S3_Gbit_TX_FAULT
PB25A/PCLKT5_2	AL21	S3_Gbit_SFP_LOS
PB25B/PCLKC5_2	AL20	
PB25C/PCLKT5_7	AG20	
PB25D/PCLKC5_7	AG19	
PB28A	AJ19	
PB28B	AK19	
PB28C	AD18	
PB28D	AE18	
PB29A	AM21	
PB29B	AM20	DBAD
PB29C	AH21	DWAIT
PB29D	AH20	DGOOD
PB31A	AJ18	DINT
PB31B	AK18	
PB31C	AH19	
PB31D	AH18	
PB32A	AL19	
PB32B	AM19	
PB32C	AH17	
PB32D	AG17	S1_Gbit_SFP_MOD0
PB33A	AL18	S1_Gbit_SFP_MOD1
PB33B	AM18	S1_Gbit_SFP_MOD2
PB33C	AC17	S2_Gbit_SFP_MOD0
PB33D	AD17	S2_Gbit_SFP_MOD1
PB35A	AL17	S2_Gbit_SFP_MOD2
PB35B	AM17	S3_Gbit_SFP_MOD0
PB35C	AE17	S3_Gbit_SFP_MOD1
PB35D	AF17	S3_Gbit_SFP_MOD2

LFSCM3GA25EP1-5FFN1020C

S1_Gbit_SFP_MOD[2..0]
S2_Gbit_SFP_MOD[2..0]
S3_Gbit_SFP_MOD[2..0]

LVTTL BANK

LFSC1D

FS_PE[17..0]

RIGHT_BOTTOM
BANK 4

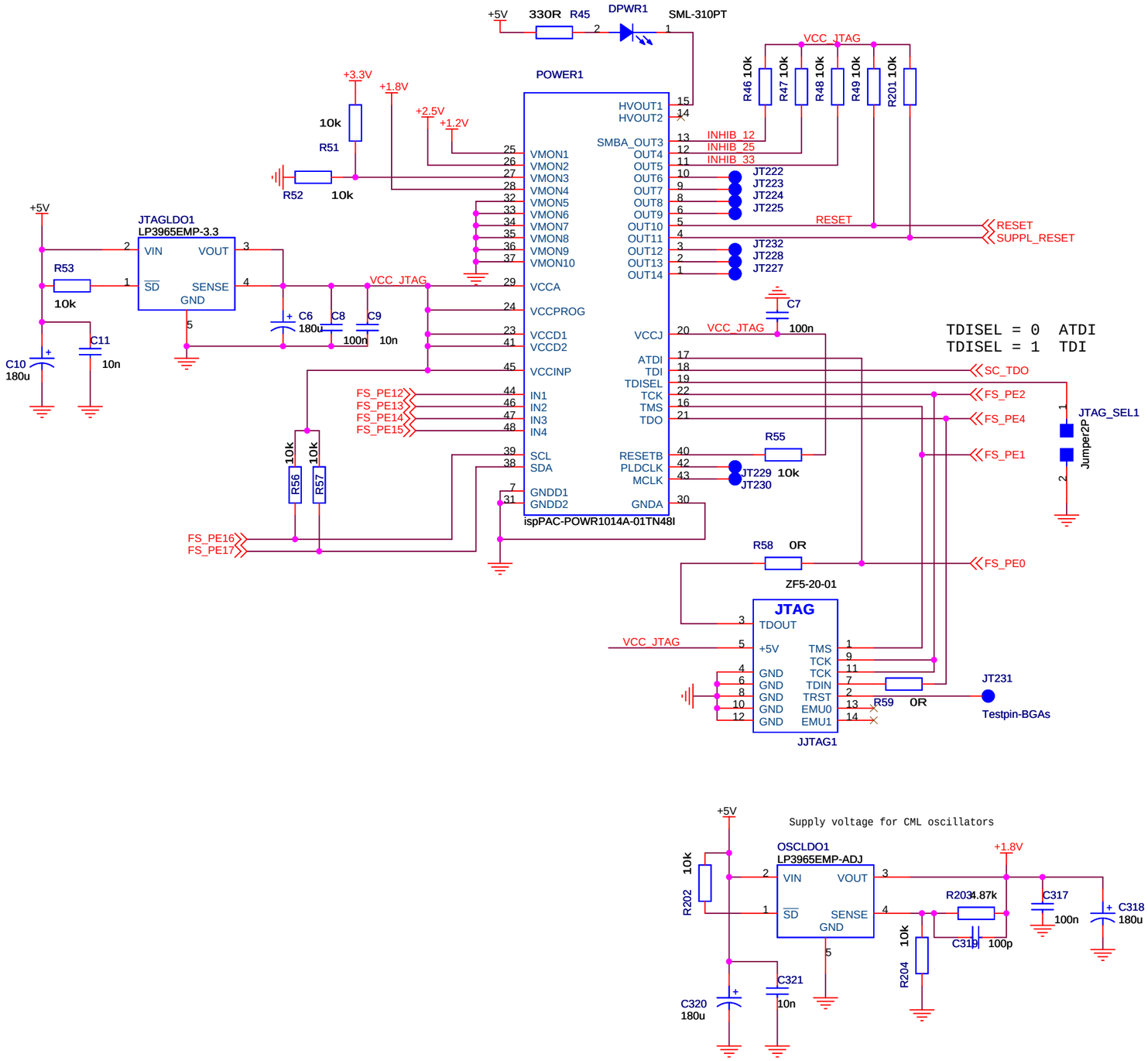
FS_PE5	AM16	PB37A
FS_PE6	AL16	PB37B
	AF16	PB37C
	AE16	PB37D
FS_PE7	AM15	PB38A
FS_PE8	AL15	PB38B
	AD16	PB38C
FS_PE10	AC16	PB38D
FS_PE9	AM14	PB39A
	AL14	PB39B
	AG16	PB39C
FS_PE11	AH16	PB39D
FS_PE12	AK15	PB41A
	AJ15	PB41B
	AH15	PB41C
FS_PE13	AH14	PB41D
FS_PE14	AM13	PB42A
	AM12	PB42B
	AH13	PB42C
FS_PE15	AH12	PB42D
FS_PE16	AK14	PB43A
	AJ14	PB43B
	AE15	PB43C
FS_PE17	AD15	PB43D
SFP10_MOD2	AL13	PB46A/PCLKT4_2
SFP10_MOD1	AL12	PB46B/PCLKC4_2
SFP10_MOD0	AG14	PB46C/PCLKT4_7
SFP9_MOD2	AG13	PB46D/PCLKC4_7
SFP9_MOD1	AM11	PB47A/PCLKT4_1
SFP9_MOD0	AM10	PB47B/PCLKC4_1
SFP8_MOD2	AH11	PB47C/PCLKT4_6
SFP8_MOD1	AH10	PB47D/PCLKC4_6
SFP8_MOD0	AK12	PB49A/PCLKT4_0
SFP7_MOD2	AJ12	PB49B/PCLKC4_0
SFP7_MOD1	AF14	PB49C/VREF2_4
SFP7_MOD0	AE14	PB49D

PB51A/PCLKT4_5	AL11	OPLL
PB51B/PCLKC4_5	AL10	IPLL
PB51C	AH9	
PB51D	AH8	
PB52A/PCLKT4_3	AK11	
PB52B/PCLKC4_3	AJ11	
PB52C/PCLKT4_4	AH7	
PB52D/PCLKC4_4	AH6	
PB53A	AK8	
PB53B	AJ8	
PB53C	AF11	LOK15
PB55A	AD12	LOK16
PB55B	AE12	RT16
PB56A	AM6	LOK11
PB56B	AM5	LOK10
PB56C	AC12	
PB57A	AL6	RT11
PB57B	AL5	RT10
PB59A	AG7	
PB59B	AG8	
PB60A	AK6	LOK9
PB60B	AJ6	RT9
PB60C	AF10	
PB60D	AE11	RT15
PB61A	AM4	LOK5
PB61B	AM3	RT5
PB63A	AH5	LOK6
PB63B	AH4	RT6
PB64A	AK5	LOK8
PB64B	AJ5	RT8
PB64C	AF8	LOK12
PB64D	AF7	RT12
PB65A	AL4	LOK4
PB65B	AL3	RT4
PB65C	AG5	LOK7
PB65D	AF6	RT7
PB67A	AK3	LOK3
PB67B	AJ3	RT3
PB67C/VREF1_4	AE10	LOK14
PB67D	AD10	RT14
PB68A/LRC_DLLT_IN_C/LRC_DLLT_FB_D	AL2	LOK2
PB68B/LRC_DLLC_IN_C/LRC_DLLC_FB_D	AK2	RT2
PB68C	AE9	LOK13
PB68D	AE8	RT13
PB69A/LRC_PLLT_IN_A/LRC_PLLT_FB_B	AJ1	LOK1
PB69B/LRC_PLLC_IN_A/LRC_PLLC_FB_B	AK1	RT1
PB69C/LRC_DLLT_IN_D/LRC_DLLT_FB_C	AJ2	
PB69D/LRC_DLLC_IN_D/LRC_DLLC_FB_C	AH3	

LFSCM3GA25EP1-5FFN1020C

SFP7_MOD[2..0]
SFP8_MOD[2..0]
SFP9_MOD[2..0]
SFP10_MOD[2..0]

Title	05_BANKS_4_5		
Size A3	Document Number <Doc>		Rev <RevCo
Date: Friday, May 04, 2007	Sheet 5	of 25	



Title	06_POWER_SOURCE
Size A3	Document Number <Doc>
Rev	<RevCo
Date: Tuesday, May 08, 2007	Sheet 6 of 25

Analog supply for SERDES - TN1114 p. 2

+1.2V — L1 BLM41PG471SN1L

C16 1u, C43 180u ESR = 0.4, C17 100n, C18 10n, C19 10n, C20 10n, C21 100n, C22 100n, C23 100n

Decoupling caps distributed evenly as close to the device as possible TN1114 p.2

One per pin located under device

C24 C25 C26 C27 C28 C29 C30 C31 C32 C33 C34 C35 C36 C37 C38 C39 C40 C41 C42 C44 — 22p

+1.2V_SQL

+1.2V — L2 BLM41PG471SN1L

C45 1u, C65 180u ESR = 0.4, C55 100n, C46 10n, C56 10n, C47 10n, C57 100n, C48 100n, C58 100n

One per pin located under device

C59 C60 C61 C49 C62 C63 C64 C50 C51 C66 C52 C67 C53 C68 C69 C54 — 22p

+1.2V_SQR

+1.2V — L35 BLM41PG471SN1L

C325 1u, C326 180u ESR = 0.4

+1.2VDD

translates the SFP output signal (AC coupled) to the center of the SERDES input voltage range - TN1114 p. 7

R61 300R, R62 300R

VDDIB_AL: R66 499R, C70 100n, C71 10n

VDDIB_AR: R68 499R, C72 10n, C73 100n

VDDIB_BL: R84 499R, C83 100n, C84 10n

VDDIB_BR: R85 499R, C85 10n, C86 100n

R78 300R, R81 300R

+1.2VDD: C75 C77 C79 C81 10n; C76 C78 C80 C82 10n; C87 C89 C91 C93 10n; C88 C90 C92 C94 10n

+2.5V: C95 100n, C96 10n, C97 10n, C98 100n

LFSC1I

ANALOG POWER

B31	A_VDDIB0_L	A_VDDIB0_R	B2
F29	A_VDDIB1_L	A_VDDIB1_R	F4
H27	A_VDDIB2_L	A_VDDIB2_R	H6
H26	A_VDDIB3_L	A_VDDIB3_R	H7
D30	A_VDDOB0_L	A_VDDOB0_R	D3
D29	A_VDDOB1_L	A_VDDOB1_R	D4
D27	A_VDDOB2_L	A_VDDOB2_R	D6
D26	A_VDDOB3_L	A_VDDOB3_R	D7
H25	B_VDDIB0_L	B_VDDIB0_R	H8
H24	B_VDDIB1_L	B_VDDIB1_R	H9
H22	B_VDDIB2_L	B_VDDIB2_R	H11
H21	B_VDDIB3_L	B_VDDIB3_R	H12
D25	B_VDDOB0_L	B_VDDOB0_R	D8
D24	B_VDDOB1_L	B_VDDOB1_R	D9
D22	B_VDDOB2_L	B_VDDOB2_R	D11
D21	B_VDDOB3_L	B_VDDOB3_R	D12
A28	VDDAX25_L	VDDAX25_R	A5

LFSCM3GA25EP1-5FFN1020C

LFSC1L

B10	VCC12_0	VCCAUX_0	AA11
B23	VCC12_1	VCCAUX_1	AA12
B28	VCC12_2	VCCAUX_2	AA21
B5	VCC12_3	VCCAUX_3	AA22
E11	VCC12_4	VCCAUX_4	AB11
E12	VCC12_5	VCCAUX_5	AB12
E30	VCC12_6	VCCAUX_6	AB15
E29	VCC12_7	VCCAUX_7	AB16
E27	VCC12_8	VCCAUX_8	AB17
E26	VCC12_9	VCCAUX_9	AB18
E25	VCC12_10	VCCAUX_10	AB21
E24	VCC12_11	VCCAUX_11	AB22
E22	VCC12_12	VCCAUX_12	L11
E21	VCC12_13	VCCAUX_13	L12
E3	VCC12_14	VCCAUX_14	L14
E4	VCC12_15	VCCAUX_15	L15
E6	VCC12_16	VCCAUX_16	L18
E7	VCC12_17	VCCAUX_17	L19
E8	VCC12_18	VCCAUX_18	L21
E9	VCC12_19	VCCAUX_19	L22
M14	VCC12_20	VCCAUX_20	M11
M16	VCC12_21	VCCAUX_21	M12
M17	VCC12_22	VCCAUX_22	M21
M19	VCC12_23	VCCAUX_23	M22
P12	VCC12_24	VCCAUX_24	P11
P21	VCC12_25	VCCAUX_25	P22
T12	VCC12_26	VCCAUX_26	R11
T21	VCC12_27	VCCAUX_27	R22
U12	VCC12_28	VCCAUX_28	V11
U21	VCC12_29	VCCAUX_29	V22
W12	VCC12_30	VCCAUX_30	W11
W21	VCC12_31	VCCAUX_31	W22
AA14	VCC12_32	VTT_2_0	N11
AA16	VCC12_33	VTT_2_1	R10
AA17	VCC12_34	VTT_3_0	T11
AA19	VCC12_35	VTT_3_1	U11
		VTT_3_2	Y11
		VTT_4_0	AB13
		VTT_4_1	AB14
		VTT_4_2	AC15
		VTT_5_0	AB19
		VTT_5_1	AB20
		VTT_5_2	AC18
		VTT_6_0	T22
		VTT_6_1	U22
		VTT_6_2	Y22
		VTT_7_0	N22
		VTT_7_1	R23
J10	VCCJ		
AH1	PROBE_VCC		
AH2	PROBE_GND		
AH32	XRES		
AH31	TEMP		

+2.5V

100n C74 +3.3V

1k R77

LFSCM3GA25EP1-5FFN1020C

Vcmt not used -> Vtt to GND
Vcmt used -> Vtt floating
DS1004 p.2-23

OR: R63 R64 R65 R67 R69 R70 R71 R72 R73 R74 R75 R76 R79 R80 R82 R83

VCCAUX decoupling caps

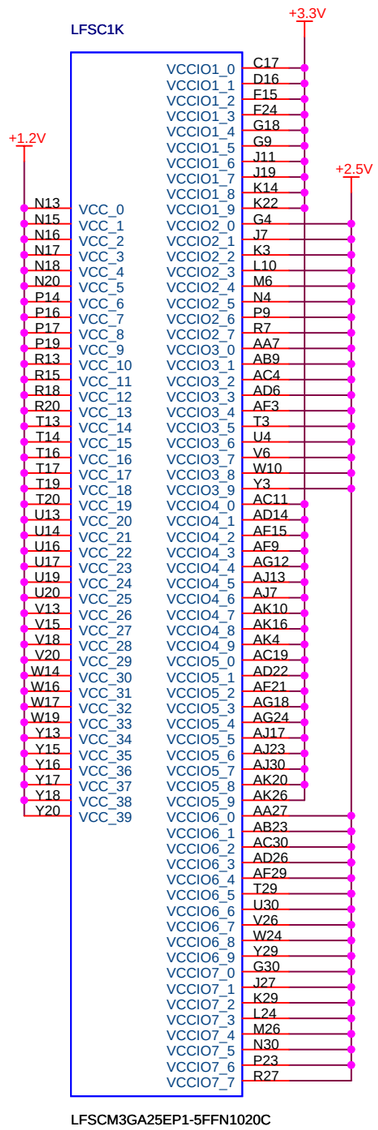
+2.5V

C99 C100 C101 C102 C103 C104 C105 C106 C107 C108 C109 C110 C111 C112 C113 C114 C115 C116 C117 C118 C119 C120 C121 C122 C123 C124 C125 C126 C127 C128 C129 C130

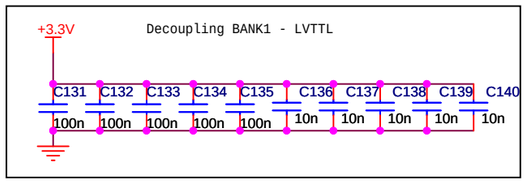
100n: C99 C100 C101 C102 C103 C104 C105 C107 C108 C109 C111 C112 C113 C114 C115 C116 C117 C118 C119 C120 C121

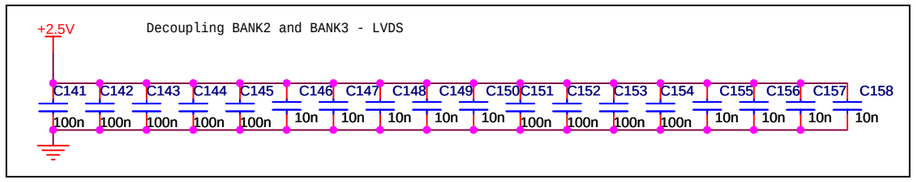
10n: C106 C110 C122 C123 C124 C125 C126 C127 C128 C129 C130

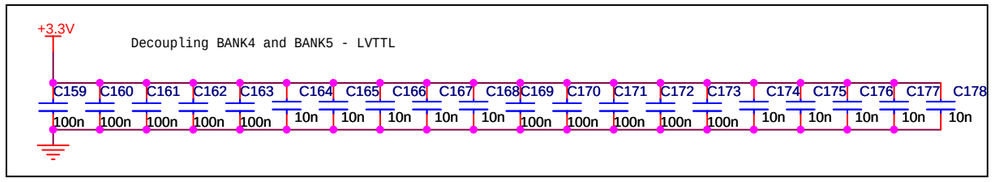
Title	07_POWER_ANALOG		
Size A3	Document Number <Doc>		Rev <RevCo
Date: Tuesday, May 08, 2007	Sheet 7 of 25		

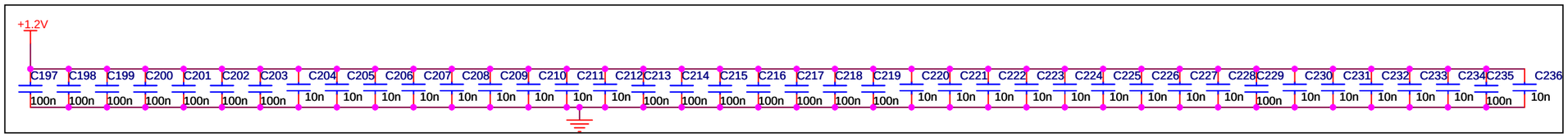


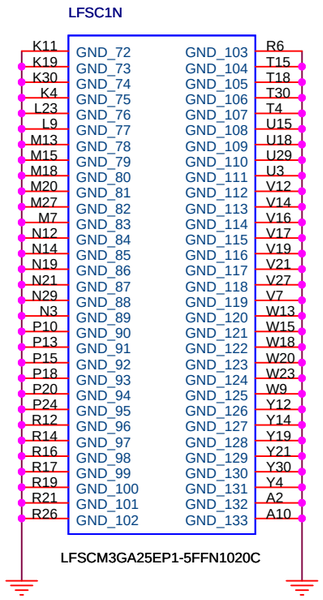
LFSCM3GA25EP1-5FFN1020C



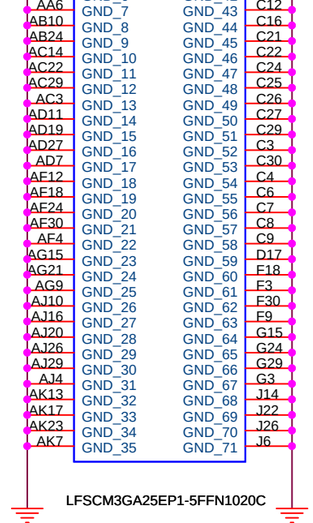






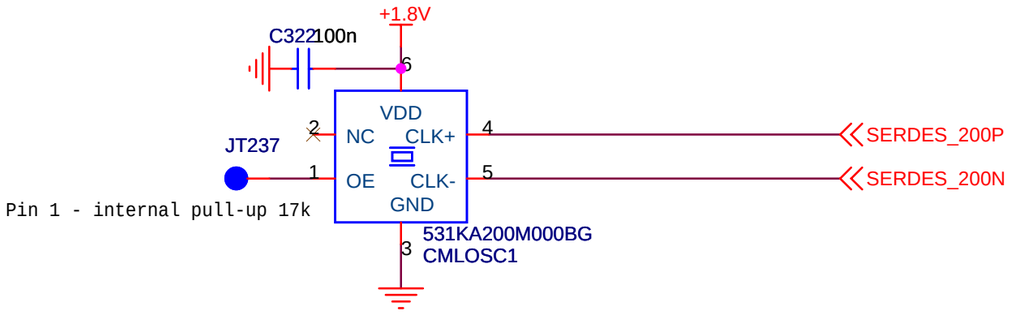


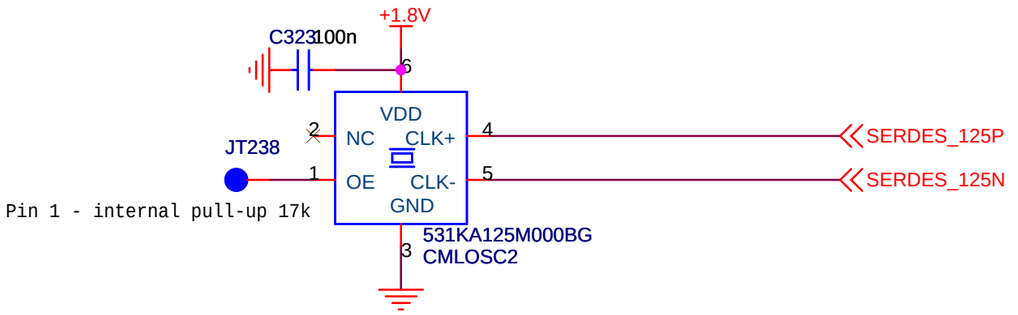
LFSCM3GA25EP1-5FFN1020C

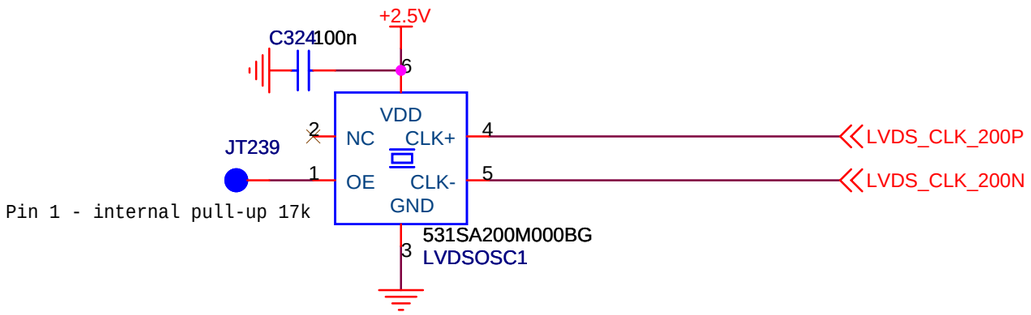


LFSCM3GA25EP1-5FFN1020C

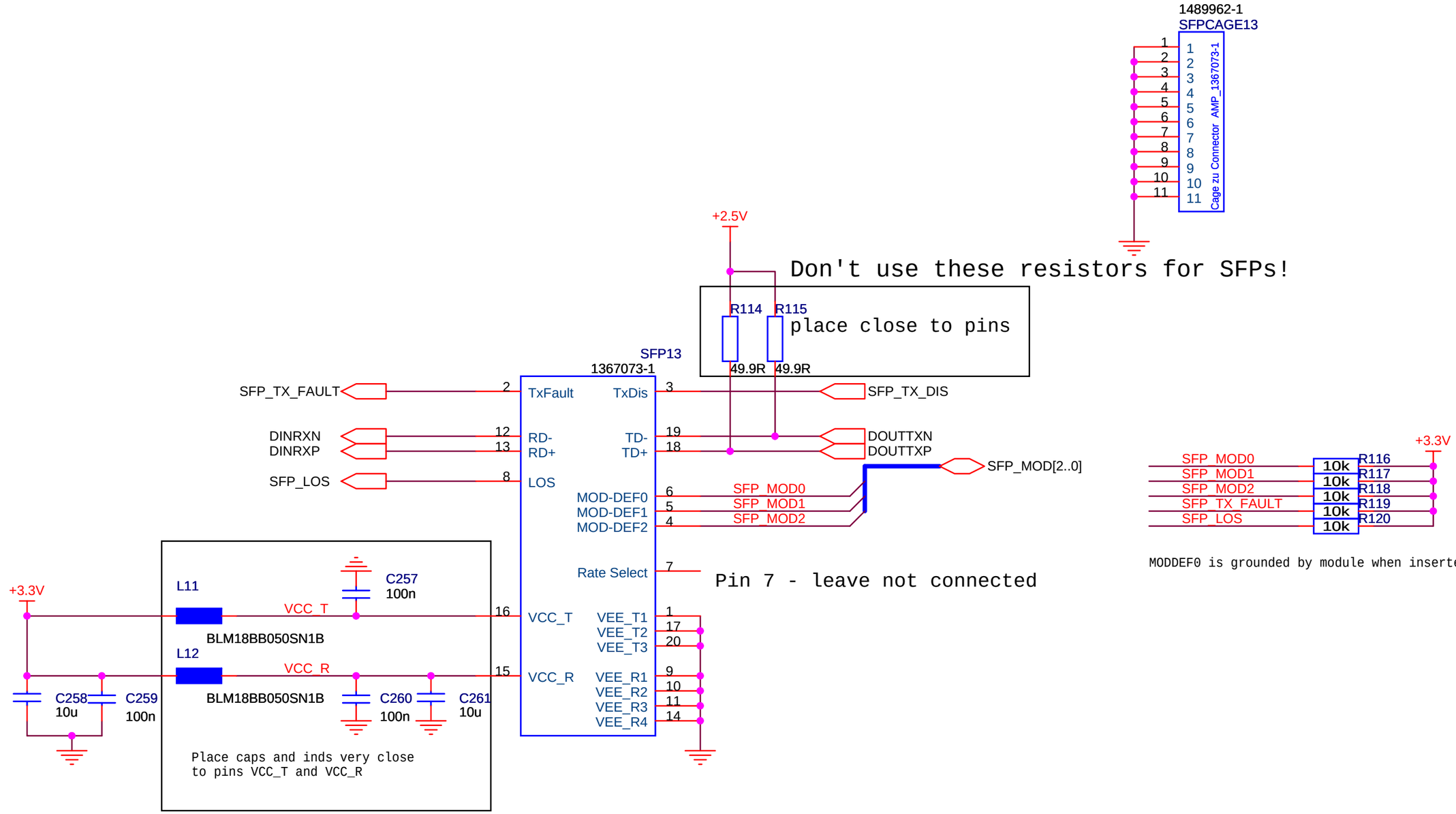
Title	08_POWER_DIGITAL	
Size A3	Document Number <Doc>	Rev <RevCo
Date: Friday, May 04, 2007	Sheet 8 of 25	



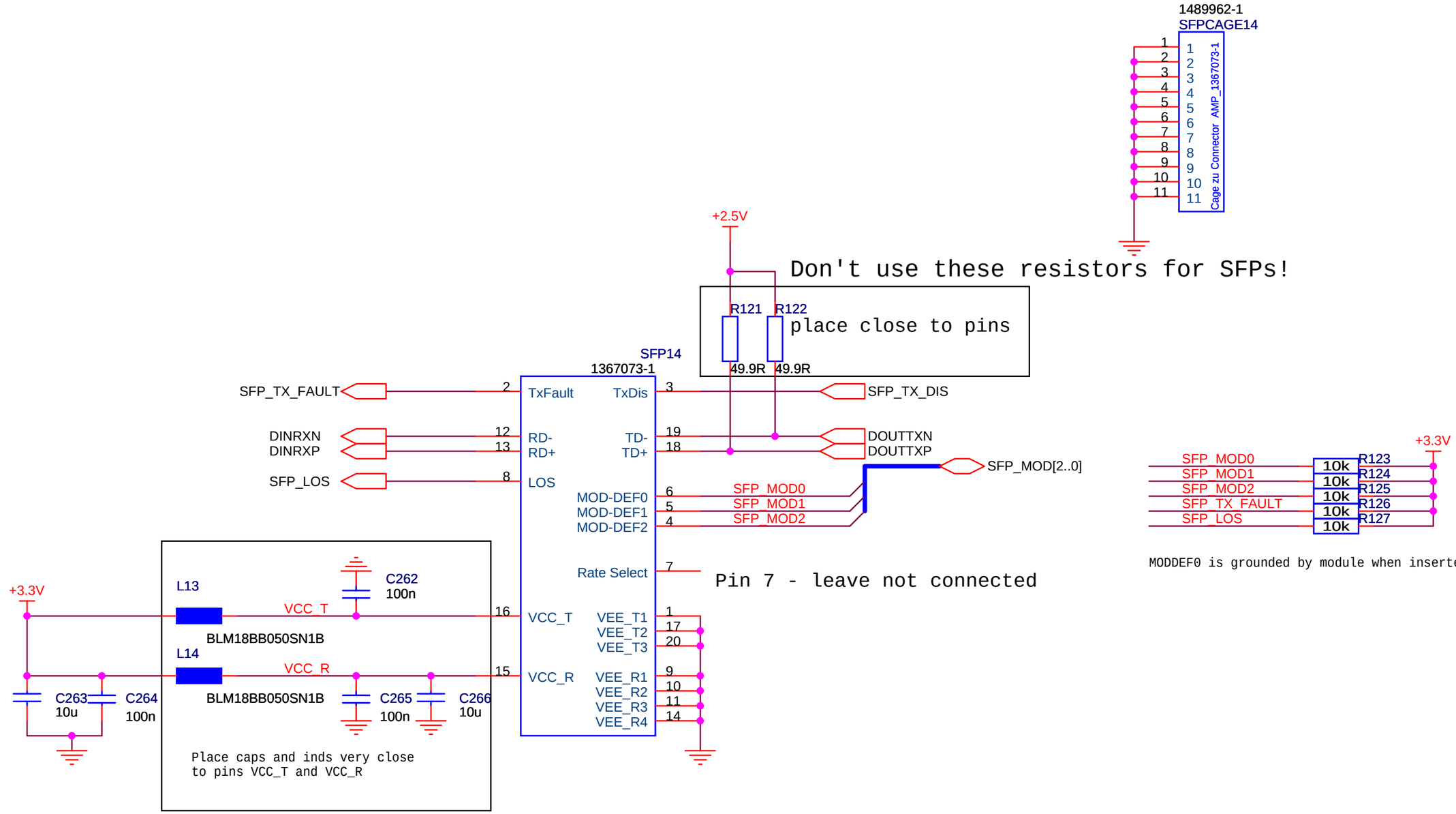




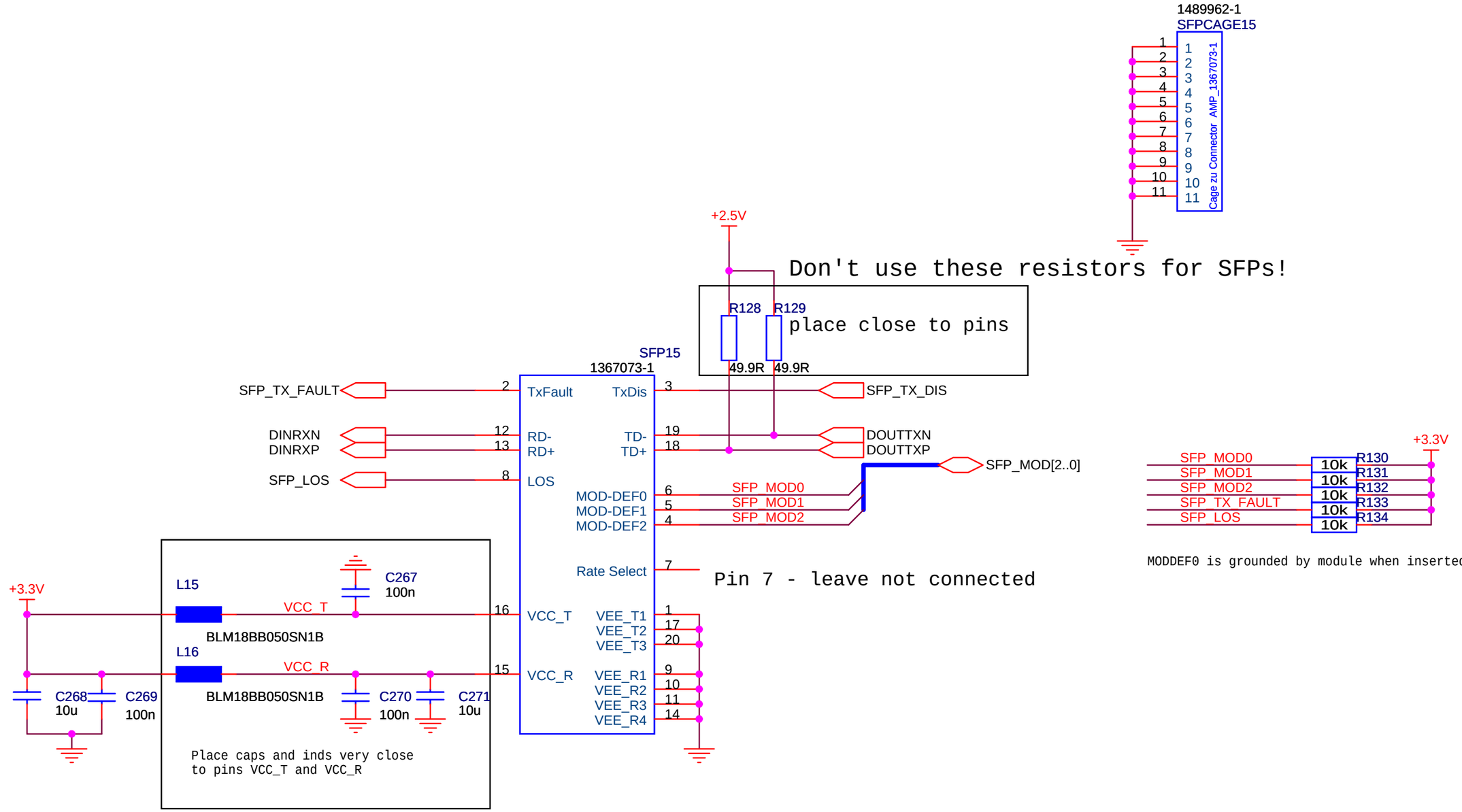
Title	**09_CLOCKING**	
Size A4	Document Number <Doc>	Rev <RevCo
Date: Friday, May 04, 2007	Sheet 9 of 25	



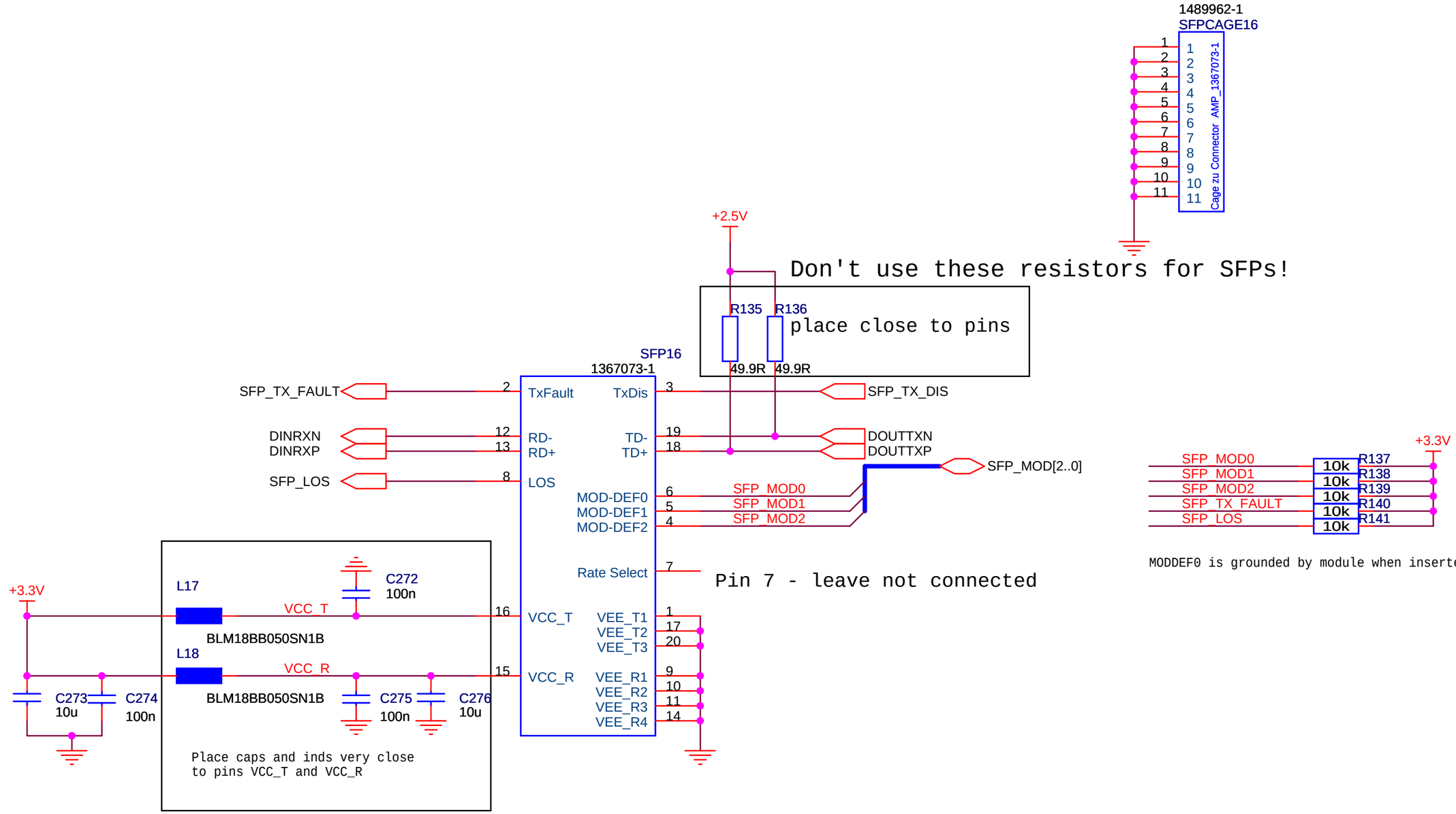
Title	SFP	
Size A4	Document Number <Doc>	Rev <RevCo
Date: Friday, May 04, 2007	Sheet 10 of 25	



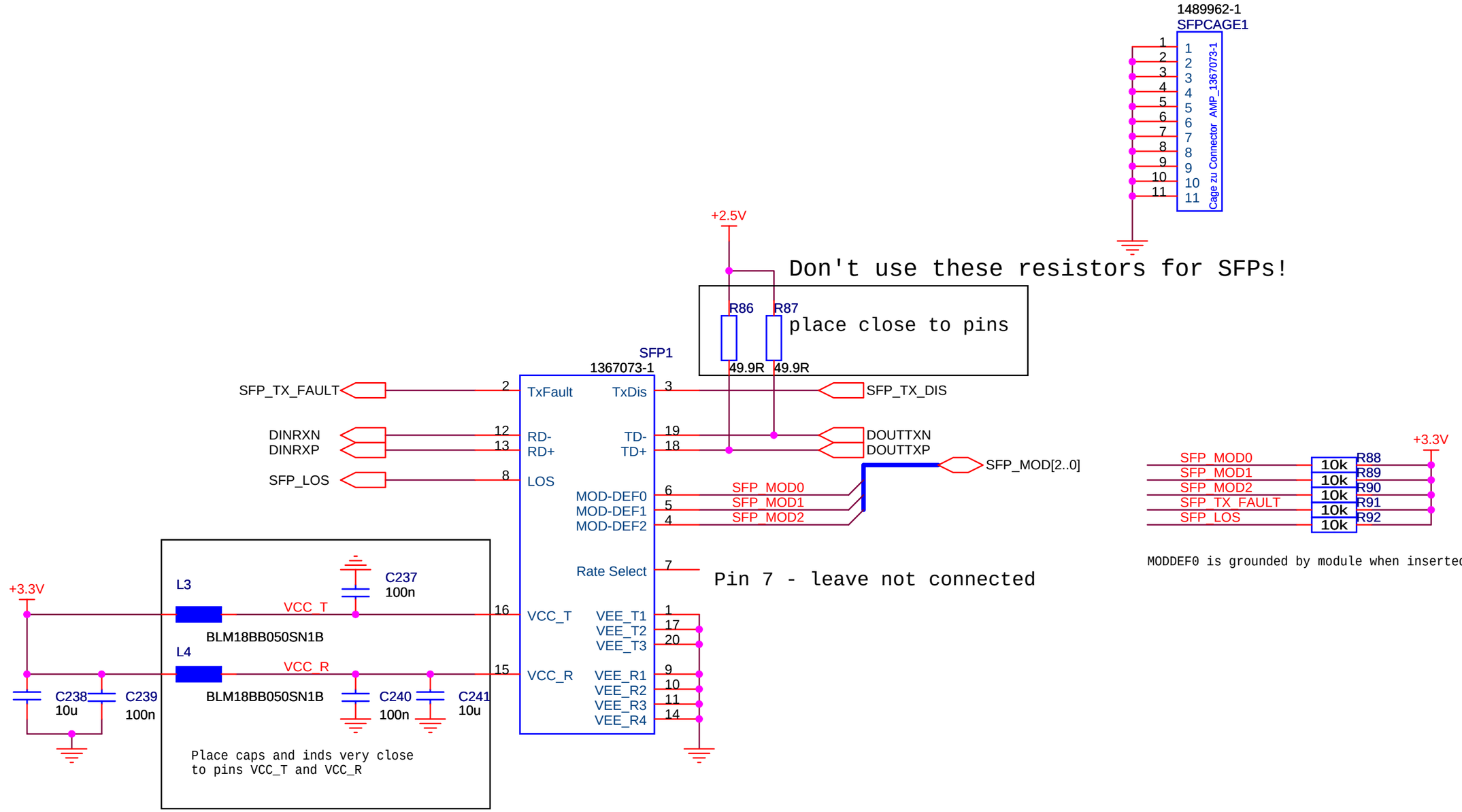
Title	SFP	
Size A4	Document Number <Doc>	Rev <RevCo
Date: Friday, May 04, 2007	Sheet 11 of 25	



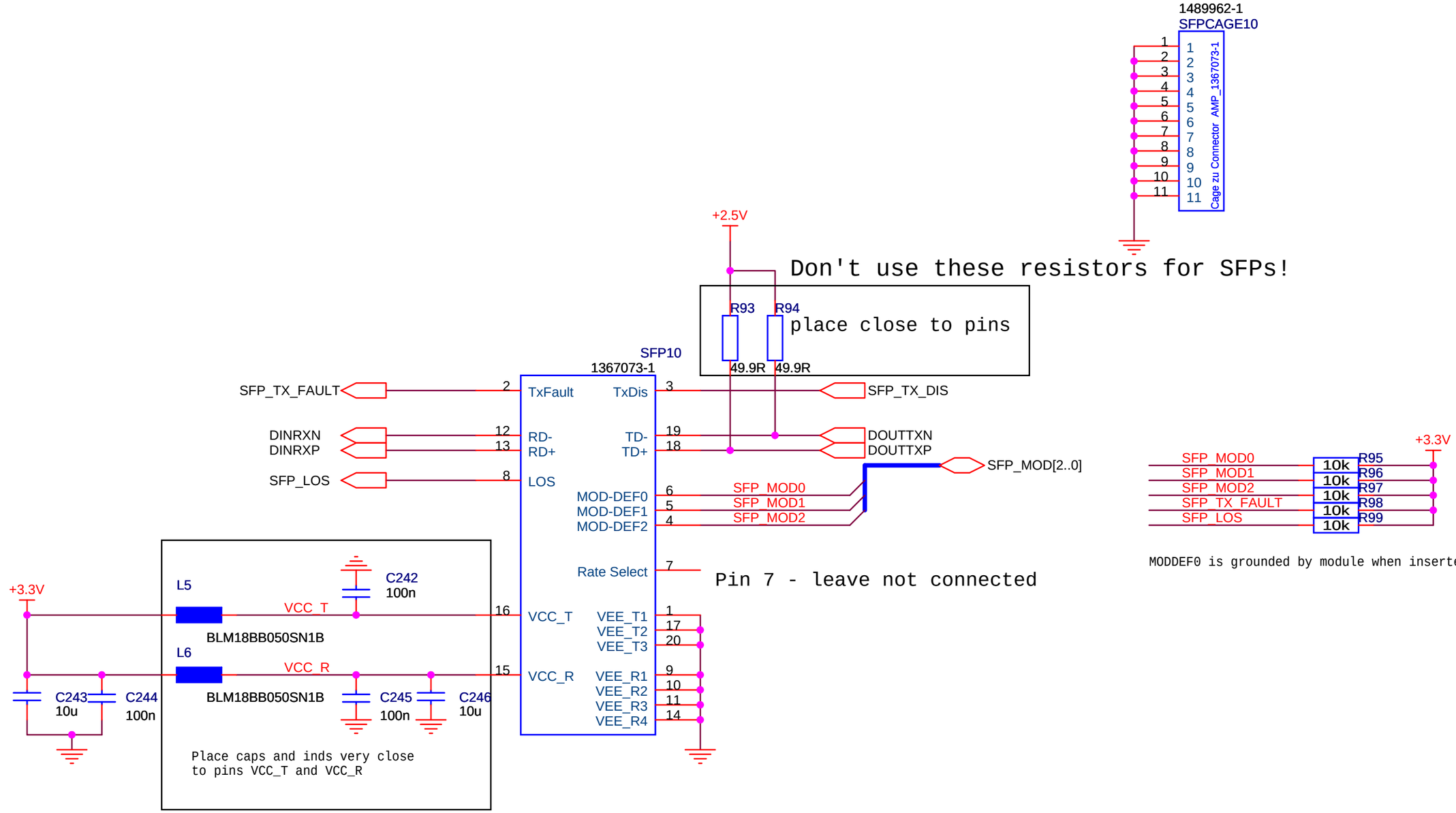
Title	SFP	
Size A4	Document Number <Doc>	Rev <RevCo
Date: Friday, May 04, 2007	Sheet 12 of 25	



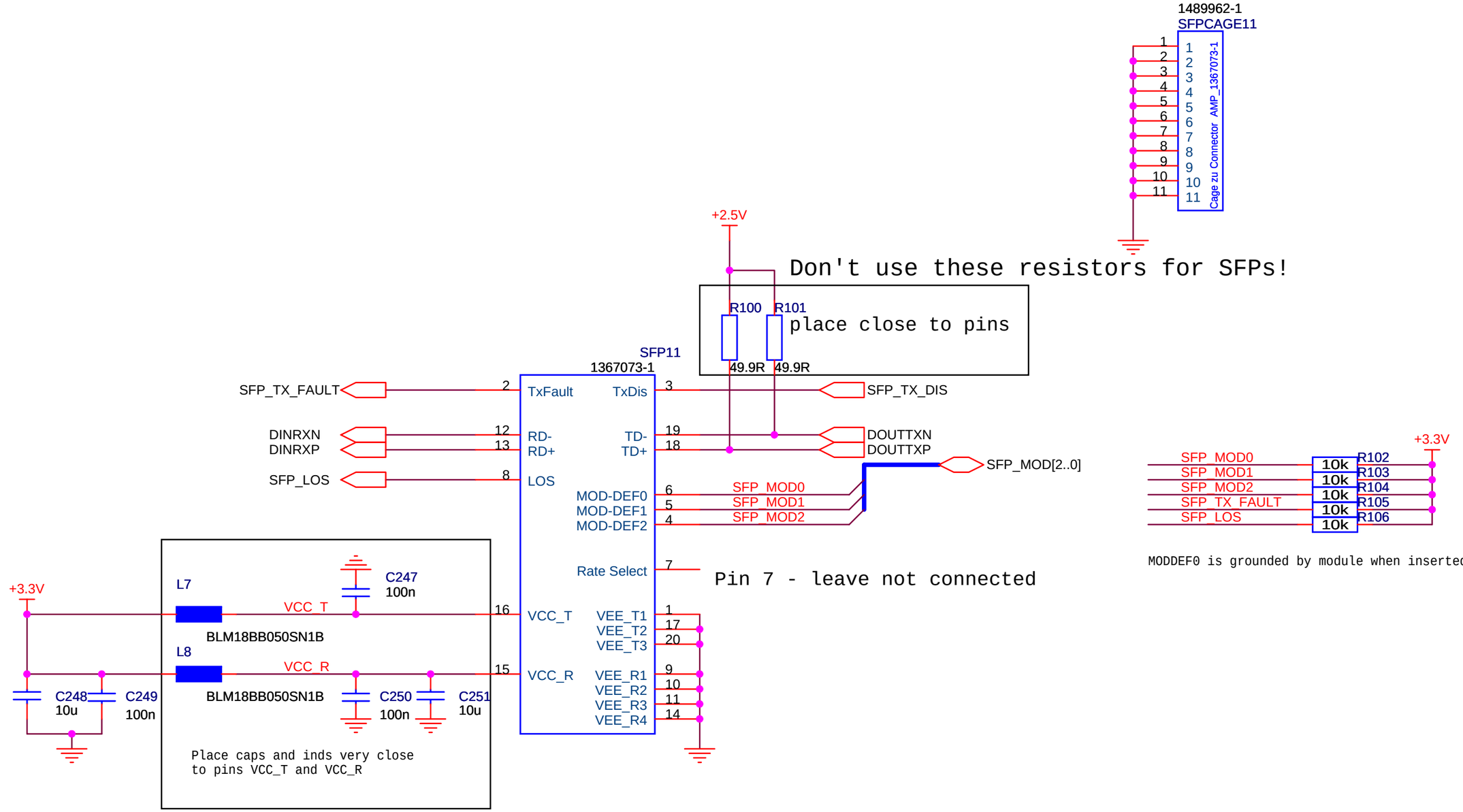
Title	SFP	
Size A4	Document Number <Doc>	Rev <RevCo
Date: Friday, May 04, 2007	Sheet 13 of 25	



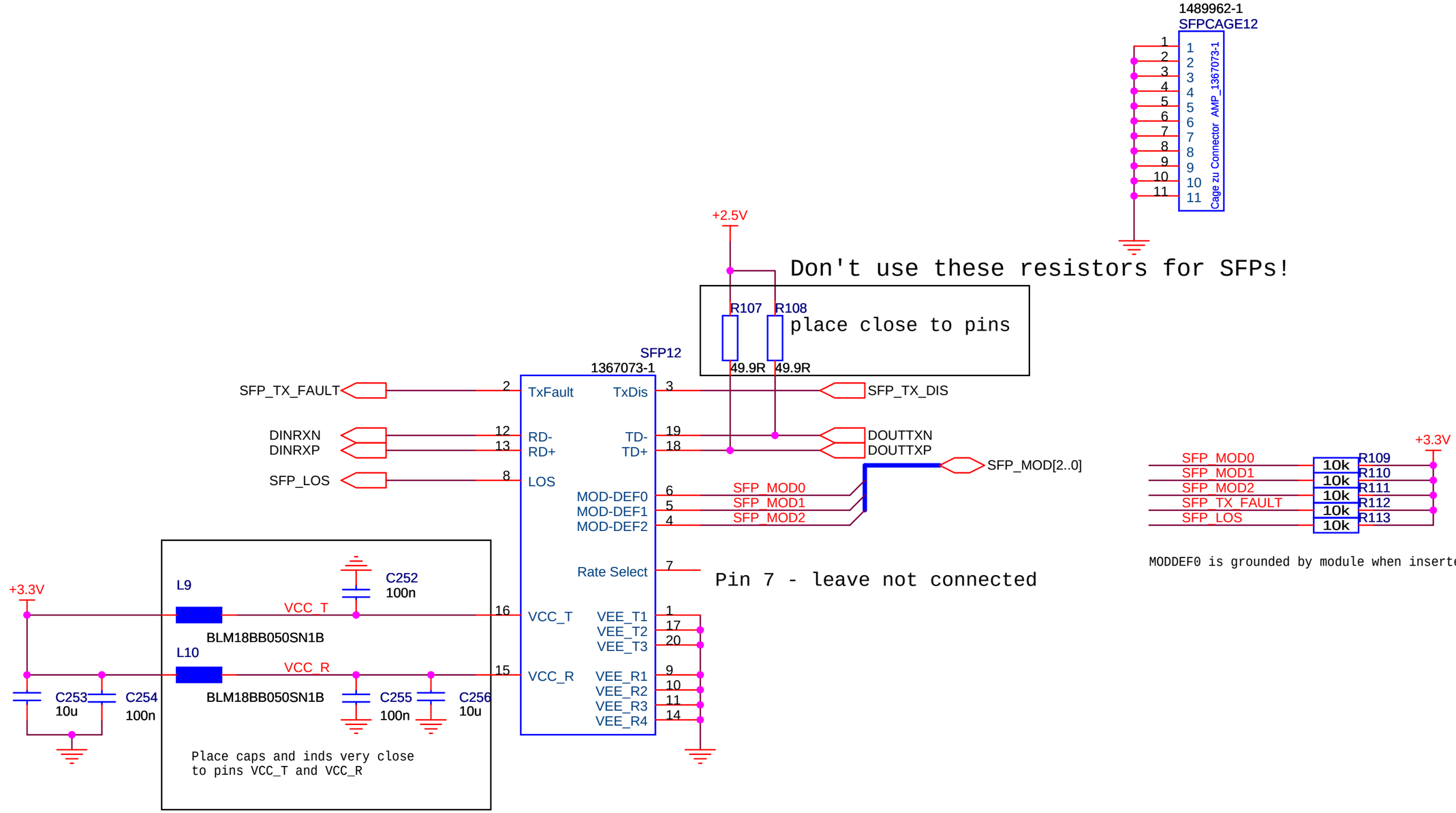
Title	SFP	
Size A4	Document Number <Doc>	Rev <RevCo
Date: Friday, May 04, 2007	Sheet 14 of 25	



Title	SFP	
Size A4	Document Number <Doc>	Rev <RevCo
Date: Friday, May 04, 2007	Sheet 15 of 25	



Title	SFP	
Size A4	Document Number <Doc>	Rev <RevCo
Date: Friday, May 04, 2007	Sheet 16 of 25	



Title	SFP	
Size A4	Document Number <Doc>	Rev <RevCo
Date: Friday, May 04, 2007	Sheet 17 of 25	

1489962-1
SFPCAGE2

Cage zu Connector AMP_1367073-1

Don't use these resistors for SFPs!

+2.5V

R142 R143
place close to pins
49.9R 49.9R

SFP2
1367073-1

SFP_TX_FAULT — 2 TxFault
SFP_TX_DIS — 3 TxDis
DINRXN — 12 RD-
DINRXP — 13 RD+
DOUTTXN — 19 TD-
DOUTTXP — 18 TD+
SFP_LOS — 8 LOS
SFP_MOD[2..0]
MOD-DEF0 — 6 — SFP_MOD0
MOD-DEF1 — 5 — SFP_MOD1
MOD-DEF2 — 4 — SFP_MOD2
Rate Select — 7

Pin 7 - leave not connected

VCC_T — 16
VCC_R — 15
VEE_T1 — 1
VEE_T2 — 17
VEE_T3 — 20
VEE_R1 — 9
VEE_R2 — 10
VEE_R3 — 11
VEE_R4 — 14

+3.3V

L19 BLM18BB050SN1B
L20 BLM18BB050SN1B
C277 100n
C278 10u
C279 100n
C280 100n
C281 10u

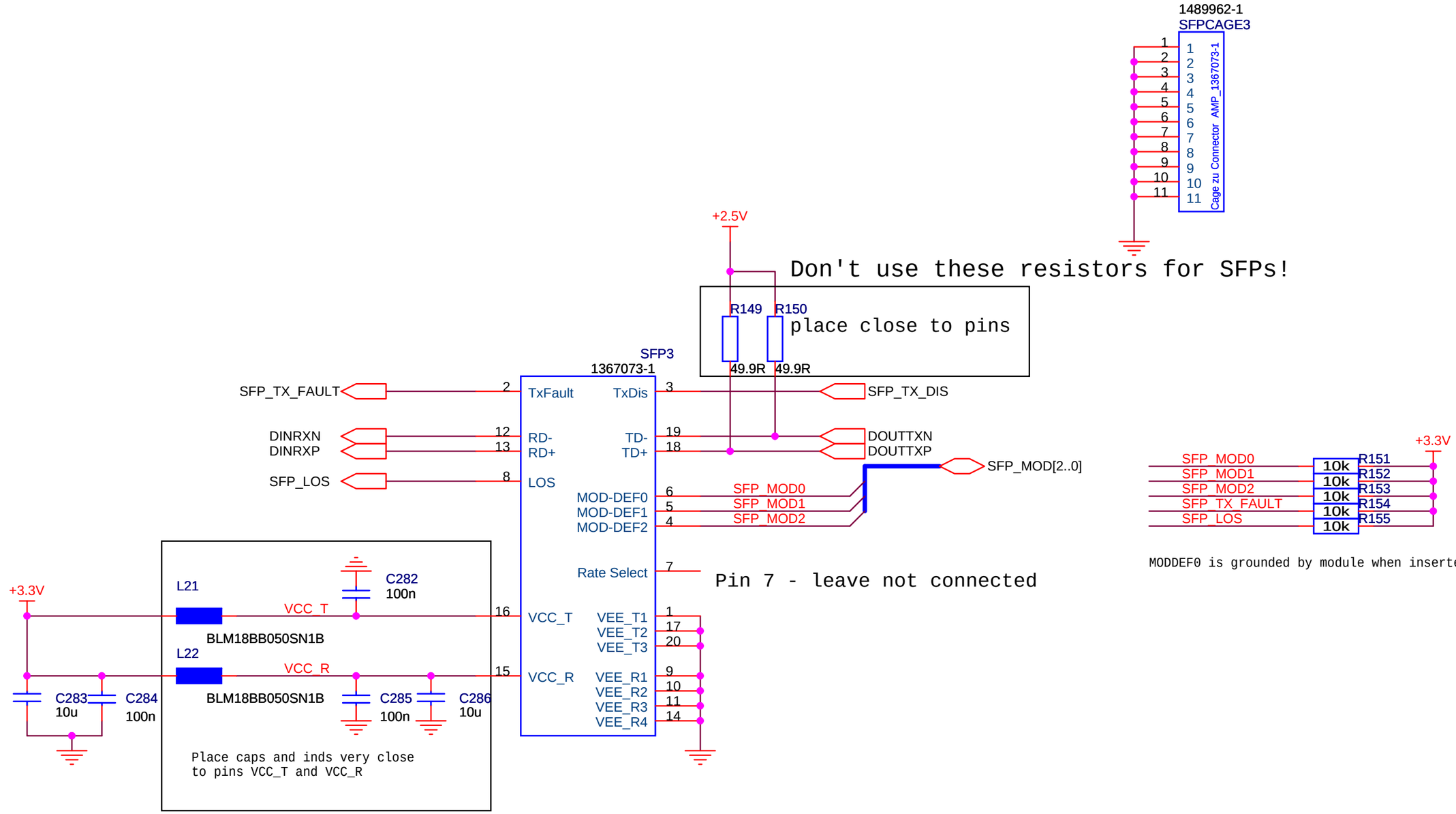
Place caps and inds very close
to pins VCC_T and VCC_R

+3.3V

SFP_MOD0 — 10k — R144
SFP_MOD1 — 10k — R145
SFP_MOD2 — 10k — R146
SFP_TX_FAULT — 10k — R147
SFP_LOS — 10k — R148

MODDEF0 is grounded by module when inserted

Title: SFP		
Size: A4	Document Number: <Doc>	Rev: <RevCo
Date: Friday, May 04, 2007	Sheet 18 of 25	



Title	SFP	
Size A4	Document Number <Doc>	Rev <RevCo
Date: Friday, May 04, 2007	Sheet 19 of 25	

1489962-1
SFPCAGE4

Cage zu Connector AMP_1367073-1

Don't use these resistors for SFPs!

+2.5V

R156 R157
place close to pins
49.9R 49.9R

SFP4
1367073-1

SFP_TX_FAULT — 2 TxFault
SFP_TX_DIS — 3 TxDis
DINRXN — 12 RD-
DINRXP — 13 RD+
DOUTTXN — 19 TD-
DOUTTXP — 18 TD+
SFP_LOS — 8 LOS
SFP_MOD[2..0]
MOD-DEF0 — 6 — SFP_MOD0
MOD-DEF1 — 5 — SFP_MOD1
MOD-DEF2 — 4 — SFP_MOD2
Rate Select — 7

Pin 7 - leave not connected

VCC_T — 16
VCC_R — 15
VEE_T1 — 1
VEE_T2 — 17
VEE_T3 — 20
VEE_R1 — 9
VEE_R2 — 10
VEE_R3 — 11
VEE_R4 — 14

+3.3V

L23 BLM18BB050SN1B
L24 BLM18BB050SN1B
C287 100n
C288 10u
C289 100n
C290 100n
C291 10u

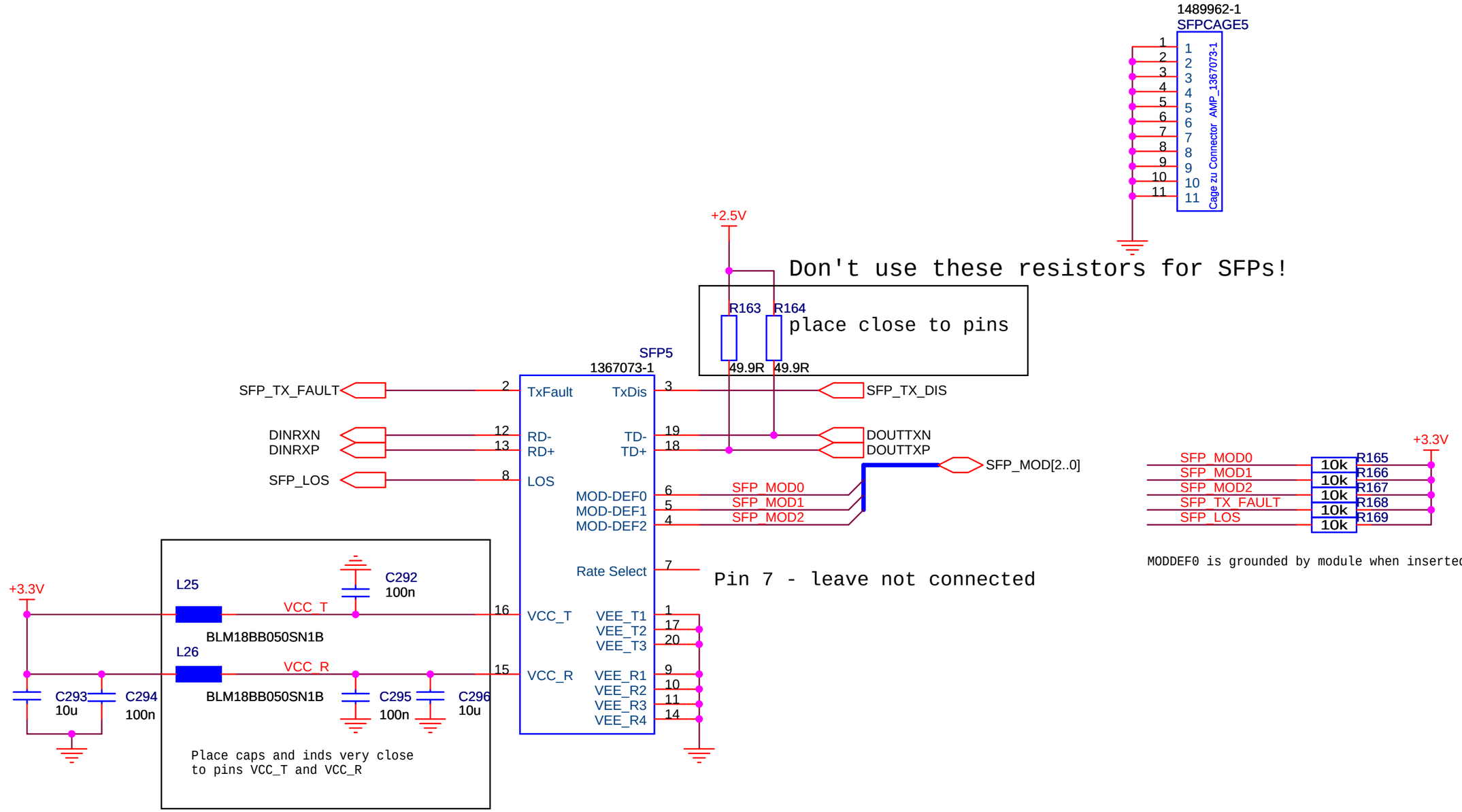
Place caps and inds very close
to pins VCC_T and VCC_R

+3.3V

SFP_MOD0 — 10k — R158
SFP_MOD1 — 10k — R159
SFP_MOD2 — 10k — R160
SFP_TX_FAULT — 10k — R161
SFP_LOS — 10k — R162

MODDEF0 is grounded by module when inserted

Title: SFP		
Size: A4	Document Number: <Doc>	Rev: <RevCo
Date: Friday, May 04, 2007	Sheet 20 of 25	



Title	SFP	
Size A4	Document Number <Doc>	Rev <RevCo
Date: Friday, May 04, 2007	Sheet 21 of 25	

1489962-1
SFPCAGE6

Cage zu Connector AMP_1367073-1

Don't use these resistors for SFPs!

+2.5V

R170 R171
place close to pins
49.9R 49.9R

SFP6
1367073-1

SFP_TX_FAULT — 2 TxFault
SFP_TX_DIS — 3 TxDis
DINRXN — 12 RD-
DINRXP — 13 RD+
DOUTTXN — 19 TD-
DOUTTXP — 18 TD+
SFP_LOS — 8 LOS
SFP_MOD[2..0]
MOD-DEF0 — 6 — SFP_MOD0
MOD-DEF1 — 5 — SFP_MOD1
MOD-DEF2 — 4 — SFP_MOD2
Rate Select — 7

Pin 7 - leave not connected

VCC_T — 16
VCC_R — 15
VEE_T1 — 1
VEE_T2 — 17
VEE_T3 — 20
VEE_R1 — 9
VEE_R2 — 10
VEE_R3 — 11
VEE_R4 — 14

+3.3V

L27 BLM18BB050SN1B VCC_T
L28 BLM18BB050SN1B VCC_R

C297 100n
C298 10u
C299 100n
C300 100n
C301 10u

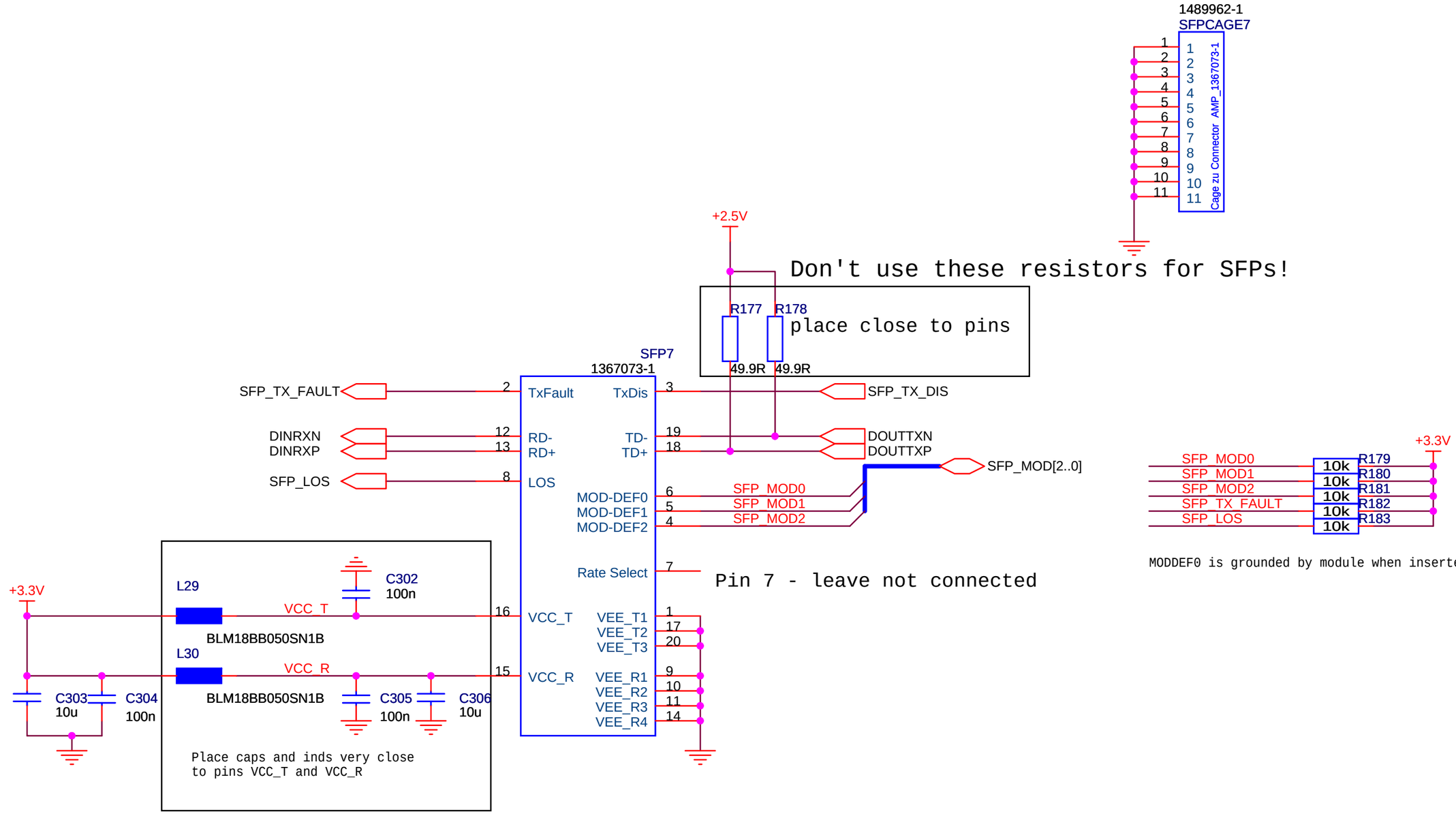
Place caps and inds very close
to pins VCC_T and VCC_R

+3.3V

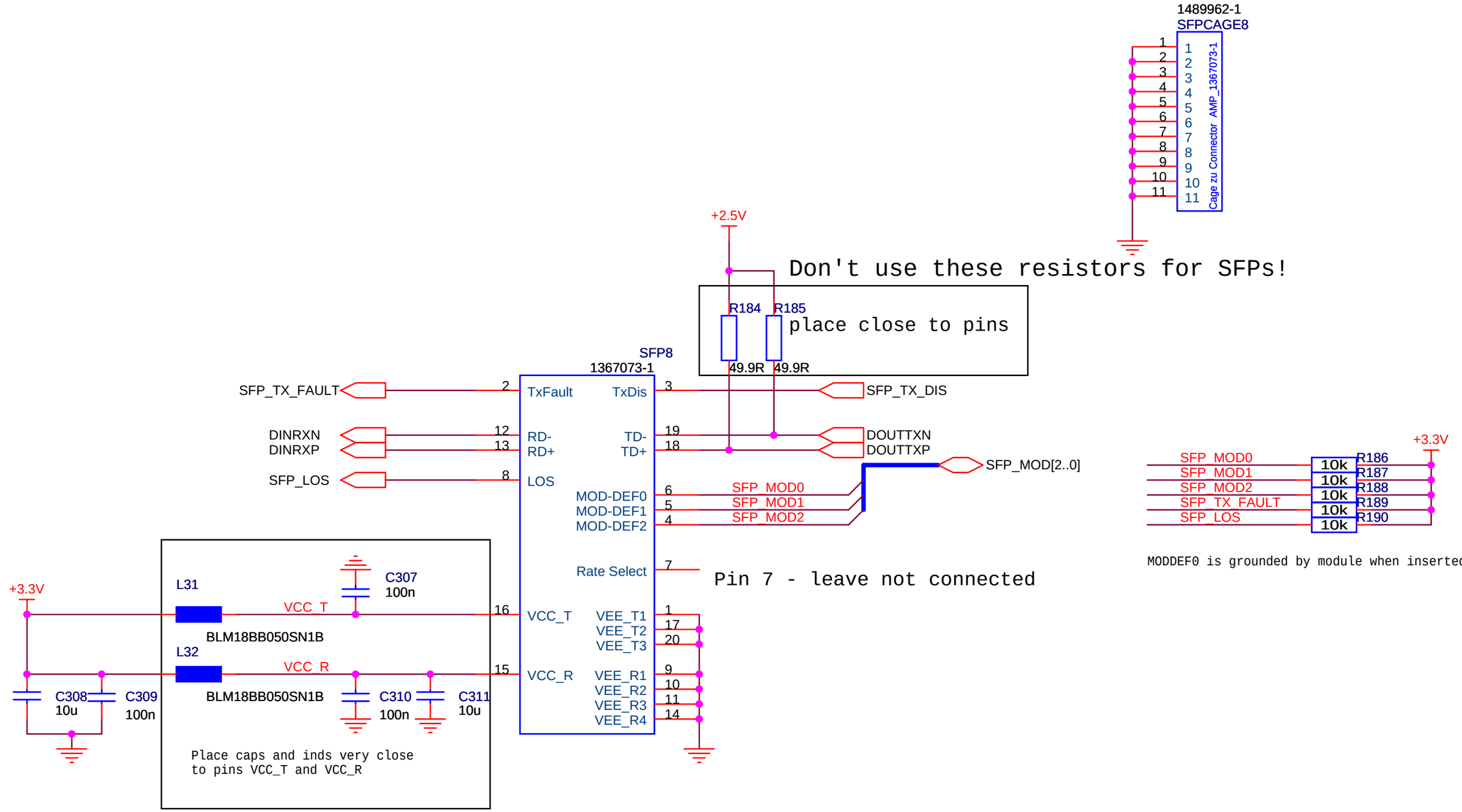
SFP_MOD0 — 10k — R172
SFP_MOD1 — 10k — R173
SFP_MOD2 — 10k — R174
SFP_TX_FAULT — 10k — R175
SFP_LOS — 10k — R176

MODDEF0 is grounded by module when inserted

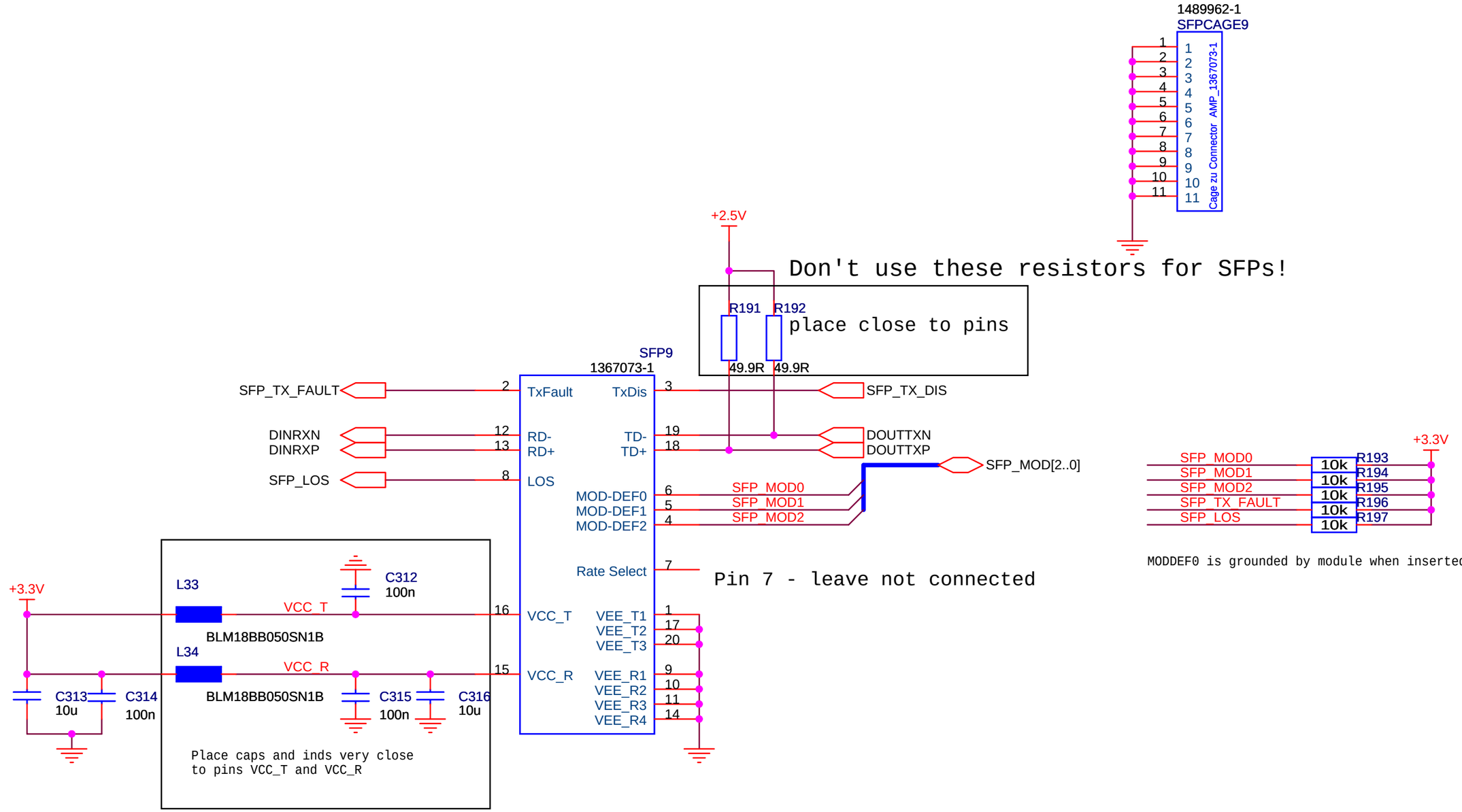
Title: SFP		
Size: A4	Document Number: <Doc>	Rev: <RevCo
Date: Friday, May 04, 2007	Sheet 22 of 25	



Title	SFP	
Size A4	Document Number <Doc>	Rev <RevCo
Date: Friday, May 04, 2007	Sheet 23 of 25	



Title	SFP	
Size A4	Document Number <Doc>	Rev <RevCo
Date: Friday, May 04, 2007	Sheet 24 of 25	



Title	SFP	
Size A4	Document Number <Doc>	Rev <RevCo
Date: Friday, May 04, 2007	Sheet 25 of 25	