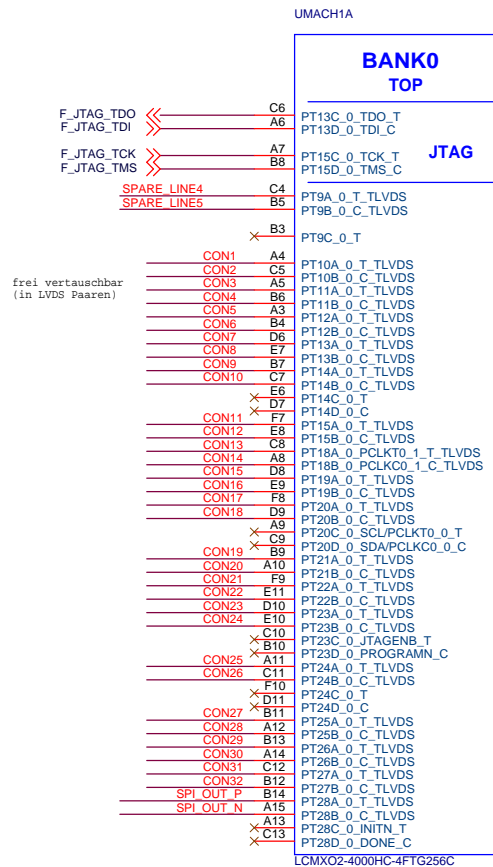
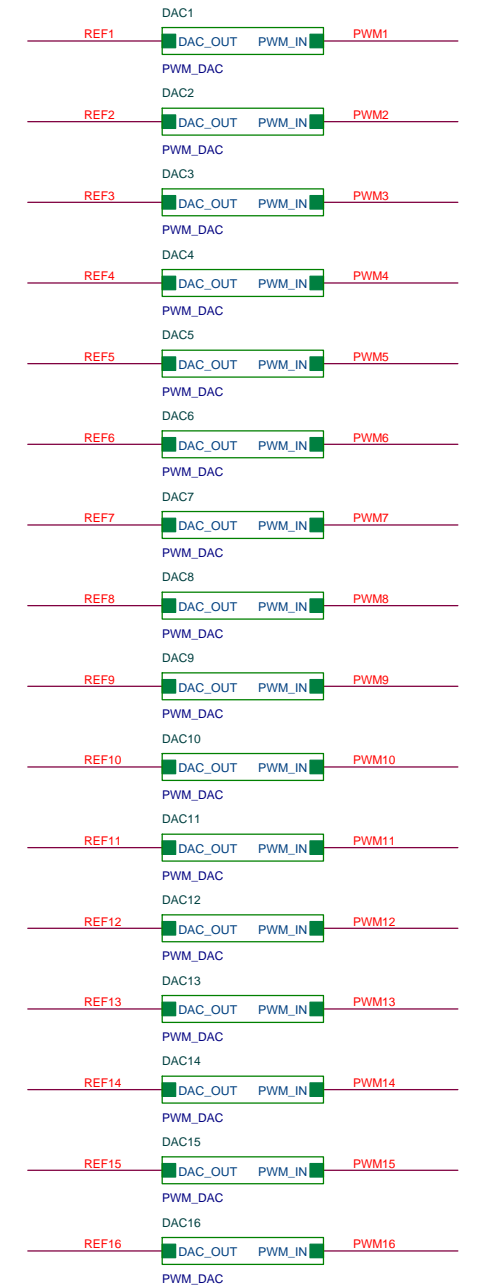
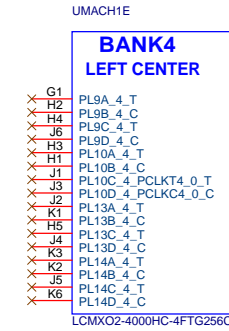
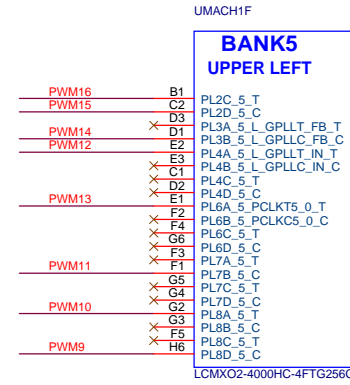
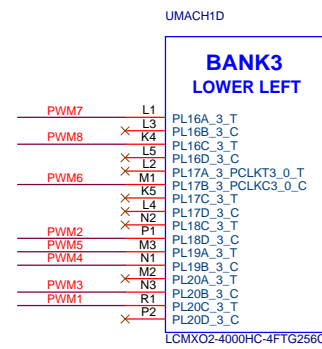


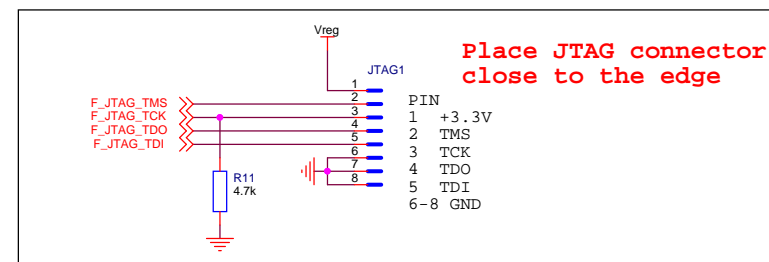
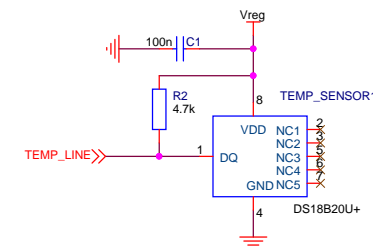
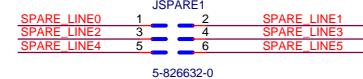
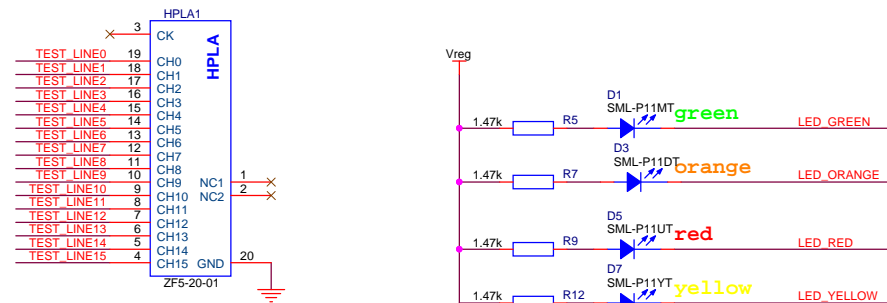
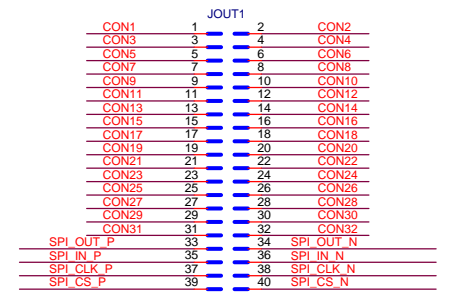
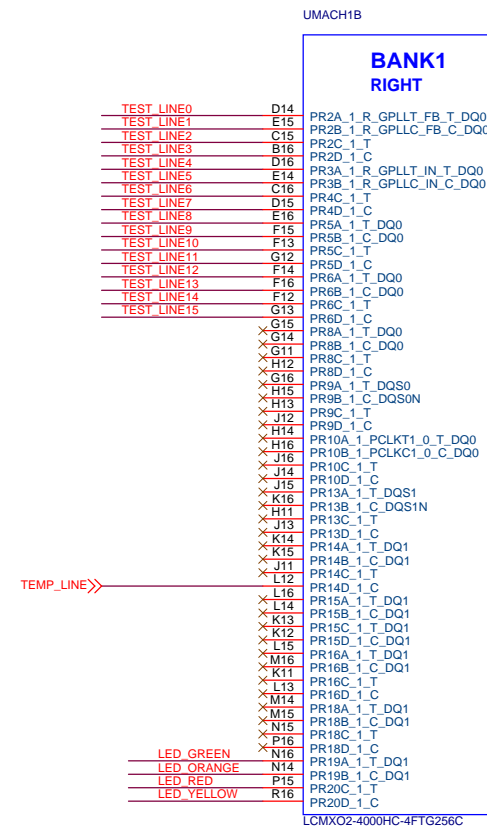
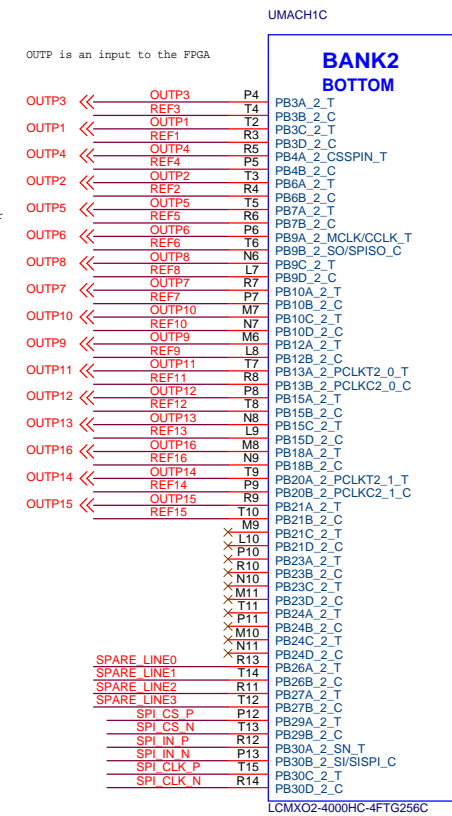
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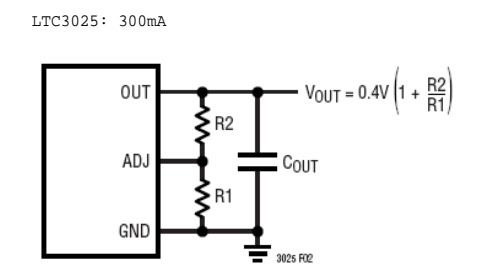
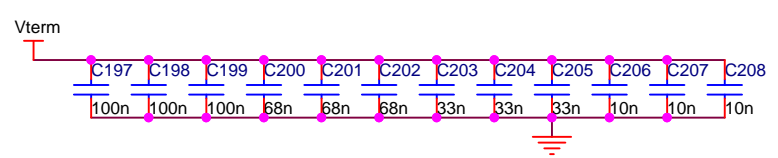
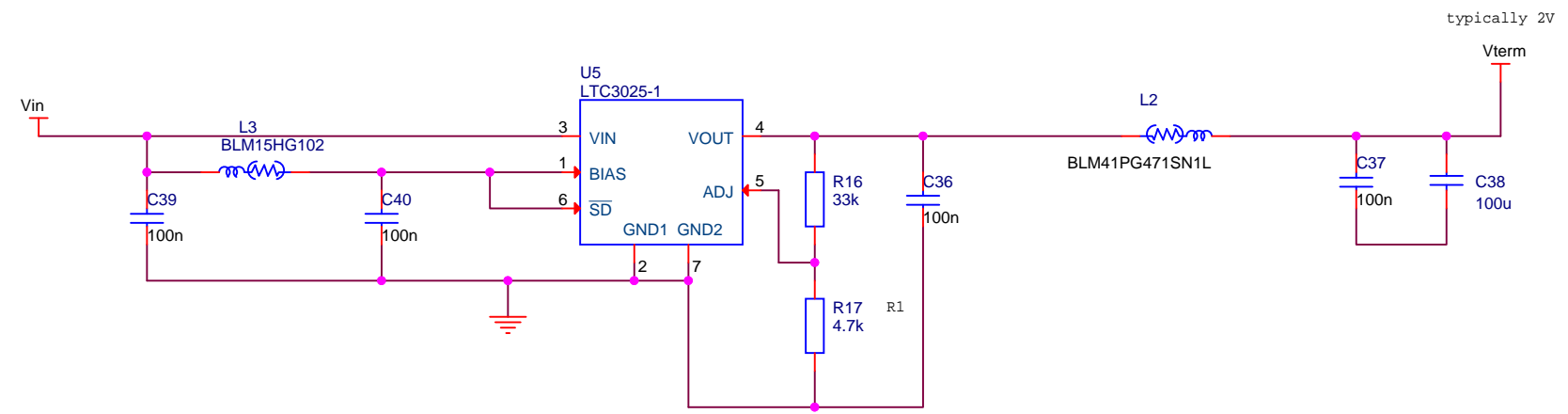
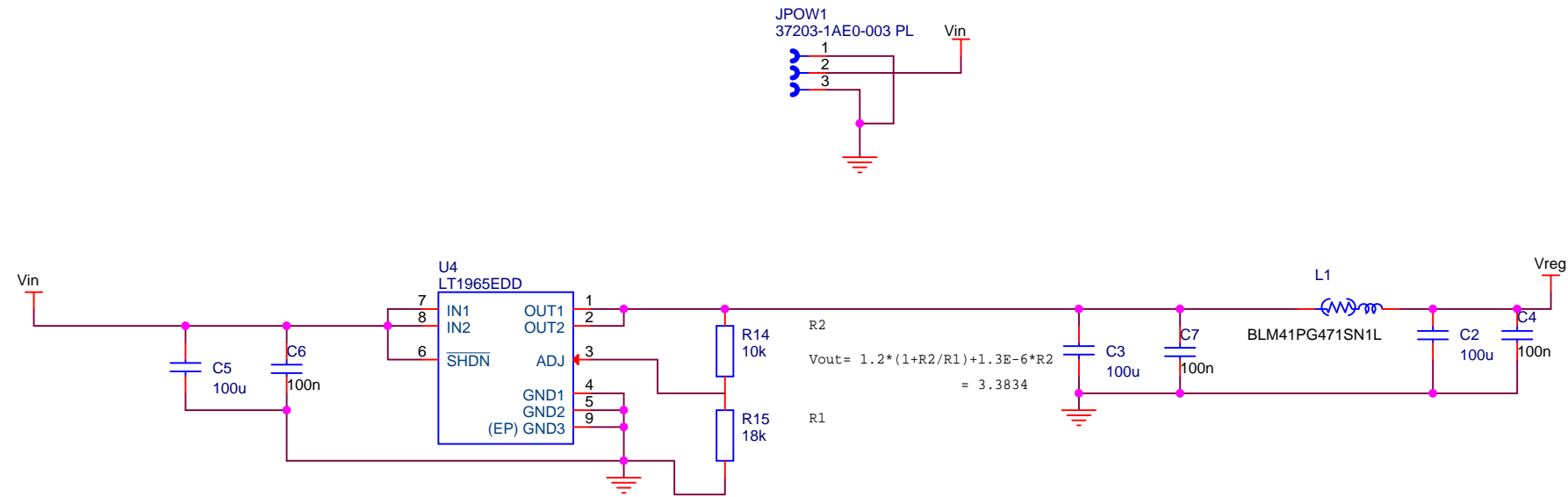
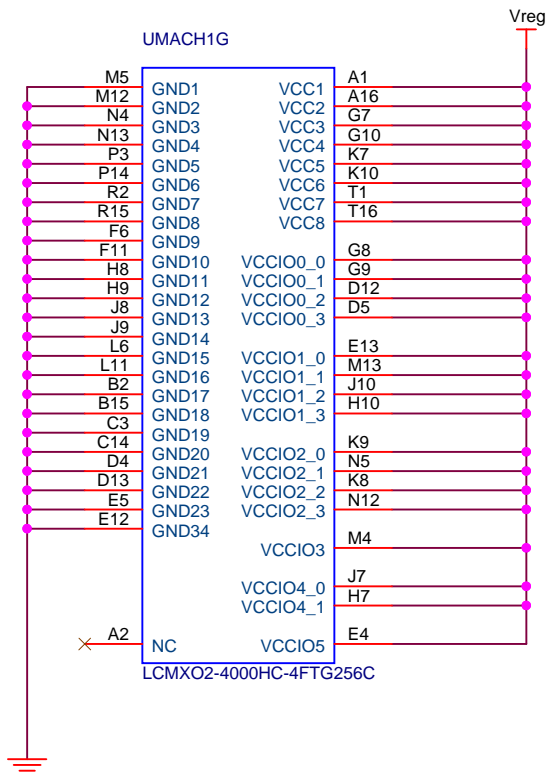
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Modified: Friday, July 20, 2012 Size: A3 Page: 1 / 35
Designer: M.Traxler Layouter: S.Voltz



Bottom side: All LVDS receiver can have a termination resistors.

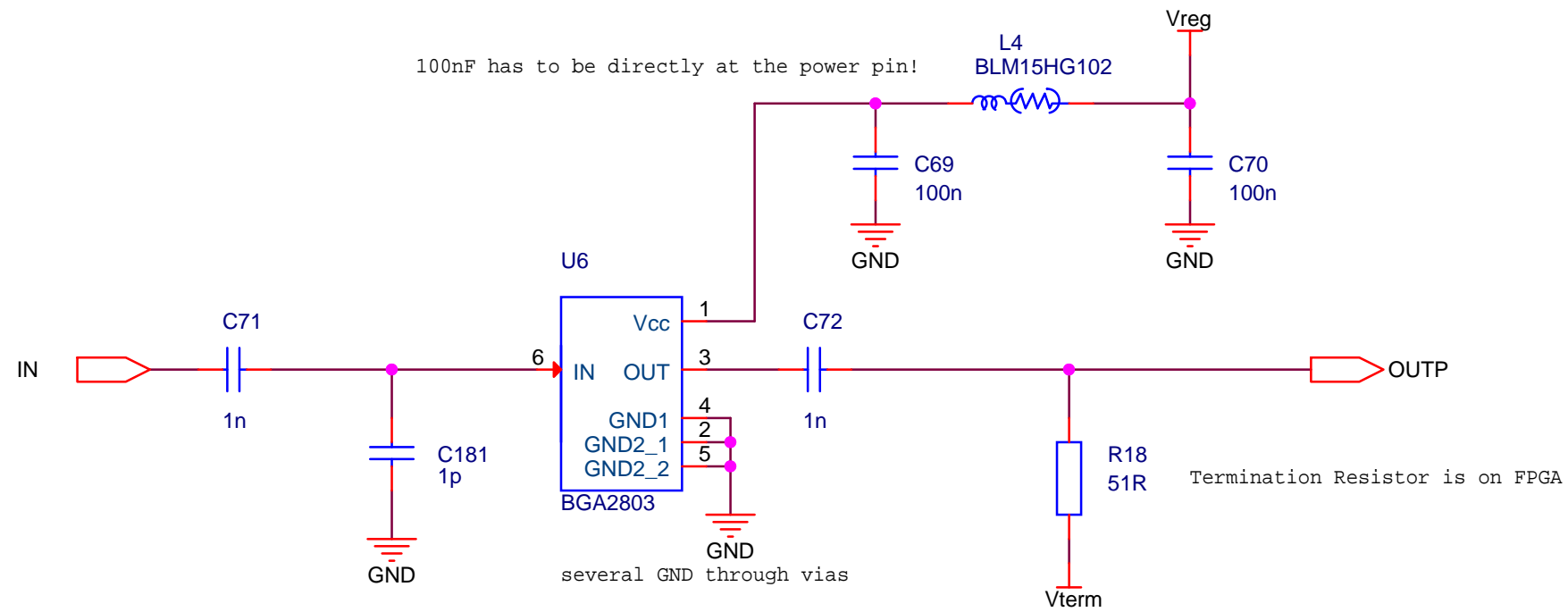




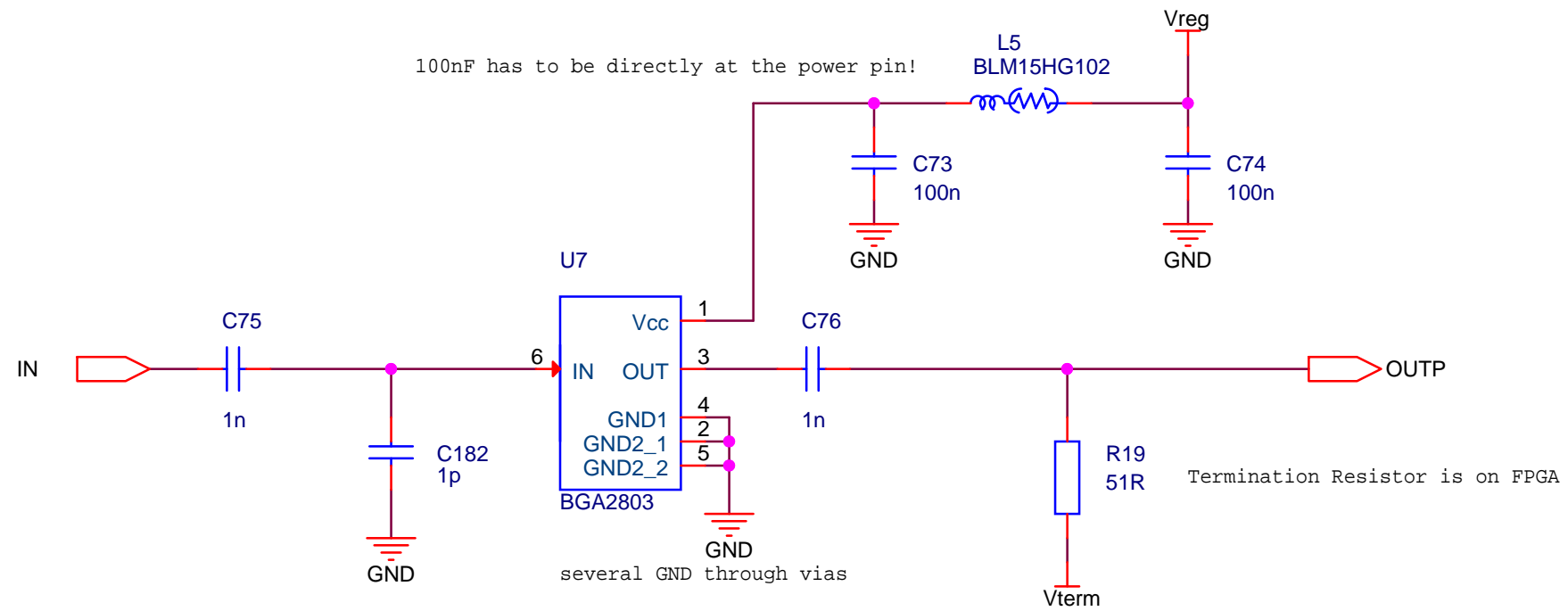
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03_FPGA-Power

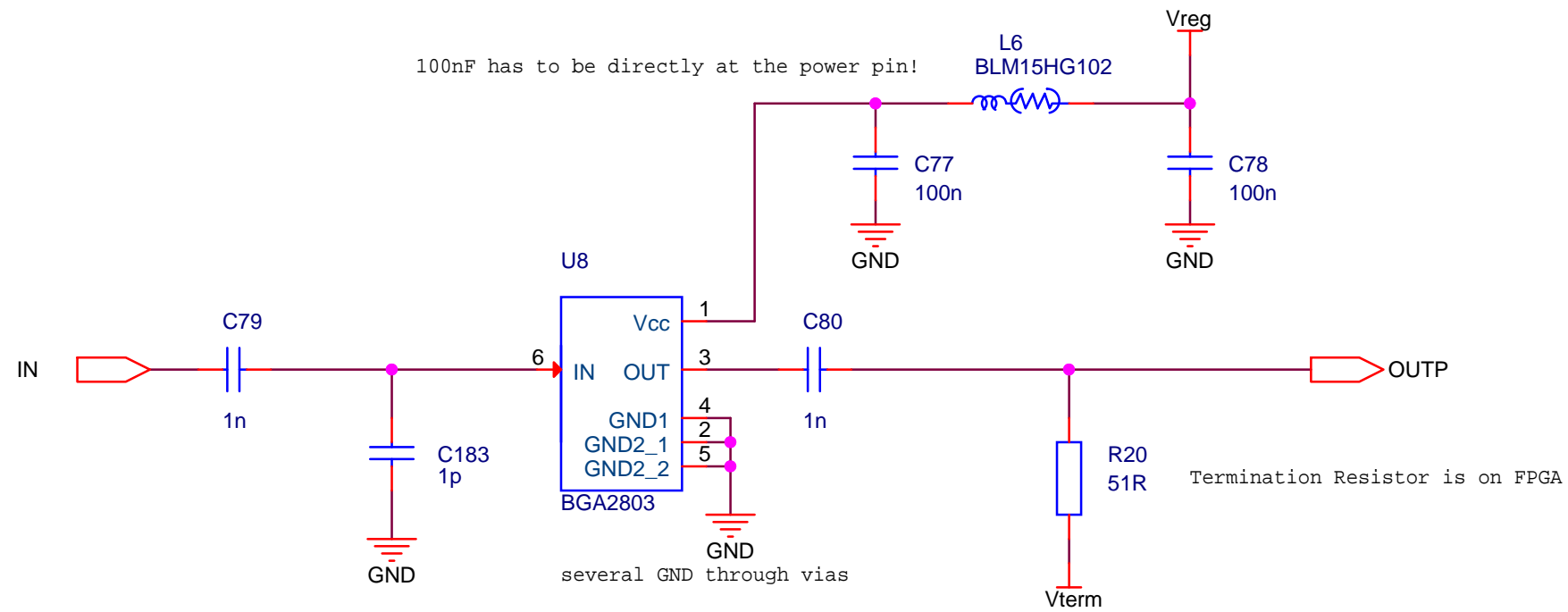
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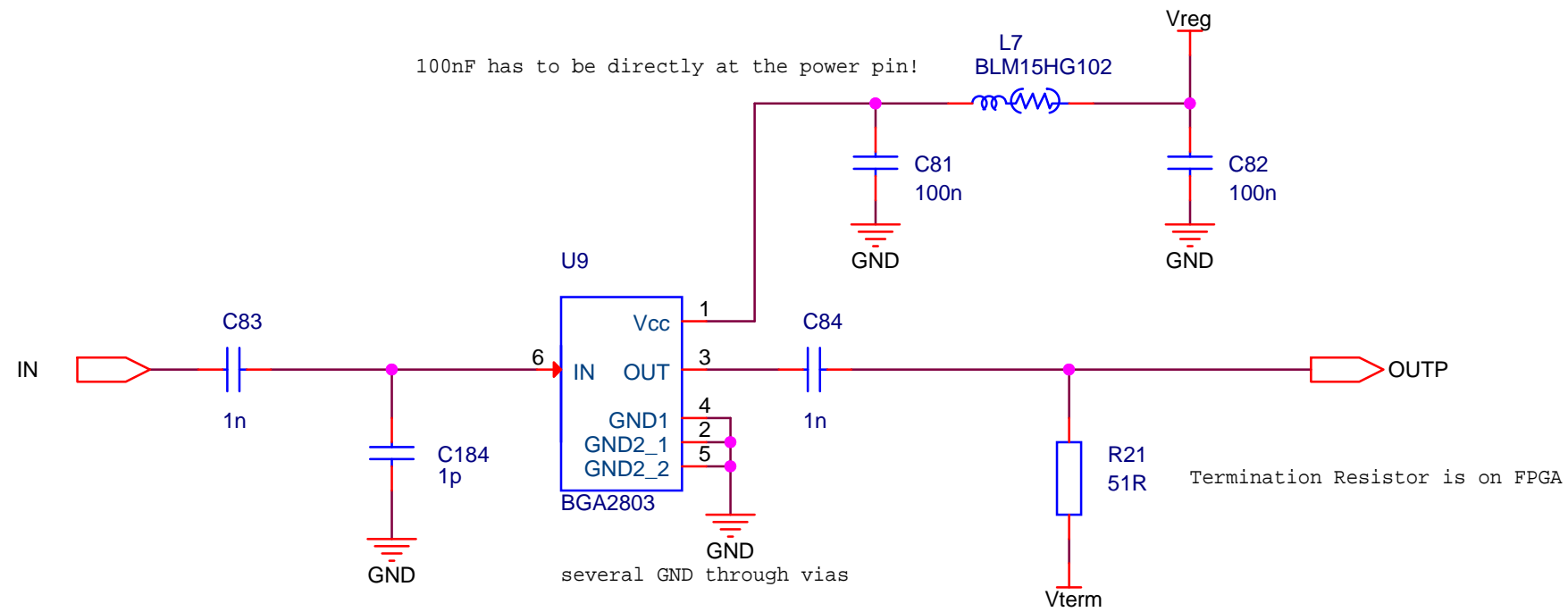
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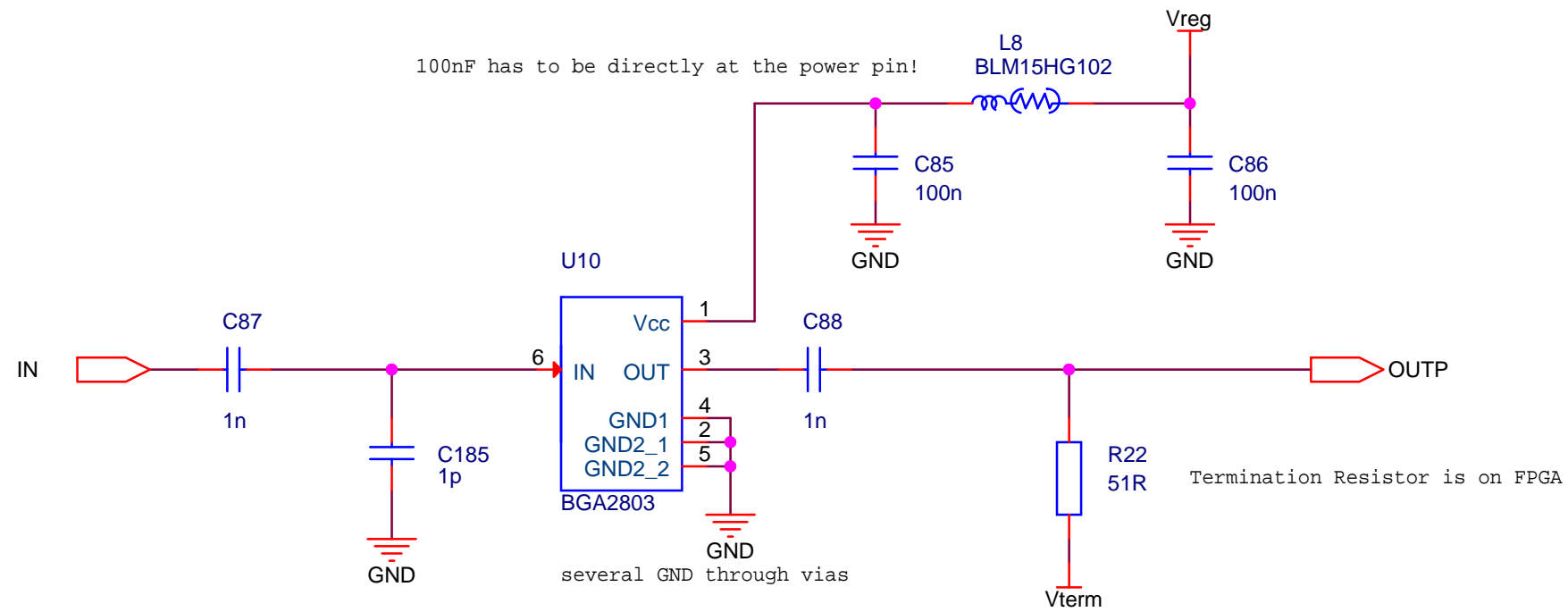
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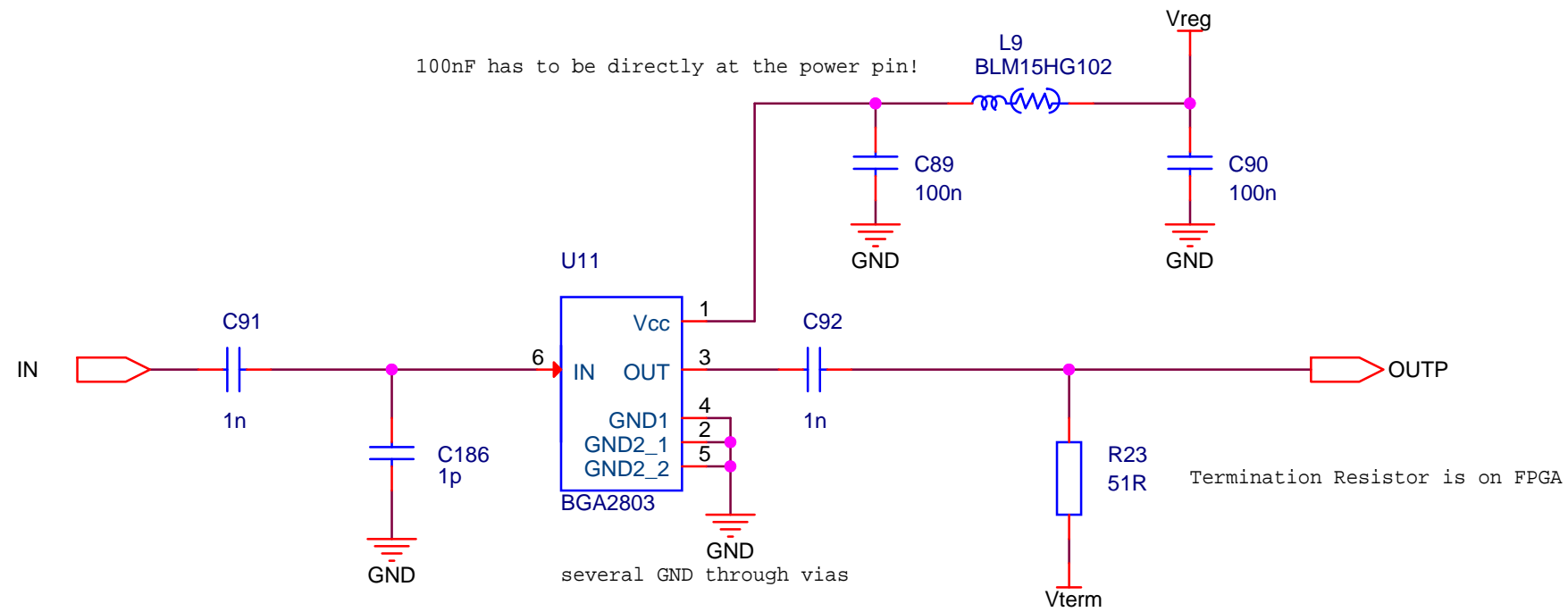
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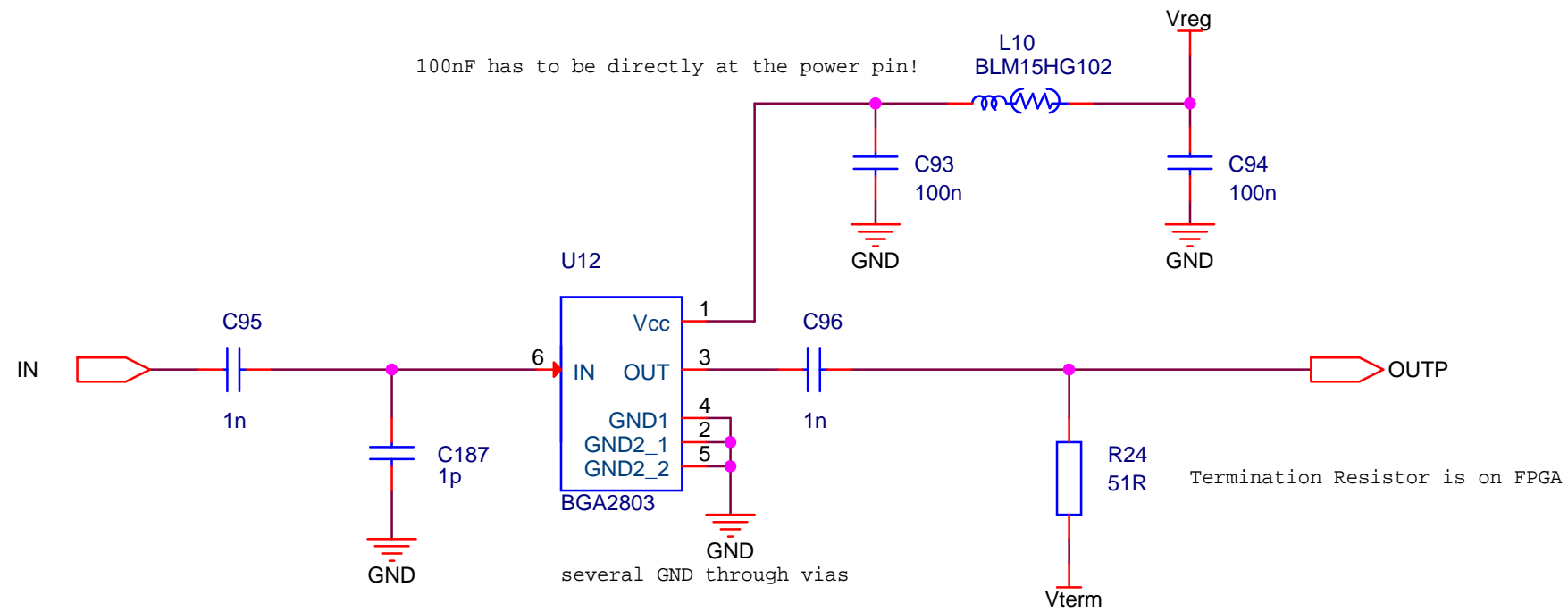
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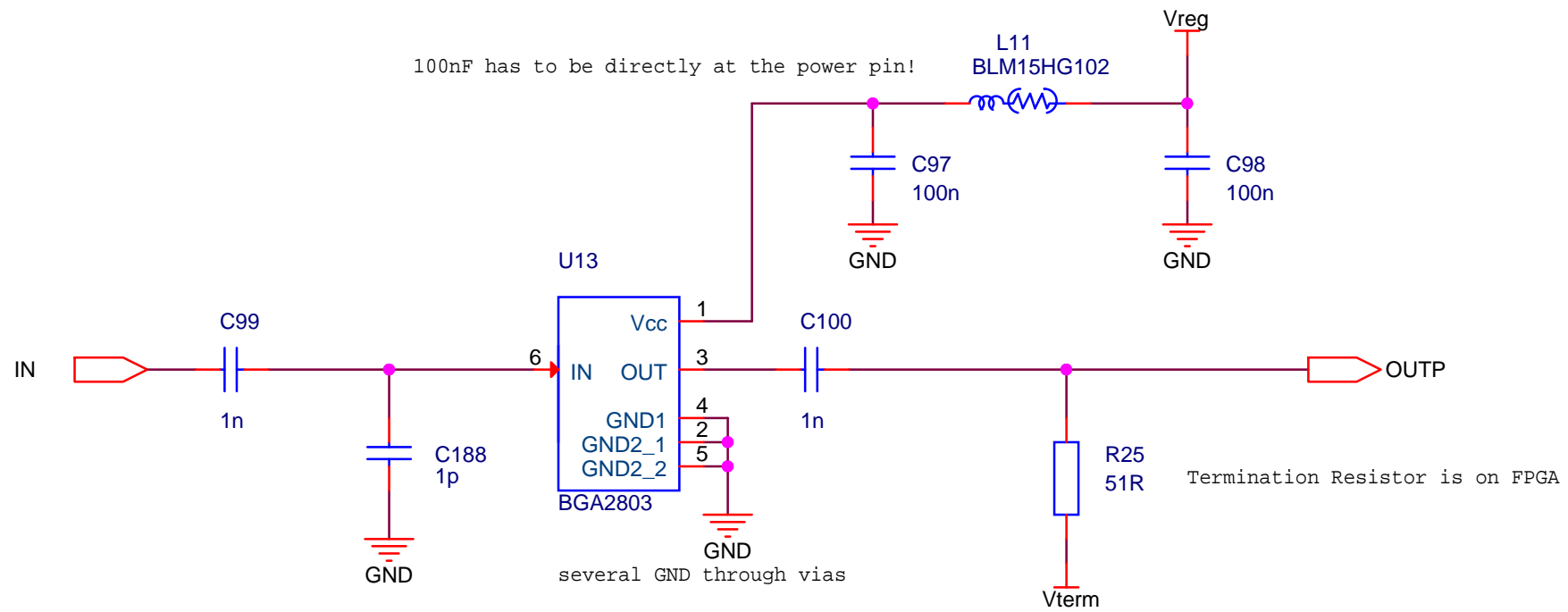
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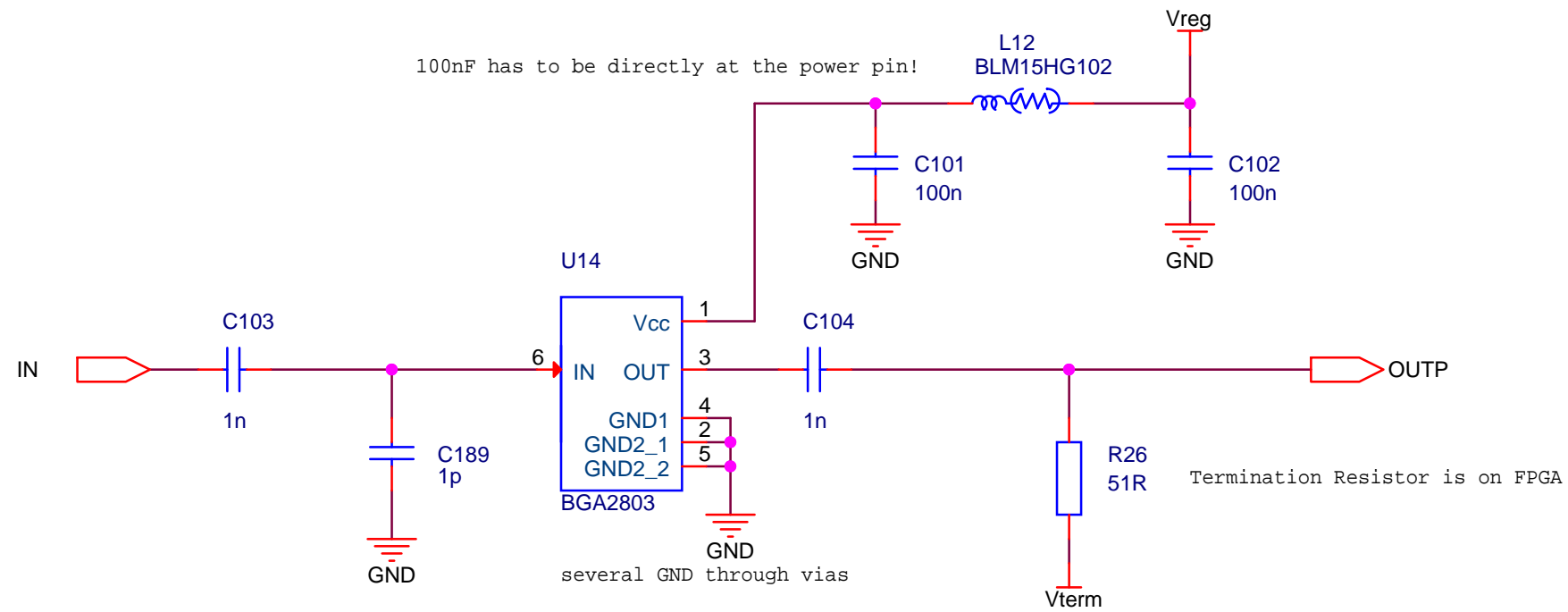
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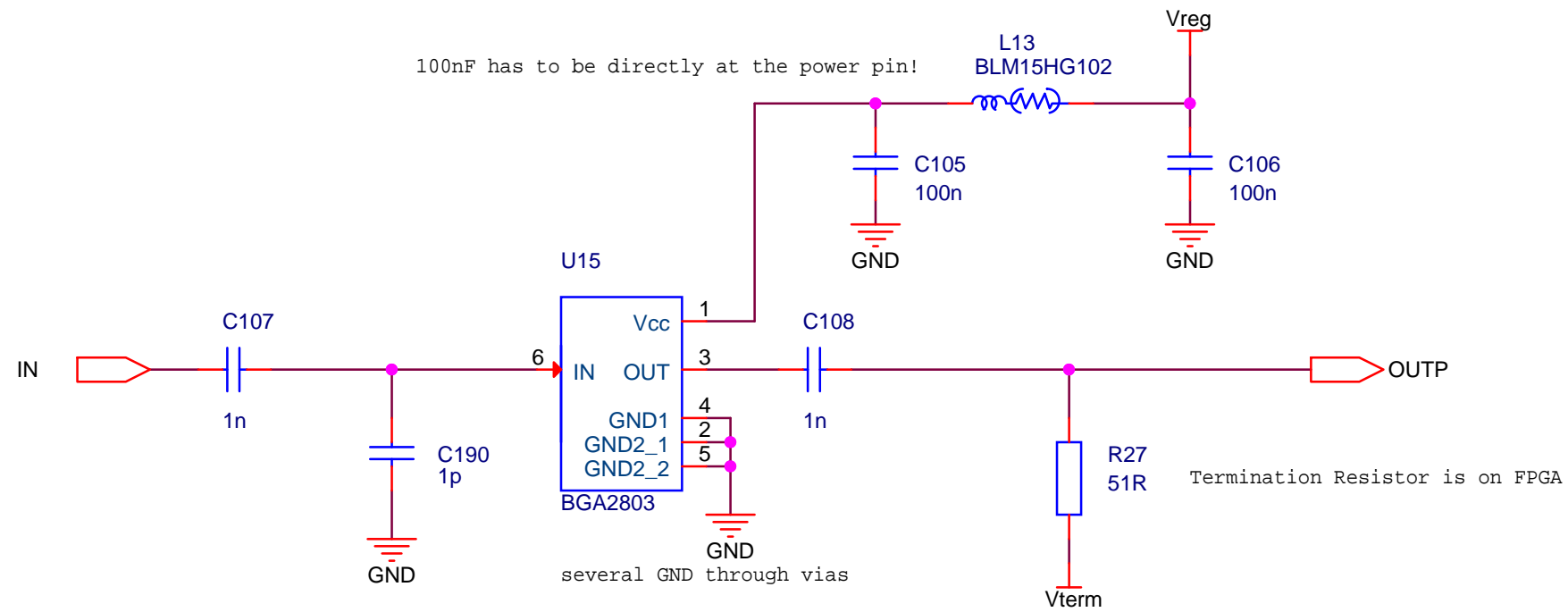
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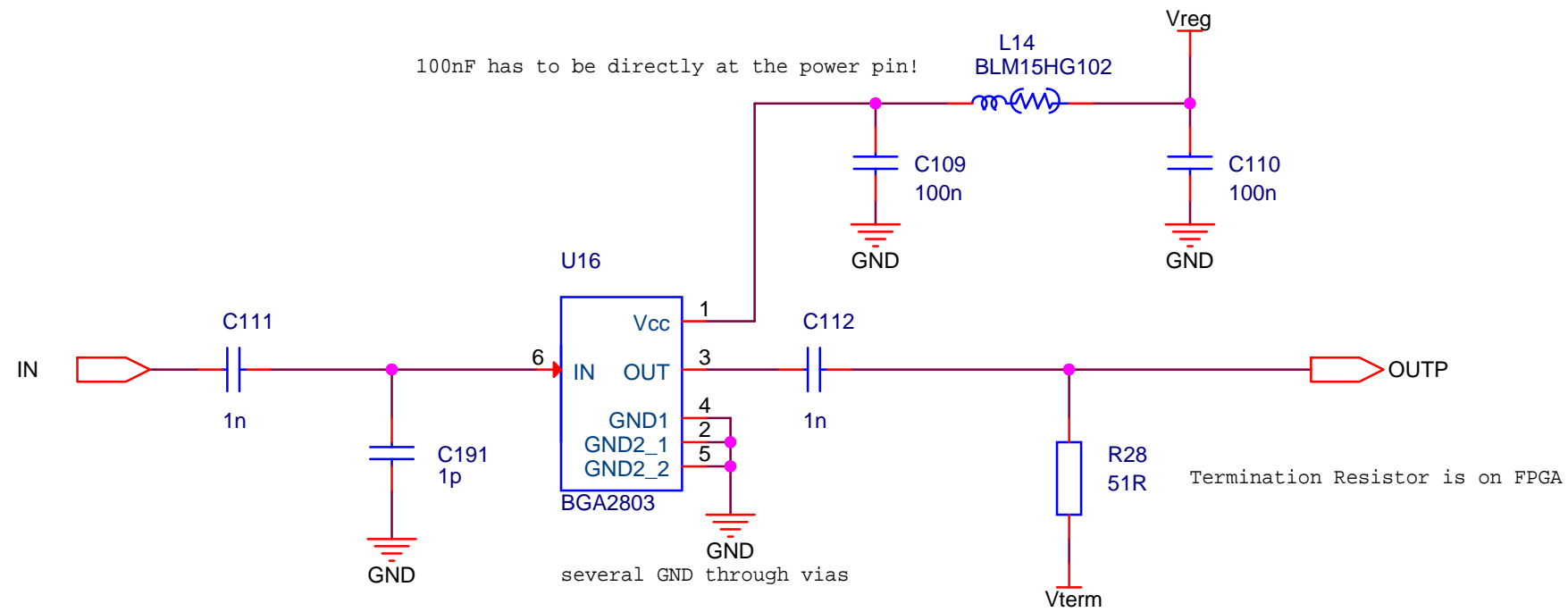
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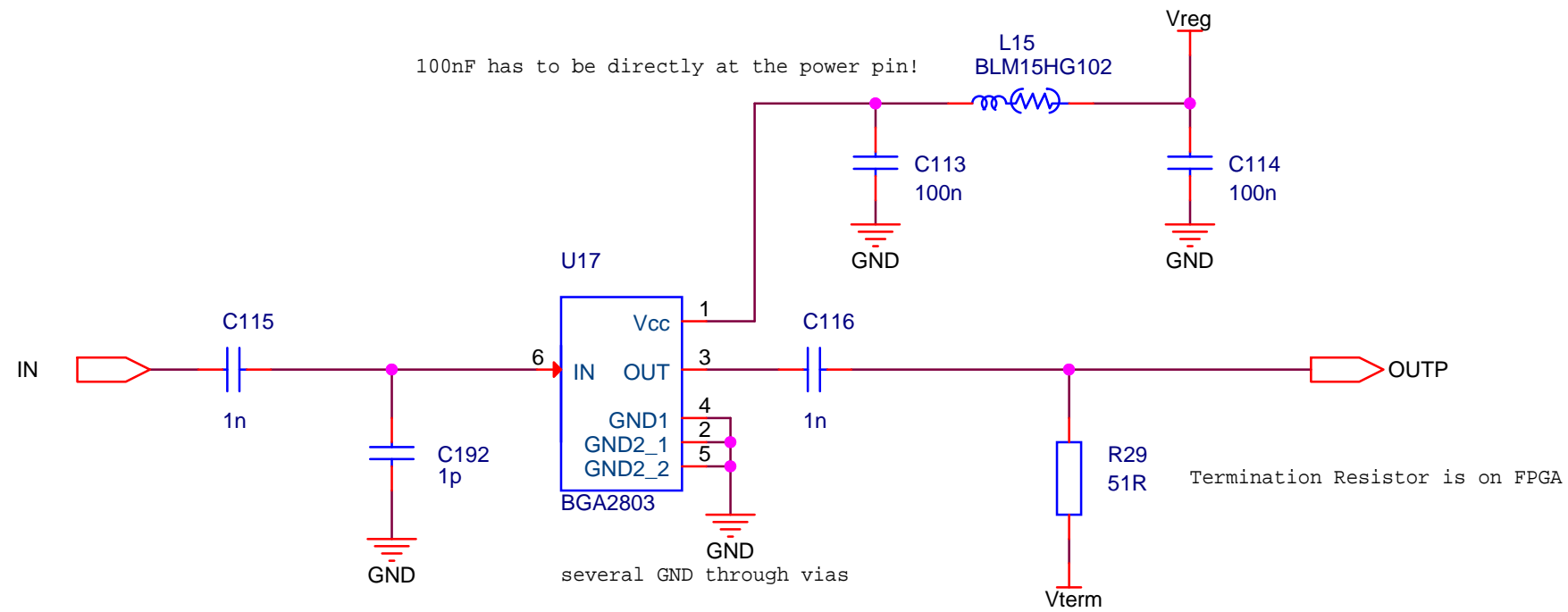
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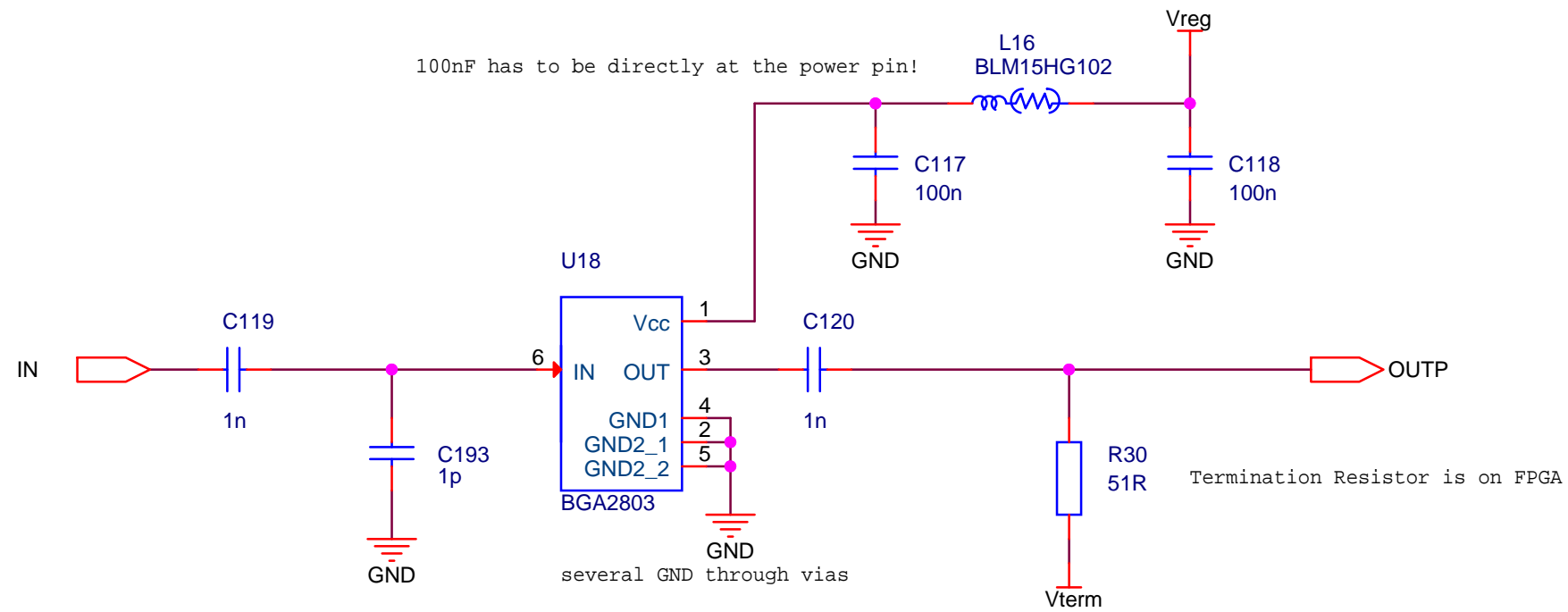
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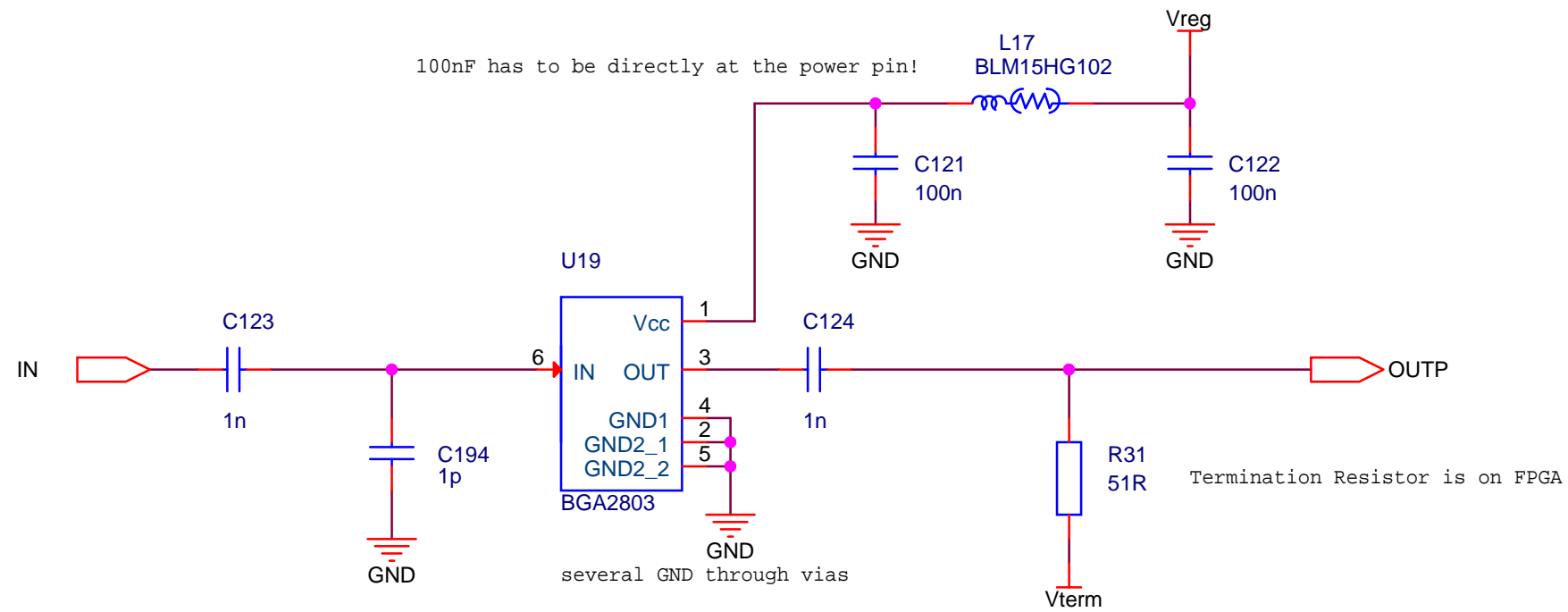
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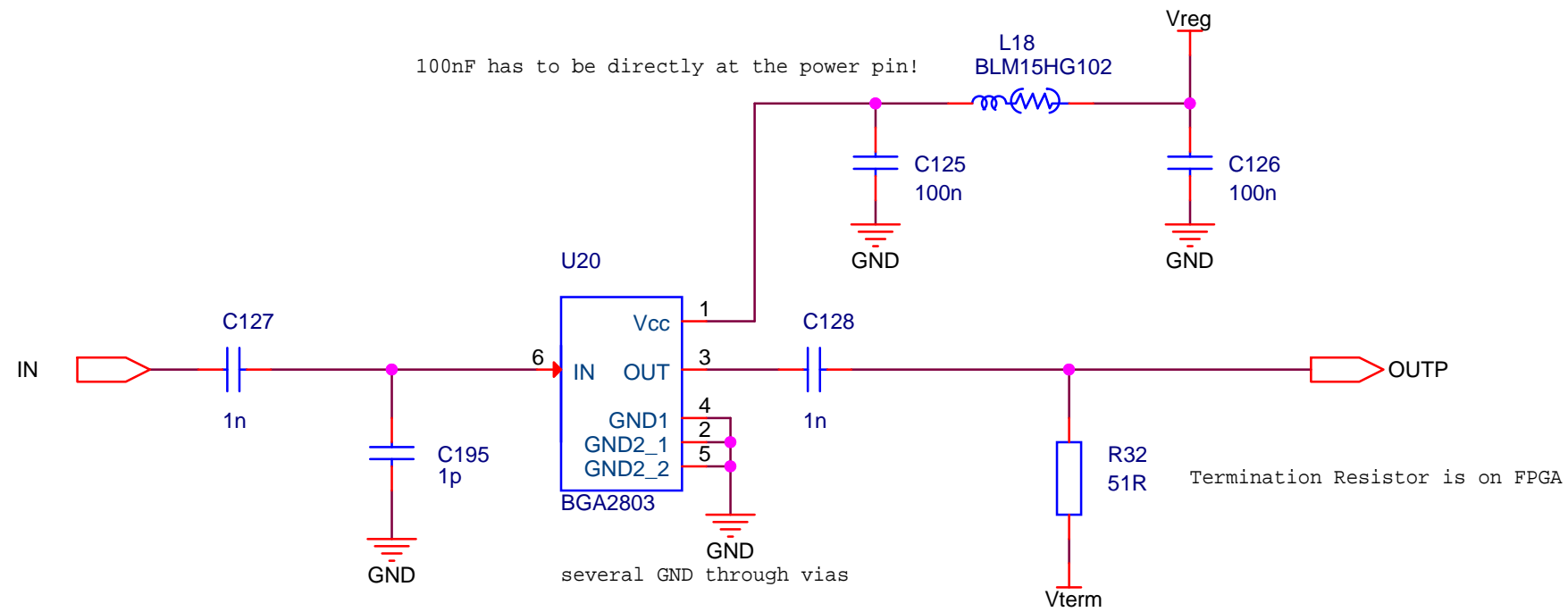
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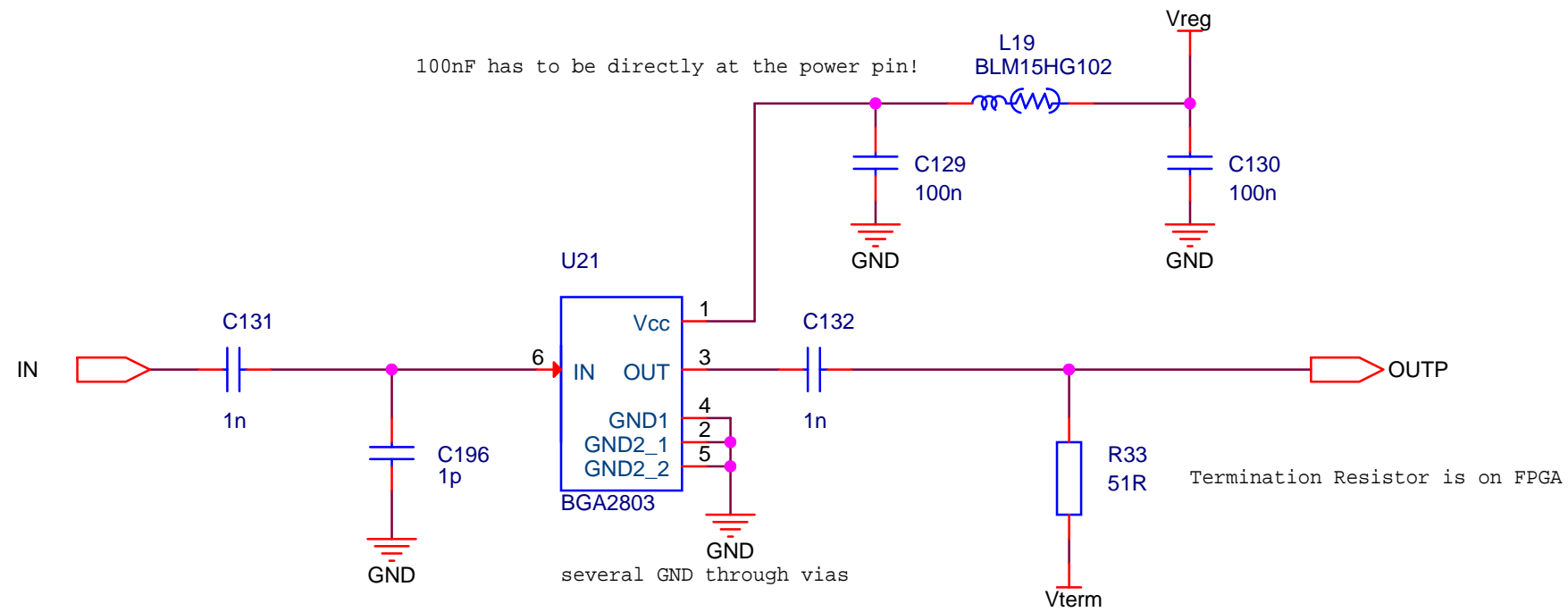
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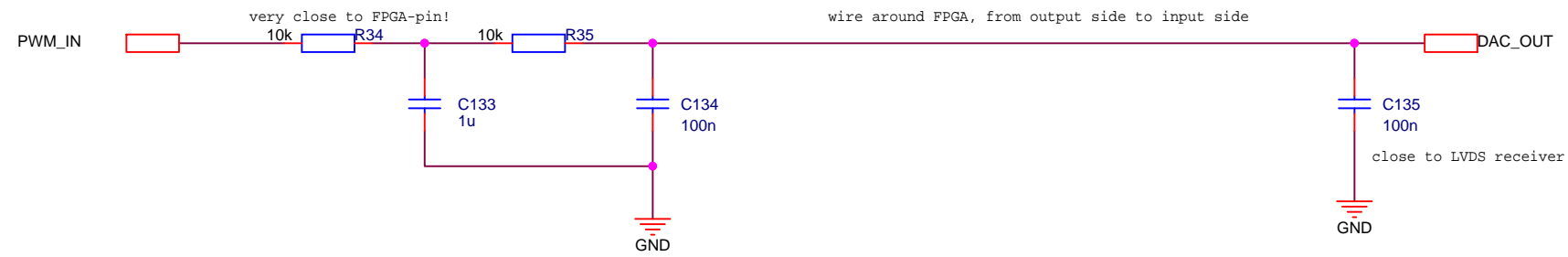
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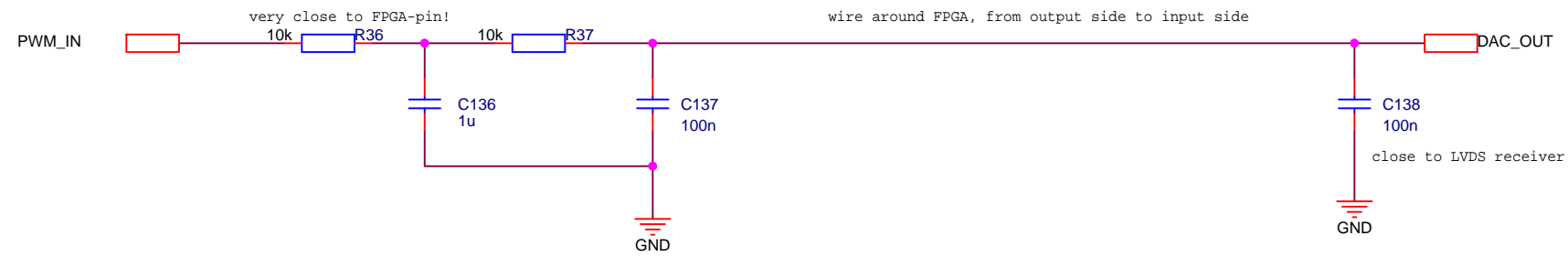
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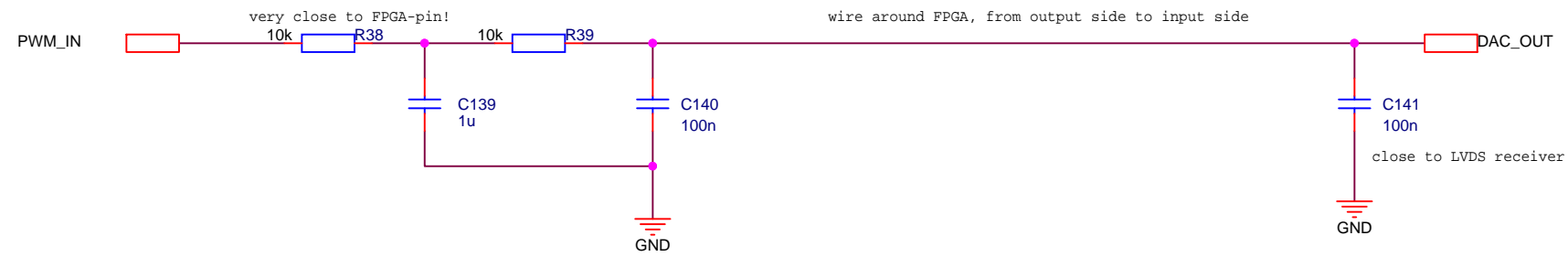


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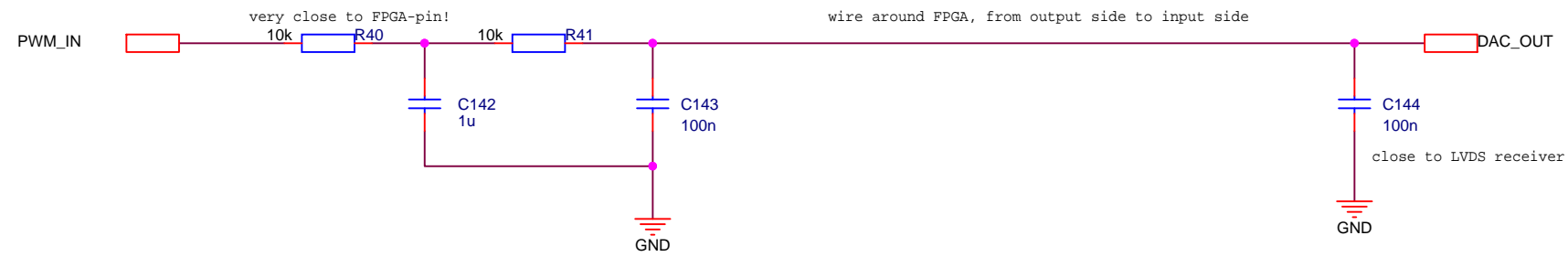


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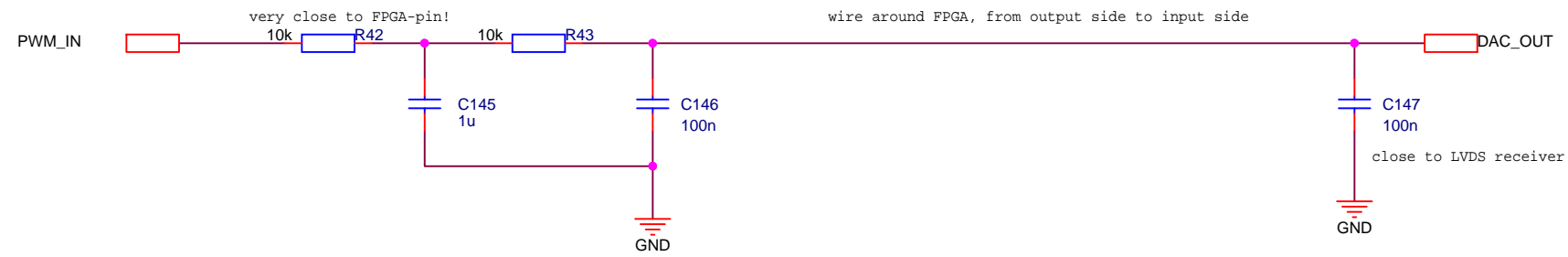




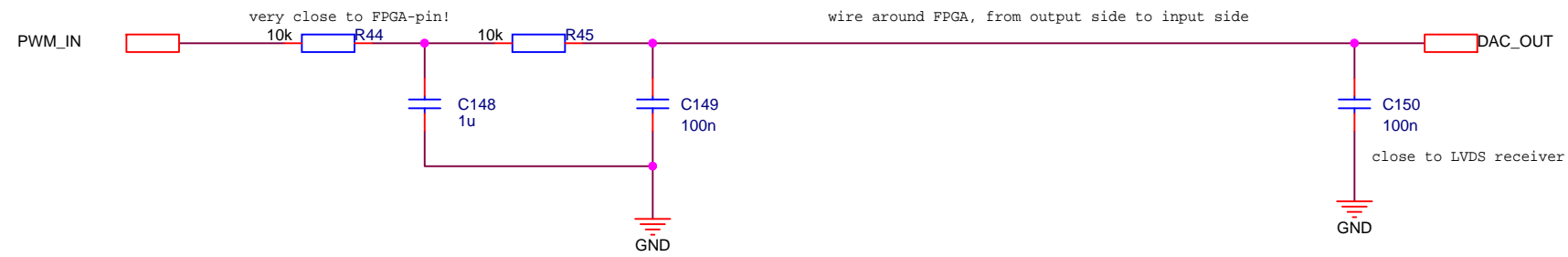
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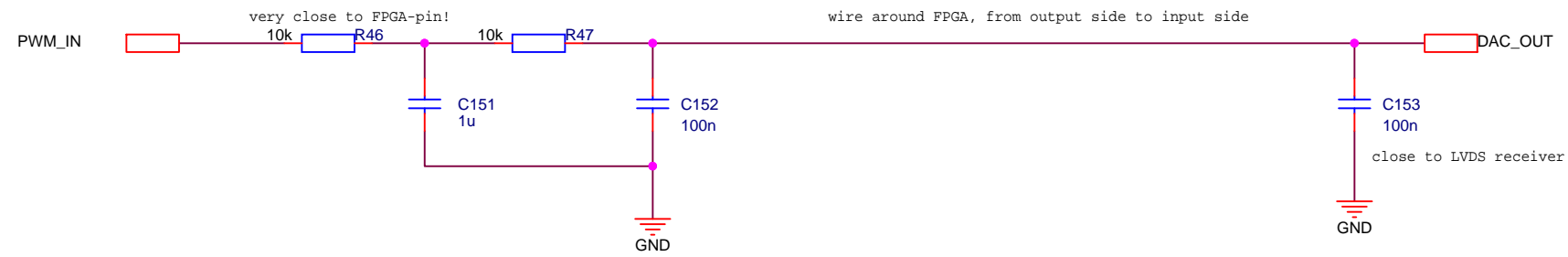
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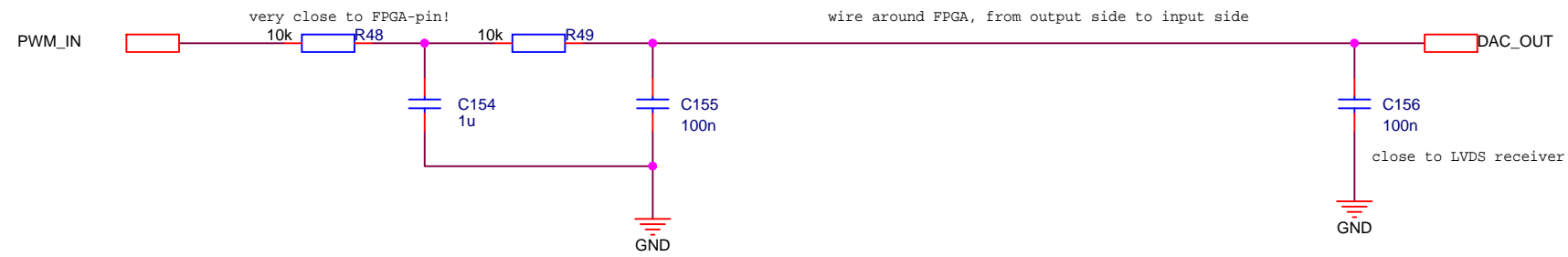
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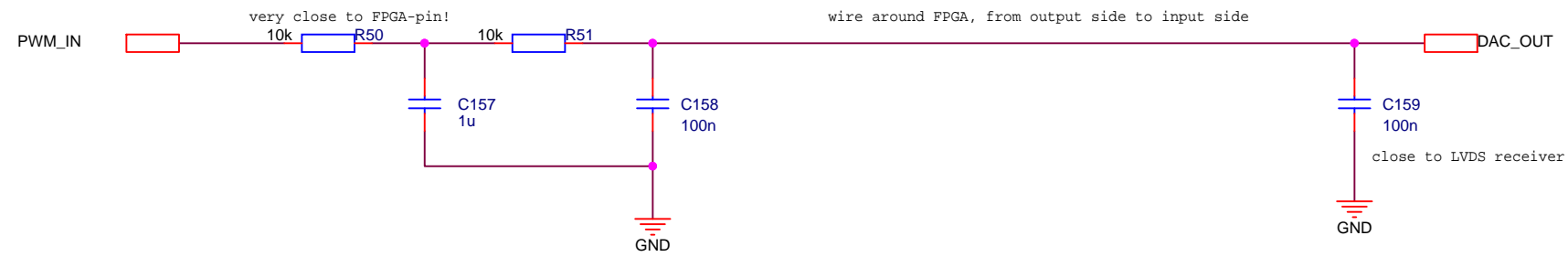


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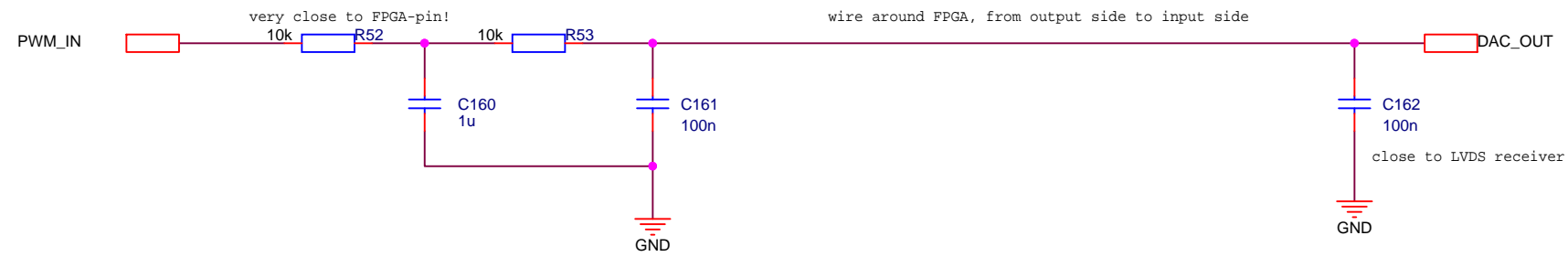


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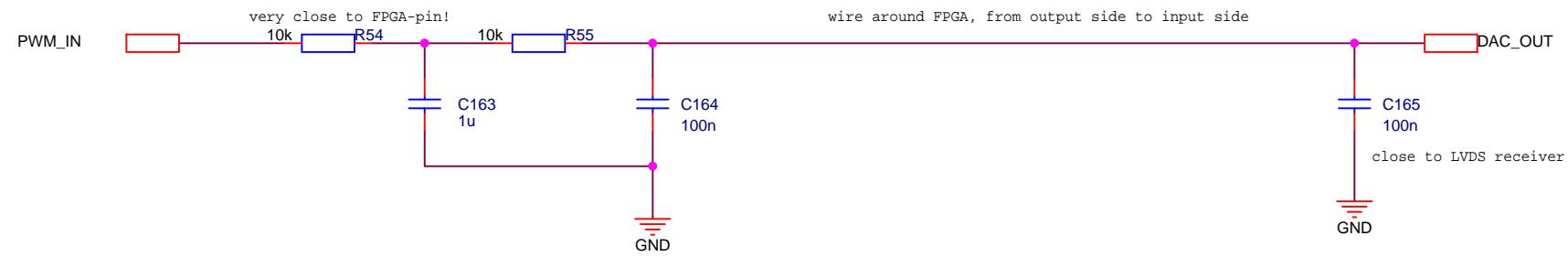


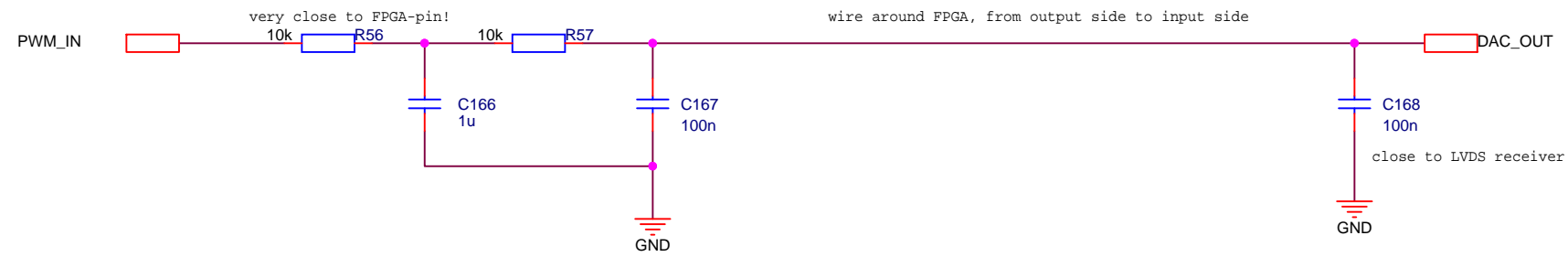


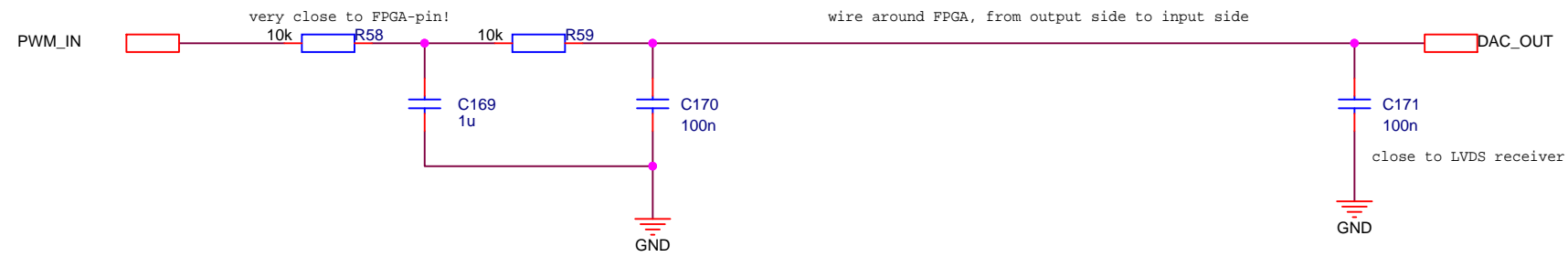
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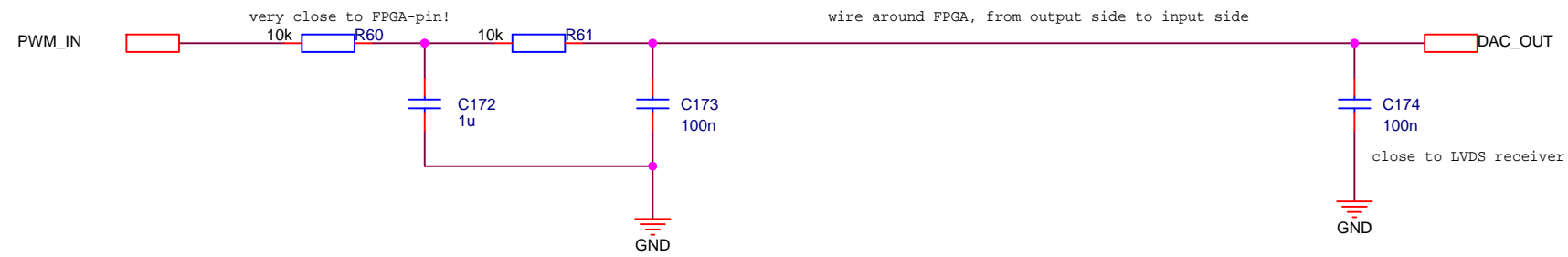
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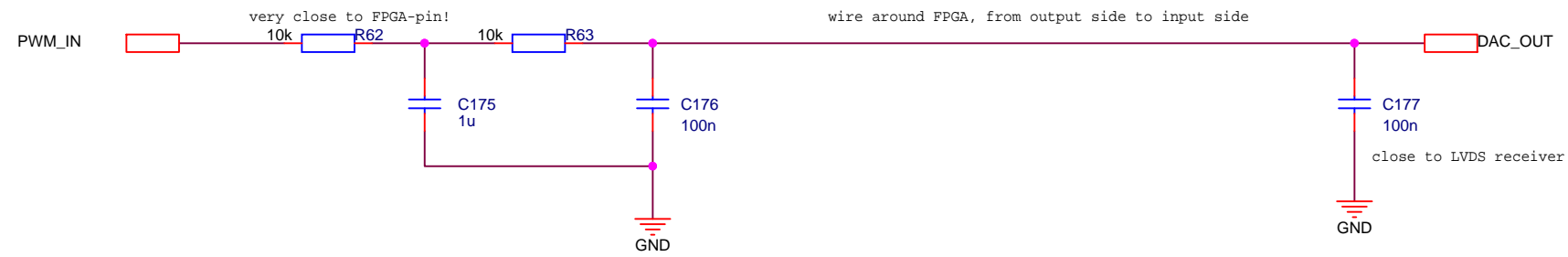


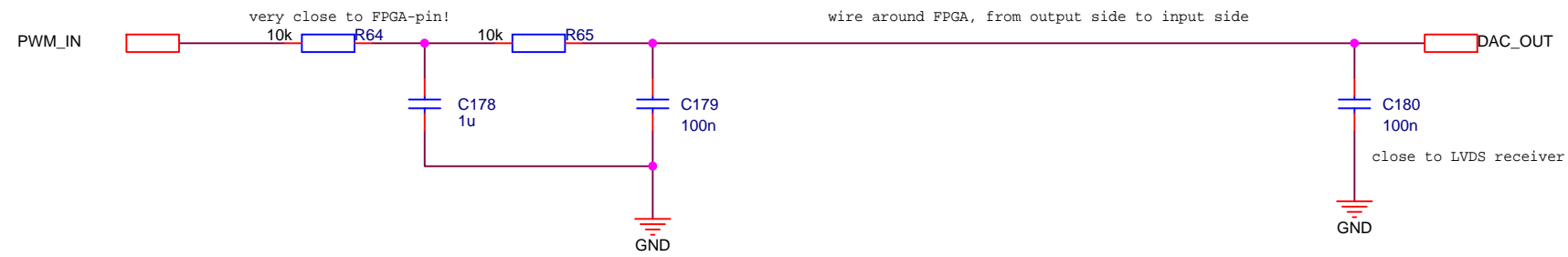




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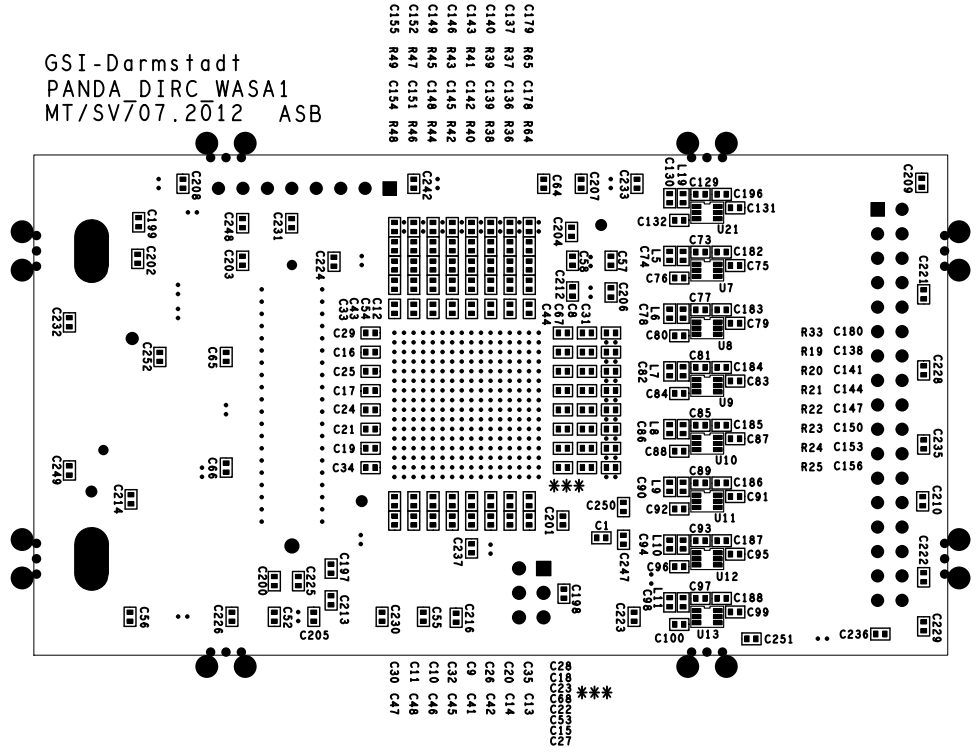






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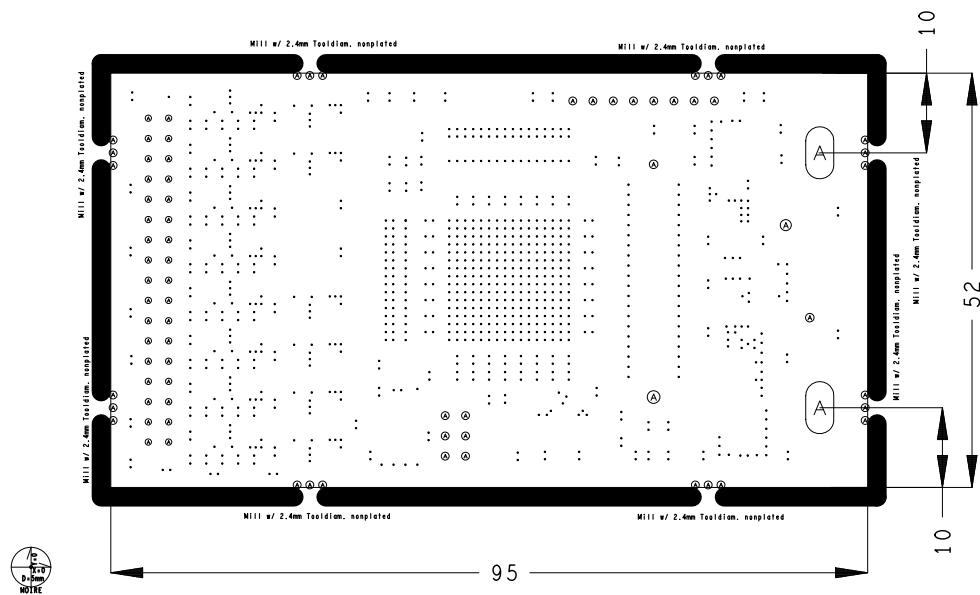
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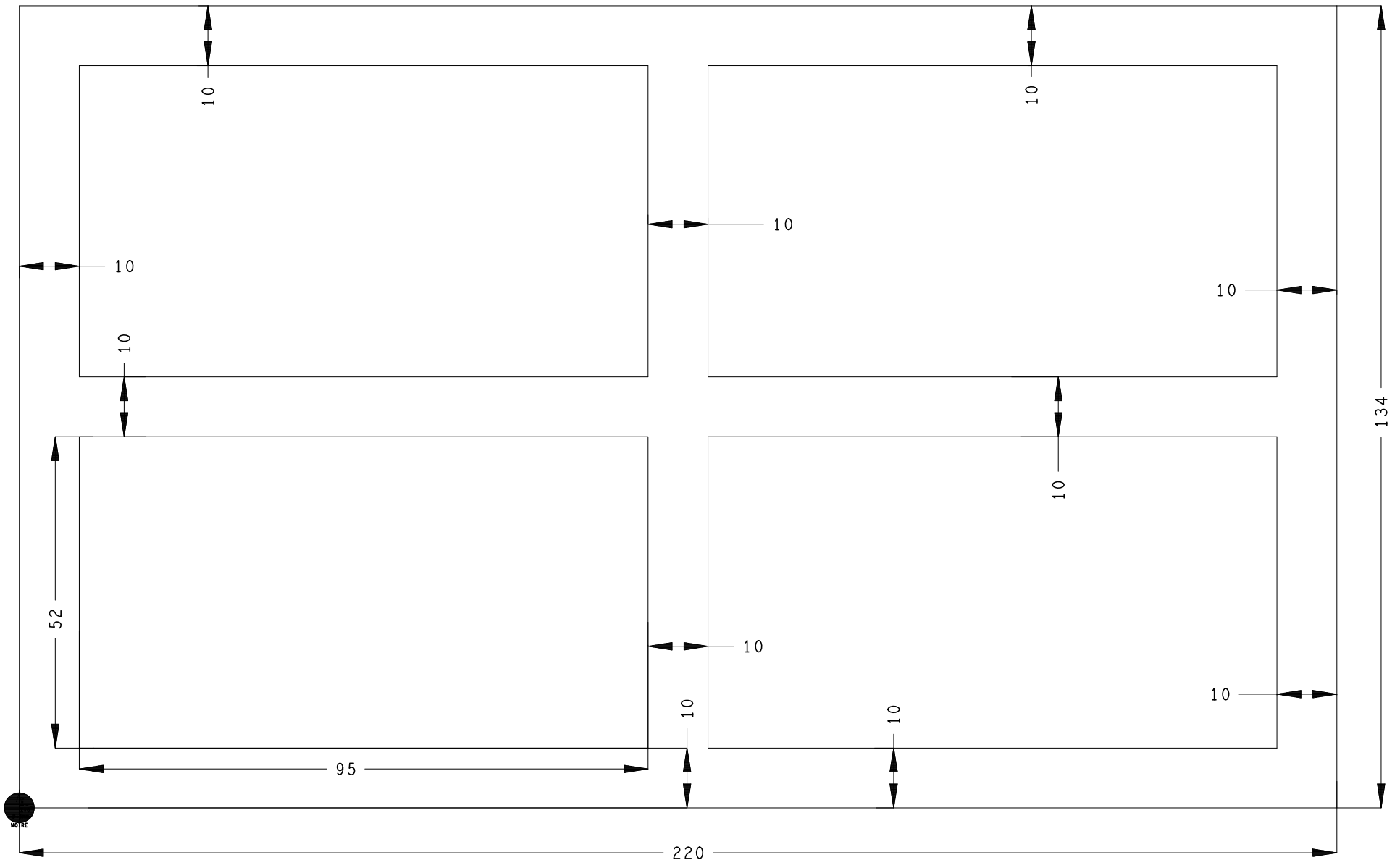
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DRILL CHART: TOP to BOTTOM			
ALL UNITS ARE IN MILLIMETERS			
FIGURE	SIZE	PLATED	QTY
.	0.2	PLATED	930
•	0.4	PLATED	1
◦	0.8	PLATED	34
◉	1.0	PLATED	14
◊	1.0	NON-PLATED	24
◌	1.1	NON-PLATED	2
⊙	1.4	NON-PLATED	1
⊚	1.6	NON-PLATED	1
⊛	2.4	NON-PLATED	16
(A)	6.5x3.5	NON-PLATED	2

TOTAL HOLES: 1025

Layer Nickname

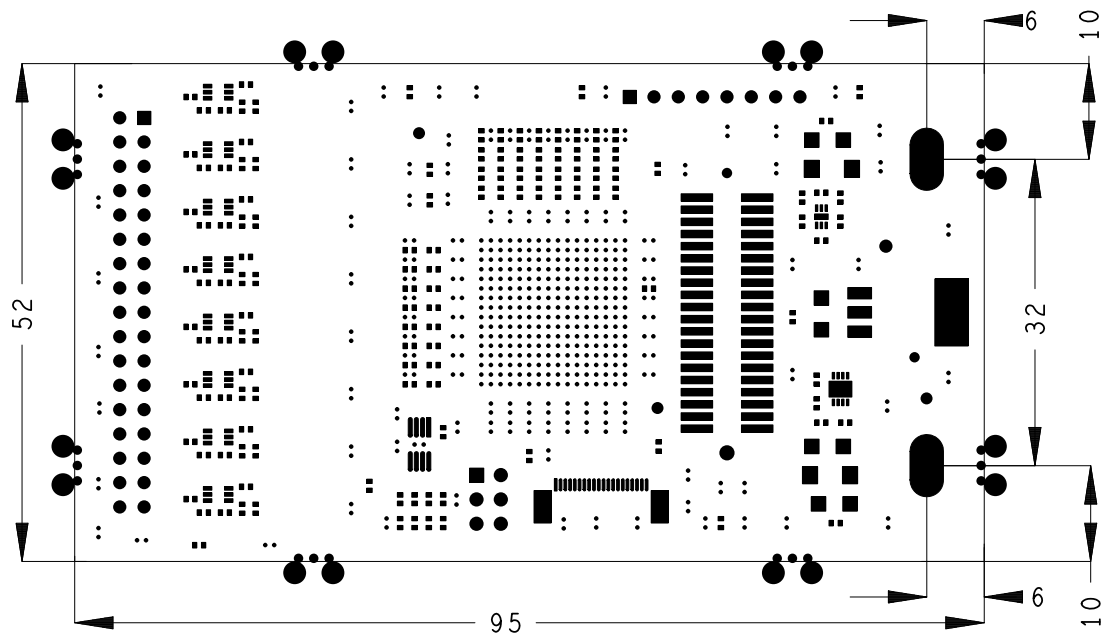
Dr d



Jobname	Date	Designer	Layouter
PANDA-DIRC-WASA1	07.2012	M.Traxler	S.Voltz

Layer Nickname

Fab

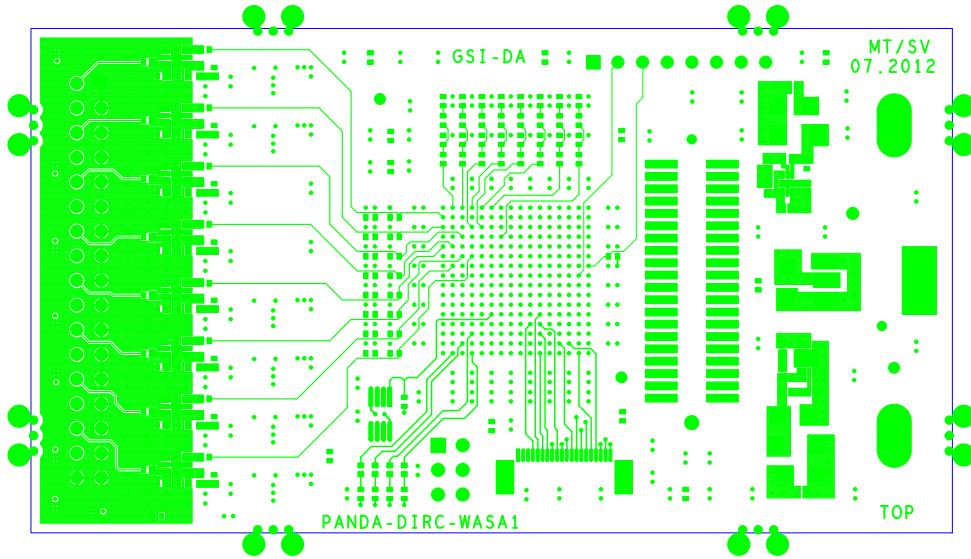


Jobname	Date	Designer	Layouter
PANDA-DIRC-WASA1	07.2012	M.Traxler	S.Voltz

Layer Nickname

Not

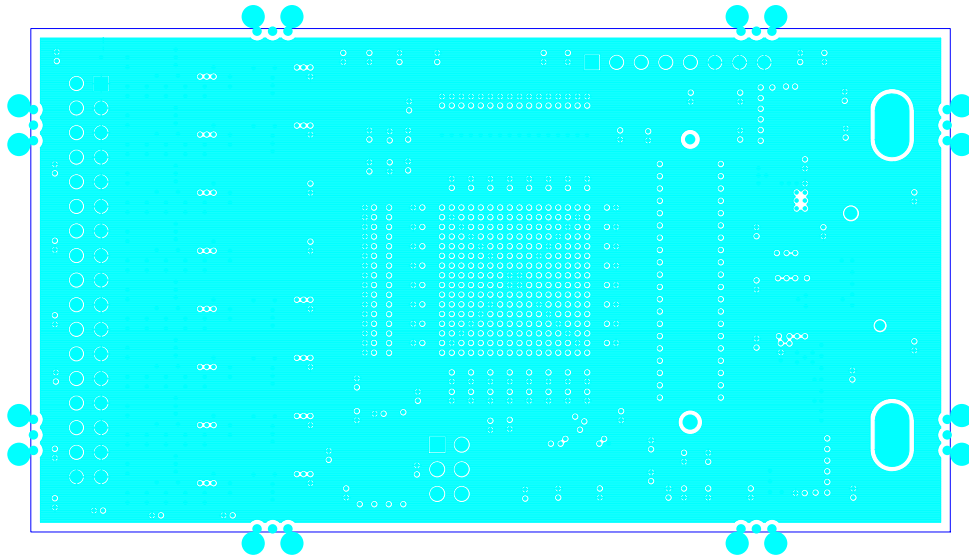
Signals



Jobname	Date	Designer	Layouter
PANDA-DIRC-WASA1	07.2012	M.Traxler	S.Voltz

Layer Nickname
Top

GND-Plane

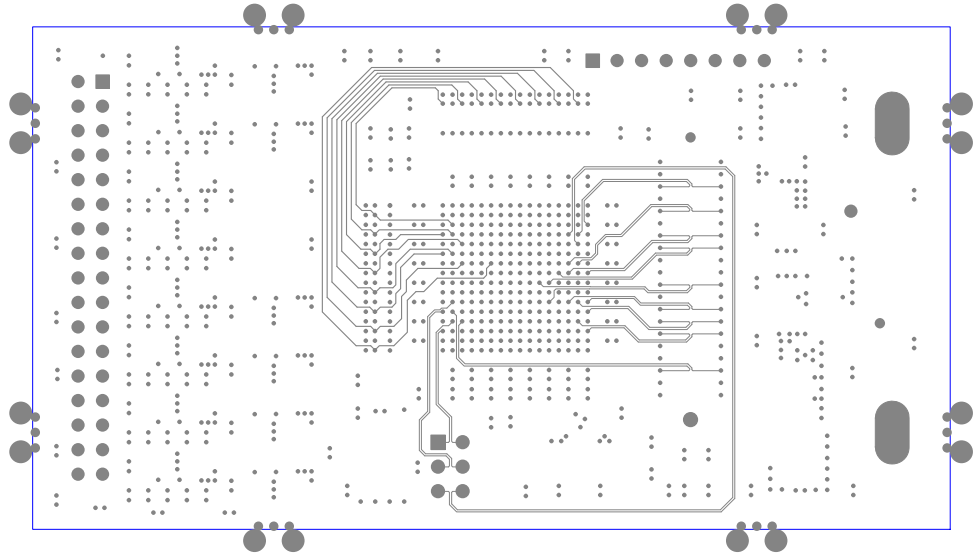


Jobname	Date	Designer	Layouter
PANDA-DIRC-WASA1	07.2012	M.Traxler	S.Voltz

Layer Nickname

I01

Diff.Pairs

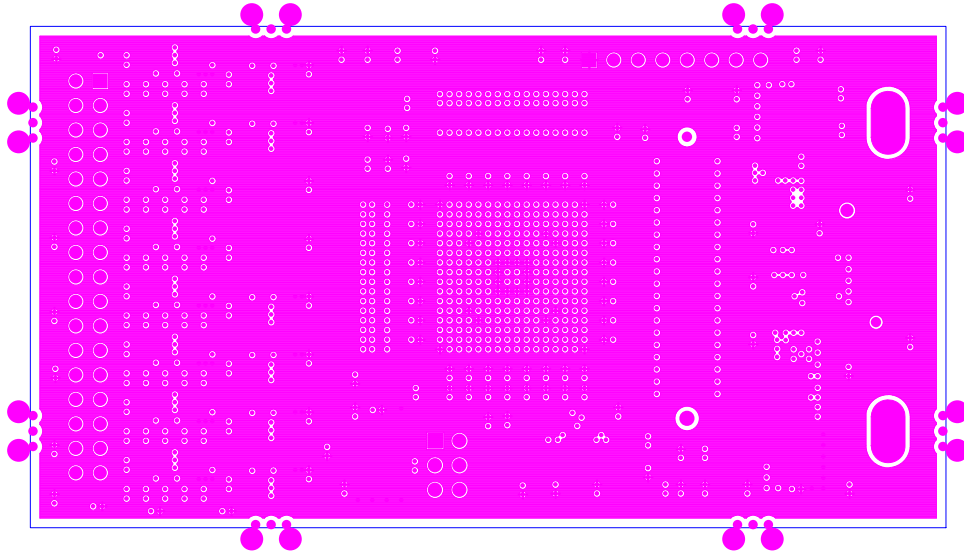


Jobname	Date	Designer	Layouter
PANDA-DIRC-WASA1	07.2012	M.Traxler	S.Voltz

Layer Nickname

I02

VREG-Plane

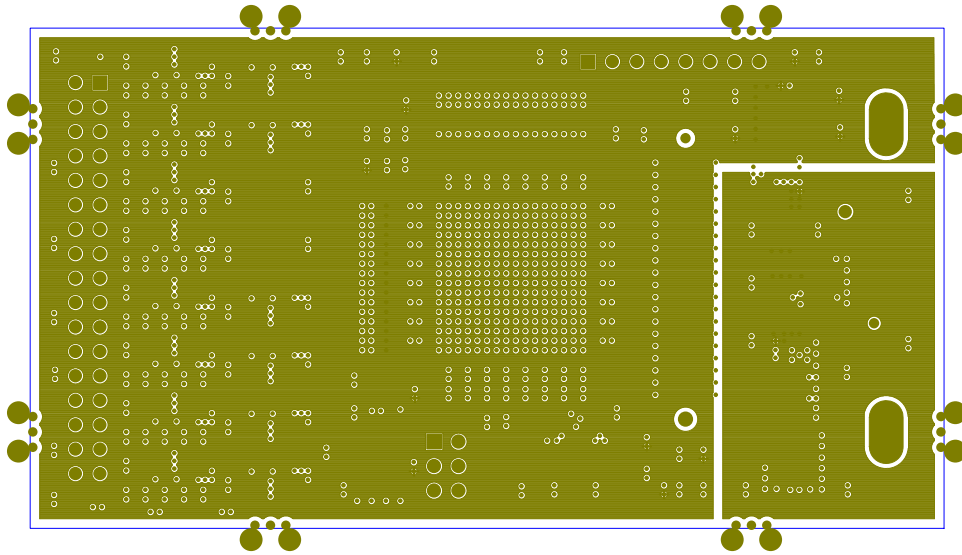


Jobname	Date	Designer	Layouter
PANDA-DIRC-WASA1	07.2012	M.Traxler	S.Voltz

Layer Nickname

I03

VTERM-Plane, VIN-Plane

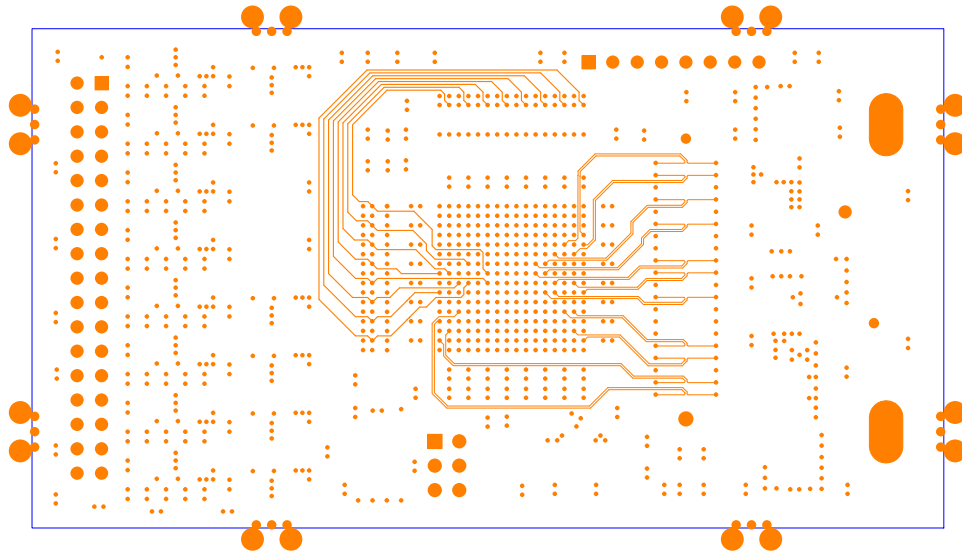


Jobname	Date	Designer	Layouter
PANDA-DIRC-WASA1	07.2012	M.Traxler	S.Voltz

Layer Nickname

I04

Diff.Pairs

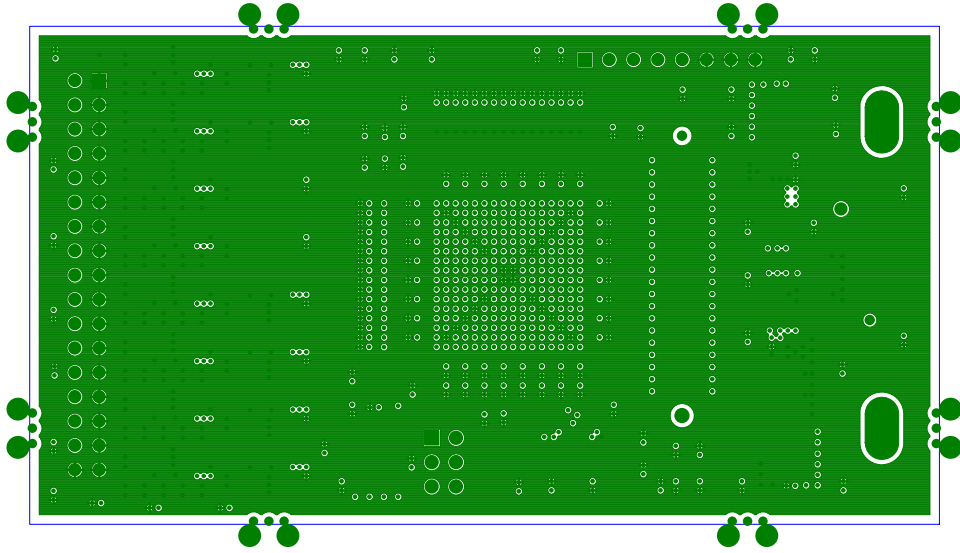


Jobname	Date	Designer	Layouter
PANDA-DIRC-WASA1	07.2012	M.Traxler	S.Voltz

Layer Nickname

I05

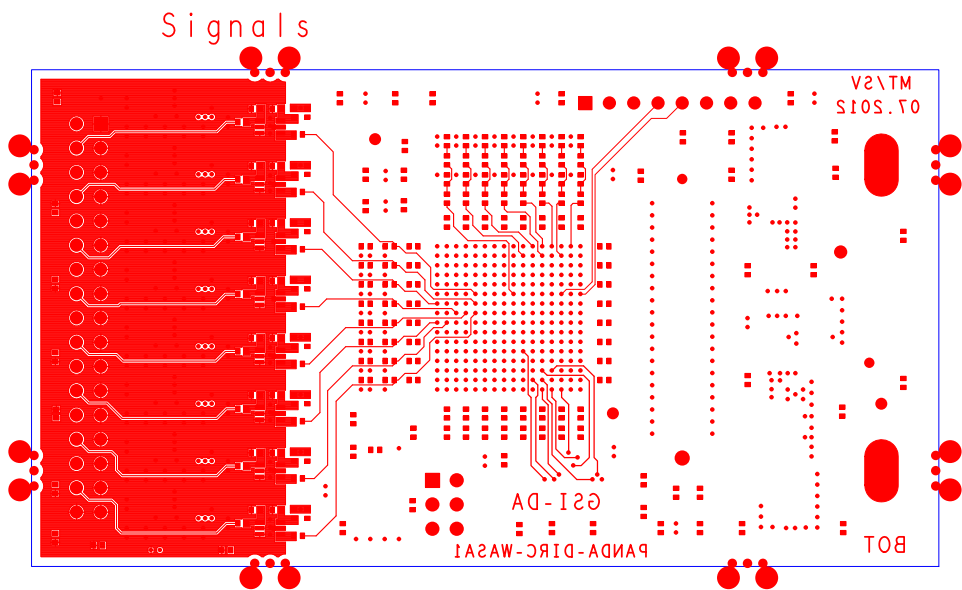
GND - Plane



Jobname	Date	Designer	Layouter
PANDA-DIRC-WASA1	07.2012	M.Traxler	S.Voltz

Layer Nickname

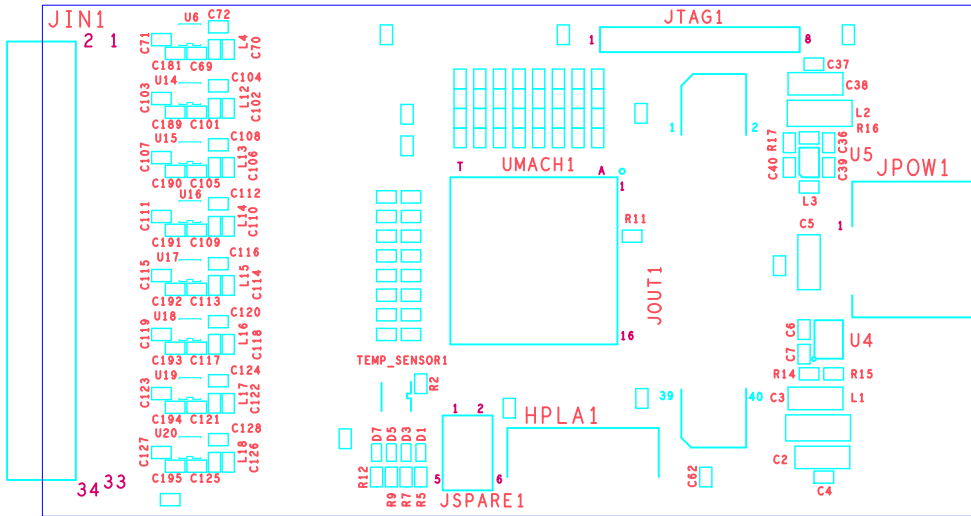
I06



Jobname	Date	Designer	Layouter
PANDA-DIRC-WASA1	07.2012	M.Traxler	S.Voltz

Layer Nickname

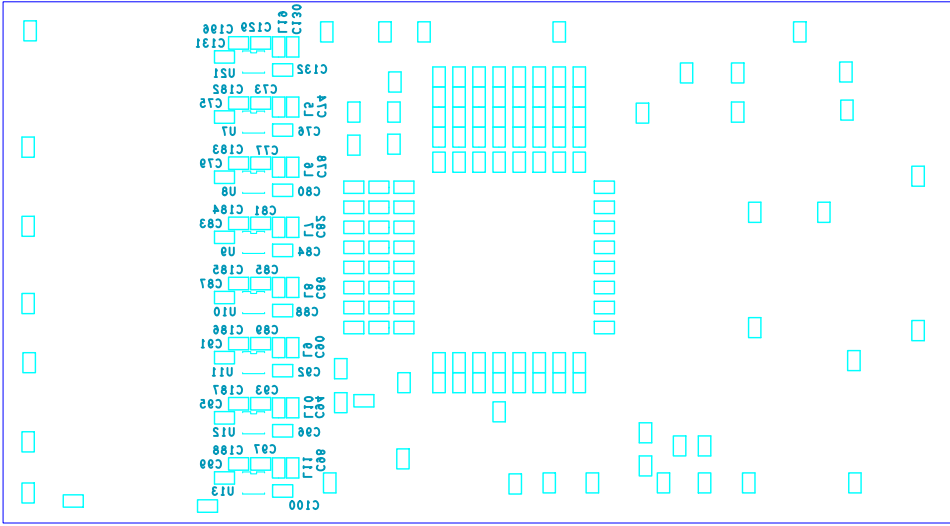
Bot



Jobname	Date	Designer	Layouter
PANDA-DIRC-WASA1	07.2012	M.Traxler	S.Voltz

Layer Nickname

Sst



Jobname	Date	Designer	Layouter
PANDA-DIRC-WASA1	07.2012	M.Traxler	S.Voltz

Layer Nickname

Ssb

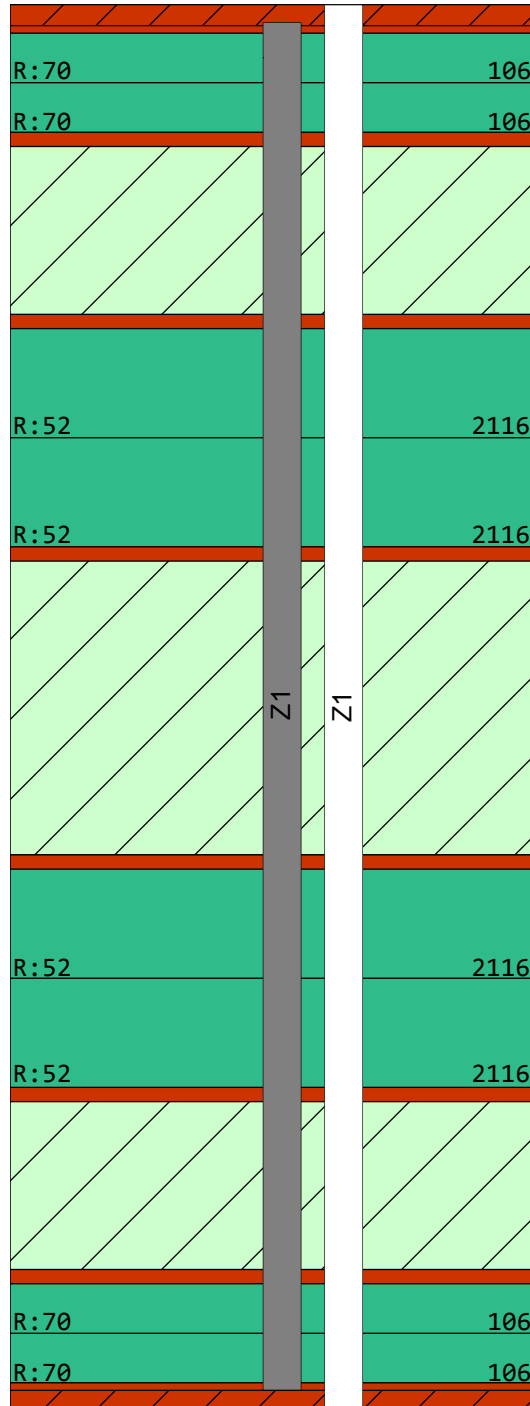
Material (µm)

Stack up

File

Assembly

25 Galvanic Cu
 9 Copper
 50 NP-155F-B
 43 NP-155F-B
 17 Copper
 200 NP-155F-TL
 17 Copper
 109 NP-155F-B
 113 NP-155F-B
 17 Copper
 350 NP-155F-TL
 17 Copper
 113 NP-155F-B
 109 NP-155F-B
 17 Copper
 200 NP-155F-TL
 17 Copper
 43 NP-155F-B
 50 NP-155F-B
 9 Copper
 25 Galvanic Cu



BS ⓘ

I2

I3 ⓘ

I4

A1

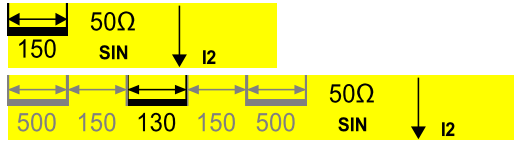
I5

I6 ⓘ

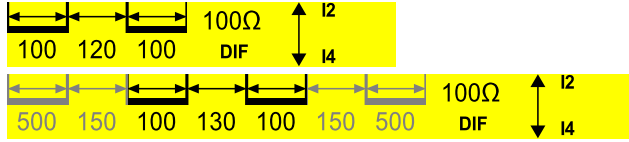
I7

LS ⓘ

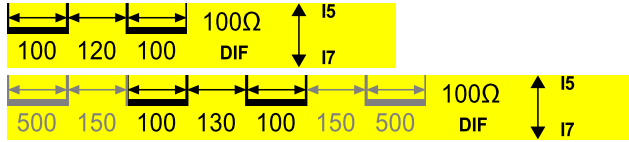
bs



i3



i6



Is

