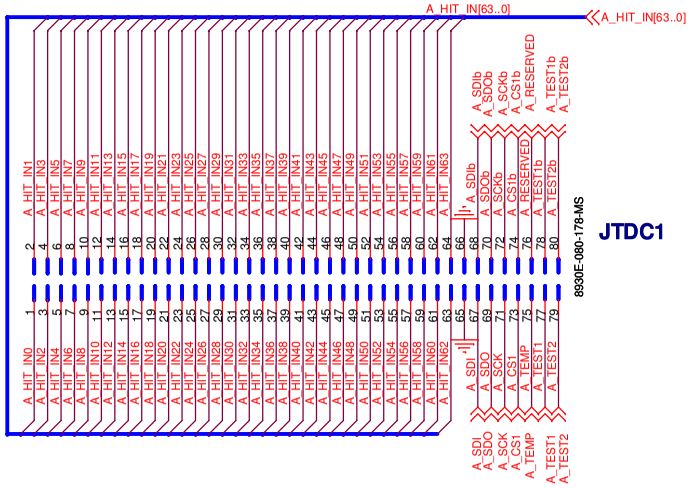
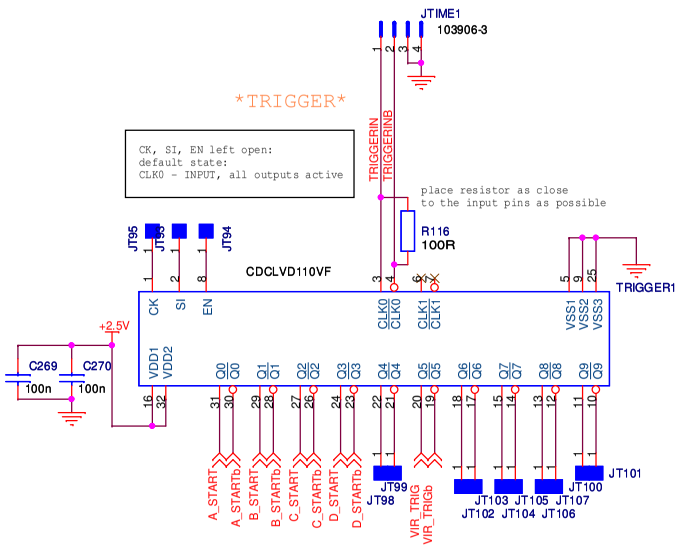
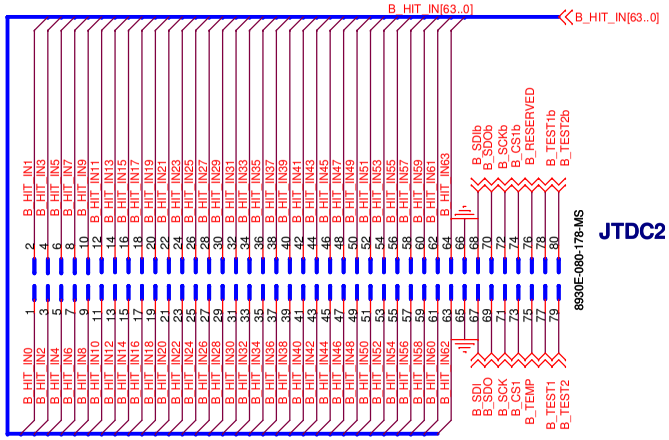
TDC A



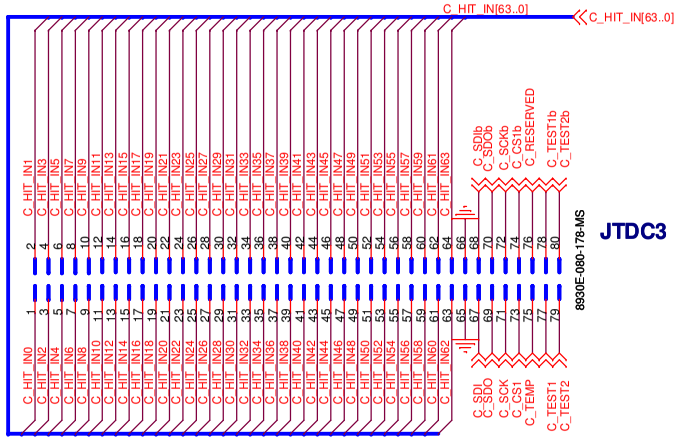


Peter, please make each next START diff. lines
0.5cm longer then the former ones.
e.g. if A_START and A_STARTb have 35 mm then
B_START and B_STARTb should have 40mm

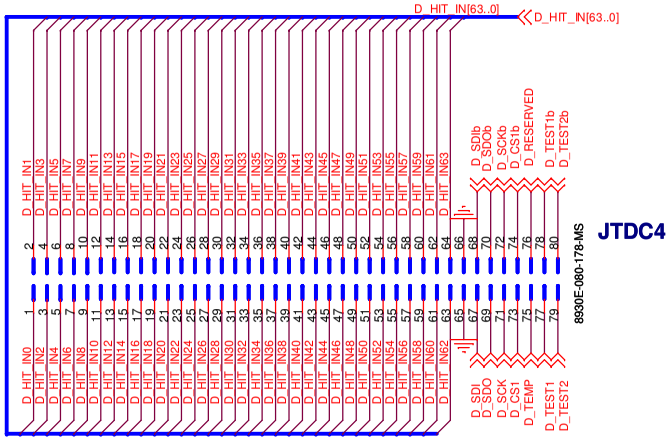
TDC B



TDC C



TDC D



Title	HadesTRB2 - TIME INPUTS	
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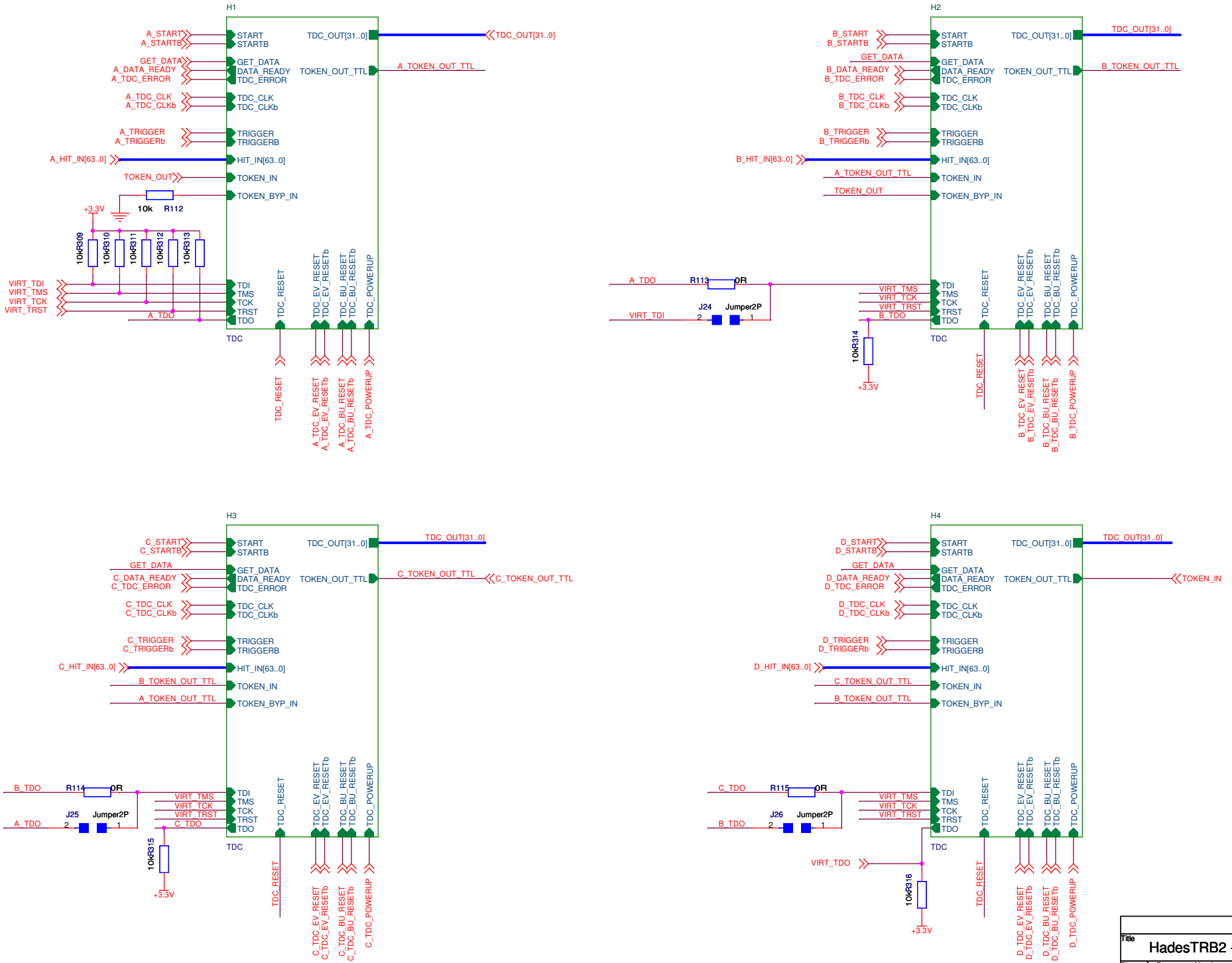
H1
A_START
A_STARTB
START
STARTB
TDC_OUT[31..0]
TDC_OUT[31..0]
GET_DATA
A_DATA_READY
A_TDC_ERROR
GET_DATA
DATA_READY
TDC_ERROR
TOKEN_OUT_TTL
A_TOKEN_OUT_TTL
A_TDC_CLK
A_TDC_CLKb
TDC_CLK
TDC_CLKb
A_TRIGGER
A_TRIGGERb
TRIGGER
TRIGGERB
A_HIT_IN[63..0]
HIT_IN[63..0]
TOKEN_OUT
TOKEN_IN
TOKEN_BYP_IN
+3.3V
10k R112
10kR309
10kR310
10kR311
10kR312
10kR313
VIRT_TDI
VIRT_TMS
VIRT_TCK
VIRT_TRST
A_TDO
TDI
TMS
TCK
TRST
TDO
TDC_RESET
TDC_EV_RESET
TDC_EV_RESETb
TDC_BU_RESET
TDC_BU_RESETb
TDC_POWERUP
TDC
TDC_RESET
A_TDC_EV_RESET
A_TDC_EV_RESETb
A_TDC_BU_RESET
A_TDC_BU_RESETb
A_TDC_POWERUP
H2
B_START
B_STARTB
START
STARTB
TDC_OUT[31..0]
TDC_OUT[31..0]
GET_DATA
B_DATA_READY
B_TDC_ERROR
GET_DATA
DATA_READY
TDC_ERROR
TOKEN_OUT_TTL
B_TOKEN_OUT_TTL
B_TDC_CLK
B_TDC_CLKb
TDC_CLK
TDC_CLKb
B_TRIGGER
B_TRIGGERb
TRIGGER
TRIGGERB
B_HIT_IN[63..0]
HIT_IN[63..0]
A_TOKEN_OUT_TTL
TOKEN_IN
TOKEN_OUT
TOKEN_BYP_IN
A_TDO
R113 0R
VIRT_TDI
J24 Jumper2P
2
1
VIRT_TMS
VIRT_TCK
VIRT_TRST
B_TDO
10kR314
+3.3V
TDI
TMS
TCK
TRST
TDO
TDC_RESET
TDC_EV_RESET
TDC_EV_RESETb
TDC_BU_RESET
TDC_BU_RESETb
TDC_POWERUP
TDC
TDC_RESET
B_TDC_EV_RESET
B_TDC_EV_RESETb
B_TDC_BU_RESET
B_TDC_BU_RESETb
B_TDC_POWERUP
H3
C_START
C_STARTB
START
STARTB
TDC_OUT[31..0]
TDC_OUT[31..0]
GET_DATA
C_DATA_READY
C_TDC_ERROR
GET_DATA
DATA_READY
TDC_ERROR
TOKEN_OUT_TTL
C_TOKEN_OUT_TTL
C_TOKEN_OUT_TTL
C_TDC_CLK
C_TDC_CLKb
TDC_CLK
TDC_CLKb
C_TRIGGER
C_TRIGGERb
TRIGGER
TRIGGERB
C_HIT_IN[63..0]
HIT_IN[63..0]
B_TOKEN_OUT_TTL
TOKEN_IN
A_TOKEN_OUT_TTL
TOKEN_BYP_IN
B_TDO
R114 0R
VIRT_TMS
VIRT_TCK
VIRT_TRST
C_TDO
J25 Jumper2P
2
1
A_TDO
10kR315
+3.3V
TDI
TMS
TCK
TRST
TDO
TDC_RESET
TDC_EV_RESET
TDC_EV_RESETb
TDC_BU_RESET
TDC_BU_RESETb
TDC_POWERUP
TDC
TDC_RESET
C_TDC_EV_RESET
C_TDC_EV_RESETb
C_TDC_BU_RESET
C_TDC_BU_RESETb
C_TDC_POWERUP
H4
D_START
D_STARTB
START
STARTB
TDC_OUT[31..0]
TDC_OUT[31..0]
GET_DATA
D_DATA_READY
D_TDC_ERROR
GET_DATA
DATA_READY
TDC_ERROR
TOKEN_OUT_TTL
TOKEN_IN
D_TDC_CLK
D_TDC_CLKb
TDC_CLK
TDC_CLKb
D_TRIGGER
D_TRIGGERb
TRIGGER
TRIGGERB
D_HIT_IN[63..0]
HIT_IN[63..0]
C_TOKEN_OUT_TTL
TOKEN_IN
B_TOKEN_OUT_TTL
TOKEN_BYP_IN
C_TDO
R115 0R
VIRT_TMS
VIRT_TCK
VIRT_TRST
B_TDO
J26 Jumper2P
2
1
VIRT_TDO
10kR316
+3.3V
TDI
TMS
TCK
TRST
TDO
TDC_RESET
TDC_EV_RESET
TDC_EV_RESETb
TDC_BU_RESET
TDC_BU_RESETb
TDC_POWERUP
TDC
TDC_RESET
D_TDC_EV_RESET
D_TDC_EV_RESETb
D_TDC_BU_RESET
D_TDC_BU_RESETb
D_TDC_POWERUP
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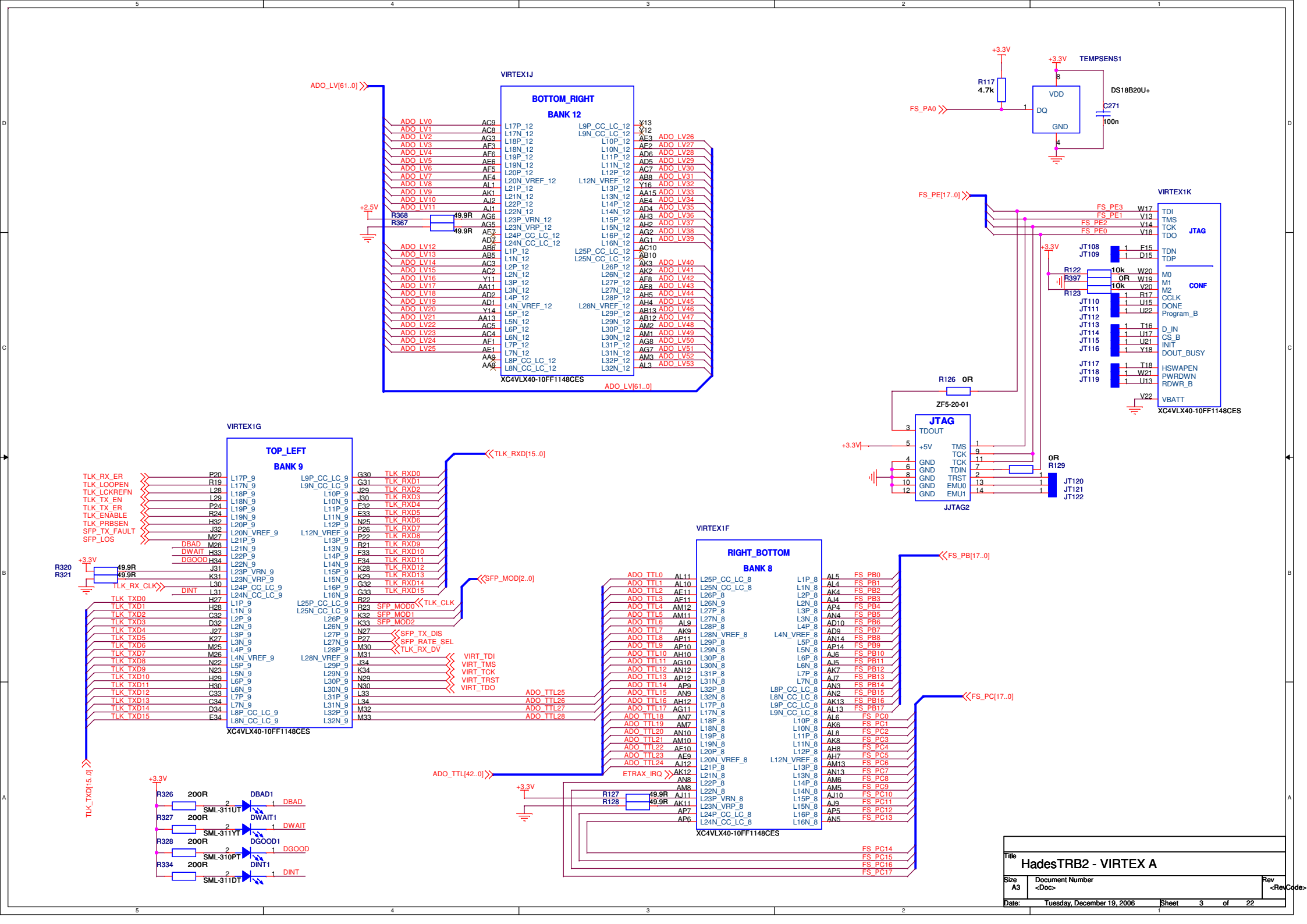

Title	HadesTRB2 - VIRTEX A		
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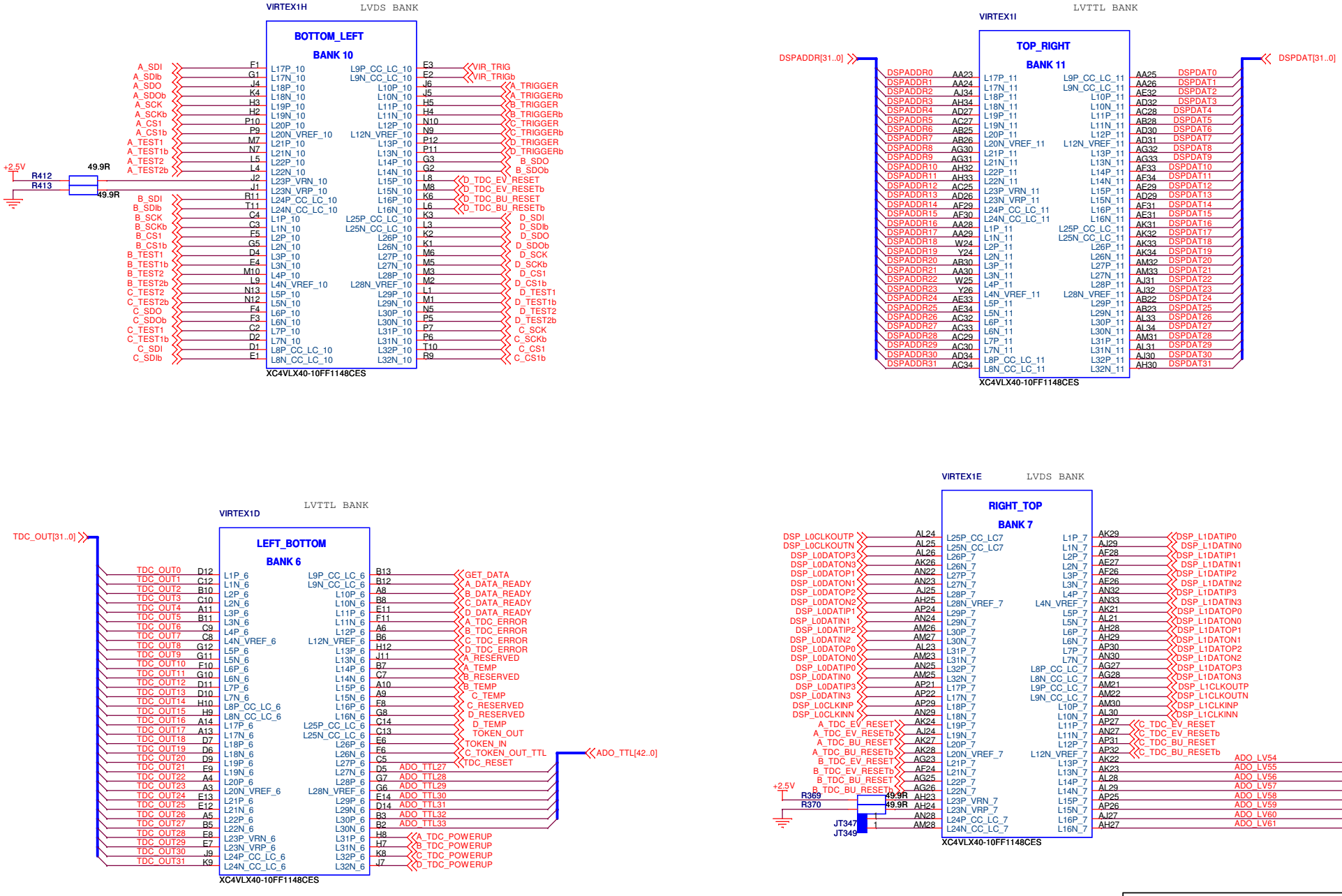

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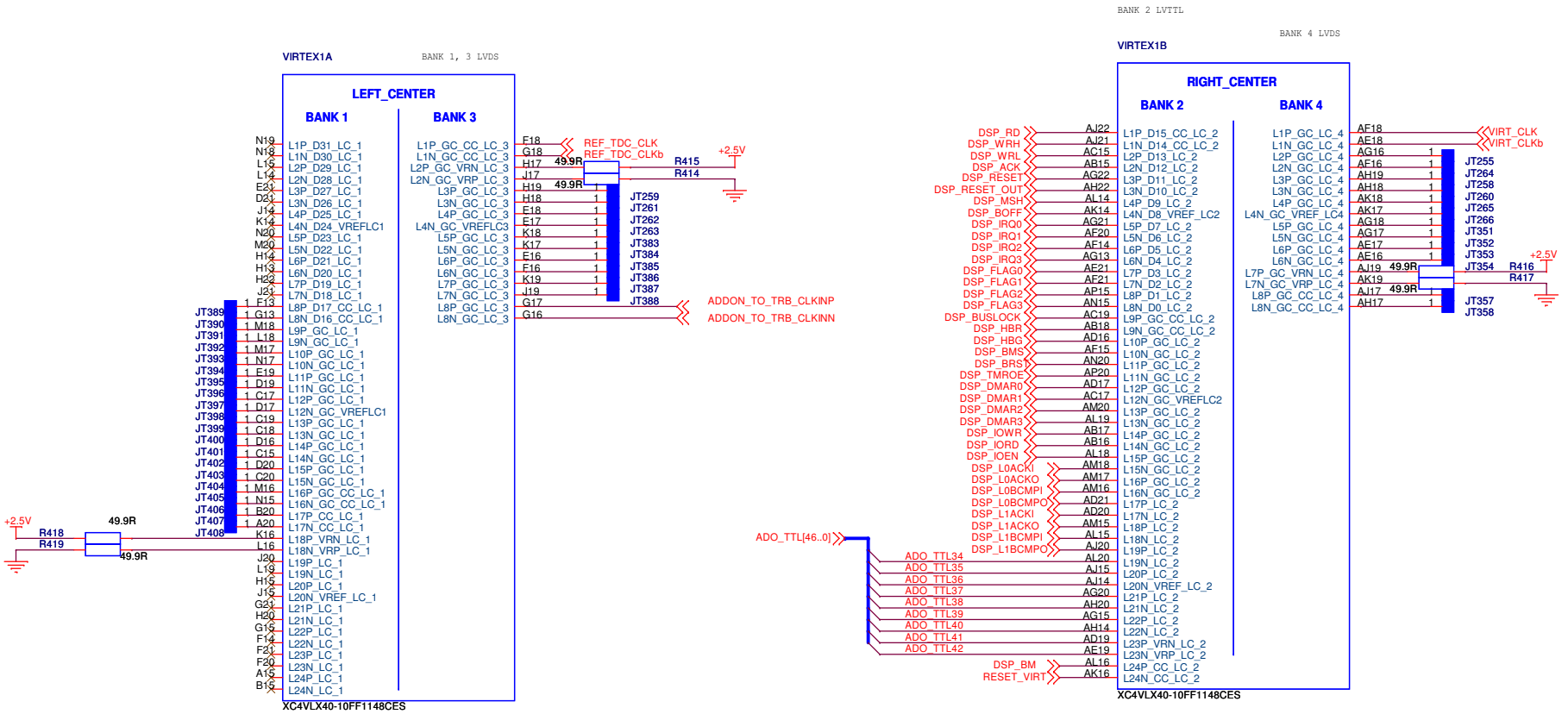

DSP control - banks 2, 7, 11

Title	HadesTRB2 - VIRTEX C	
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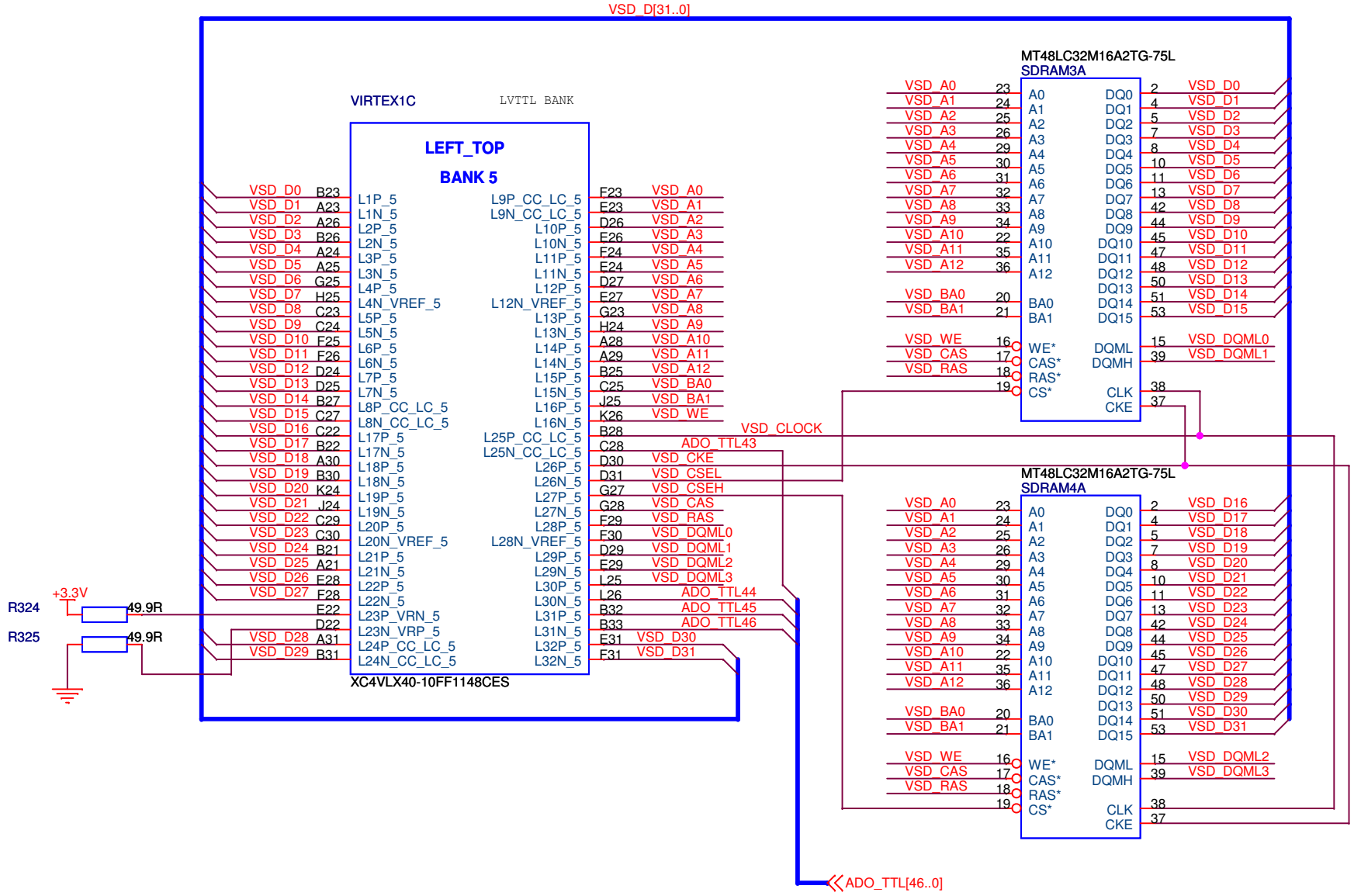

Title	HadesTRB2 - VIRTEX SDRAM		
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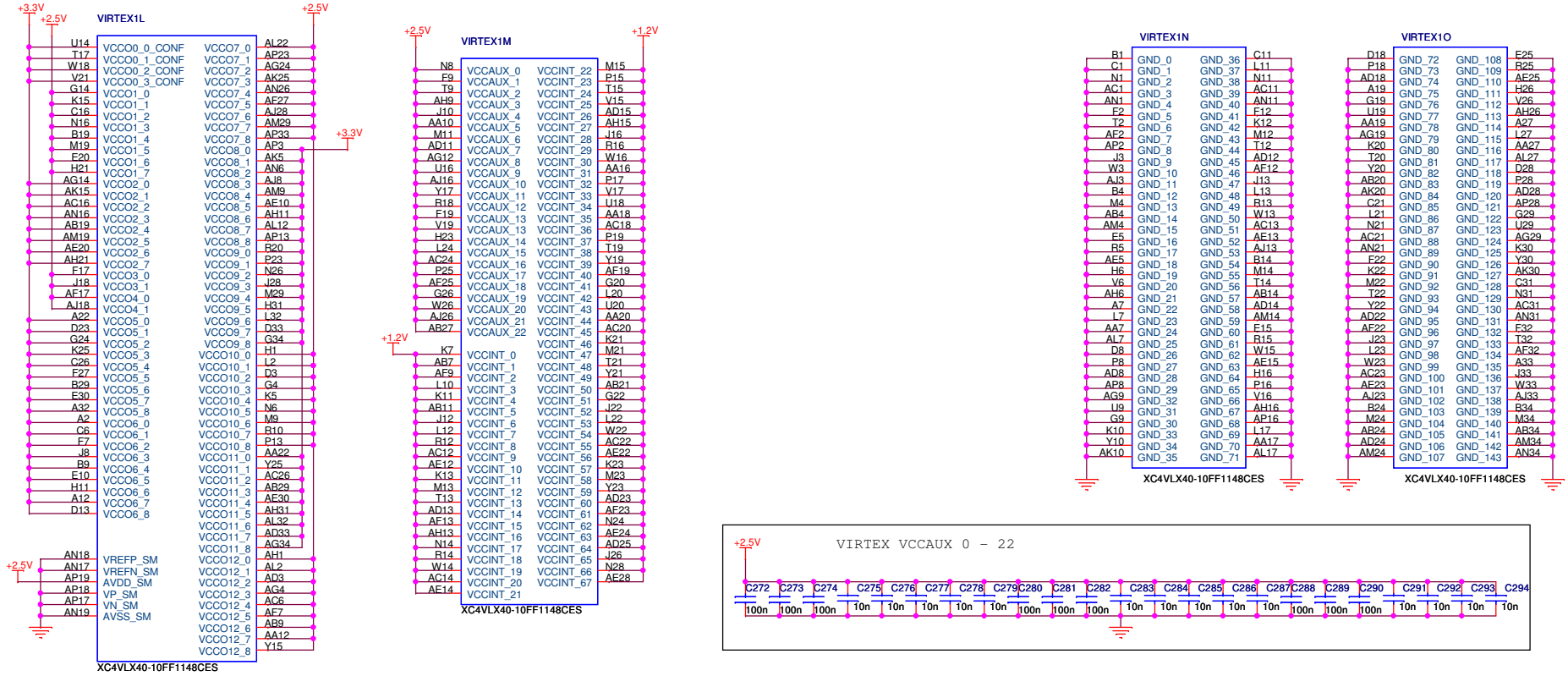

Title	HadesTRB2 - VIRTEX SUPPLY
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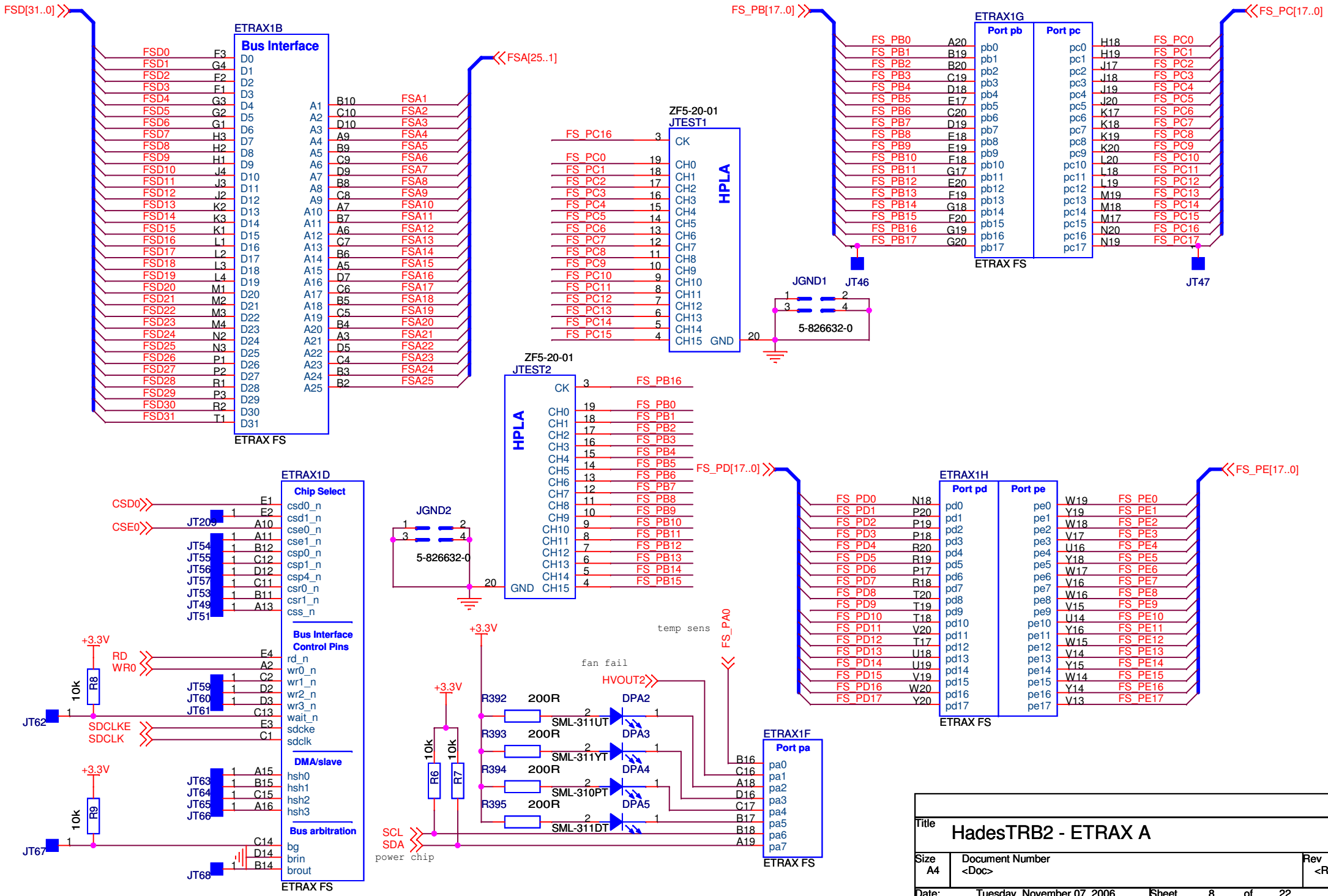
FSD[31..0]
ETRAX1B
Bus Interface
FSA[25..1]
ETRAX FS
FS_PB[17..0]
ETRAX1G
Port pb
Port pc
FS_PC[17..0]
JT46
JT47
JGND1
5-826632-0
ZF5-20-01
JTEST1
HPLA
JTEST2
JGND2
FS_PD[17..0]
ETRAX1H
Port pd
Port pe
FS_PE[17..0]
ETRAX1D
Chip Select
Bus Interface Control Pins
DMA/slave
Bus arbitration
+3.3V
temp sens
fan fail
HVOUT2
FS_PA0
R392 200R
R393 200R
R394 200R
R395 200R
SML-311UT
SML-311YT
SML-310PT
SML-311DT
DPA2
DPA3
DPA4
DPA5
ETRAX1F
Port pa
SCL
SDA
power chip
Title
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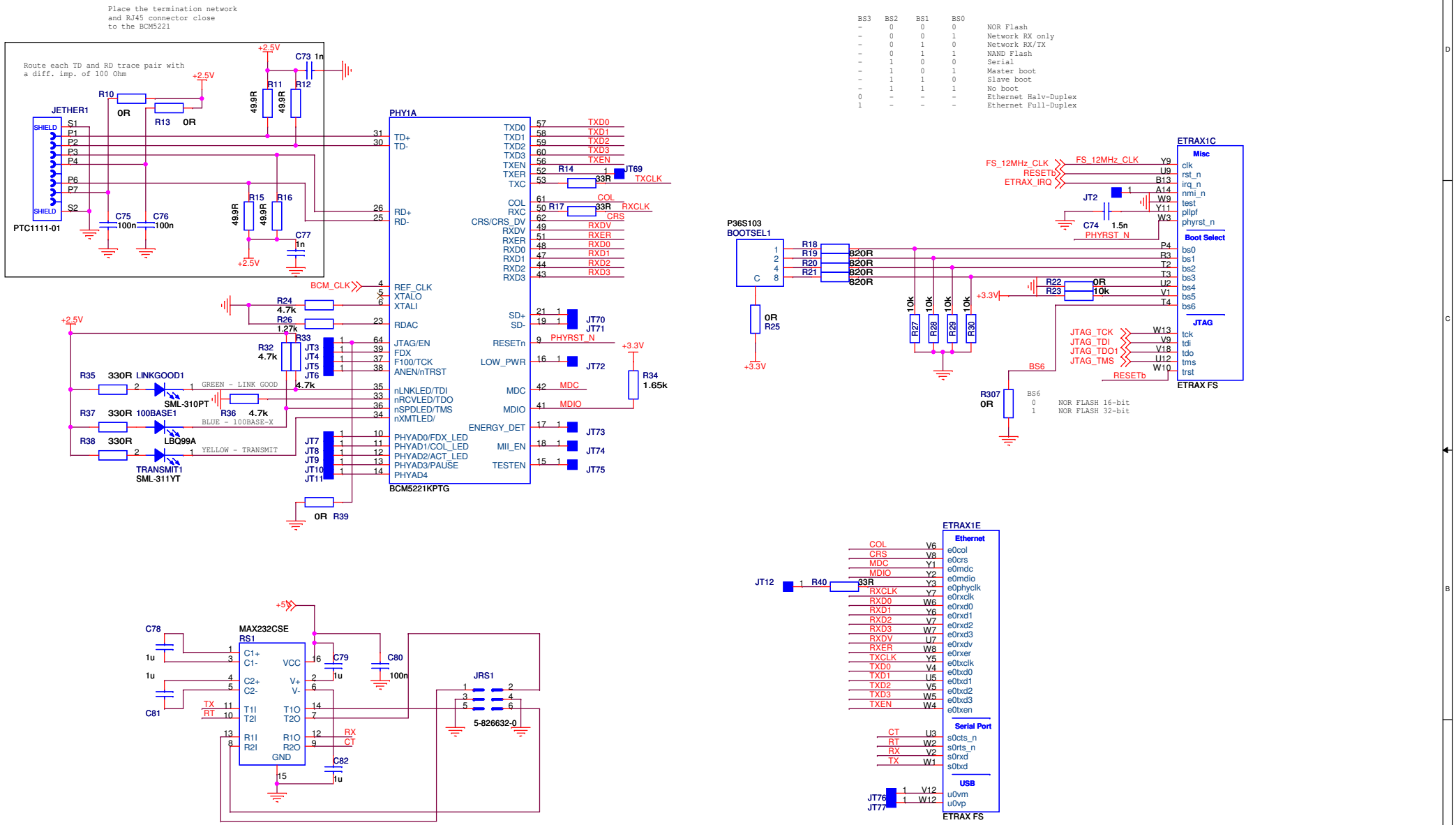

Title	HadesTRB2 - ETRAX B
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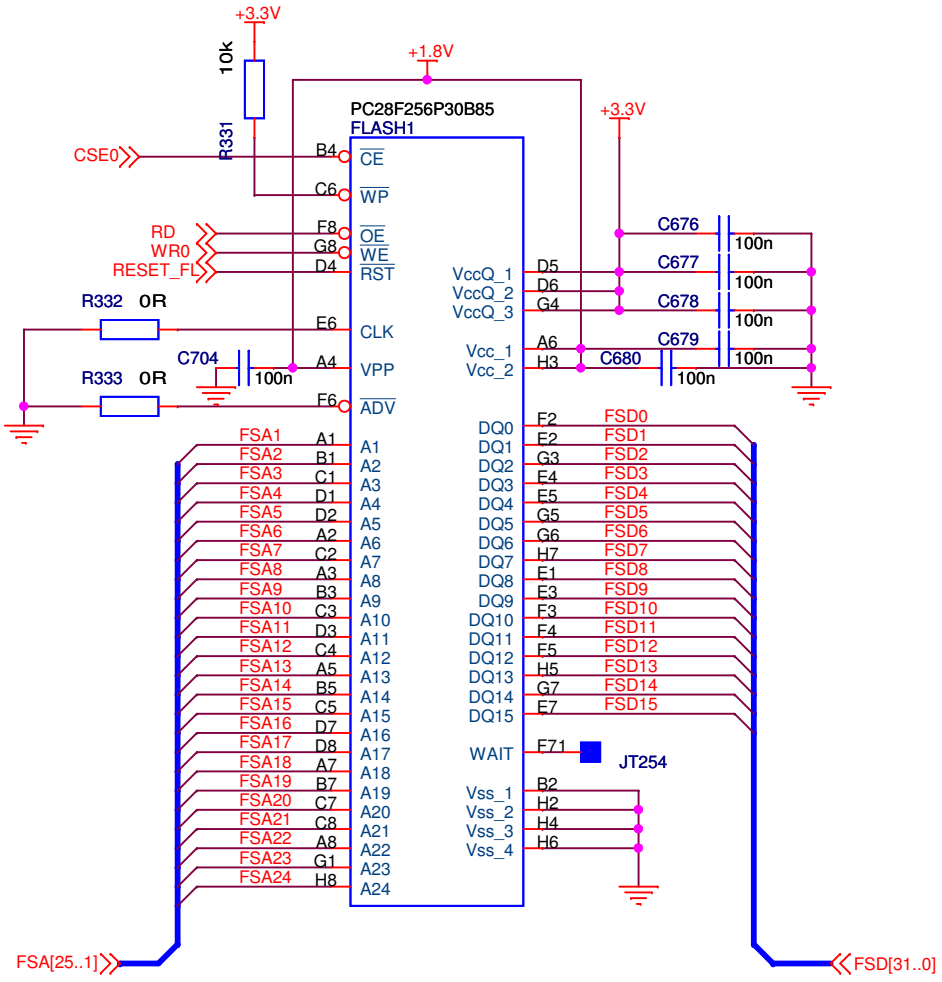

Title	HadesTRB2 - FLASH MEMORY	
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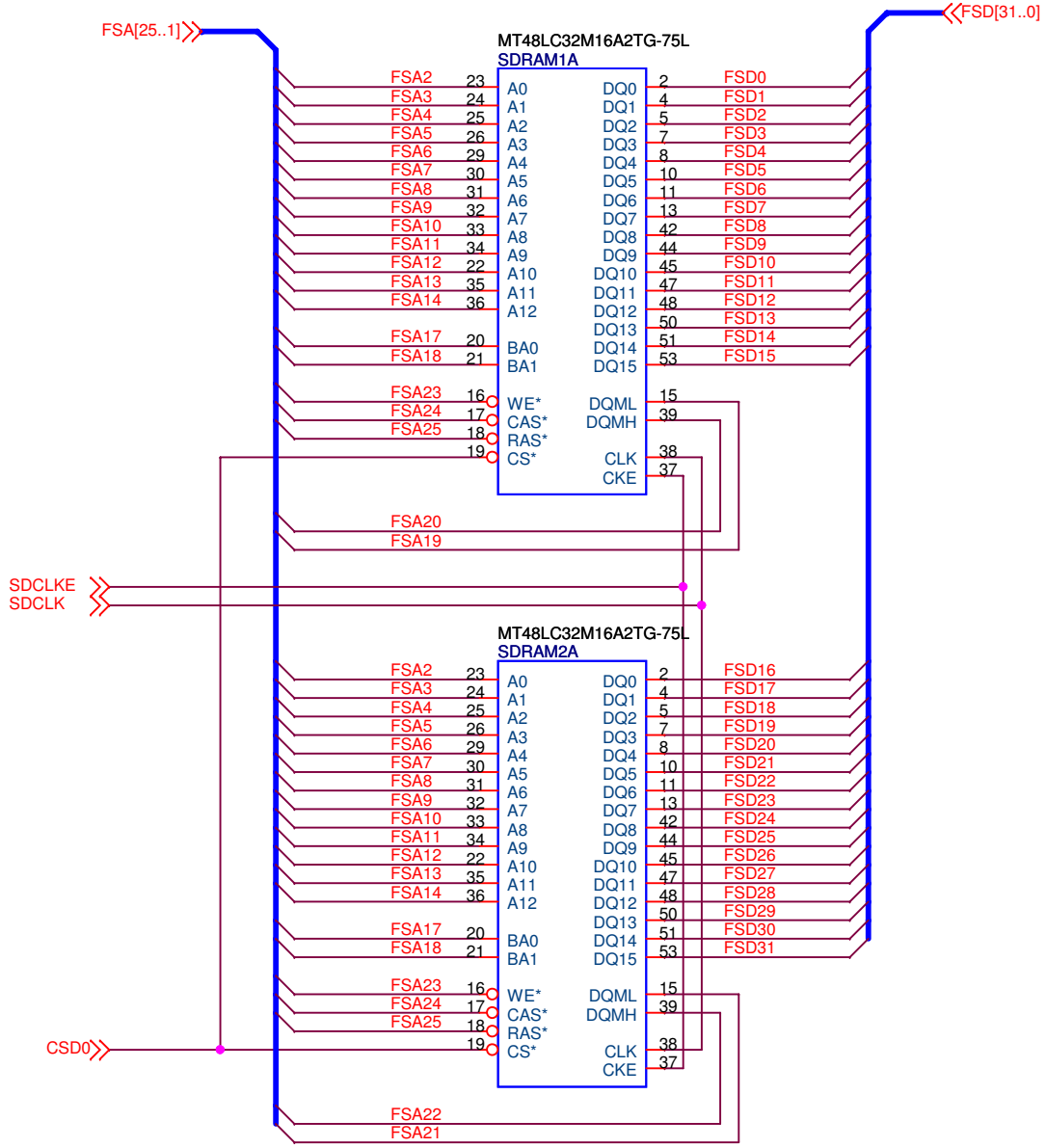

Title	HadesTRB2 - ETRAX SDRAM	
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Routing:
order should be: DAT0, DAT1, CLK, DAT2, DAT3,
no via in between those signals,
only 45° turns (no 90°),
length should be matched for one direction and one port
(they are full duplex)
Peter, please read EE-179 System Design Guidlines.

SHARC I/O is 3.3V compliant

DS - drive strength
default 101

SCLKRAT[2..0]	ratio	(CCLK=ratio * SCLK)
0 0 0 (default)	4	CCLK = 500 MHz
0 1 0	6	CCLK = 600 MHz

Place In CAPS DIRECTLY to DSP pins

Title	HadesTRB2 - SHARC
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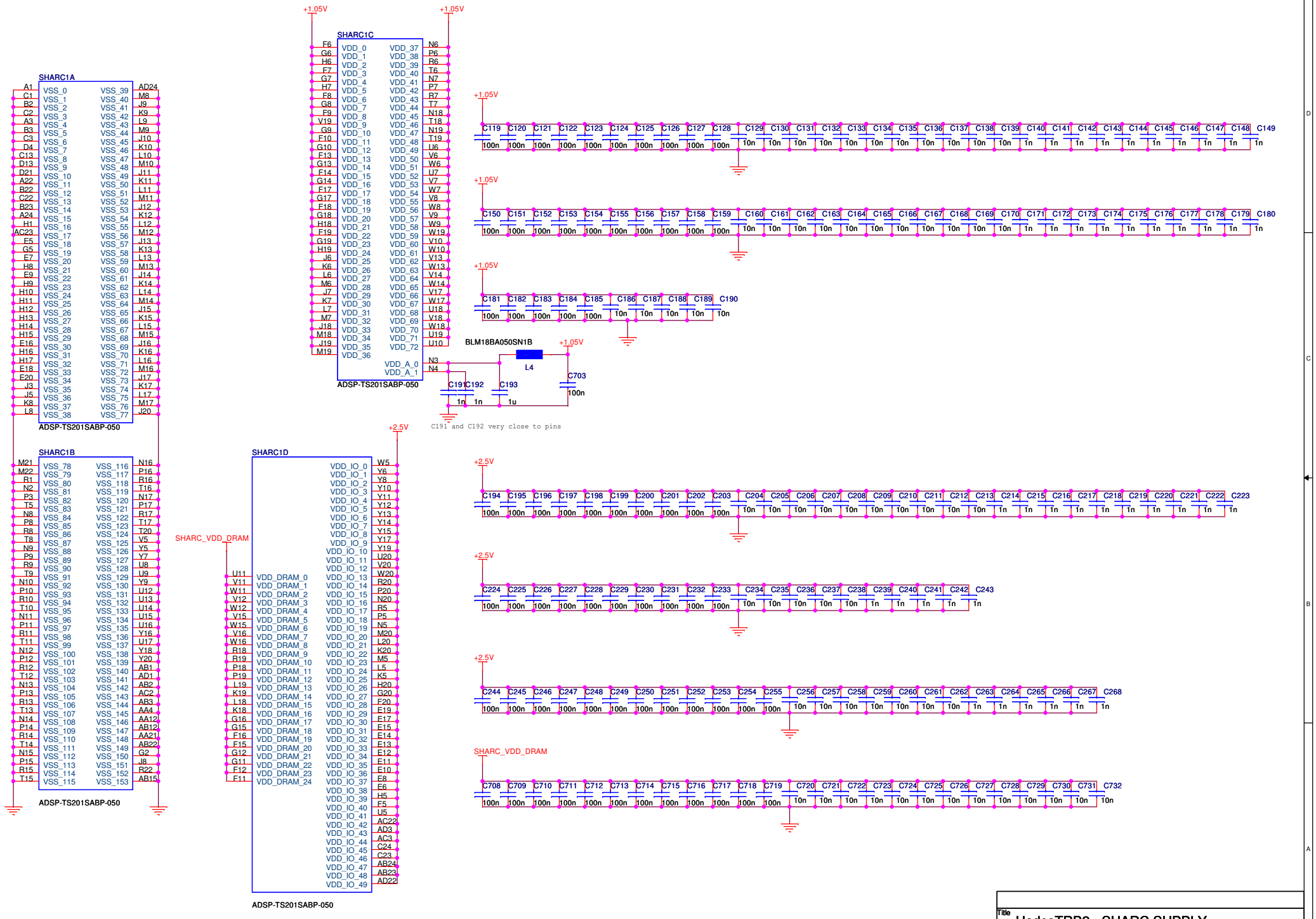

Title: HadesTRB2 - SHARC SUPPLY

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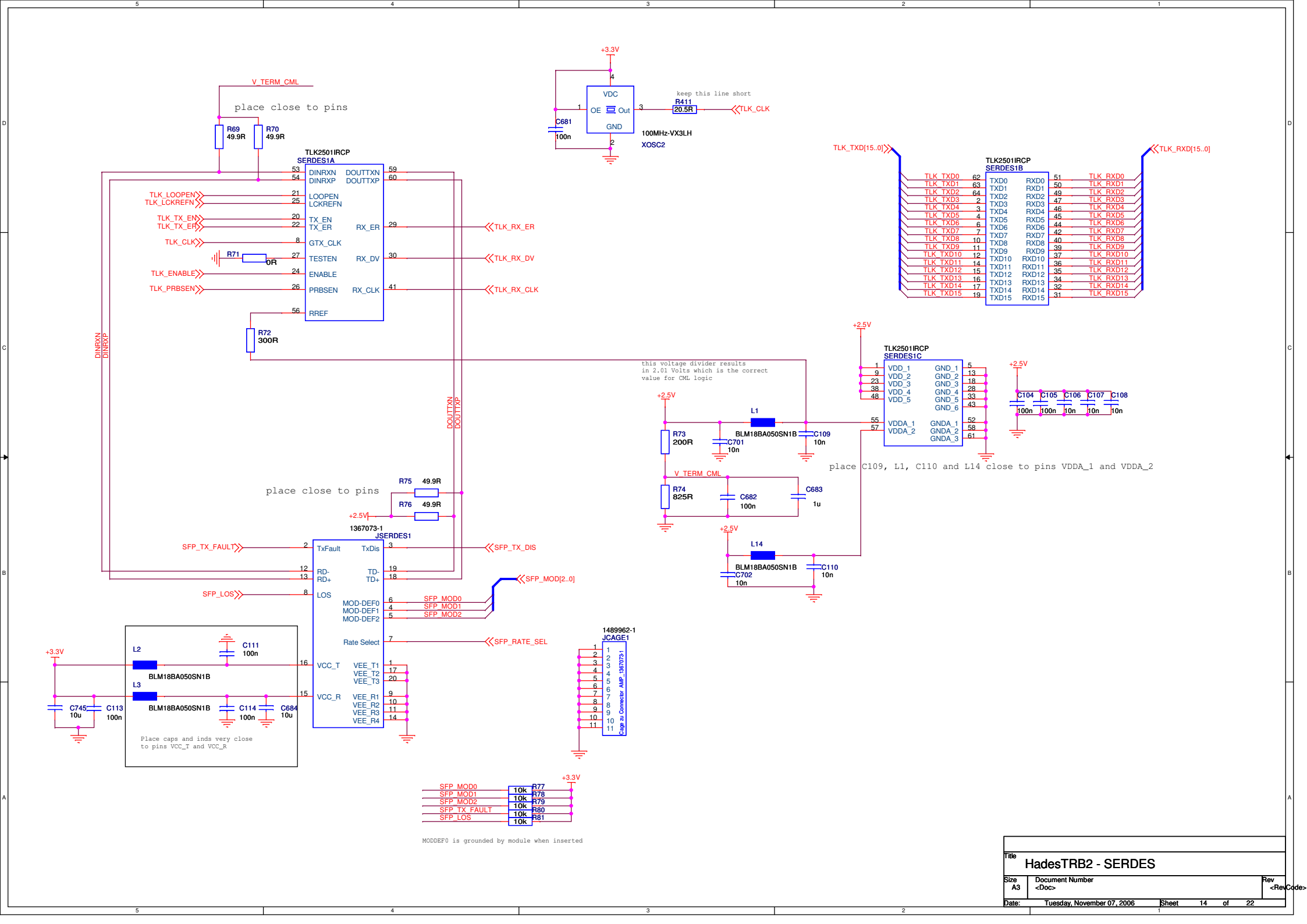
+3.3V
VDC
OE
Out
GND
100MHz-VX3LH
XOSC2
C681
100n
keep this line short
R411
20.5R
TLK_CLK
V_TERM_CML
place close to pins
R69
49.9R
R70
49.9R
TLK2501IRCP
SERDES1A
DINRXN
DINRXP
DOUTTXN
DOUTTXP
TLK_LOOPEN
TLK_LCKREFN
LOOPEN
LCKREFN
TLK_TX_EN
TLK_TX_ER
TX_EN
TX_ER
RX_ER
TLK_RX_ER
TLK_CLK
GTX_CLK
R71
0R
TESTEN
RX_DV
TLK_RX_DV
TLK_ENABLE
ENABLE
TLK_PRBSEN
PRBSEN
RX_CLK
TLK_RX_CLK
RREF
R72
300R
TLK_TXD[15..0]
TLK_RXD[15..0]
TLK2501IRCP
SERDES1B
TXD0
TXD1
TXD2
TXD3
TXD4
TXD5
TXD6
TXD7
TXD8
TXD9
TXD10
TXD11
TXD12
TXD13
TXD14
TXD15
RXD0
RXD1
RXD2
RXD3
RXD4
RXD5
RXD6
RXD7
RXD8
RXD9
RXD10
RXD11
RXD12
RXD13
RXD14
RXD15
this voltage divider results
in 2.01 Volts which is the correct
value for CML logic
+2.5V
TLK2501IRCP
SERDES1C
VDD_1
VDD_2
VDD_3
VDD_4
VDD_5
GND_1
GND_2
GND_3
GND_4
GND_5
GND_6
VDDA_1
VDDA_2
GNDA_1
GNDA_2
GNDA_3
L1
BLM18BA050SN1B
R73
200R
C701
10n
C109
10n
V_TERM_CML
R74
825R
C682
100n
C683
1u
L14
BLM18BA050SN1B
C702
10n
C110
10n
C104
C105
C106
C107
C108
100n
100n
10n
10n
10n
place C109, L1, C110 and L14 close to pins VDDA_1 and VDDA_2
DINRXN
DINRXP
DOUTTXN
DOUTTXP
place close to pins
R75
49.9R
R76
49.9R
+2.5V
1367073-1
JSERDES1
SFP_TX_FAULT
TxFault
TxDis
SFP_TX_DIS
RD-
RD+
TD-
TD+
SFP_LOS
LOS
MOD-DEF0
MOD-DEF1
MOD-DEF2
SFP_MOD0
SFP_MOD1
SFP_MOD2
SFP_MOD[2..0]
Rate Select
SFP_RATE_SEL
VCC_T
VCC_R
VEE_T1
VEE_T2
VEE_T3
VEE_R1
VEE_R2
VEE_R3
VEE_R4
+3.3V
L2
L3
BLM18BA050SN1B
BLM18BA050SN1B
C111
100n
C745
10u
C113
100n
C114
100n
C684
10u
Place caps and inds very close
to pins VCC_T and VCC_R
1489962-1
JCAGE1
Cage zu Connector AMP_1367073-1
SFP_MOD0
SFP_MOD1
SFP_MOD2
SFP_TX_FAULT
SFP_LOS
10k
R77
R78
R79
R80
R81
+3.3V
MODDEF0 is grounded by module when inserted
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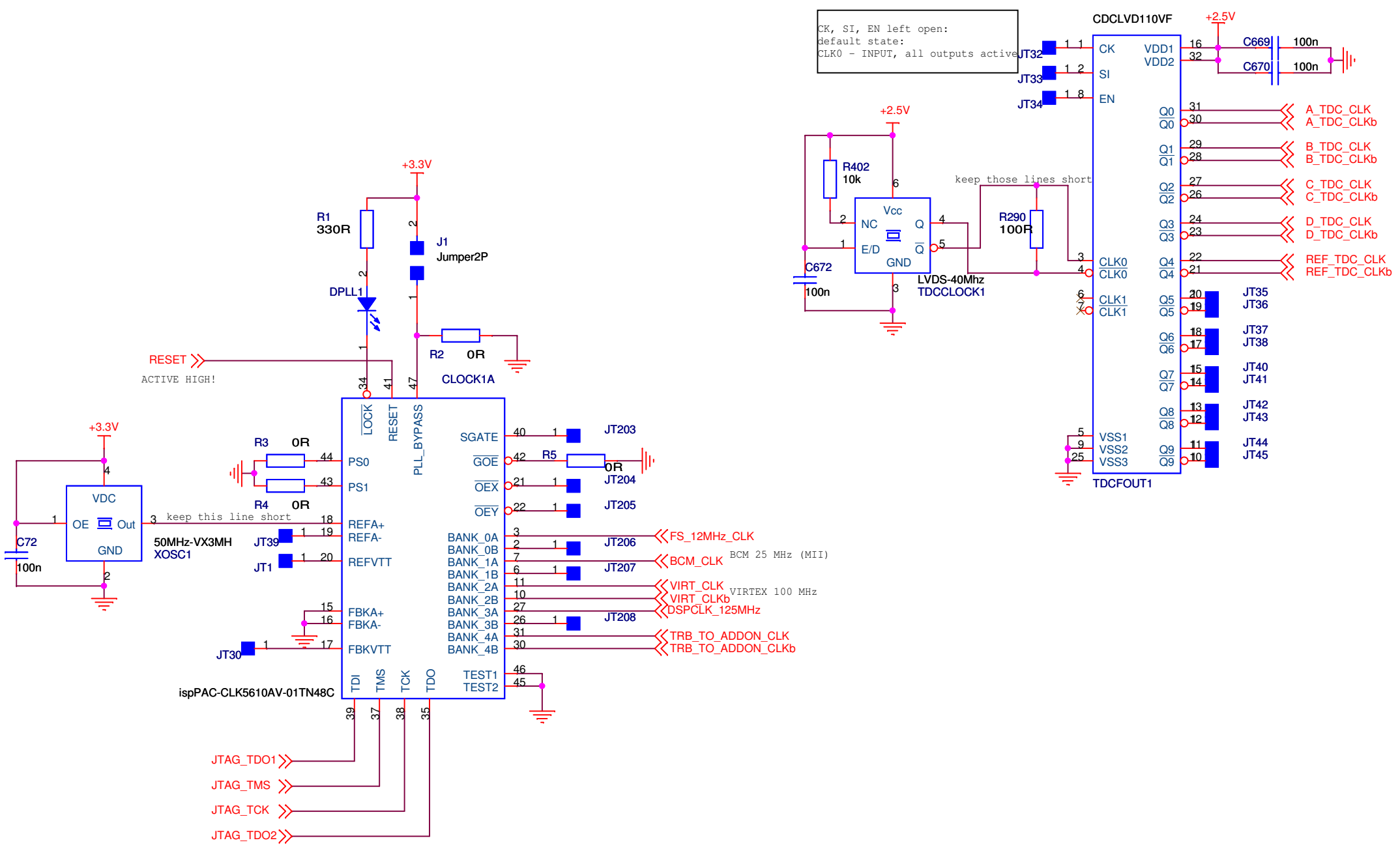

Title	HadesTRB2 - CLOCKS	
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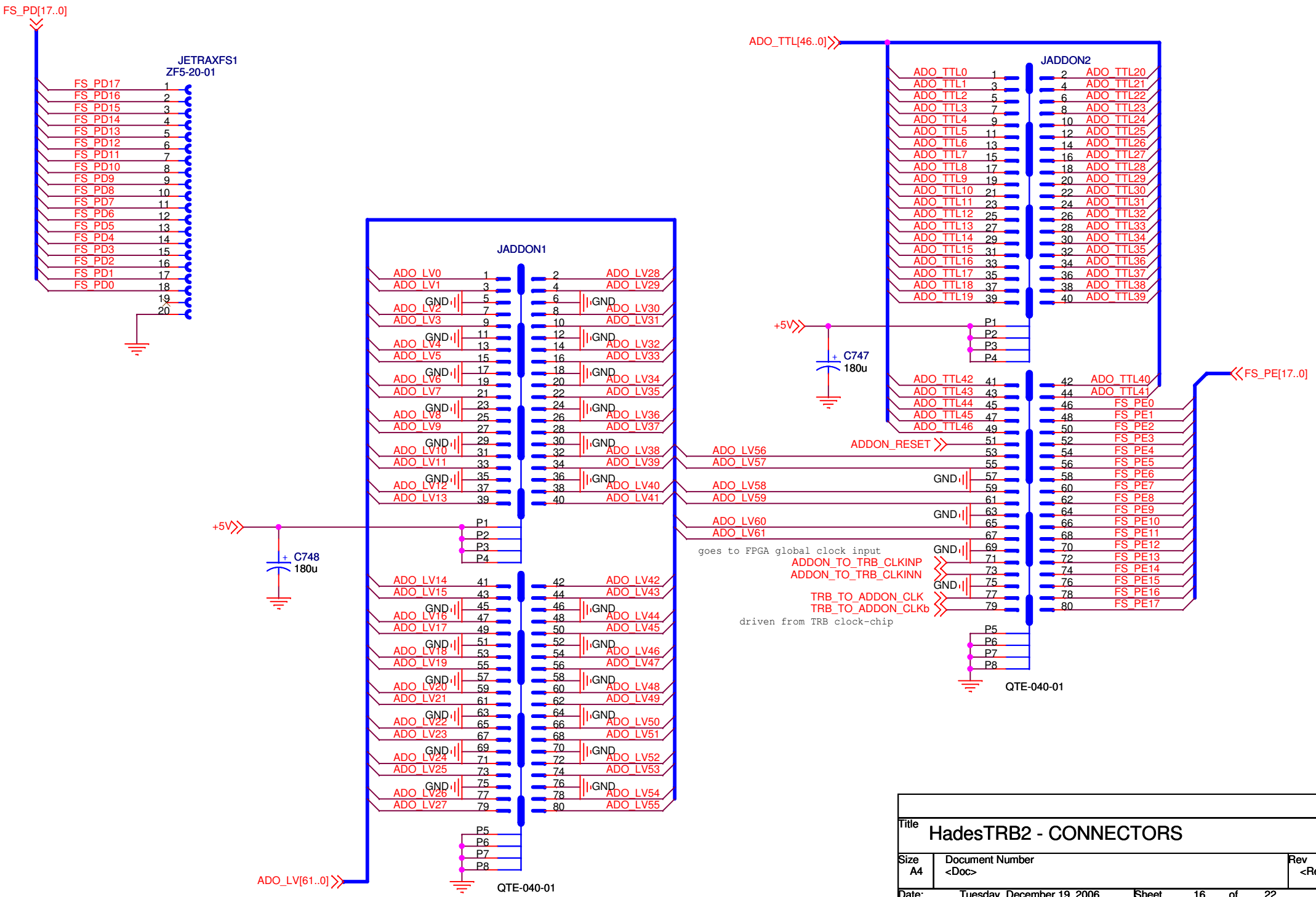
FS_PD[17..0]
JETRAXFS1
ZF5-20-01
FS_PD17 1
FS_PD16 2
FS_PD15 3
FS_PD14 4
FS_PD13 5
FS_PD12 6
FS_PD11 7
FS_PD10 8
FS_PD9 9
FS_PD8 10
FS_PD7 11
FS_PD6 12
FS_PD5 13
FS_PD4 14
FS_PD3 15
FS_PD2 16
FS_PD1 17
FS_PD0 18
19
20
JADDON1
ADO_LV0 1
ADO_LV1 3
GND 5
ADO_LV2 7
ADO_LV3 9
GND 11
ADO_LV4 13
ADO_LV5 15
GND 17
ADO_LV6 19
ADO_LV7 21
GND 23
ADO_LV8 25
ADO_LV9 27
GND 29
ADO_LV10 31
ADO_LV11 33
GND 35
ADO_LV12 37
ADO_LV13 39
2 ADO_LV28
4 ADO_LV29
6 GND
8 ADO_LV30
10 ADO_LV31
12 GND
14 ADO_LV32
16 ADO_LV33
18 GND
20 ADO_LV34
22 ADO_LV35
24 GND
26 ADO_LV36
28 ADO_LV37
30 GND
32 ADO_LV38
34 ADO_LV39
36 GND
38 ADO_LV40
40 ADO_LV41
P1
P2
P3
P4
ADO_LV14 41
ADO_LV15 43
GND 45
ADO_LV16 47
ADO_LV17 49
GND 51
ADO_LV18 53
ADO_LV19 55
GND 57
ADO_LV20 59
ADO_LV21 61
GND 63
ADO_LV22 65
ADO_LV23 67
GND 69
ADO_LV24 71
ADO_LV25 73
GND 75
ADO_LV26 77
ADO_LV27 79
42 ADO_LV42
44 ADO_LV43
46 GND
48 ADO_LV44
50 ADO_LV45
52 GND
54 ADO_LV46
56 ADO_LV47
58 GND
60 ADO_LV48
62 ADO_LV49
64 GND
66 ADO_LV50
68 ADO_LV51
70 GND
72 ADO_LV52
74 ADO_LV53
76 GND
78 ADO_LV54
80 ADO_LV55
P5
P6
P7
P8
QTE-040-01
+5V
C748
180u
ADO_LV[61..0]
ADO_TTL[46..0]
JADDON2
ADO_TTL0 1
ADO_TTL1 3
ADO_TTL2 5
ADO_TTL3 7
ADO_TTL4 9
ADO_TTL5 11
ADO_TTL6 13
ADO_TTL7 15
ADO_TTL8 17
ADO_TTL9 19
ADO_TTL10 21
ADO_TTL11 23
ADO_TTL12 25
ADO_TTL13 27
ADO_TTL14 29
ADO_TTL15 31
ADO_TTL16 33
ADO_TTL17 35
ADO_TTL18 37
ADO_TTL19 39
2 ADO_TTL20
4 ADO_TTL21
6 ADO_TTL22
8 ADO_TTL23
10 ADO_TTL24
12 ADO_TTL25
14 ADO_TTL26
16 ADO_TTL27
18 ADO_TTL28
20 ADO_TTL29
22 ADO_TTL30
24 ADO_TTL31
26 ADO_TTL32
28 ADO_TTL33
30 ADO_TTL34
32 ADO_TTL35
34 ADO_TTL36
36 ADO_TTL37
38 ADO_TTL38
40 ADO_TTL39
P1
P2
P3
P4
+5V
C747
180u
ADO_TTL42 41
ADO_TTL43 43
ADO_TTL44 45
ADO_TTL45 47
ADO_TTL46 49
ADDON_RESET 51
GND 53
GND 55
GND 57
GND 59
GND 61
GND 63
GND 65
GND 67
GND 69
GND 71
GND 73
GND 75
GND 77
79
42 ADO_TTL40
44 ADO_TTL41
46 FS_PE0
48 FS_PE1
50 FS_PE2
52 FS_PE3
54 FS_PE4
56 FS_PE5
58 FS_PE6
60 FS_PE7
62 FS_PE8
64 FS_PE9
66 FS_PE10
68 FS_PE11
70 FS_PE12
72 FS_PE13
74 FS_PE14
76 FS_PE15
78 FS_PE16
80 FS_PE17
FS_PE[17..0]
P5
P6
P7
P8
QTE-040-01
ADO_LV56
ADO_LV57
ADO_LV58
ADO_LV59
ADO_LV60
ADO_LV61
goes to FPGA global clock input
ADDON_TO_TRB_CLKINP
ADDON_TO_TRB_CLKINN
TRB_TO_ADDON_CLK
TRB_TO_ADDON_CLKb
driven from TRB clock-chip
Title
HadesTRB2 - CONNECTORS
Size
A4
Document Number
<Doc>
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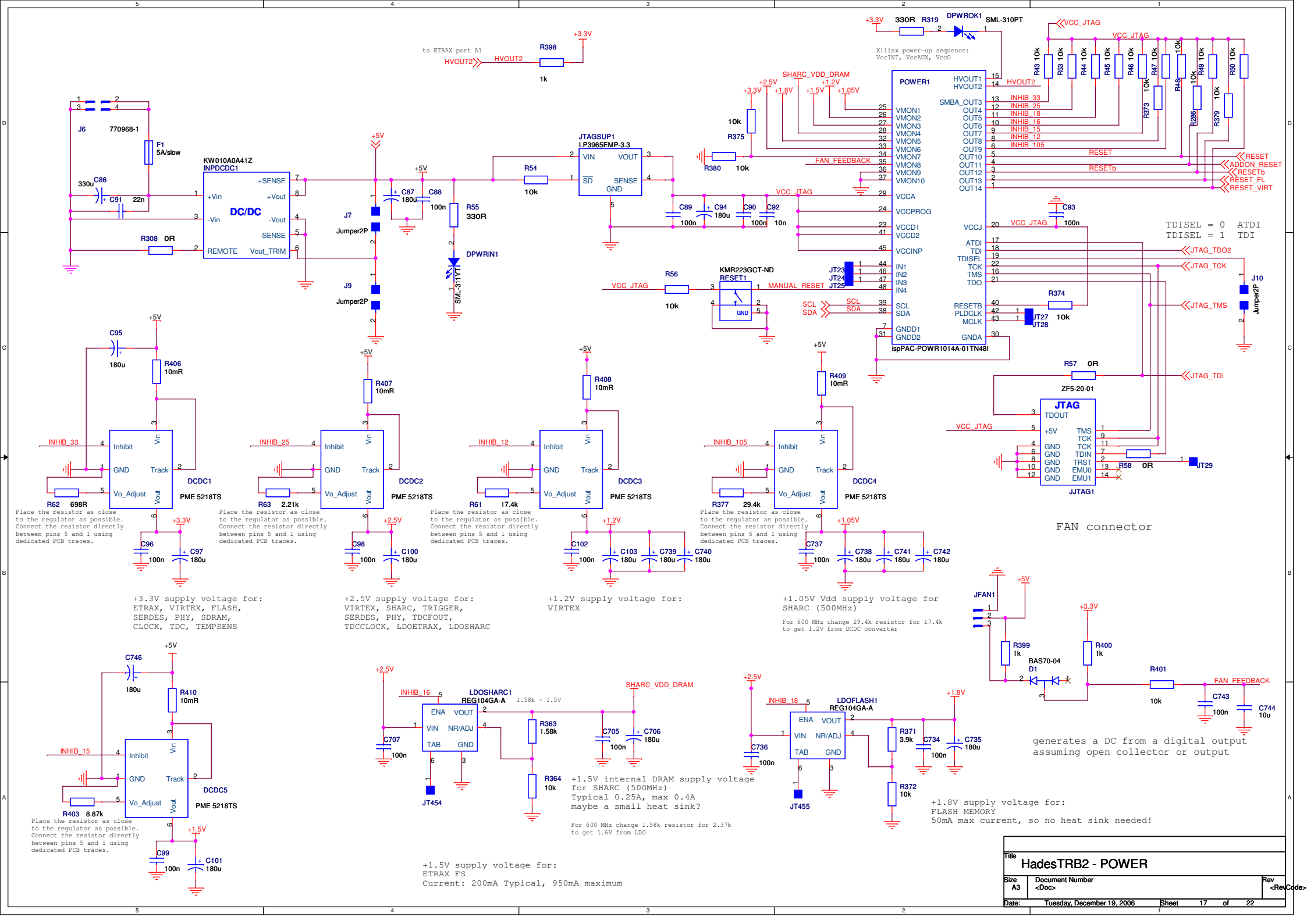
J6 770968-1
F1 5A/slow
KW010A0A41Z INPDCDC1
DC/DC
+Vin -Vin REMOTE +SENSE +Vout -Vout -SENSE Vout_TRIM
330u C86
C91 22n
R308 0R
J7 Jumper2P
J9 Jumper2P
C87 180u
C88 100n
R55 330R
DPWRIN1
SML-311YT
JTAGSUP1 LP3965EMP-3.3
VIN VOUT SD SENSE GND
R54 10k
C89 100n
C94 180u
C90 100n
C92 10n
VCC_JTAG
R56 10k
KMR223GCT-ND RESET1
MANUAL_RESET
to ETRAX port A1
HVOUT2
R398 1k
+3.3V 330R R319 DPWROK1 SML-310PT
Xilinx power-up sequence:
VccINT, VccAUX, VccO
SHARC_VDD_DRAM
R375 10k
R380 10k
FAN_FEEDBACK
POWER1
VMON1 VMON2 VMON3 VMON4 VMON5 VMON6 VMON7 VMON8 VMON9 VMON10
VCCA VCCPROG VCCD1 VCCD2 VCCINP
IN1 IN2 IN3 IN4
SCL SDA
GNDD1 GNDD2
HVOUT1 HVOUT2
SMBA_OUT3 OUT4 OUT5 OUT6 OUT7 OUT8 OUT9 OUT10 OUT11 OUT12 OUT13 OUT14
VCCJ ATDI TDI TDISEL TCK TMS TDO
RESETB PLDCLK MCLK
GNDA
ispPAC-POWR1014A-01TN48I
INHIB_33 INHIB_25 INHIB_16 INHIB_18 INHIB_15 INHIB_12 INHIB_105
RESET ADDON_RESET RESETb RESET_FL RESET_VIRT
R43 10k R53 10k R44 10k R45 10k R46 10k R47 10k R48 10k R49 10k R50 10k
R373 10k R286 10k R379 10k
C93 100n
R374 10k
JT27 JT28
TDISEL = 0 ATDI
TDISEL = 1 TDI
JTAG_TDO2 JTAG_TCK JTAG_TMS JTAG_TDI
J10 Jumper2P
R57 0R ZF5-20-01
JTAG TDOUT +5V TMS TCK GND TCK GND TDIN GND TRST GND EMU0 GND EMU1
JJTAG1
R58 0R JT29
C95 180u
R406 10mR
DCDC1 PME 5218TS
Inhibit Vin GND Track Vo_Adjust Vout
R62 698R
C96 100n
C97 180u
R407 10mR
DCDC2 PME 5218TS
R63 2.21k
C98 100n
C100 180u
R408 10mR
DCDC3 PME 5218TS
R61 17.4k
C102 100n
C103 180u
C739 180u
C740 180u
R409 10mR
DCDC4 PME 5218TS
R377 29.4k
C737 100n
C738 180u
C741 180u
C742 180u
Place the resistor as close to the regulator as possible. Connect the resistor directly between pins 5 and 1 using dedicated PCB traces.
+3.3V supply voltage for:
ETRAX, VIRTEX, FLASH,
SERDES, PHY, SDRAM,
CLOCK, TDC, TEMPSENS
+2.5V supply voltage for:
VIRTEX, SHARC, TRIGGER,
SERDES, PHY, TDCFOUT,
TDCCLOCK, LDOETRAX, LDOSHARC
+1.2V supply voltage for:
VIRTEX
+1.05V Vdd supply voltage for
SHARC (500MHz)
For 600 MHz change 29.4k resistor for 17.4k
to get 1.2V from DCDC converter
FAN connector
C746 180u
R410 10mR
DCDC5 PME 5218TS
R403 8.87k
C99 100n
C101 180u
LDOSHARC1 REG104GA-A
ENA VOUT VIN NR/ADJ TAB GND
1.58k - 1.5V
R363 1.58k
R364 10k
C705 100n
C706 180u
C707 100n
JT454
+1.5V internal DRAM supply voltage
for SHARC (500MHz)
Typical 0.25A, max 0.4A
maybe a small heat sink?
For 600 MHz change 1.58k resistor for 2.37k
to get 1.6V from LDO
+1.5V supply voltage for:
ETRAX FS
Current: 200mA Typical, 950mA maximum
LDOFLASH1 REG104GA-A
R371 3.9k
R372 10k
C734 100n
C735 180u
C736 100n
JT455
+1.8V supply voltage for:
FLASH MEMORY
50mA max current, so no heat sink needed!
JFAN1
R399 1k
R400 1k
BAS70-04 D1
R401 10k
C743 100n
C744 10u
generates a DC from a digital output
assuming open collector or output
Title HadesTRB2 - POWER
Size A3
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Date: Tuesday, December 19, 2006
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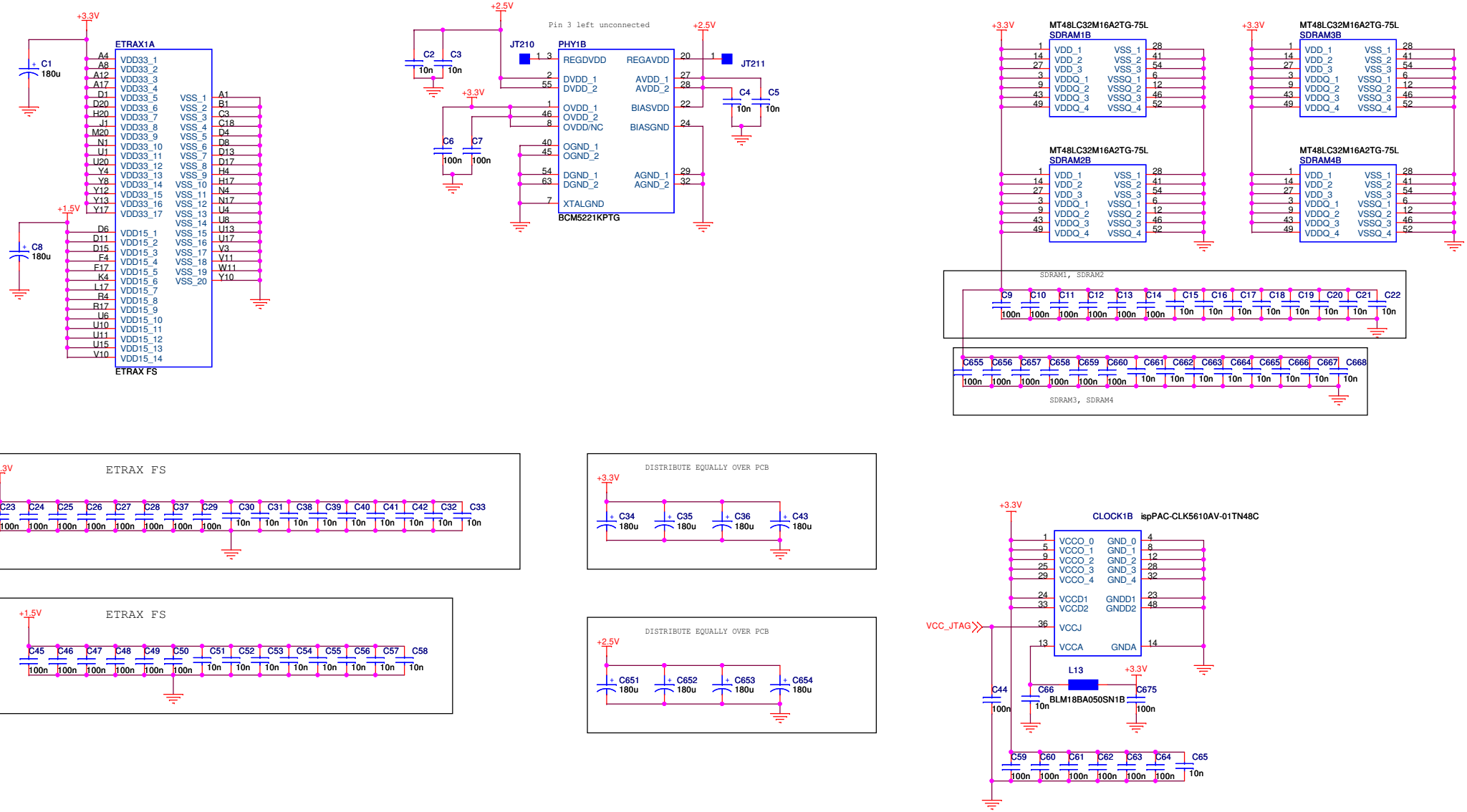
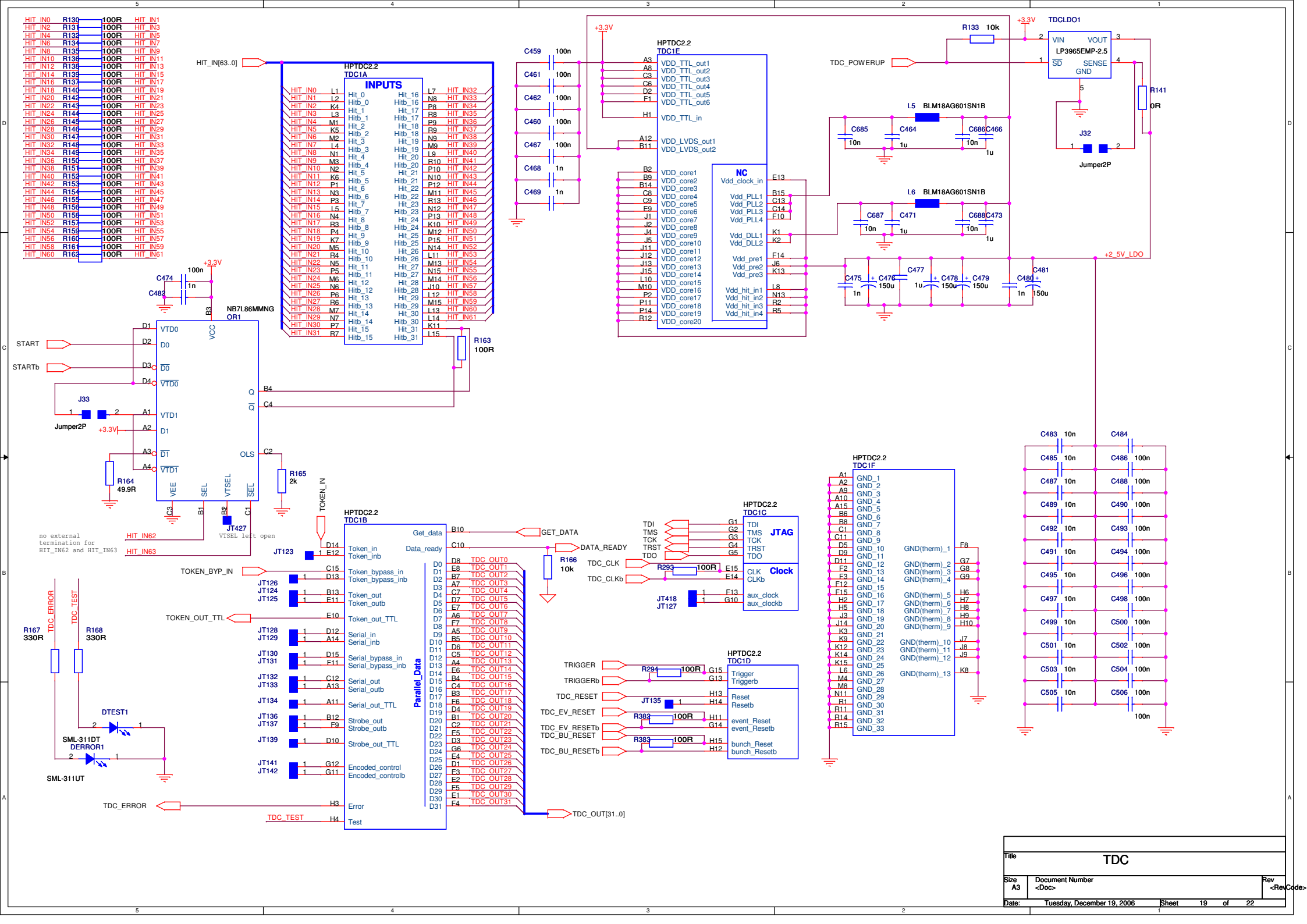

ETRAX FS
BCM5221KPTG
Pin 3 left unconnected
MT48LC32M16A2TG-75L
SDRAM1B
SDRAM2B
SDRAM3B
SDRAM4B
SDRAM1, SDRAM2
SDRAM3, SDRAM4
DISTRIBUTE EQUALLY OVER PCB
CLOCK1B ispPAC-CLK5610AV-01TN48C
BLM18BA050SN1B
VCC_JTAG
HadesTRB2 - CAPACITORS
Tuesday, November 07, 2006


HIT_IN0 R130 100R HIT_IN1
HIT_IN2 R131 100R HIT_IN3
HIT_IN4 R132 100R HIT_IN5
HIT_IN6 R134 100R HIT_IN7
HIT_IN8 R135 100R HIT_IN9
HIT_IN10 R136 100R HIT_IN11
HIT_IN12 R138 100R HIT_IN13
HIT_IN14 R139 100R HIT_IN15
HIT_IN16 R137 100R HIT_IN17
HIT_IN18 R140 100R HIT_IN19
HIT_IN20 R142 100R HIT_IN21
HIT_IN22 R143 100R HIT_IN23
HIT_IN24 R144 100R HIT_IN25
HIT_IN26 R145 100R HIT_IN27
HIT_IN28 R146 100R HIT_IN29
HIT_IN30 R147 100R HIT_IN31
HIT_IN32 R148 100R HIT_IN33
HIT_IN34 R149 100R HIT_IN35
HIT_IN36 R150 100R HIT_IN37
HIT_IN38 R151 100R HIT_IN39
HIT_IN40 R152 100R HIT_IN41
HIT_IN42 R153 100R HIT_IN43
HIT_IN44 R154 100R HIT_IN45
HIT_IN46 R155 100R HIT_IN47
HIT_IN48 R156 100R HIT_IN49
HIT_IN50 R158 100R HIT_IN51
HIT_IN52 R157 100R HIT_IN53
HIT_IN54 R159 100R HIT_IN55
HIT_IN56 R160 100R HIT_IN57
HIT_IN58 R161 100R HIT_IN59
HIT_IN60 R162 100R HIT_IN61
HIT_IN[63..0]
HPTDC2.2
TDC1A
INPUTS
Hit_0 Hitb_0 Hit_1 Hitb_1 Hit_2 Hitb_2 Hit_3 Hitb_3 Hit_4 Hitb_4 Hit_5 Hitb_5 Hit_6 Hitb_6 Hit_7 Hitb_7 Hit_8 Hitb_8 Hit_9 Hitb_9 Hit_10 Hitb_10 Hit_11 Hitb_11 Hit_12 Hitb_12 Hit_13 Hitb_13 Hit_14 Hitb_14 Hit_15 Hitb_15
Hit_16 Hitb_16 Hit_17 Hitb_17 Hit_18 Hitb_18 Hit_19 Hitb_19 Hit_20 Hitb_20 Hit_21 Hitb_21 Hit_22 Hitb_22 Hit_23 Hitb_23 Hit_24 Hitb_24 Hit_25 Hitb_25 Hit_26 Hitb_26 Hit_27 Hitb_27 Hit_28 Hitb_28 Hit_29 Hitb_29 Hit_30 Hitb_30 Hit_31 Hitb_31
C459 100n
C461 100n
C462 100n
C460 100n
C467 100n
C468 1n
C469 1n
+3.3V
HPTDC2.2
TDC1E
VDD_TTL_out1 VDD_TTL_out2 VDD_TTL_out3 VDD_TTL_out4 VDD_TTL_out5 VDD_TTL_out6
VDD_TTL_in
VDD_LVDS_out1 VDD_LVDS_out2
VDD_core1 VDD_core2 VDD_core3 VDD_core4 VDD_core5 VDD_core6 VDD_core7 VDD_core8 VDD_core9 VDD_core10 VDD_core11 VDD_core12 VDD_core13 VDD_core14 VDD_core15 VDD_core16 VDD_core17 VDD_core18 VDD_core19 VDD_core20
NC
Vdd_clock_in
Vdd_PLL1 Vdd_PLL2 Vdd_PLL3 Vdd_PLL4
Vdd_DLL1 Vdd_DLL2
Vdd_pre1 Vdd_pre2 Vdd_pre3
Vdd_hit_in1 Vdd_hit_in2 Vdd_hit_in3 Vdd_hit_in4
TDC_POWERUP
R133 10k
TDCLDO1
VIN VOUT
LP3965EMP-2.5
SD SENSE GND
R141 0R
J32
Jumper2P
L5 BLM18AG601SN1B
L6 BLM18AG601SN1B
C685 10n
C464 1u
C686 10n
C466 1u
C687 10n
C471 1u
C688 10n
C473 1u
C475 1n
C476 150u
C477 1u
C478 150u
C479 150u
C480 1n
C481 150u
+2_5V_LDO
C474 1n
C482 100n
+3.3V
NB7L86MMNG
OR1
VTD0 D0 VTD1 D1 VCC Q QI OLS VEE SEL VTSEL SEL
START
STARTb
J33
Jumper2P
R163 100R
R164 49.9R
R165 2k
JT427
VTSEL left open
no external termination for HIT_IN62 and HIT_IN63
HIT_IN62
HIT_IN63
TOKEN_IN
HPTDC2.2
TDC1B
Get_data Data_ready
Token_in Token_inb Token_bypass_in Token_bypass_inb Token_out Token_outb Token_out_TTL Serial_in Serial_inb Serial_bypass_in Serial_bypass_inb Serial_out Serial_outb Serial_out_TTL Strobe_out Strobe_outb Strobe_out_TTL Encoded_control Encoded_controlb Error Test
Parallel_Data
TDC_OUT0 TDC_OUT1 TDC_OUT2 TDC_OUT3 TDC_OUT4 TDC_OUT5 TDC_OUT6 TDC_OUT7 TDC_OUT8 TDC_OUT9 TDC_OUT10 TDC_OUT11 TDC_OUT12 TDC_OUT13 TDC_OUT14 TDC_OUT15 TDC_OUT16 TDC_OUT17 TDC_OUT18 TDC_OUT19 TDC_OUT20 TDC_OUT21 TDC_OUT22 TDC_OUT23 TDC_OUT24 TDC_OUT25 TDC_OUT26 TDC_OUT27 TDC_OUT28 TDC_OUT29 TDC_OUT30 TDC_OUT31
TDC_OUT[31..0]
JT123
JT126 JT124 JT125
JT128 JT129
JT130 JT131
JT132 JT133
JT134
JT136 JT137
JT139
JT141 JT142
TOKEN_BYP_IN
TOKEN_OUT_TTL
TDC_ERROR
TDC_TEST
R167 330R
R168 330R
DTEST1
SML-311DT
DERROR1
SML-311UT
GET_DATA
DATA_READY
R166 10k
HPTDC2.2
TDC1C
JTAG
TDI TMS TCK TRST TDO
Clock
CLK CLKb aux_clock aux_clockb
TDC_CLK
TDC_CLKb
R293 100R
JT418 JT127
HPTDC2.2
TDC1D
Trigger Triggerb Reset Resetb event_Reset event_Resetb bunch_Reset bunch_Resetb
TRIGGER
TRIGGERb
TDC_RESET
TDC_EV_RESET
TDC_EV_RESETb
TDC_BU_RESET
TDC_BU_RESETb
R294 100R
JT135
R382 100R
R383 100R
HPTDC2.2
TDC1F
GND_1 GND_2 GND_3 GND_4 GND_5 GND_6 GND_7 GND_8 GND_9 GND_10 GND_11 GND_12 GND_13 GND_14 GND_15 GND_16 GND_17 GND_18 GND_19 GND_20 GND_21 GND_22 GND_23 GND_24 GND_25 GND_26 GND_27 GND_28 GND_29 GND_30 GND_31 GND_32 GND_33
GND(therm)_1 GND(therm)_2 GND(therm)_3 GND(therm)_4 GND(therm)_5 GND(therm)_6 GND(therm)_7 GND(therm)_8 GND(therm)_9 GND(therm)_10 GND(therm)_11 GND(therm)_12 GND(therm)_13
C483 10n C484
C485 10n C486 100n
C487 10n C488 100n
C489 10n C490 100n
C492 10n C493 100n
C491 10n C494 100n
C495 10n C496 100n
C497 10n C498 100n
C499 10n C500 100n
C501 10n C502 100n
C503 10n C504 100n
C505 10n C506 100n
100n
Title
TDC
Size A3
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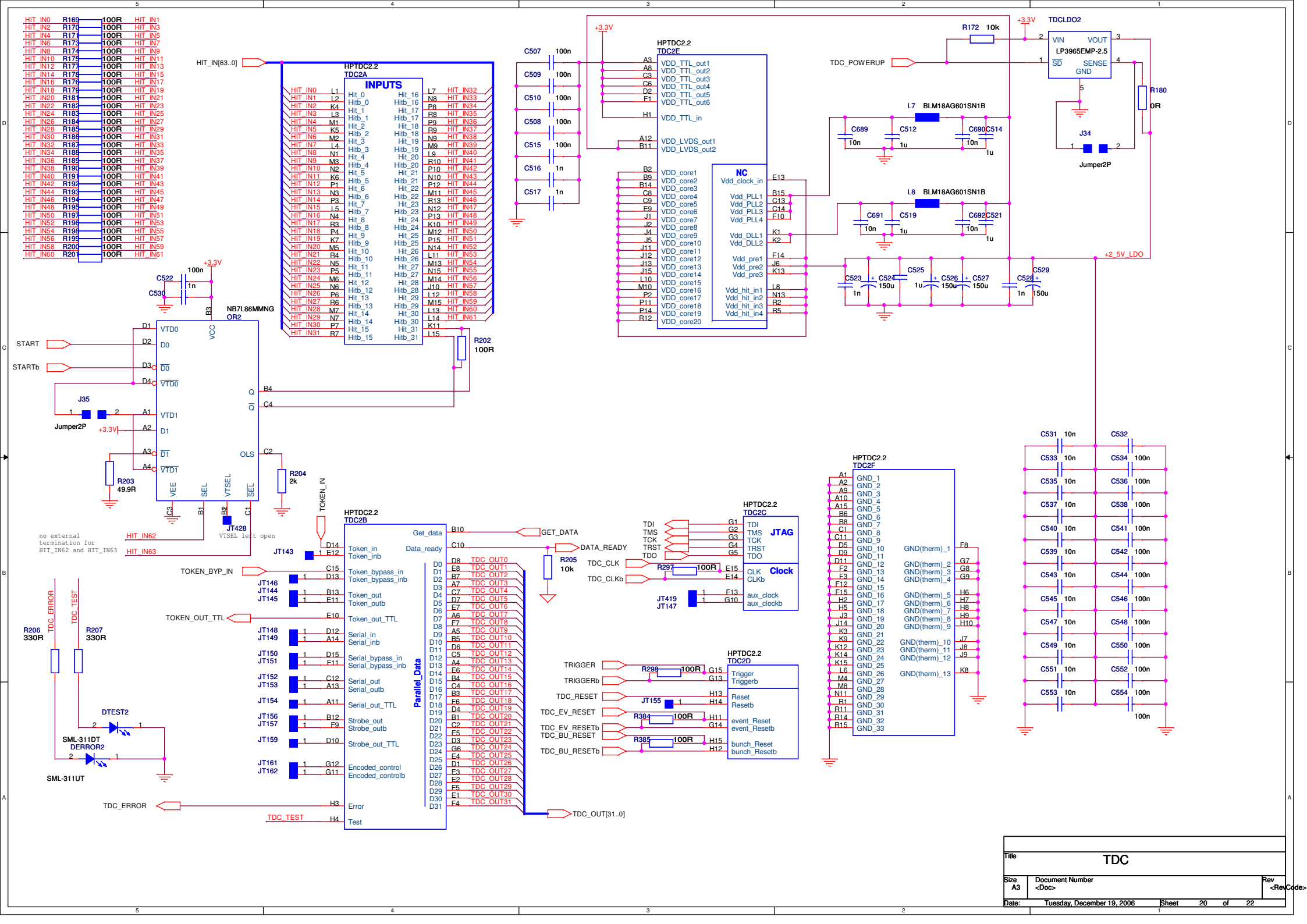
HIT_IN[63..0]
HPTDC2.2
TDC2A
INPUTS
HPTDC2.2
TDC2E
TDC_POWERUP
TDCLDO2
LP3965EMP-2.5
R172 10k
R180 0R
L7 BLM18AG601SN1B
L8 BLM18AG601SN1B
Jumper2P
+2_5V_LDO
NB7L86MMNG
OR2
START
STARTb
J35
R202 100R
R203 49.9R
R204 2k
JT428
VTSEL left open
no external termination for HIT_IN62 and HIT_IN63
HPTDC2.2
TDC2B
Parallel_Data
TOKEN_BYP_IN
TOKEN_OUT_TTL
R206 330R
R207 330R
DTEST2
SML-311DT
DERROR2
SML-311UT
TDC_ERROR
TDC_TEST
GET_DATA
DATA_READY
R205 10k
HPTDC2.2
TDC2C
JTAG
Clock
TDC_CLK
TDC_CLKb
R297 100R
JT419
JT147
HPTDC2.2
TDC2D
TRIGGER
TRIGGERb
TDC_RESET
TDC_EV_RESET
TDC_EV_RESETb
TDC_BU_RESET
TDC_BU_RESETb
R298 100R
JT155
R384 100R
R385 100R
TDC_OUT[31..0]
HPTDC2.2
TDC2F
GND_1
GND_2
GND_3
GND_4
GND_5
GND_6
GND_7
GND_8
GND_9
GND_10
GND_11
GND_12
GND_13
GND_14
GND_15
GND_16
GND_17
GND_18
GND_19
GND_20
GND_21
GND_22
GND_23
GND_24
GND_25
GND_26
GND_27
GND_28
GND_29
GND_30
GND_31
GND_32
GND_33
GND(therm)_1
GND(therm)_2
GND(therm)_3
GND(therm)_4
GND(therm)_5
GND(therm)_6
GND(therm)_7
GND(therm)_8
GND(therm)_9
GND(therm)_10
GND(therm)_11
GND(therm)_12
GND(therm)_13
Title
TDC
Size A3
Document Number <Doc>
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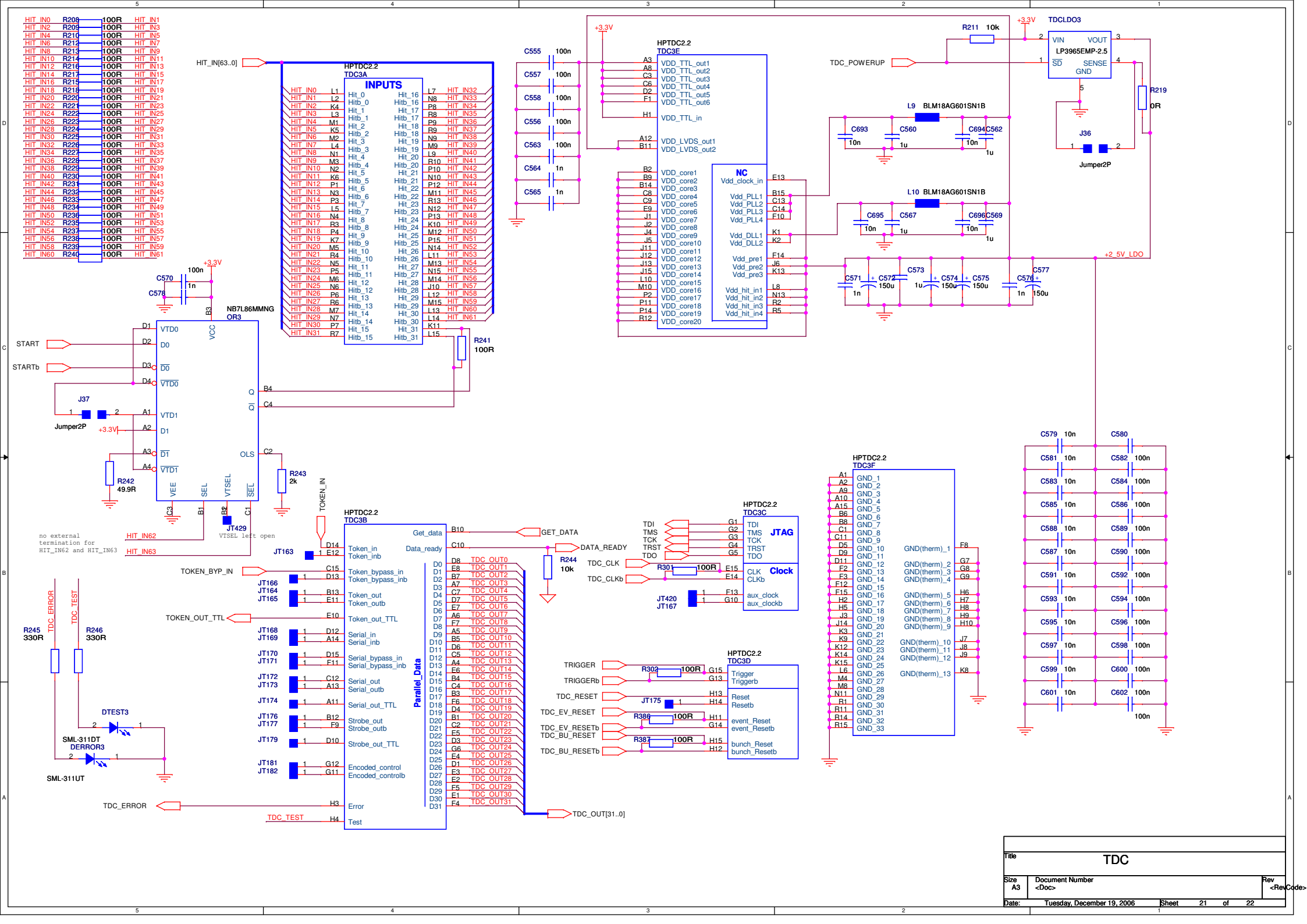
HIT_IN0 R208 100R HIT_IN1
HIT_IN2 R209 100R HIT_IN3
HIT_IN4 R210 100R HIT_IN5
HIT_IN6 R212 100R HIT_IN7
HIT_IN8 R213 100R HIT_IN9
HIT_IN10 R214 100R HIT_IN11
HIT_IN12 R216 100R HIT_IN13
HIT_IN14 R217 100R HIT_IN15
HIT_IN16 R215 100R HIT_IN17
HIT_IN18 R218 100R HIT_IN19
HIT_IN20 R220 100R HIT_IN21
HIT_IN22 R221 100R HIT_IN23
HIT_IN24 R222 100R HIT_IN25
HIT_IN26 R223 100R HIT_IN27
HIT_IN28 R224 100R HIT_IN29
HIT_IN30 R225 100R HIT_IN31
HIT_IN32 R226 100R HIT_IN33
HIT_IN34 R227 100R HIT_IN35
HIT_IN36 R228 100R HIT_IN37
HIT_IN38 R229 100R HIT_IN39
HIT_IN40 R230 100R HIT_IN41
HIT_IN42 R231 100R HIT_IN43
HIT_IN44 R232 100R HIT_IN45
HIT_IN46 R233 100R HIT_IN47
HIT_IN48 R234 100R HIT_IN49
HIT_IN50 R236 100R HIT_IN51
HIT_IN52 R235 100R HIT_IN53
HIT_IN54 R237 100R HIT_IN55
HIT_IN56 R238 100R HIT_IN57
HIT_IN58 R239 100R HIT_IN59
HIT_IN60 R240 100R HIT_IN61
HIT_IN[63..0]
HPTDC2.2
TDC3A
INPUTS
HIT_IN0 L1 Hit_0 Hit_16 L7 HIT_IN32
HIT_IN1 L2 Hitb_0 Hitb_16 N8 HIT_IN33
HIT_IN2 K4 Hit_1 Hit_17 P8 HIT_IN34
HIT_IN3 L3 Hitb_1 Hitb_17 R8 HIT_IN35
HIT_IN4 M1 Hit_2 Hit_18 P9 HIT_IN36
HIT_IN5 K5 Hitb_2 Hitb_18 R9 HIT_IN37
HIT_IN6 M2 Hit_3 Hit_19 N9 HIT_IN38
HIT_IN7 L4 Hitb_3 Hitb_19 M9 HIT_IN39
HIT_IN8 N1 Hit_4 Hit_20 L9 HIT_IN40
HIT_IN9 M3 Hitb_4 Hitb_20 R10 HIT_IN41
HIT_IN10 N2 Hit_5 Hit_21 P10 HIT_IN42
HIT_IN11 K6 Hitb_5 Hitb_21 N10 HIT_IN43
HIT_IN12 P1 Hit_6 Hit_22 P12 HIT_IN44
HIT_IN13 N3 Hitb_6 Hitb_22 M11 HIT_IN45
HIT_IN14 P3 Hit_7 Hit_23 R13 HIT_IN46
HIT_IN15 L5 Hitb_7 Hitb_23 N12 HIT_IN47
HIT_IN16 N4 Hit_8 Hit_24 P13 HIT_IN48
HIT_IN17 R3 Hitb_8 Hitb_24 K10 HIT_IN49
HIT_IN18 P4 Hit_9 Hit_25 M12 HIT_IN50
HIT_IN19 K7 Hitb_9 Hitb_25 P15 HIT_IN51
HIT_IN20 M5 Hit_10 Hit_26 N14 HIT_IN52
HIT_IN21 R4 Hitb_10 Hitb_26 L11 HIT_IN53
HIT_IN22 N5 Hit_11 Hit_27 M13 HIT_IN54
HIT_IN23 P5 Hitb_11 Hitb_27 N15 HIT_IN55
HIT_IN24 M6 Hit_12 Hit_28 M14 HIT_IN56
HIT_IN25 N6 Hitb_12 Hitb_28 J10 HIT_IN57
HIT_IN26 P6 Hit_13 Hit_29 L12 HIT_IN58
HIT_IN27 R6 Hitb_13 Hitb_29 M15 HIT_IN59
HIT_IN28 M7 Hit_14 Hit_30 L13 HIT_IN60
HIT_IN29 N7 Hitb_14 Hitb_30 L14 HIT_IN61
HIT_IN30 P7 Hit_15 Hit_31 K11
HIT_IN31 R7 Hitb_15 Hitb_31 L15
R241 100R
+3.3V
C555 100n
C557 100n
C558 100n
C556 100n
C563 100n
C564 1n
C565 1n
HPTDC2.2
TDC3E
A3 VDD_TTL_out1
A8 VDD_TTL_out2
C3 VDD_TTL_out3
C6 VDD_TTL_out4
D2 VDD_TTL_out5
F1 VDD_TTL_out6
H1 VDD_TTL_in
A12 VDD_LVDS_out1
B11 VDD_LVDS_out2
B2 VDD_core1
B9 VDD_core2
B14 VDD_core3
C8 VDD_core4
C9 VDD_core5
E9 VDD_core6
J1 VDD_core7
J2 VDD_core8
J4 VDD_core9
J5 VDD_core10
J11 VDD_core11
J12 VDD_core12
J13 VDD_core13
J15 VDD_core14
L10 VDD_core15
M10 VDD_core16
P2 VDD_core17
P11 VDD_core18
P14 VDD_core19
R12 VDD_core20
NC
Vdd_clock_in E13
Vdd_PLL1 B15
Vdd_PLL2 C13
Vdd_PLL3 C14
Vdd_PLL4 F10
Vdd_DLL1 K1
Vdd_DLL2 K2
Vdd_pre1 F14
Vdd_pre2 J6
Vdd_pre3 K13
Vdd_hit_in1 L8
Vdd_hit_in2 N13
Vdd_hit_in3 R2
Vdd_hit_in4 R5
TDC_POWERUP
R211 10k
TDCLDO3
VIN VOUT
LP3965EMP-2.5
SD SENSE
GND
R219 0R
J36
Jumper2P
L9 BLM18AG601SN1B
C693 10n
C560 1u
C694 10n
C562 1u
L10 BLM18AG601SN1B
C695 10n
C567 1u
C696 10n
C569 1u
+2_5V_LDO
C571 1n
C572 150u
C573 1u
C574 150u
C575 150u
C576 1n
C577 150u
C570 100n
C578 1n
NB7L86MMNG
OR3
START
STARTb
J37
Jumper2P
R242 49.9R
R243 2k
TOKEN_IN
JT429
VTSEL left open
no external termination for HIT_IN62 and HIT_IN63
HIT_IN62
HIT_IN63
HPTDC2.2
TDC3B
Get_data
Data_ready
Token_in
Token_inb
Token_bypass_in
Token_bypass_inb
Token_out
Token_outb
Token_out_TTL
Serial_in
Serial_inb
Serial_bypass_in
Serial_bypass_inb
Serial_out
Serial_outb
Serial_out_TTL
Strobe_out
Strobe_outb
Strobe_out_TTL
Encoded_control
Encoded_controlb
Error
Test
Parallel_Data
TOKEN_BYP_TTL
TOKEN_OUT_TTL
TDC_ERROR
TDC_TEST
R245 330R
R246 330R
DTEST3
SML-311DT
DERROR3
SML-311UT
GET_DATA
DATA_READY
R244 10k
TDC_OUT[31..0]
HPTDC2.2
TDC3C
JTAG
TDI
TMS
TCK
TRST
TDO
Clock
CLK
CLKb
aux_clock
aux_clockb
TDC_CLK
TDC_CLKb
R301 100R
JT420
JT167
HPTDC2.2
TDC3D
Trigger
Triggerb
Reset
Resetb
event_Reset
event_Resetb
bunch_Reset
bunch_Resetb
TRIGGER
TRIGGERb
TDC_RESET
TDC_EV_RESET
TDC_EV_RESETb
TDC_BU_RESET
TDC_BU_RESETb
R302 100R
JT175
R386 100R
R387 100R
HPTDC2.2
TDC3F
GND_1
GND_2
GND_3
GND_4
GND_5
GND_6
GND_7
GND_8
GND_9
GND_10
GND_11
GND_12
GND_13
GND_14
GND_15
GND_16
GND_17
GND_18
GND_19
GND_20
GND_21
GND_22
GND_23
GND_24
GND_25
GND_26
GND_27
GND_28
GND_29
GND_30
GND_31
GND_32
GND_33
GND(therm)_1
GND(therm)_2
GND(therm)_3
GND(therm)_4
GND(therm)_5
GND(therm)_6
GND(therm)_7
GND(therm)_8
GND(therm)_9
GND(therm)_10
GND(therm)_11
GND(therm)_12
GND(therm)_13
C579 10n
C580
C581 10n
C582 100n
C583 10n
C584 100n
C585 10n
C586 100n
C588 10n
C589 100n
C587 10n
C590 100n
C591 10n
C592 100n
C593 10n
C594 100n
C595 10n
C596 100n
C597 10n
C598 100n
C599 10n
C600 100n
C601 10n
C602 100n
100n
Title
TDC
Size A3
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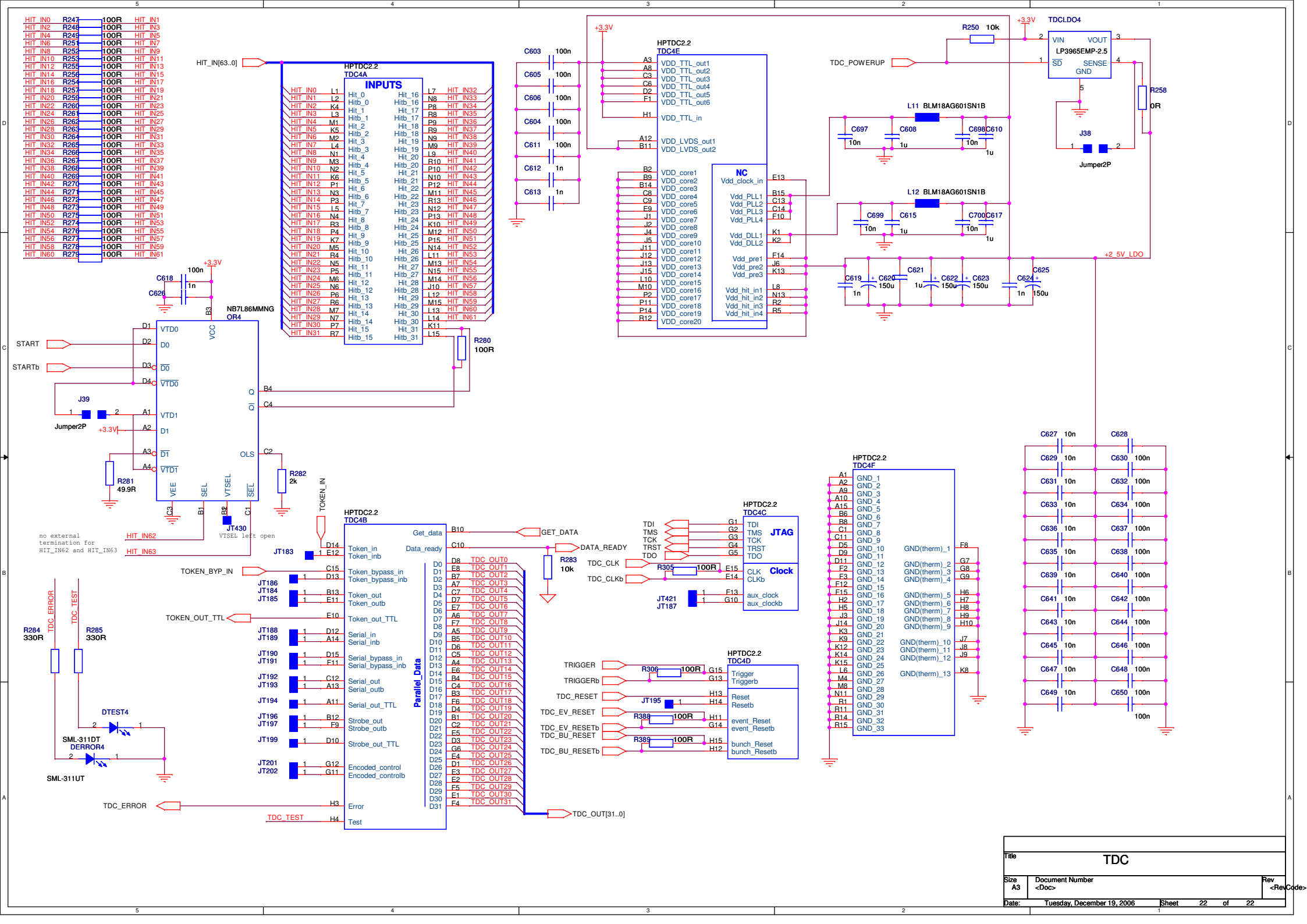
HIT_IN0 R247 100R HIT_IN1
HIT_IN2 R248 100R HIT_IN3
HIT_IN4 R249 100R HIT_IN5
HIT_IN6 R251 100R HIT_IN7
HIT_IN8 R252 100R HIT_IN9
HIT_IN10 R253 100R HIT_IN11
HIT_IN12 R255 100R HIT_IN13
HIT_IN14 R256 100R HIT_IN15
HIT_IN16 R254 100R HIT_IN17
HIT_IN18 R257 100R HIT_IN19
HIT_IN20 R259 100R HIT_IN21
HIT_IN22 R260 100R HIT_IN23
HIT_IN24 R261 100R HIT_IN25
HIT_IN26 R262 100R HIT_IN27
HIT_IN28 R263 100R HIT_IN29
HIT_IN30 R264 100R HIT_IN31
HIT_IN32 R265 100R HIT_IN33
HIT_IN34 R266 100R HIT_IN35
HIT_IN36 R267 100R HIT_IN37
HIT_IN38 R268 100R HIT_IN39
HIT_IN40 R269 100R HIT_IN41
HIT_IN42 R270 100R HIT_IN43
HIT_IN44 R271 100R HIT_IN45
HIT_IN46 R272 100R HIT_IN47
HIT_IN48 R273 100R HIT_IN49
HIT_IN50 R275 100R HIT_IN51
HIT_IN52 R274 100R HIT_IN53
HIT_IN54 R276 100R HIT_IN55
HIT_IN56 R277 100R HIT_IN57
HIT_IN58 R278 100R HIT_IN59
HIT_IN60 R279 100R HIT_IN61
HIT_IN[63..0]
HPTDC2.2
TDC4A
INPUTS
Hit_0 Hit_16 Hitb_0 Hitb_16 Hit_1 Hit_17 Hitb_1 Hitb_17 Hit_2 Hit_18 Hitb_2 Hitb_18 Hit_3 Hit_19 Hitb_3 Hitb_19 Hit_4 Hit_20 Hitb_4 Hitb_20 Hit_5 Hit_21 Hitb_5 Hitb_21 Hit_6 Hit_22 Hitb_6 Hitb_22 Hit_7 Hit_23 Hitb_7 Hitb_23 Hit_8 Hit_24 Hitb_8 Hitb_24 Hit_9 Hit_25 Hitb_9 Hitb_25 Hit_10 Hit_26 Hitb_10 Hitb_26 Hit_11 Hit_27 Hitb_11 Hitb_27 Hit_12 Hit_28 Hitb_12 Hitb_28 Hit_13 Hit_29 Hitb_13 Hitb_29 Hit_14 Hit_30 Hitb_14 Hitb_30 Hit_15 Hit_31 Hitb_15 Hitb_31
C603 100n
C605 100n
C606 100n
C604 100n
C611 100n
C612 1n
C613 1n
+3.3V
HPTDC2.2
TDC4E
VDD_TTL_out1 VDD_TTL_out2 VDD_TTL_out3 VDD_TTL_out4 VDD_TTL_out5 VDD_TTL_out6
VDD_TTL_in
VDD_LVDS_out1 VDD_LVDS_out2
VDD_core1 VDD_core2 VDD_core3 VDD_core4 VDD_core5 VDD_core6 VDD_core7 VDD_core8 VDD_core9 VDD_core10 VDD_core11 VDD_core12 VDD_core13 VDD_core14 VDD_core15 VDD_core16 VDD_core17 VDD_core18 VDD_core19 VDD_core20
NC
Vdd_clock_in
Vdd_PLL1 Vdd_PLL2 Vdd_PLL3 Vdd_PLL4
Vdd_DLL1 Vdd_DLL2
Vdd_pre1 Vdd_pre2 Vdd_pre3
Vdd_hit_in1 Vdd_hit_in2 Vdd_hit_in3 Vdd_hit_in4
TDC_POWERUP
R250 10k
TDCLDO4
VIN VOUT
LP3965EMP-2.5
SD SENSE
GND
R258 0R
J38
Jumper2P
L11 BLM18AG601SN1B
C697 10n
C608 1u
C698 10n
C610 1u
L12 BLM18AG601SN1B
C699 10n
C615 1u
C700 10n
C617 1u
+2_5V_LDO
C619 1n
C620 150u
C621 1u
C622 150u
C623 150u
C624 1n
C625 150u
C618 100n
C626 1n
+3.3V
NB7L86MMNG
OR4
VTD0 D0 VTD0 VTD1 D1 D1 VTD1
VCC VEE SEL VTSEL SEL
Q QI OLS
START
STARTb
J39
Jumper2P
R280 100R
R281 49.9R
R282 2k
JT430
VTSEL left open
no external termination for HIT_IN62 and HIT_IN63
HIT_IN62
HIT_IN63
TOKEN_IN
HPTDC2.2
TDC4B
Get_data Data_ready
Token_in Token_inb Token_bypass_in Token_bypass_inb Token_out Token_outb Token_out_TTL Serial_in Serial_inb Serial_bypass_in Serial_bypass_inb Serial_out Serial_outb Serial_out_TTL Strobe_out Strobe_outb Strobe_out_TTL Encoded_control Encoded_controlb Error Test
Parallel_Data
TDC_OUT0 TDC_OUT1 TDC_OUT2 TDC_OUT3 TDC_OUT4 TDC_OUT5 TDC_OUT6 TDC_OUT7 TDC_OUT8 TDC_OUT9 TDC_OUT10 TDC_OUT11 TDC_OUT12 TDC_OUT13 TDC_OUT14 TDC_OUT15 TDC_OUT16 TDC_OUT17 TDC_OUT18 TDC_OUT19 TDC_OUT20 TDC_OUT21 TDC_OUT22 TDC_OUT23 TDC_OUT24 TDC_OUT25 TDC_OUT26 TDC_OUT27 TDC_OUT28 TDC_OUT29 TDC_OUT30 TDC_OUT31
TDC_OUT[31..0]
GET_DATA
DATA_READY
R283 10k
JT183
JT186 JT184 JT185
JT188 JT189
JT190 JT191
JT192 JT193
JT194
JT196 JT197
JT199
JT201 JT202
TOKEN_BYP_IN
TOKEN_OUT_TTL
TDC_ERROR
TDC_TEST
R284 330R
R285 330R
DTEST4
SML-311DT
DERROR4
SML-311UT
HPTDC2.2
TDC4C
JTAG
TDI TMS TCK TRST TDO
Clock
CLK CLKb aux_clock aux_clockb
TDC_CLK
TDC_CLKb
R305 100R
JT421 JT187
HPTDC2.2
TDC4D
Trigger Triggerb Reset Resetb event_Reset event_Resetb bunch_Reset bunch_Resetb
TRIGGER
TRIGGERb
TDC_RESET
TDC_EV_RESET
TDC_EV_RESETb
TDC_BU_RESET
TDC_BU_RESETb
R306 100R
JT195
R388 100R
R389 100R
HPTDC2.2
TDC4F
GND_1 GND_2 GND_3 GND_4 GND_5 GND_6 GND_7 GND_8 GND_9 GND_10 GND_11 GND_12 GND_13 GND_14 GND_15 GND_16 GND_17 GND_18 GND_19 GND_20 GND_21 GND_22 GND_23 GND_24 GND_25 GND_26 GND_27 GND_28 GND_29 GND_30 GND_31 GND_32 GND_33
GND(therm)_1 GND(therm)_2 GND(therm)_3 GND(therm)_4 GND(therm)_5 GND(therm)_6 GND(therm)_7 GND(therm)_8 GND(therm)_9 GND(therm)_10 GND(therm)_11 GND(therm)_12 GND(therm)_13
C627 10n
C628
C629 10n
C630 100n
C631 10n
C632 100n
C633 10n
C634 100n
C636 10n
C637 100n
C635 10n
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TDC
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