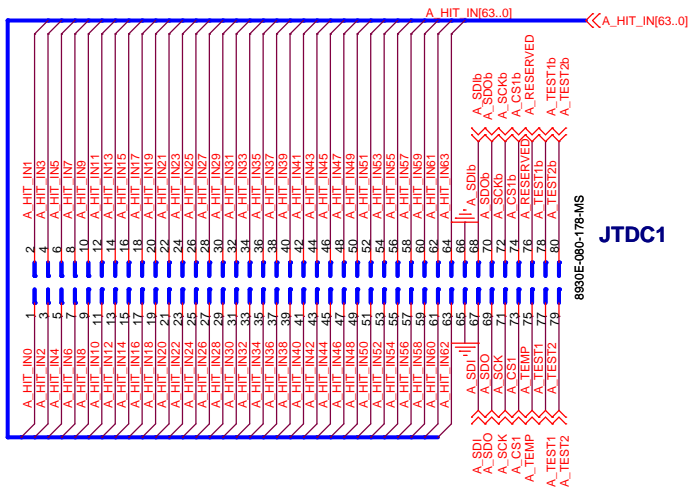
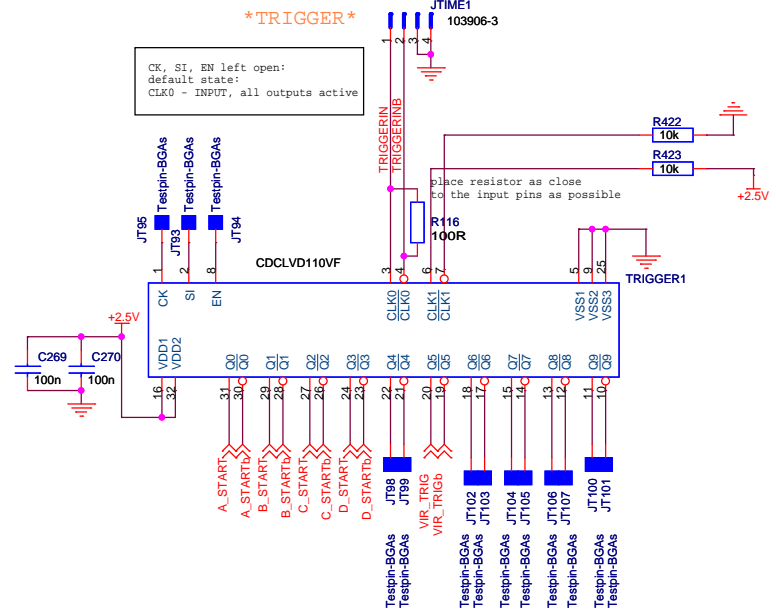


TDC A

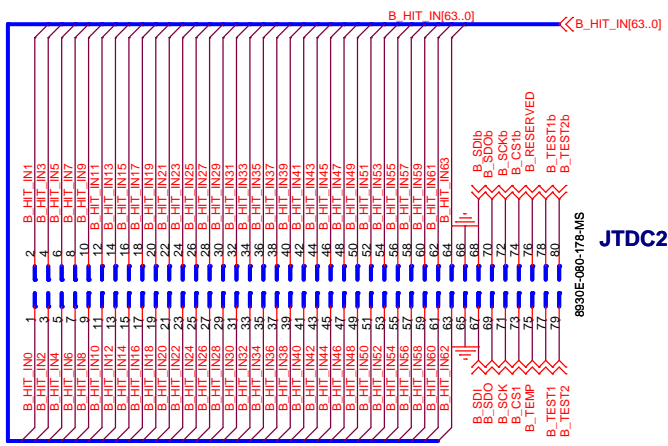


JTDC1



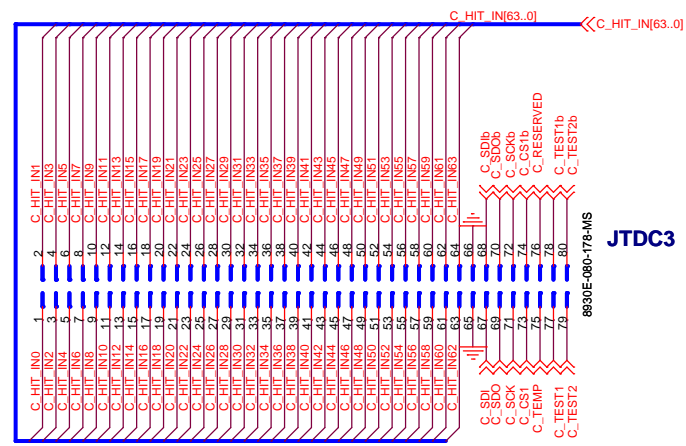
Peter, please make each next START diff. lines 0.5cm longer then the former ones. e.g. if A\_START and A\_STARTb have 35 mm then B\_START and B\_STARTb should have 40mm

TDC B



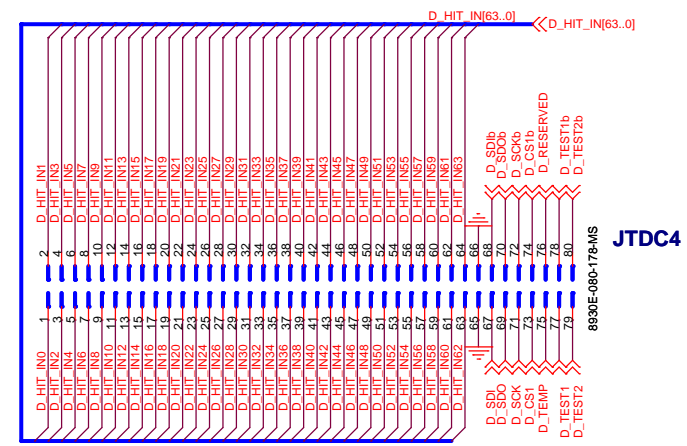
JTDC2

TDC C

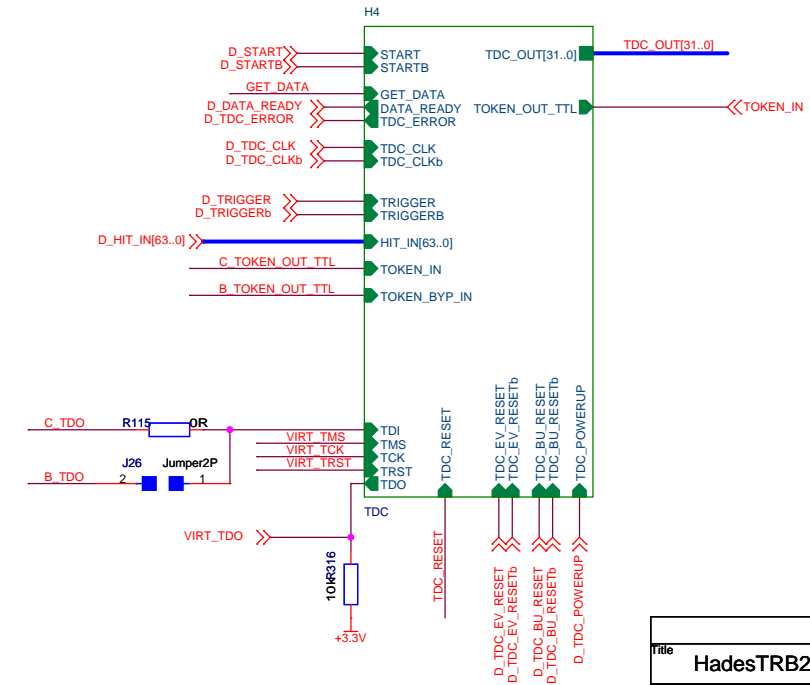
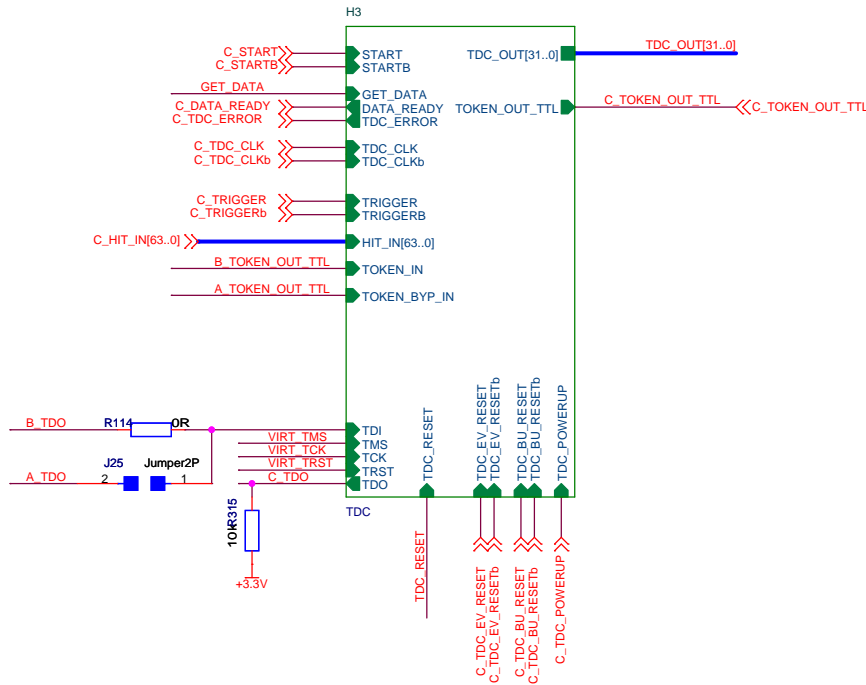
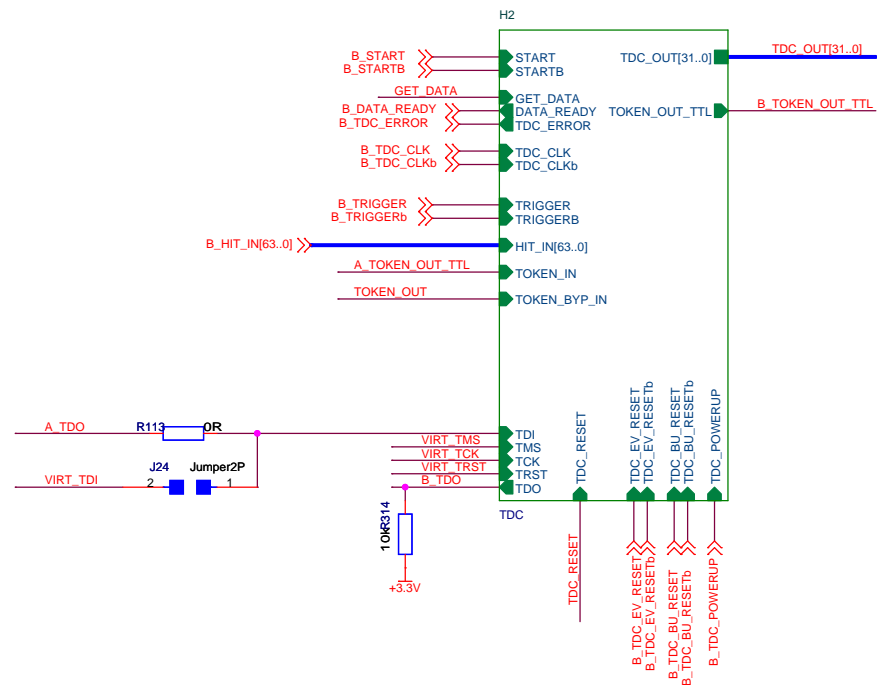
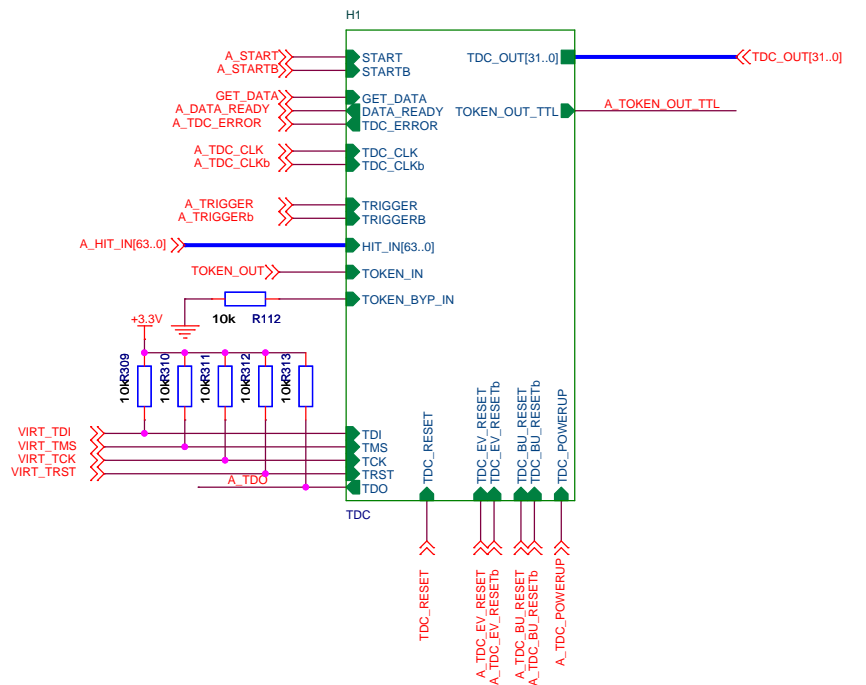


JTDC3

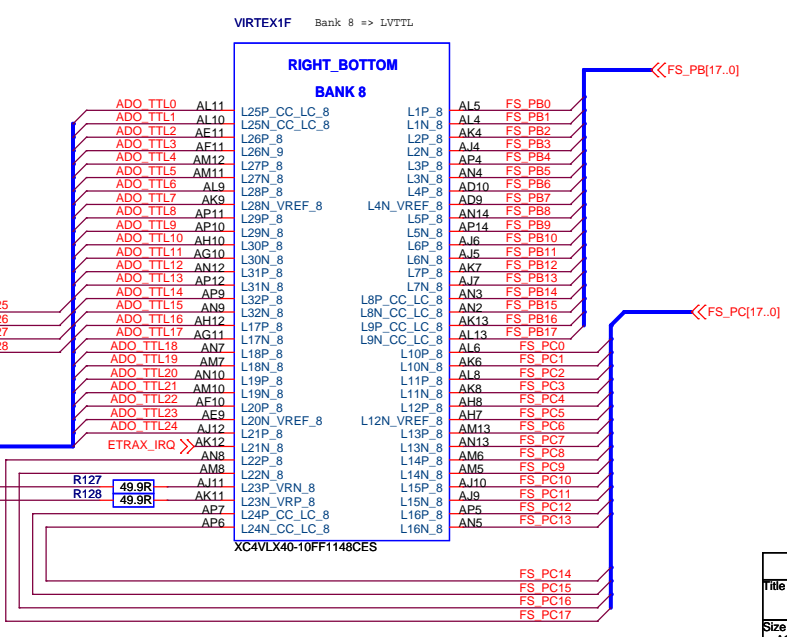
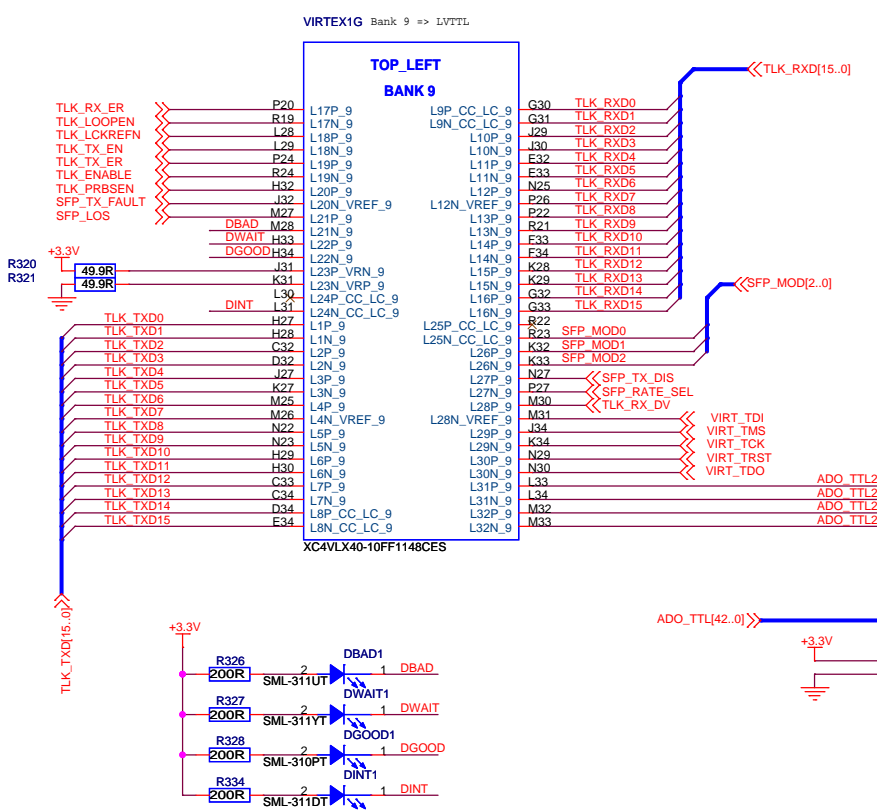
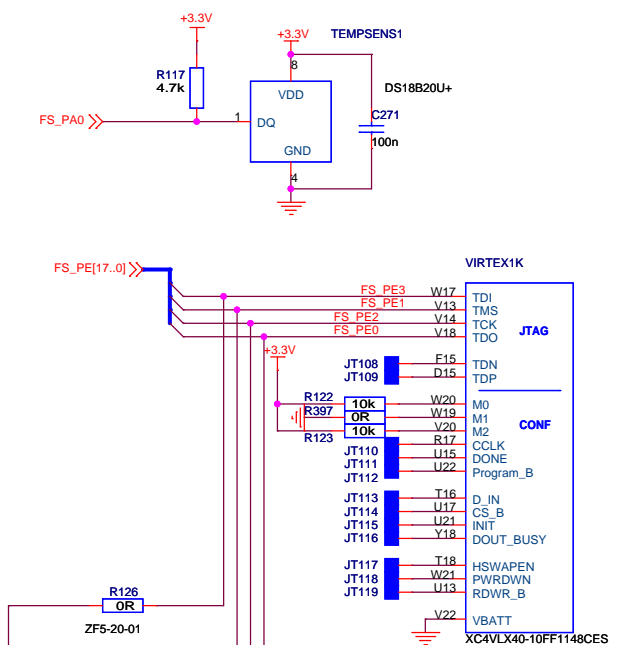
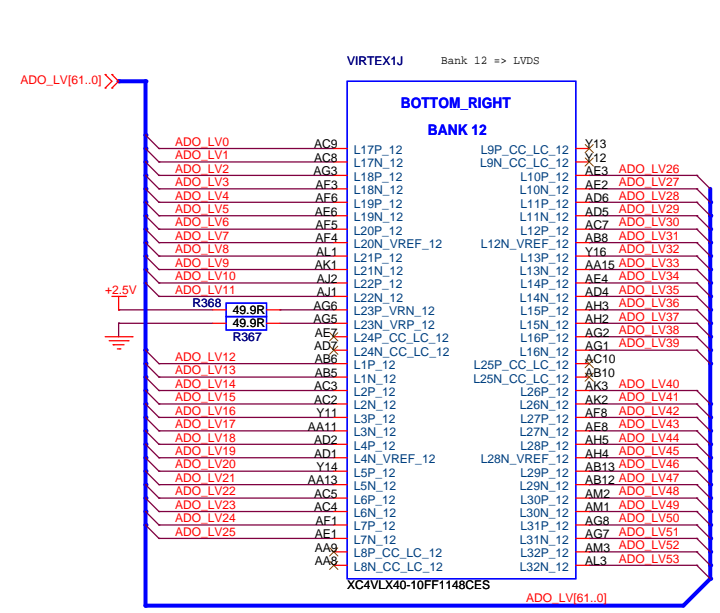
TDC D



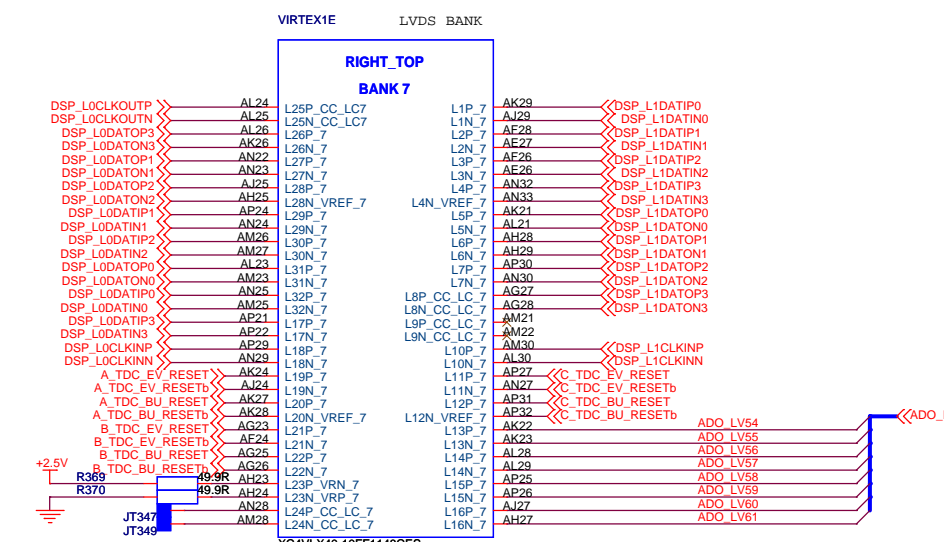
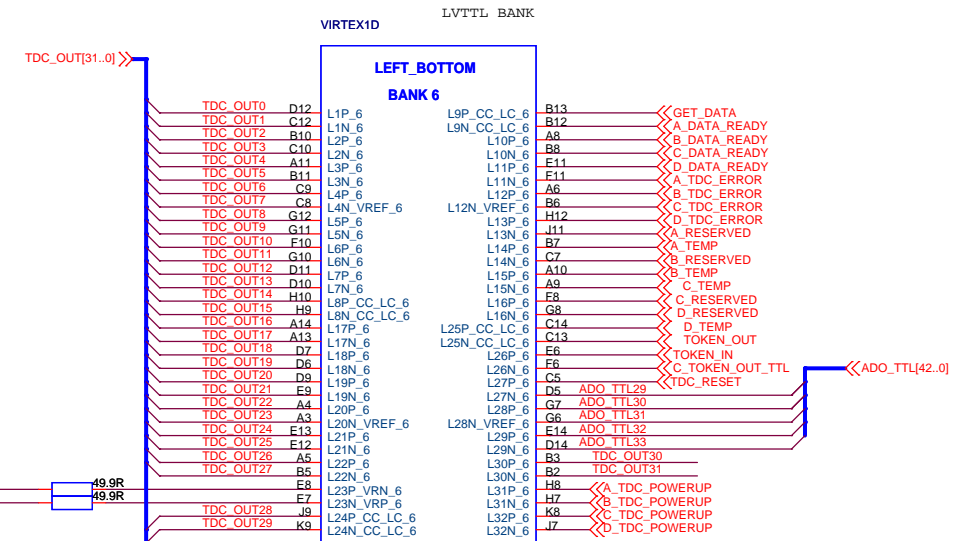
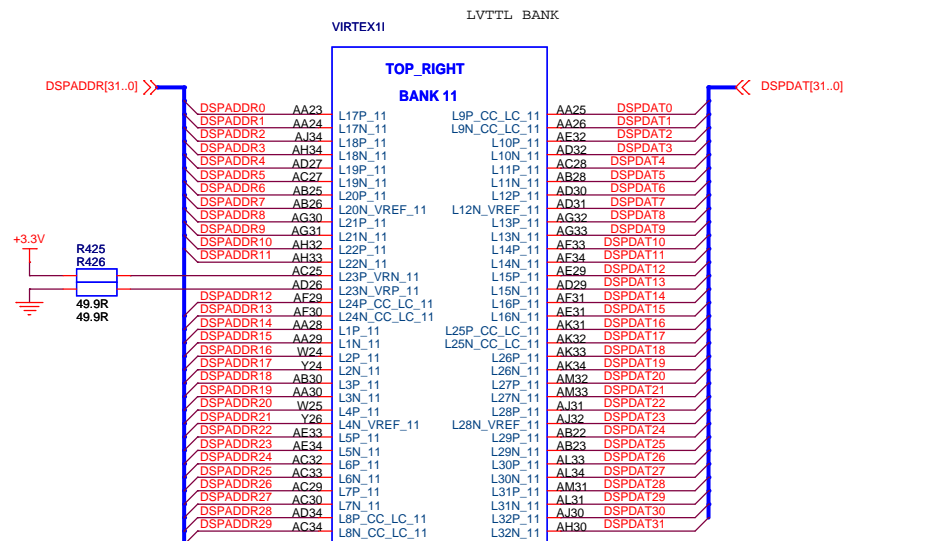
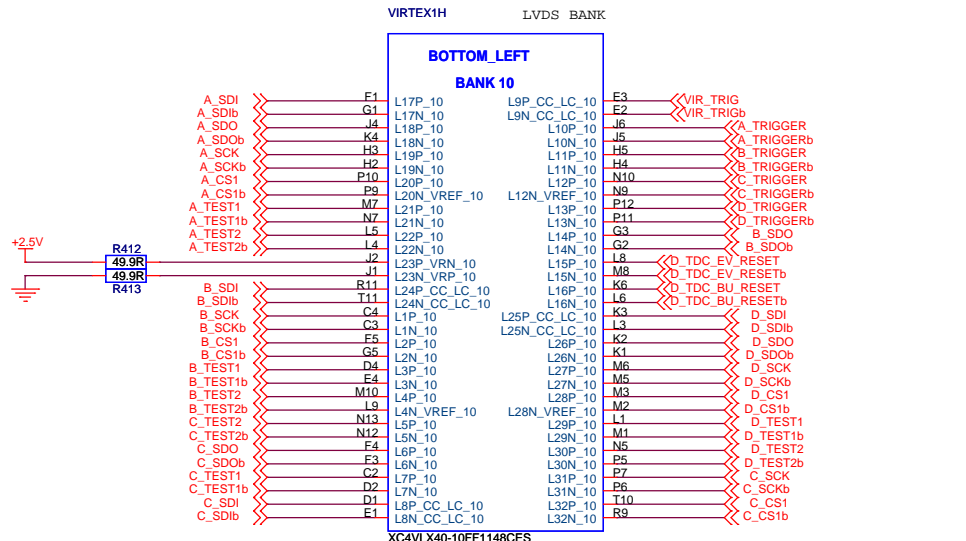
JTDC4

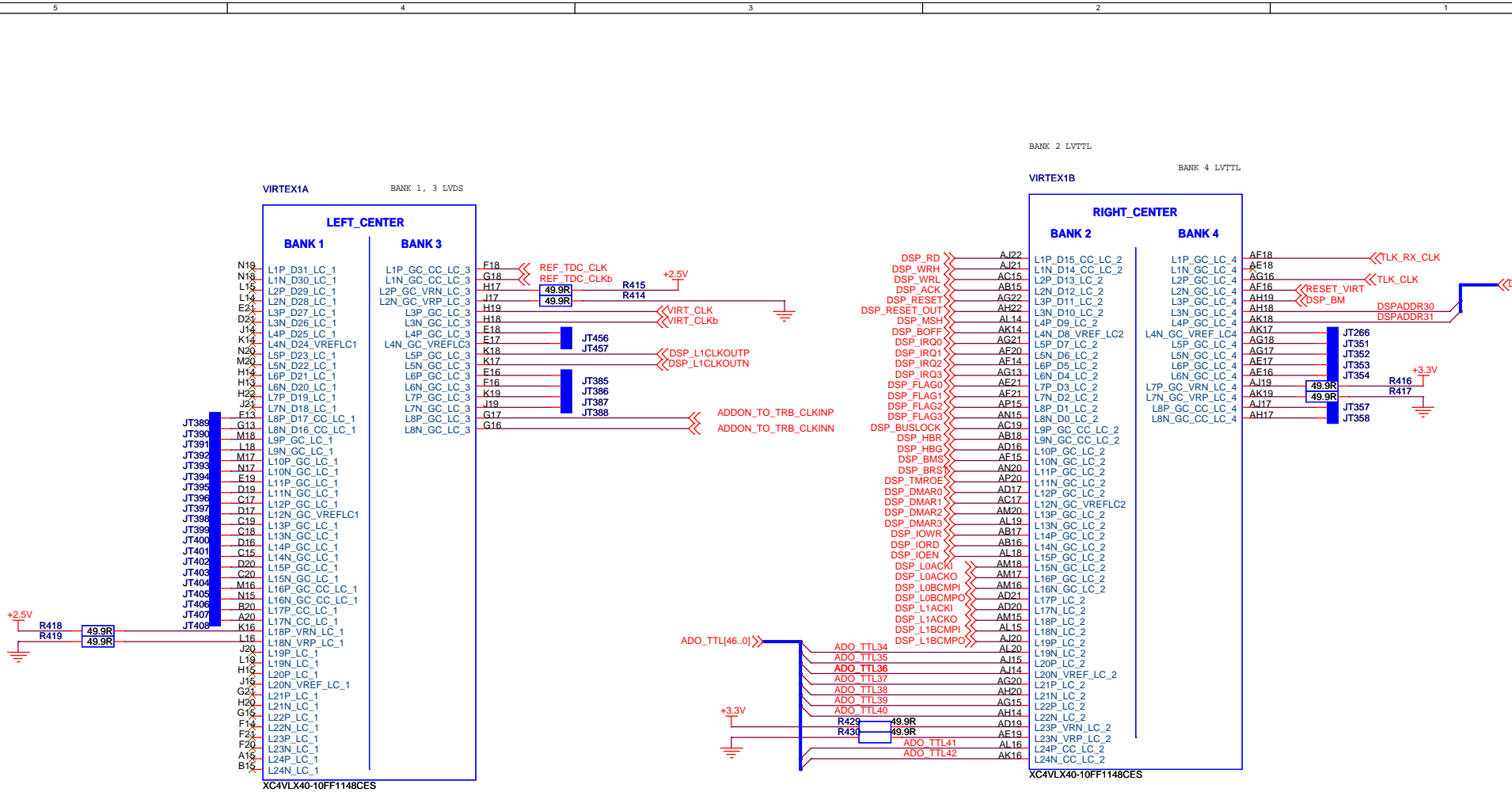


Title		
HadesTRB2 - TIME		
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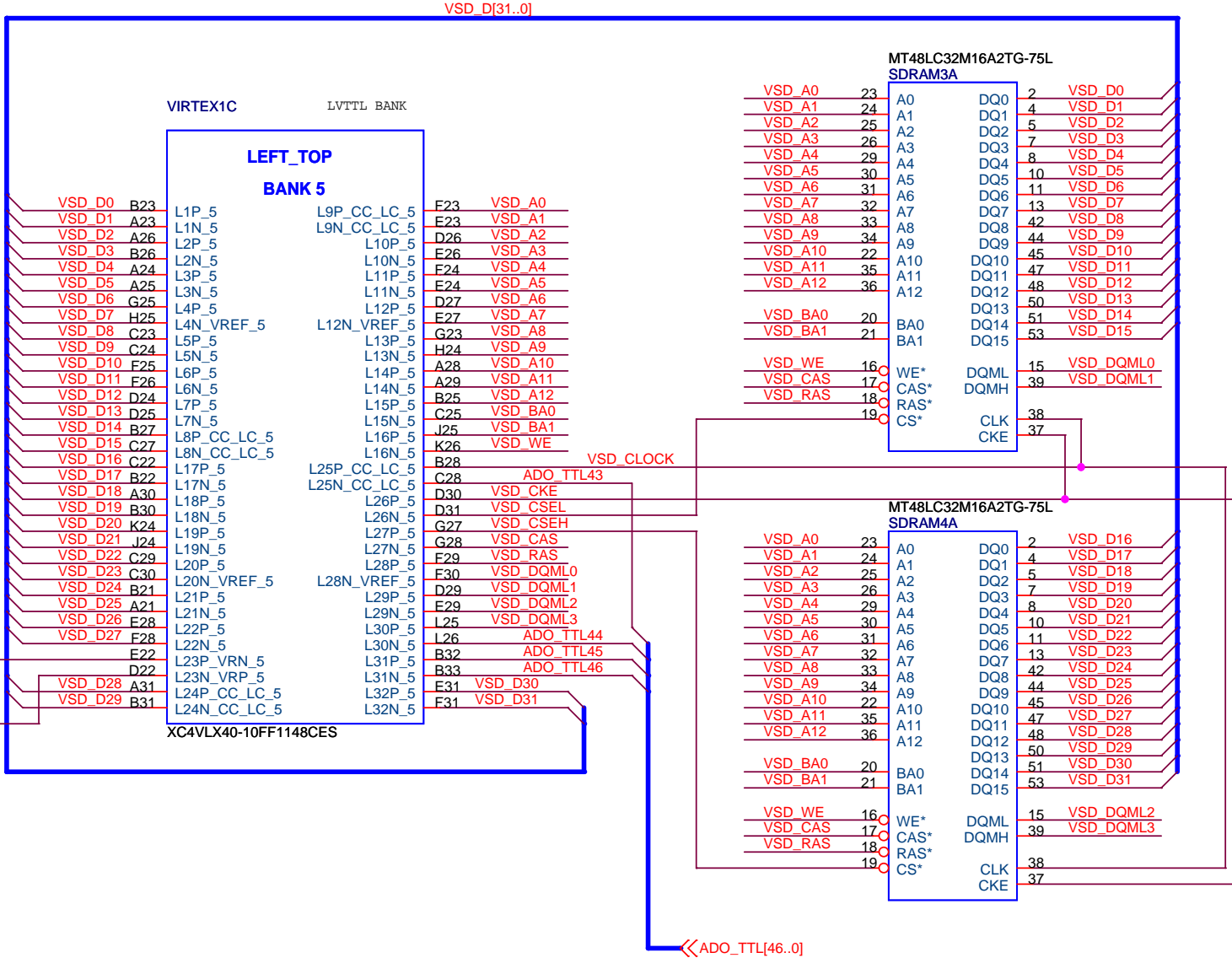
Title		
HadesTRB2 - VIRTEX A		
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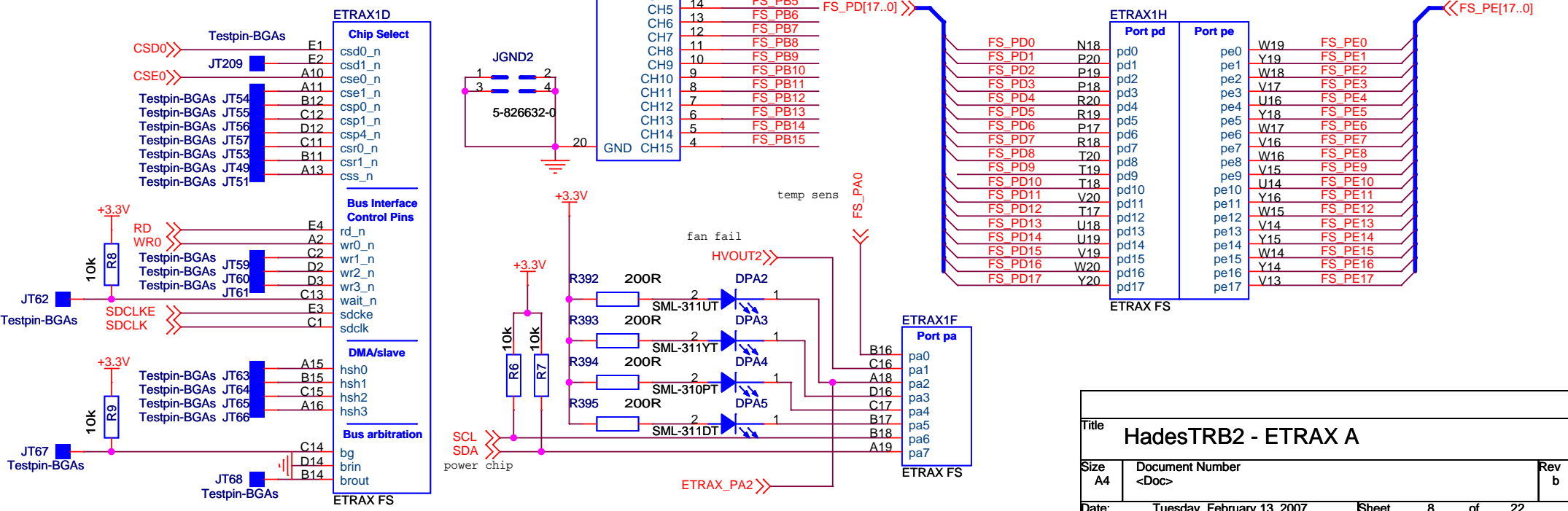
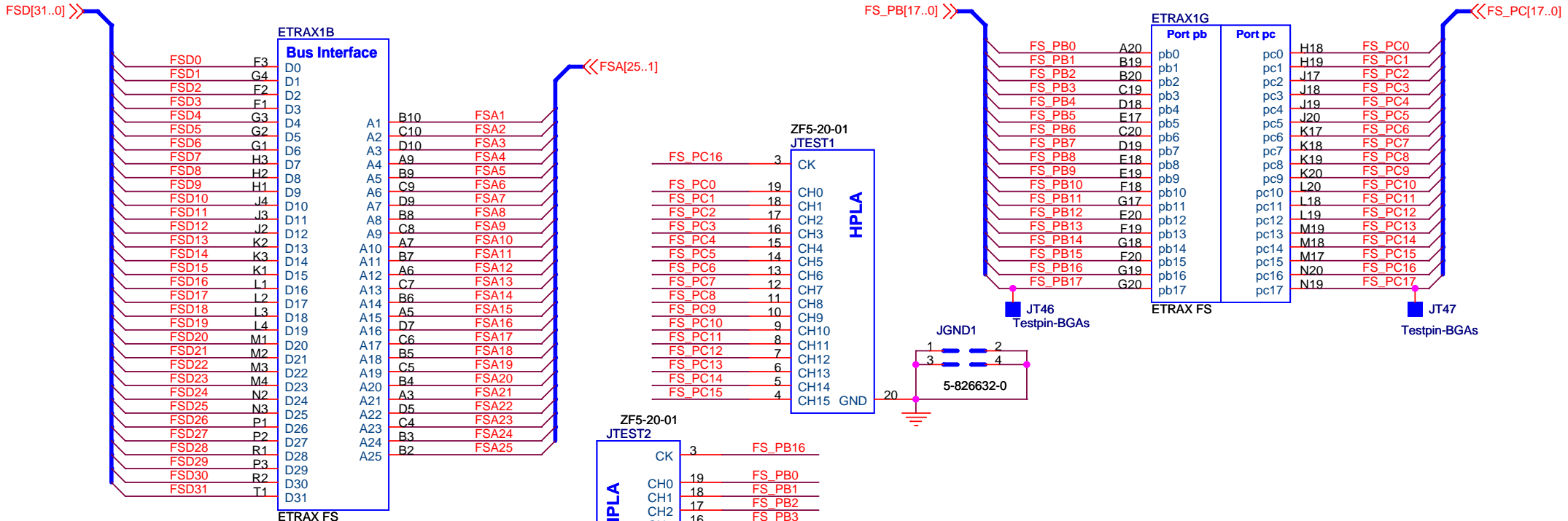
DSP control - banks 2, 7, 11

Title		
HadesTRB2 - VIRTEX C		
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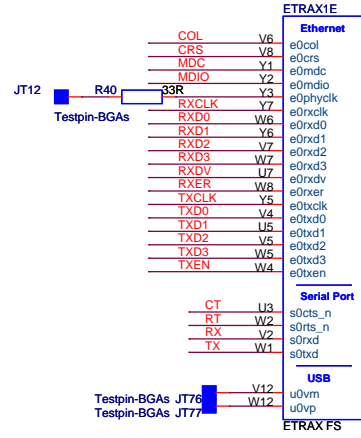
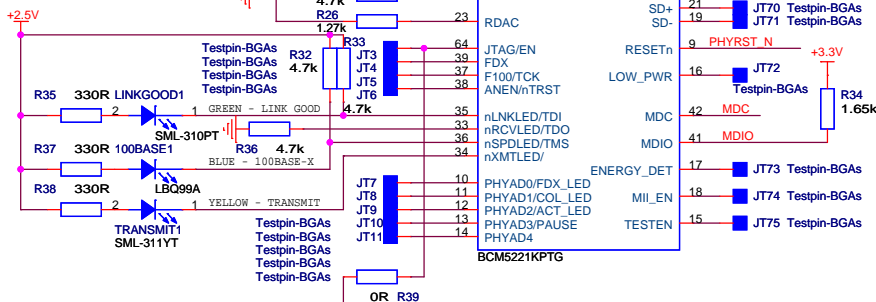
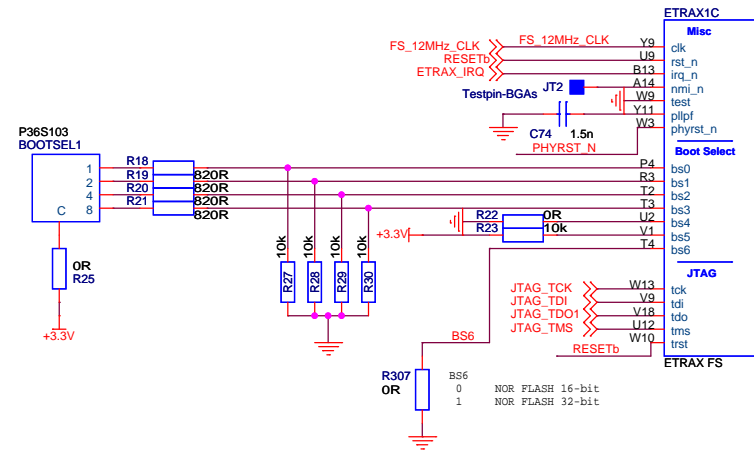
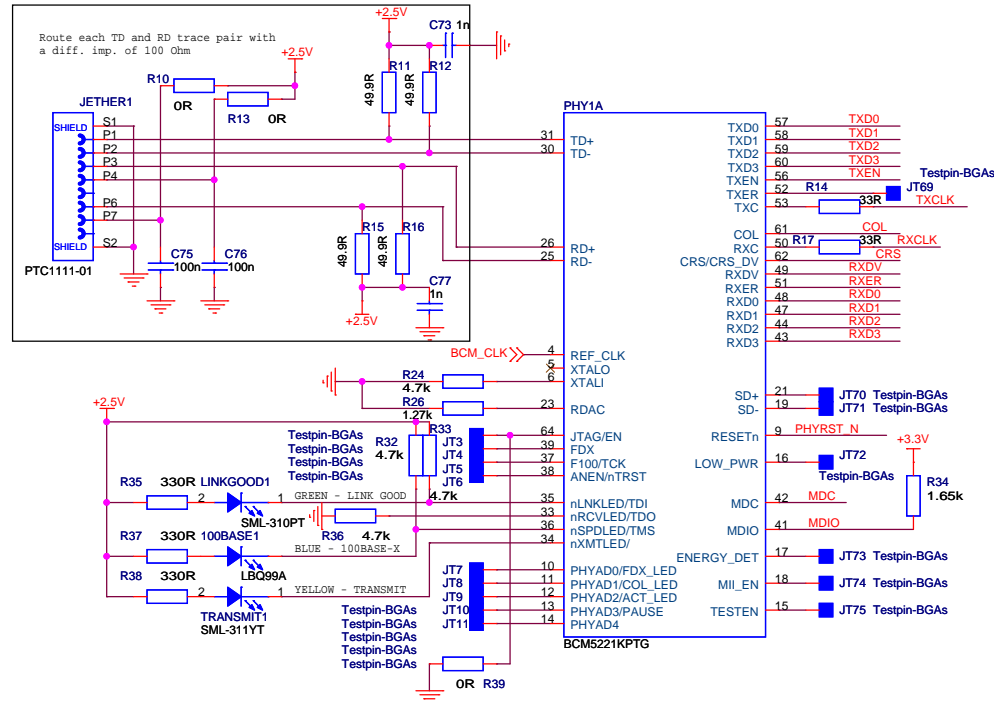


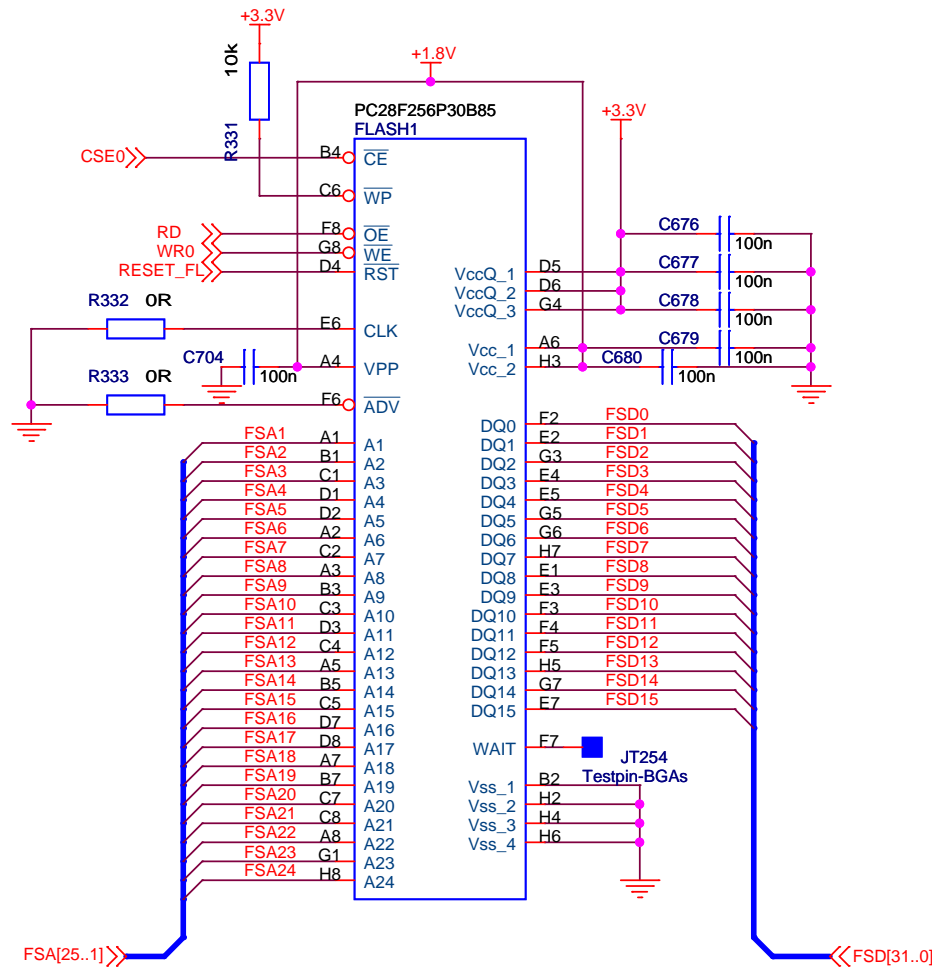
Title		
HadesTRB2 - ETRAX A		
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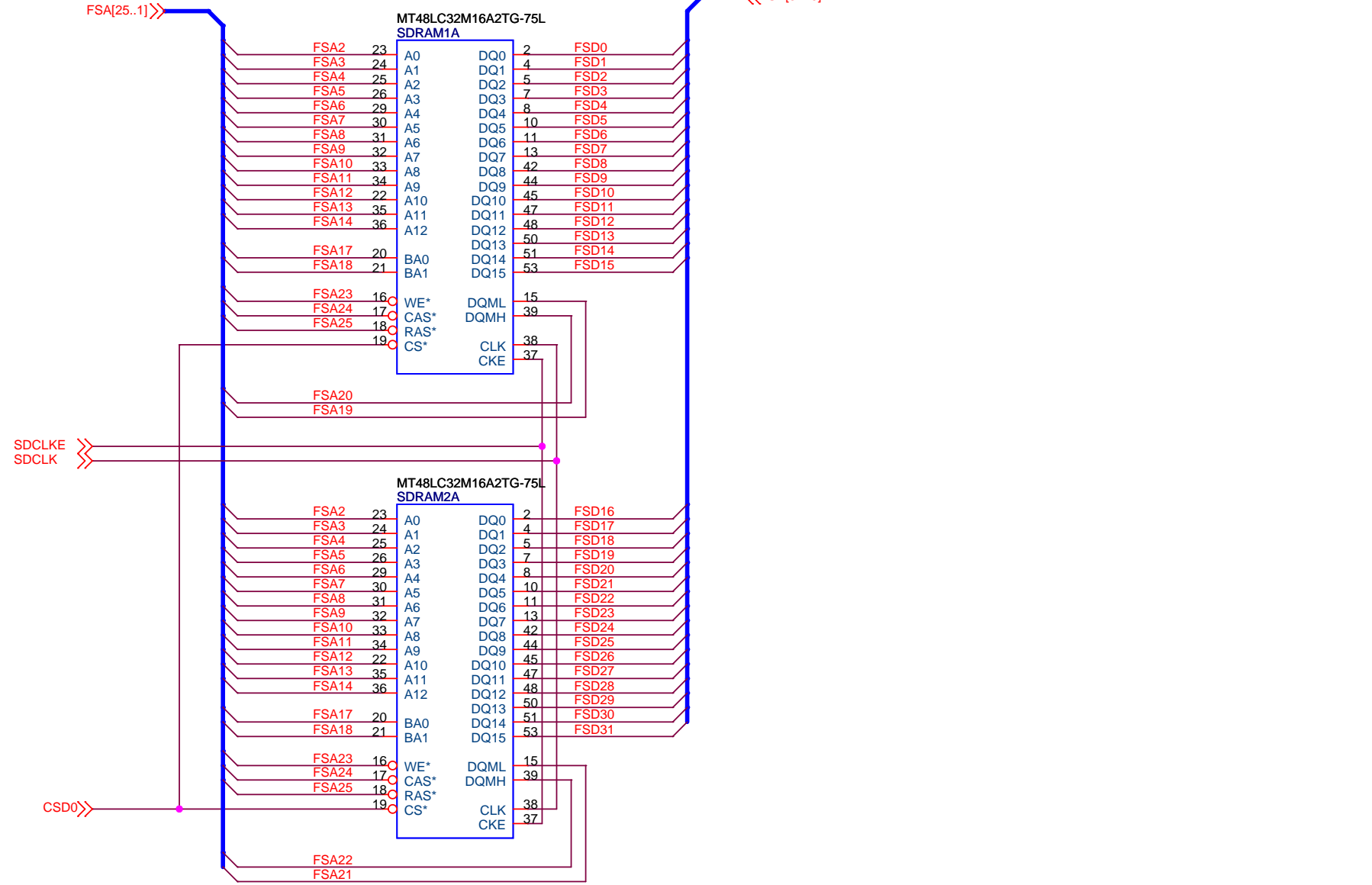
Place the termination network and RJ45 connector close to the BCM5221

BS3	BS2	BS1	BS0	
-	0	0	0	NOR Flash
-	0	0	1	Network RX only
-	0	1	0	Network RX/TX
-	0	1	1	NAND Flash
-	1	0	0	Serial
-	1	0	1	Master boot
-	1	1	0	Slave boot
-	1	1	1	No boot
0	-	-	-	Ethernet Half-Duplex
1	-	-	-	Ethernet Full-Duplex



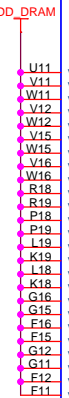
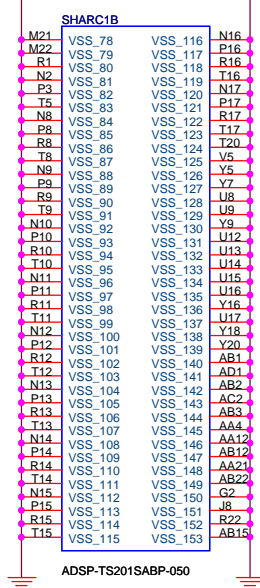
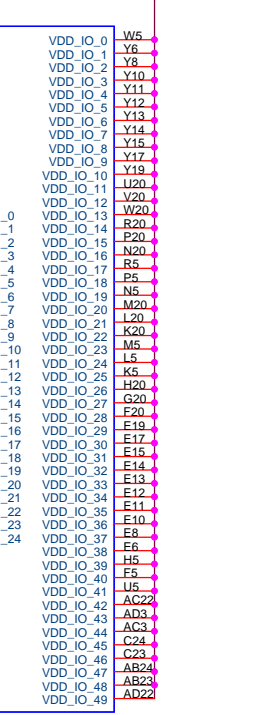
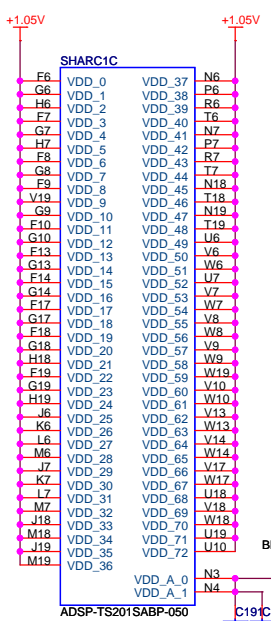
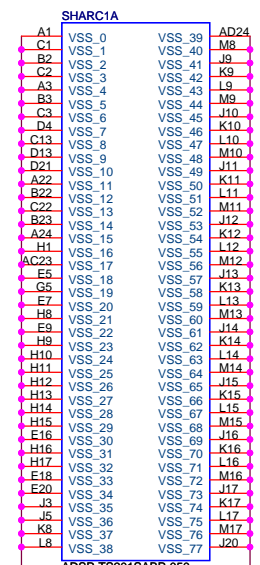


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HadesTRB2 - FLASH MEMORY		
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Title		
HadesTRB2 - ETRAX SDRAM		
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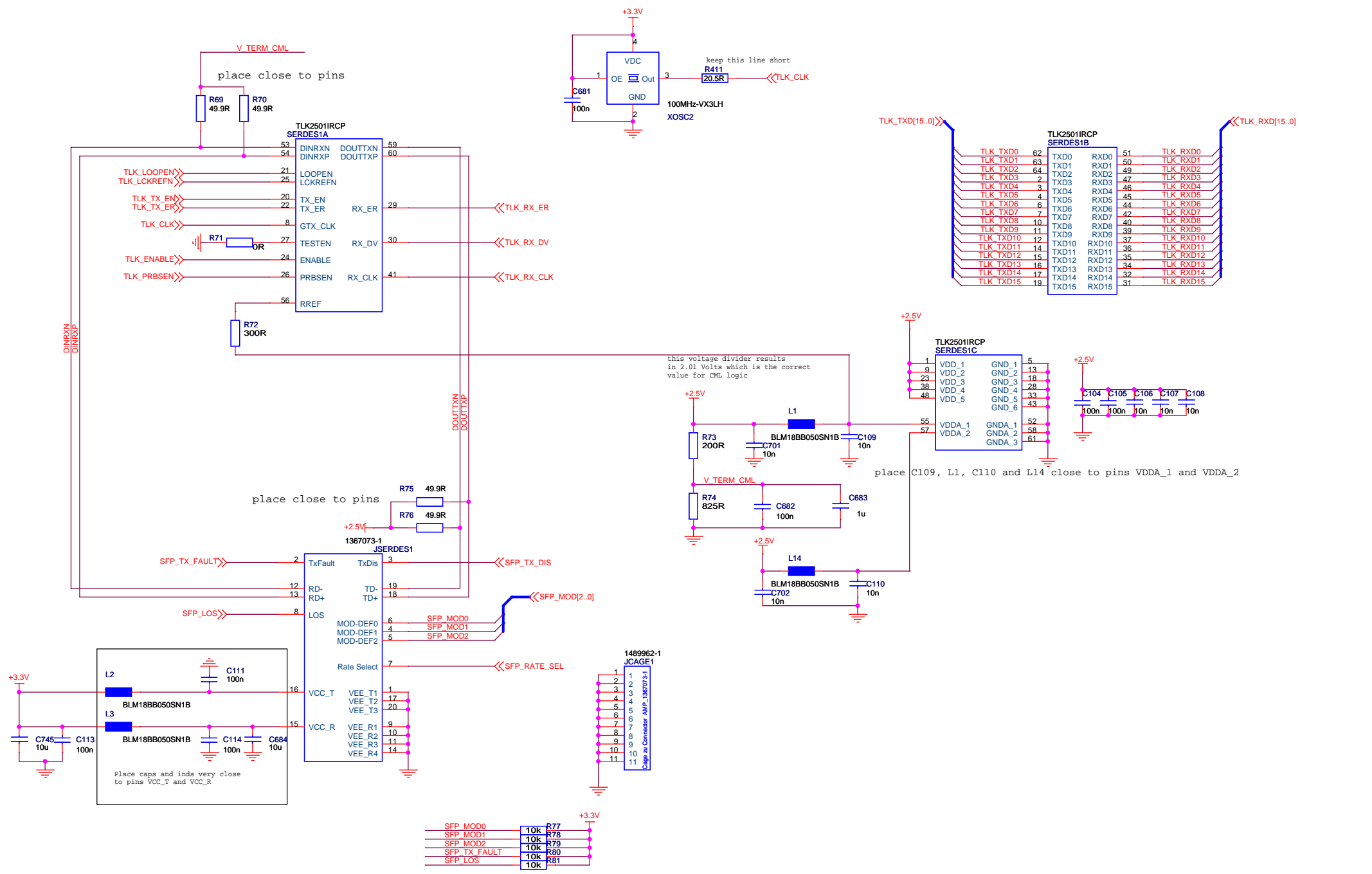


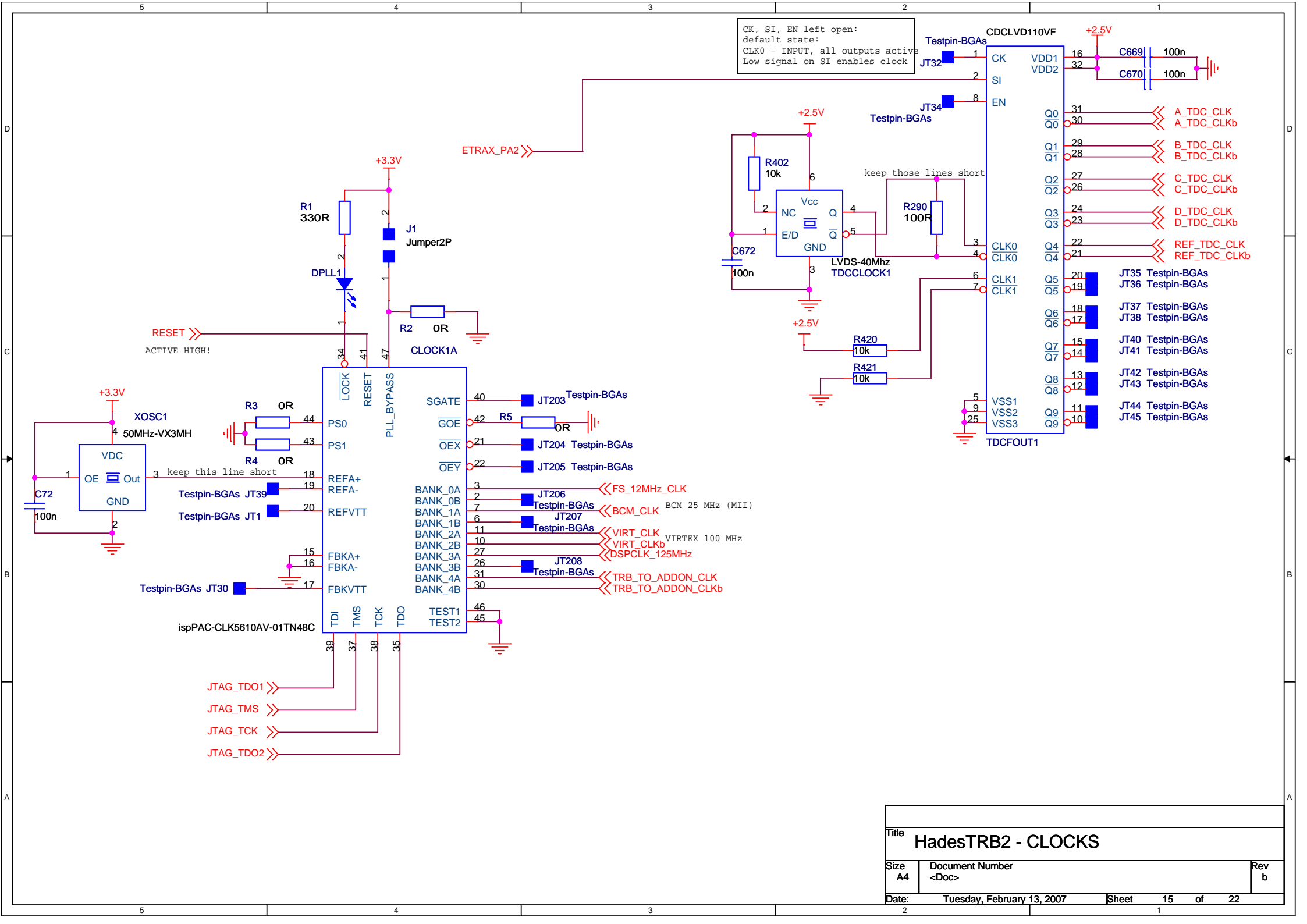


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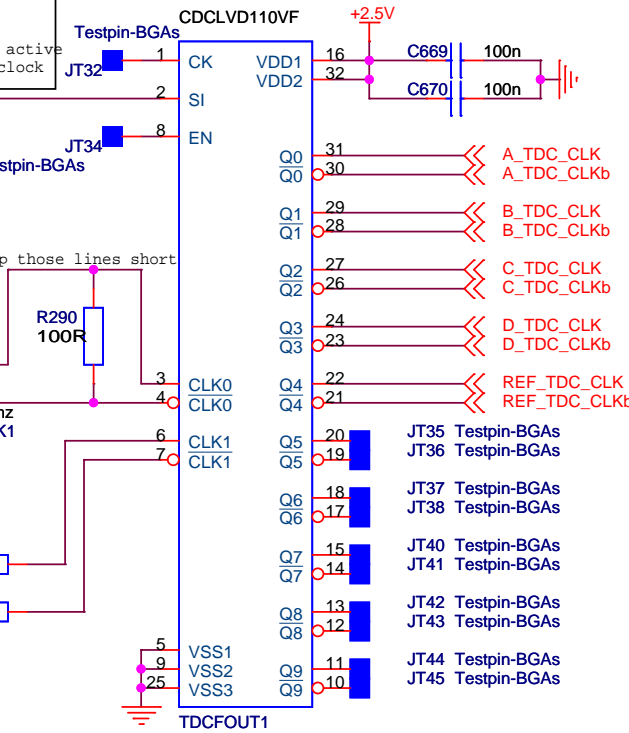


Title		
HadesTRB2 - SHARC SUPPLY		
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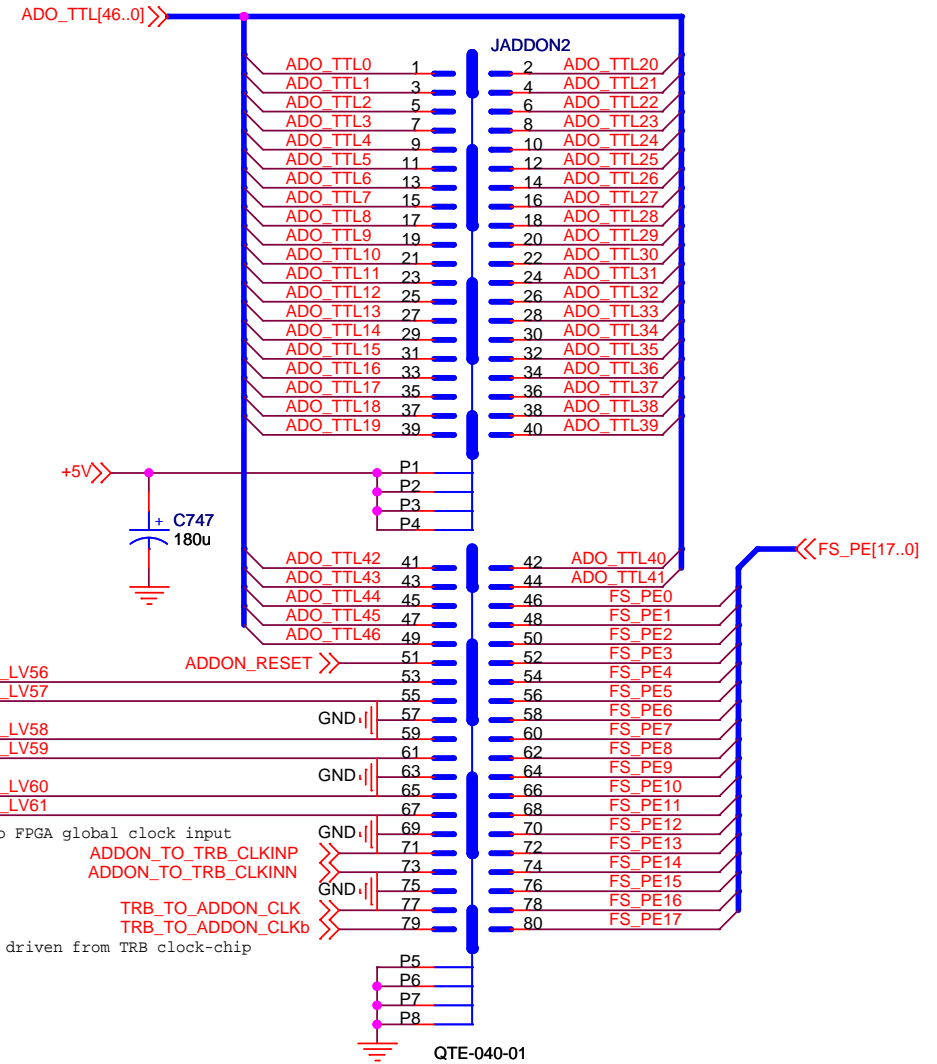
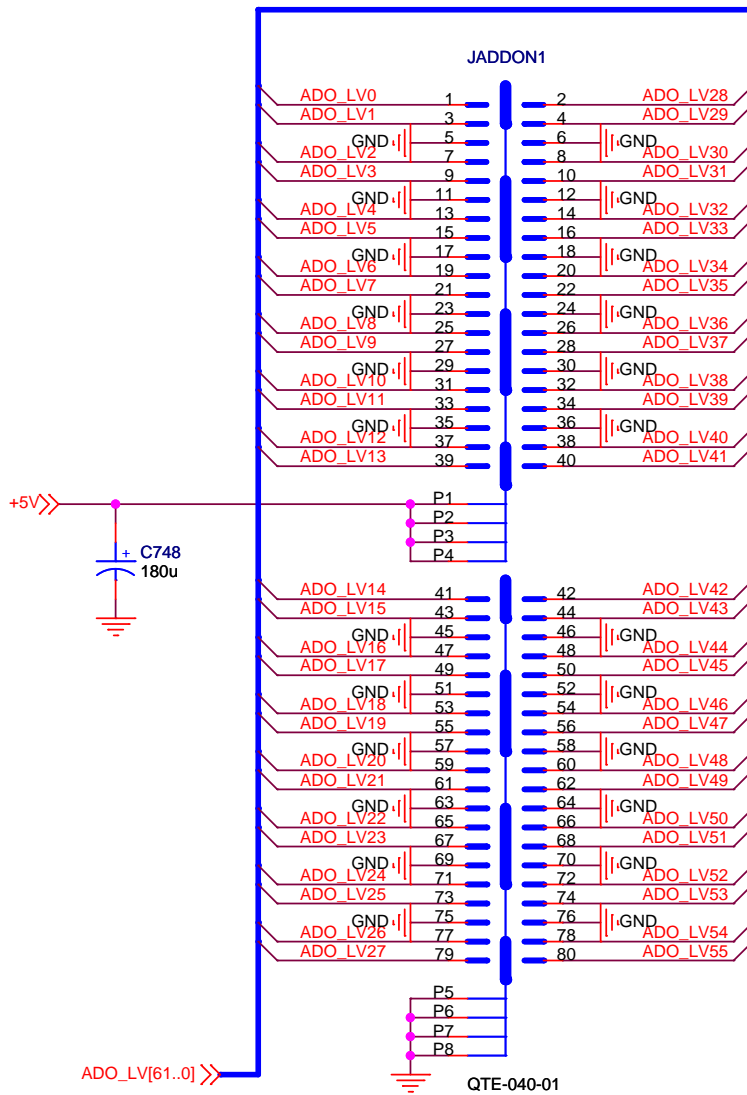
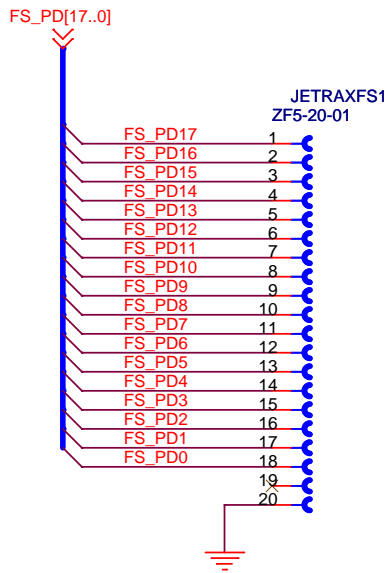


CK, SI, EN left open:  
 default state:  
 CLK0 - INPUT, all outputs active  
 Low signal on SI enables clock

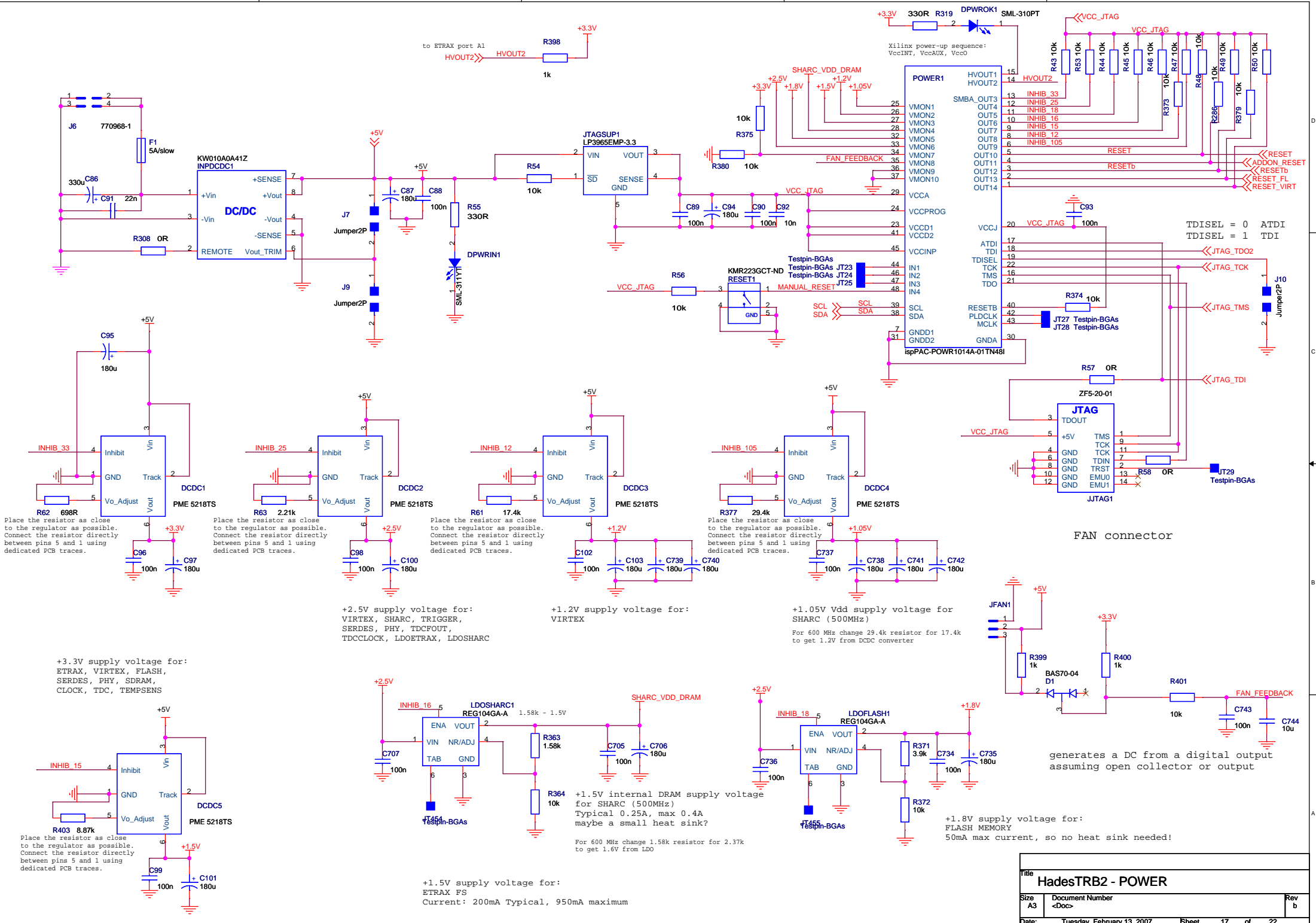


Title		
HadesTRB2 - CLOCKS		
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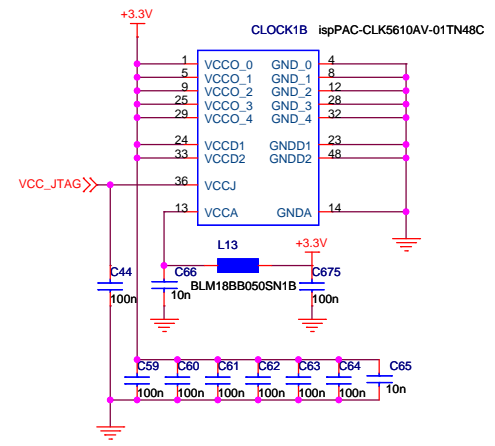
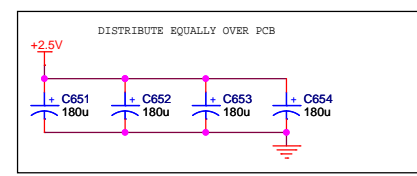
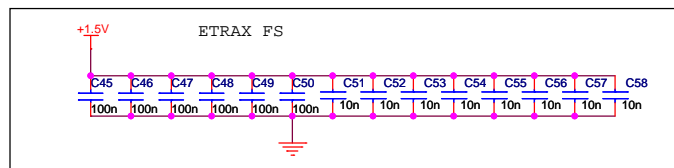
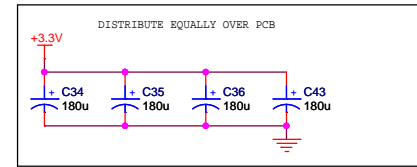
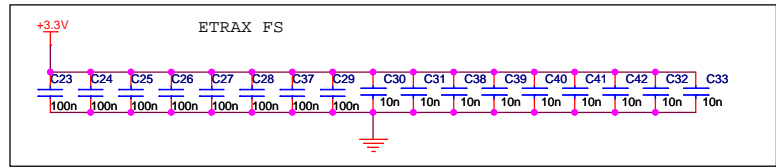
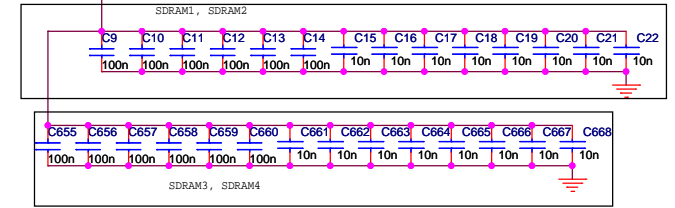
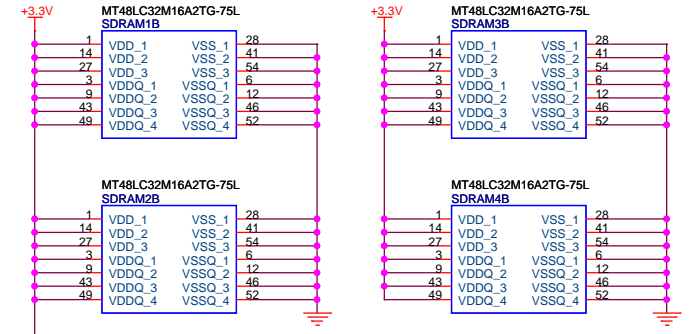
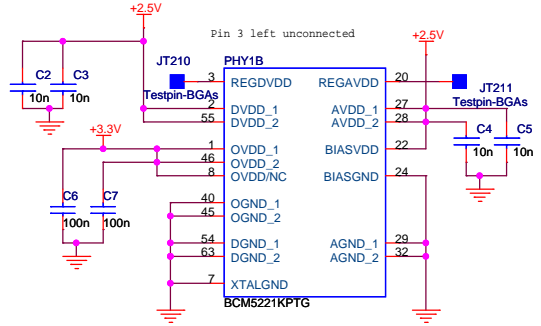
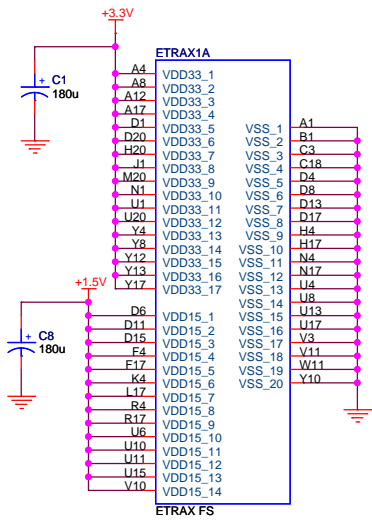


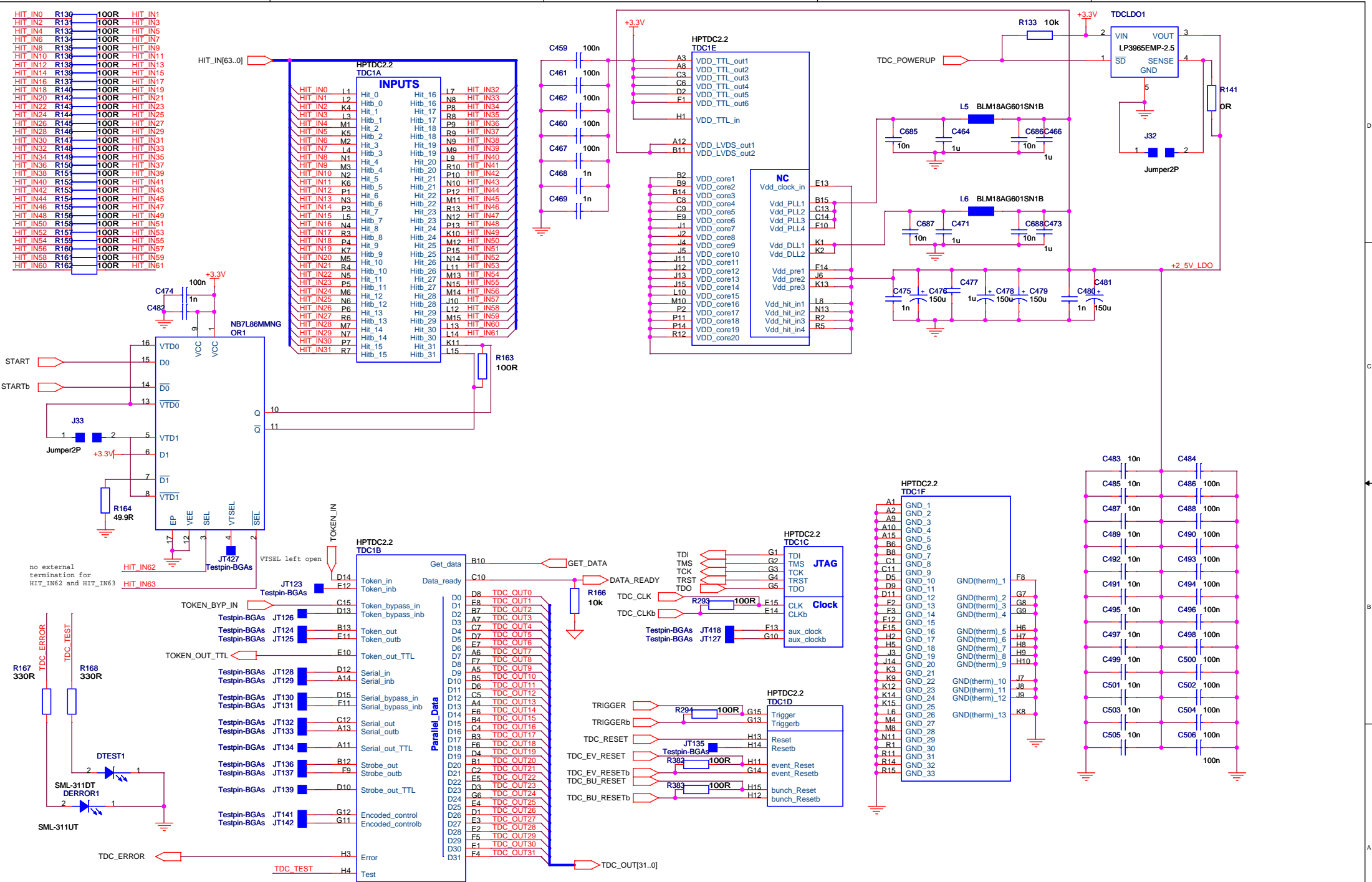


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HadesTRB2 - CONNECTORS		
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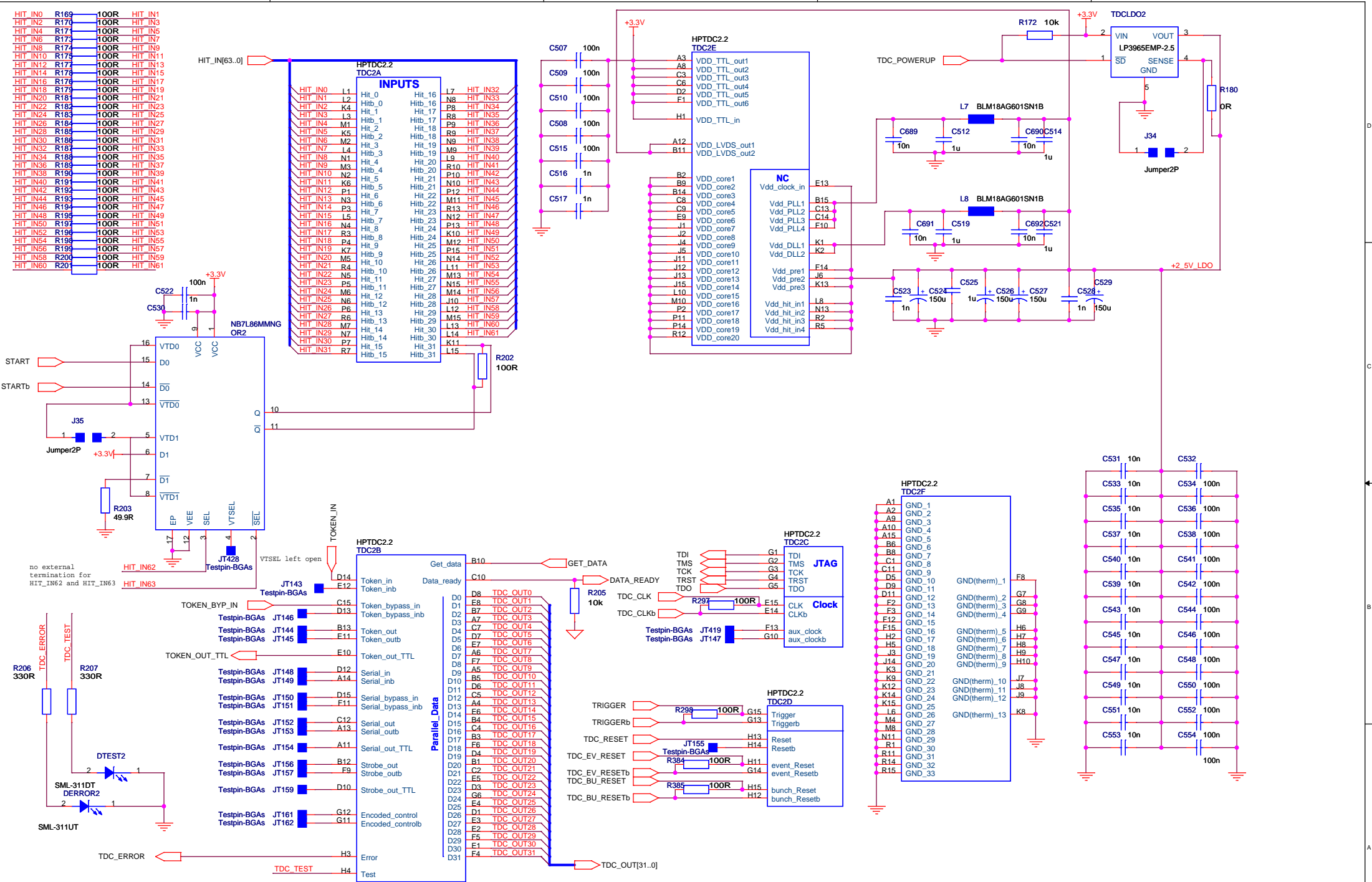


Title		
<b>HadesTRB2 - POWER</b>		
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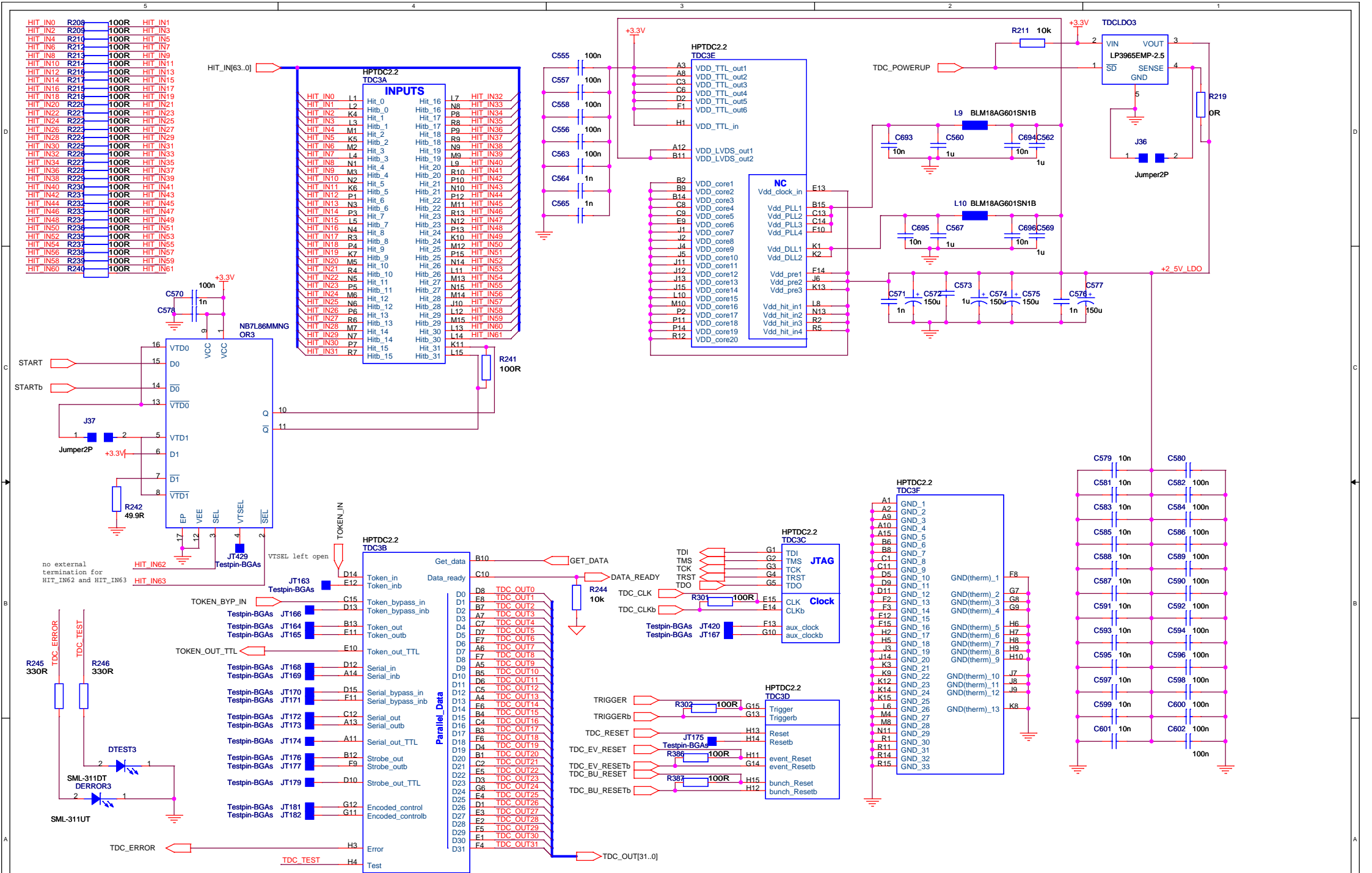




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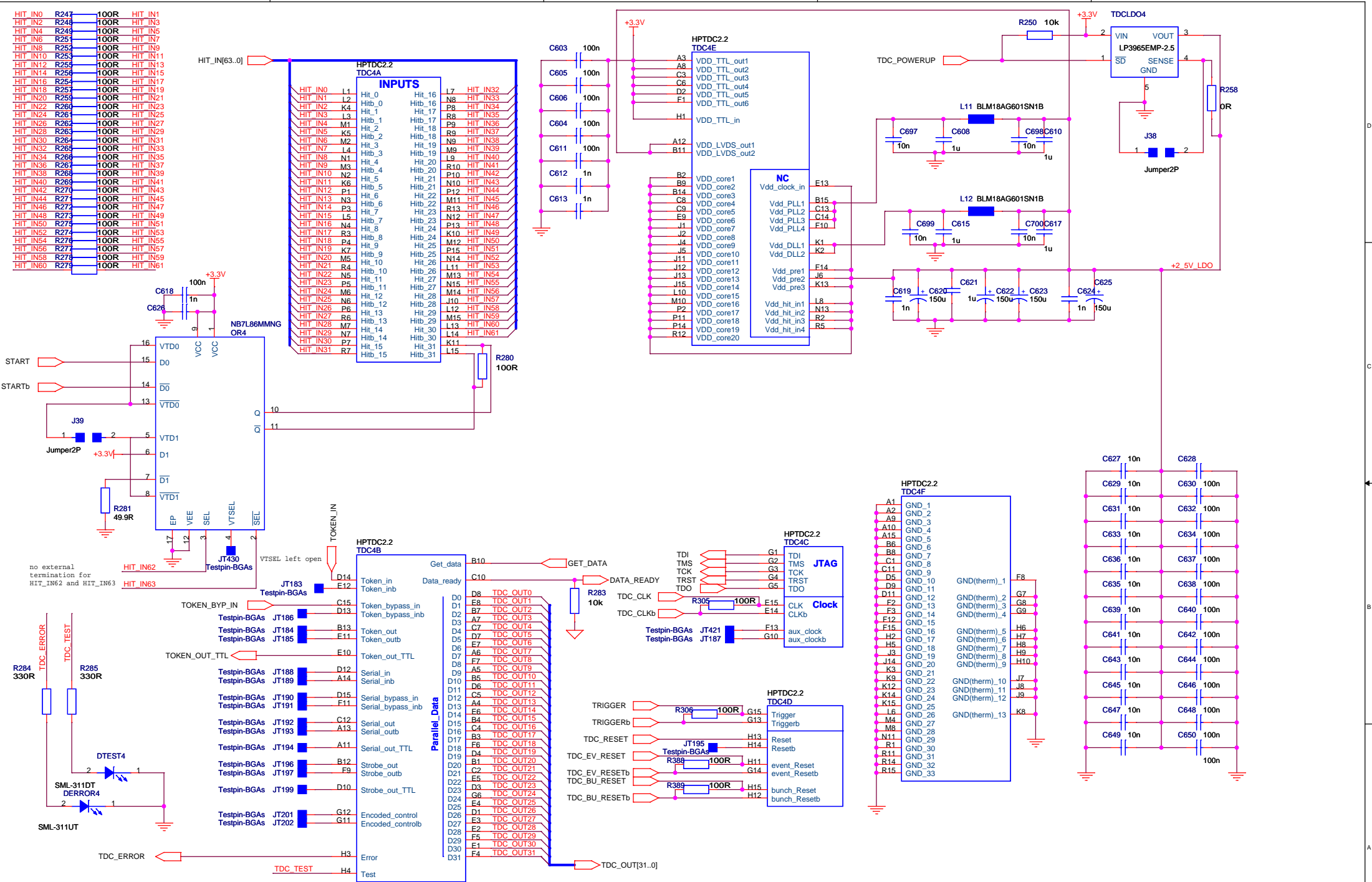


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