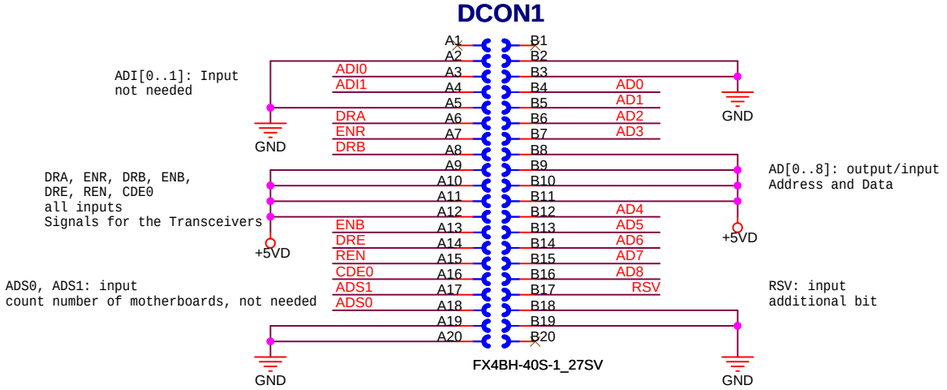
Voltage translators for 5V->3.3V and vice versa

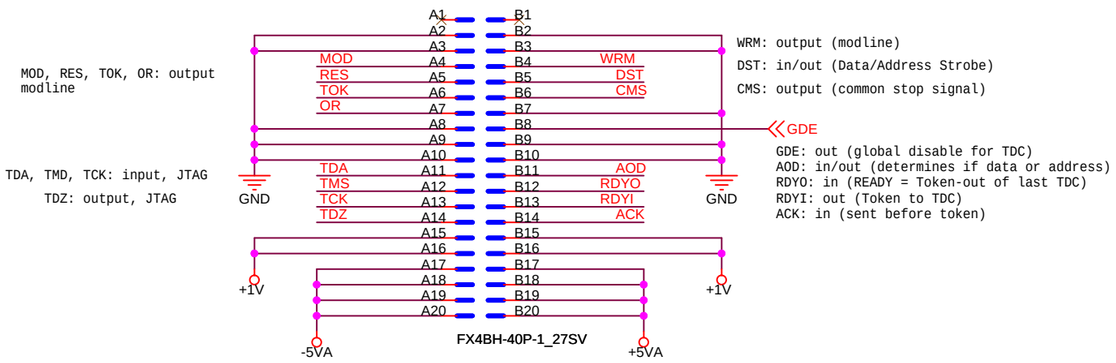
Connectors to the Motherboard

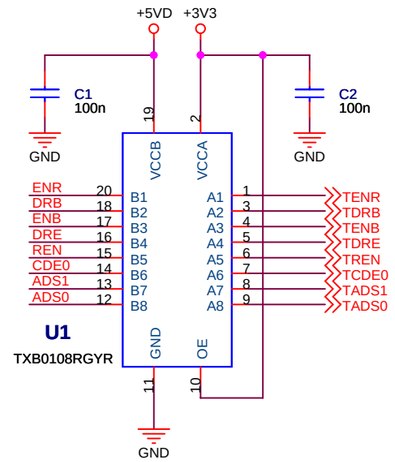
All directions are seen from this "driver card"

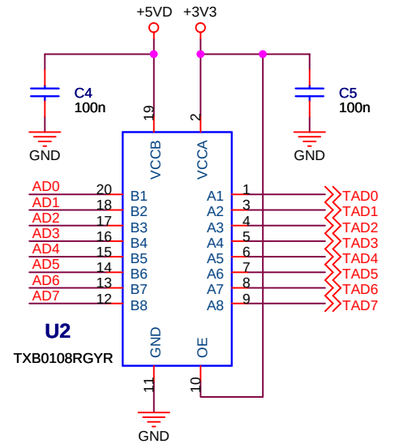
DCON1

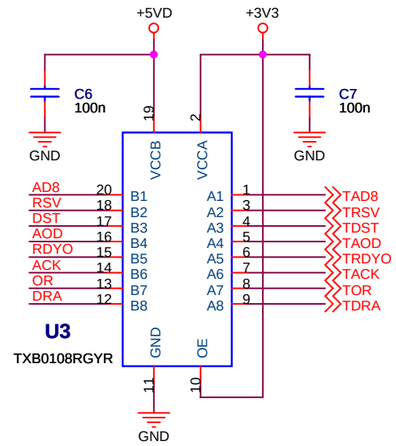


DCON2

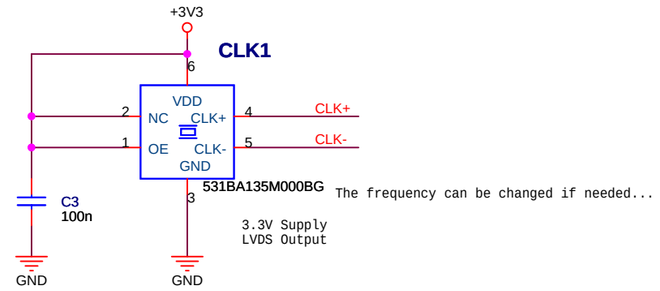


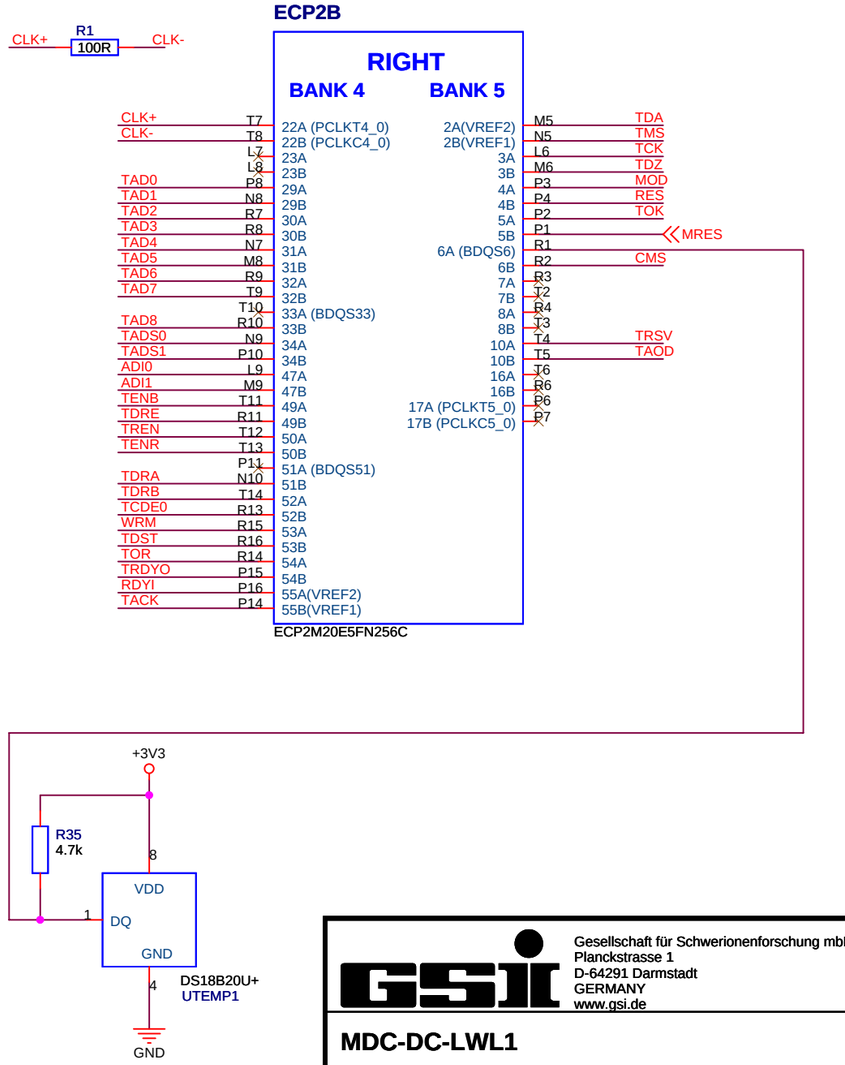






System Clock





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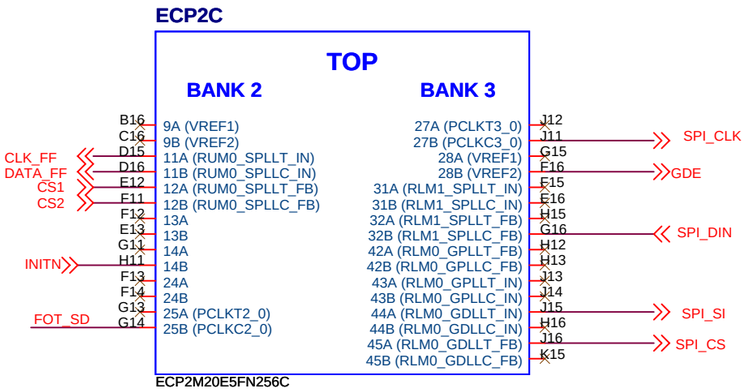
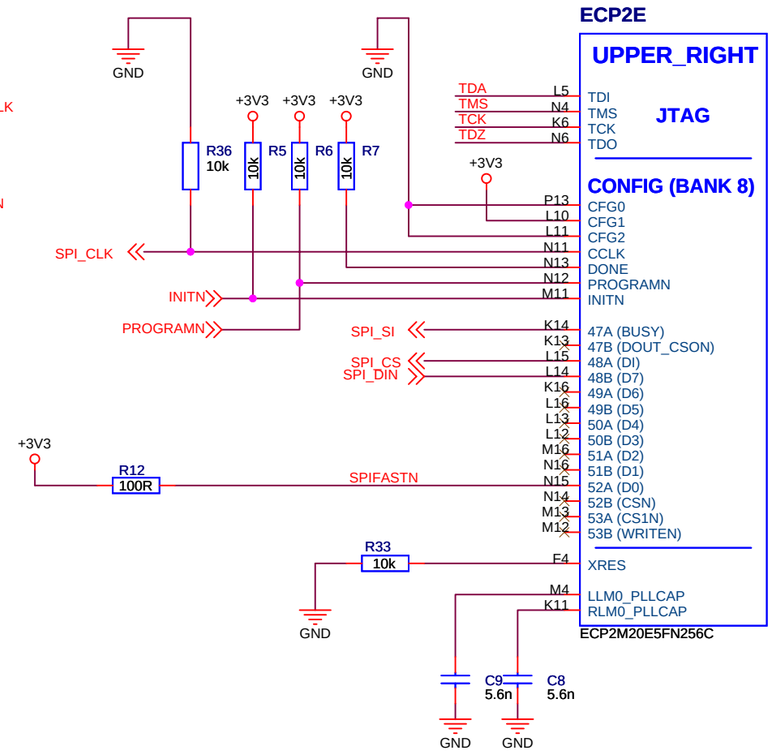
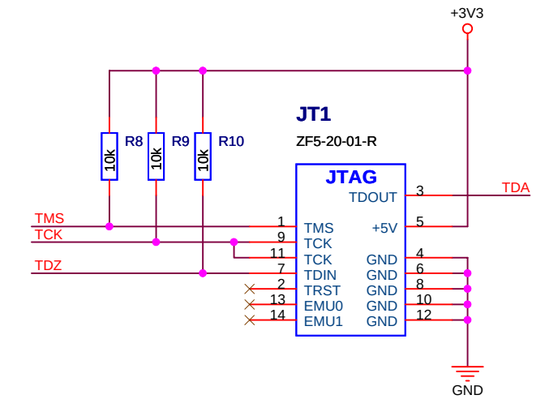
MDC-DC-LWL1

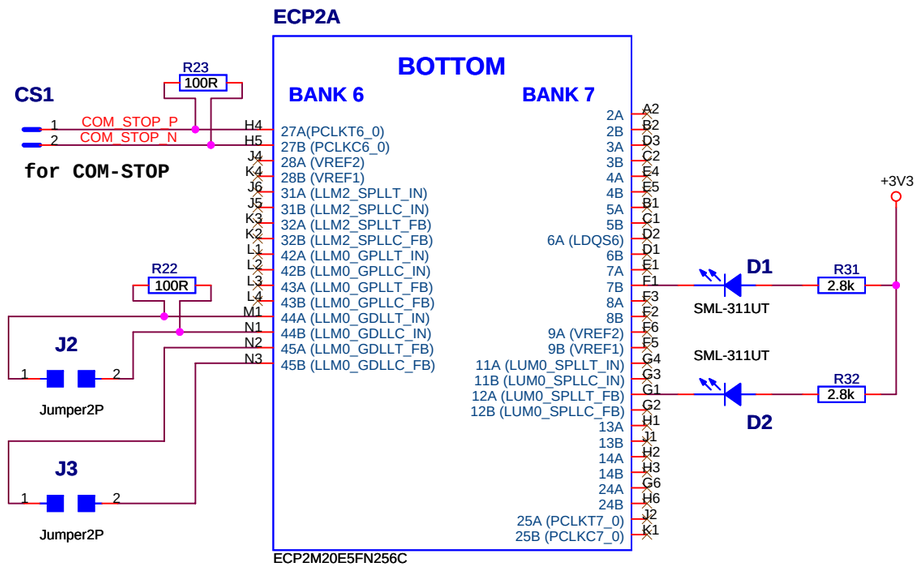
Design: K:\GSIJOB\MDC-DC-LWL\MDC-DC-LWL1\MDC-DC-LWL1.DSN	
Modified: Wednesday, September 05, 2007	Size: A3 Page: 1 / 4
Designer: <Designer>	Layouter: <Layouter>

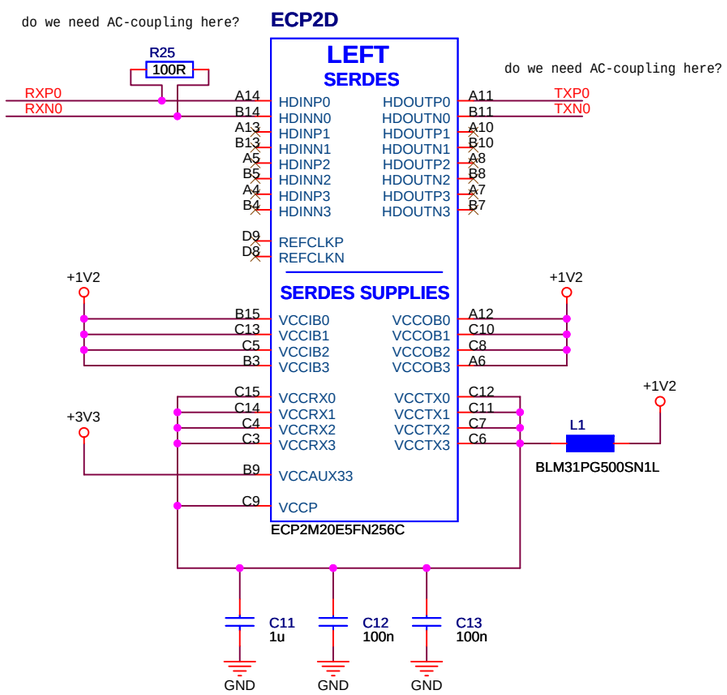
Banks 2,3,6 and 7 have 50% outputs with LVDS capability
For correct LVDS output levels the corresponding VCCIOs have to be 2.5V, which is not the case on this PCB
LVDS Input will work on all pairs, even with VCCIO at 3.3V

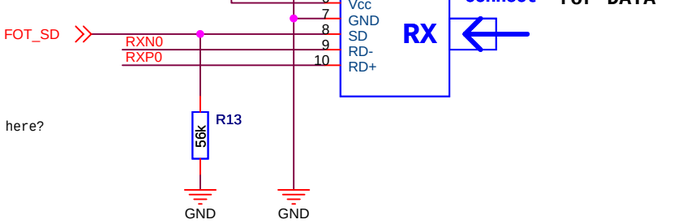












Firecomms FOT: Fiber optics transceiver
Works up to 270MBit/s
LVDS in and output, directly connected to the SERDES of the LatticeECP2M

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MDC-DC-LWL1

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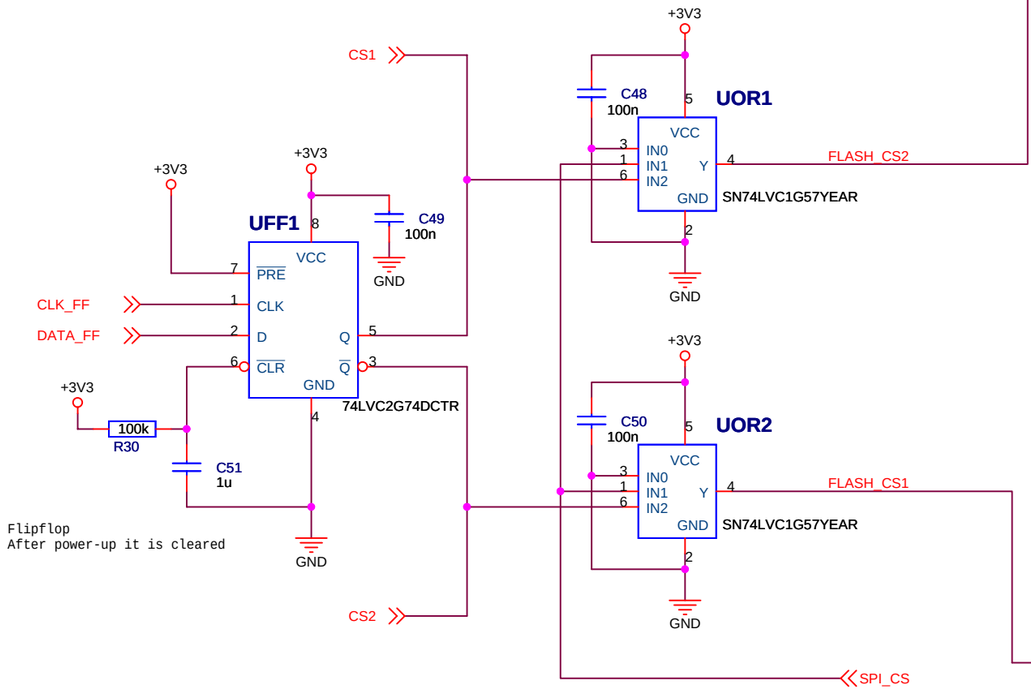
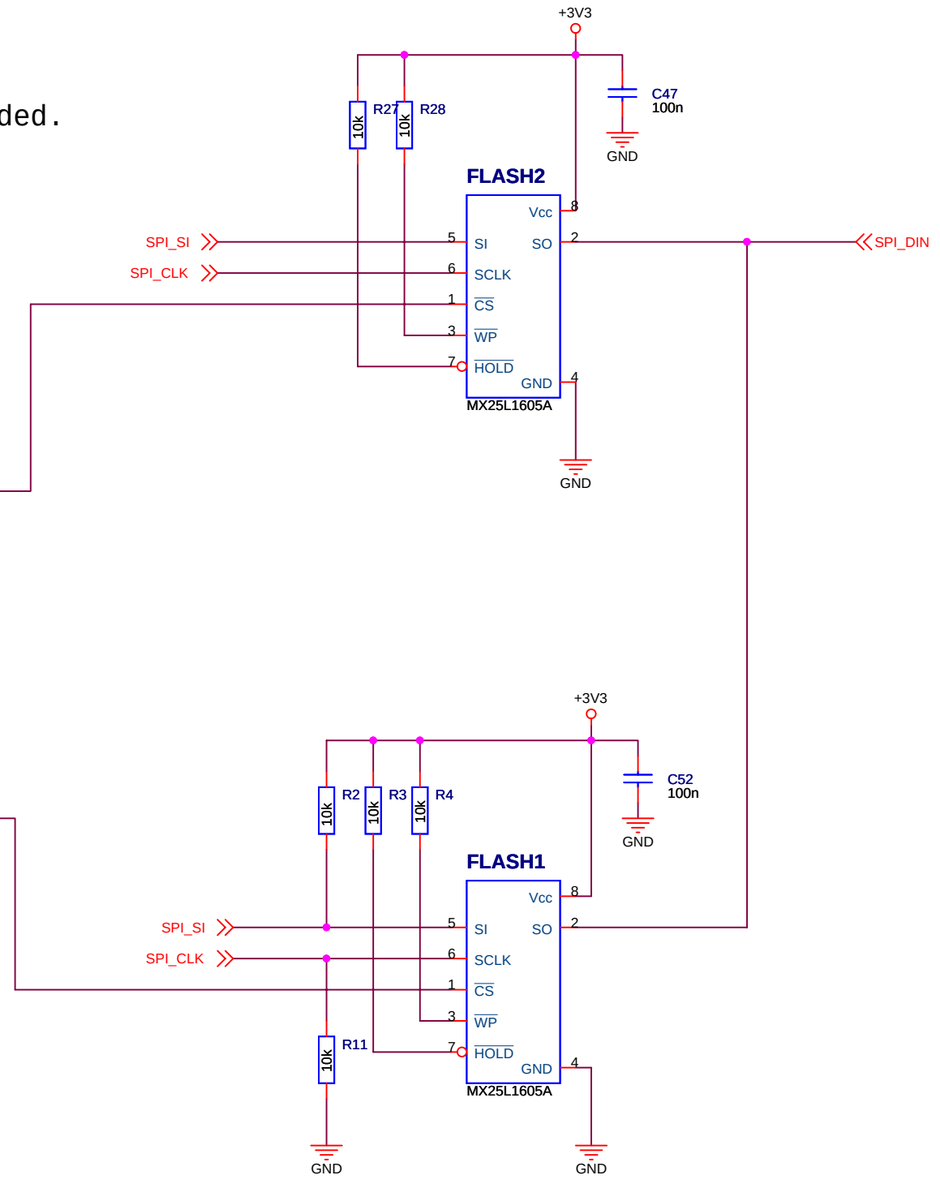
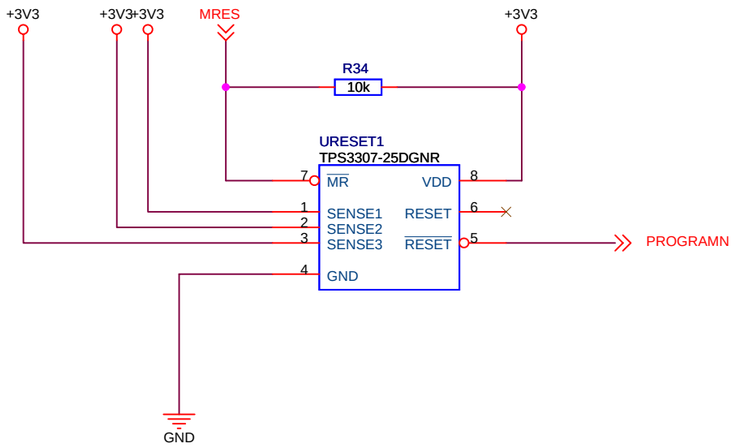
Modified: Wednesday, September 05, 2007	Size: A3	Page: 2 / 4
Designer: <Designer>	Layouter: <Layouter>	

Circuitry to assure that on powerup always the working design is loaded.





These are multi-purpose gates.
In this configuration (pin 3 to GND) they are OR gates
with one input negated.
Therefore it is required, that the FPGA asserts (low) the
ChipSelect (SPI_CS) and additionallly, that the CS1/2 is low,
to assert a CS of Flash1 or Flash2.
After the first booting, the FPGA can put a '1' to the data input
of the FlipFlop and give a clock, then the other FLASH is selected.
This then can be programmed and with asserting the
ManualReset pin on the ResetChip, the FPGA will get a
PROGRAMN pulse, which will reload the FPGA with the new design.



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MDC-DC-LWL1

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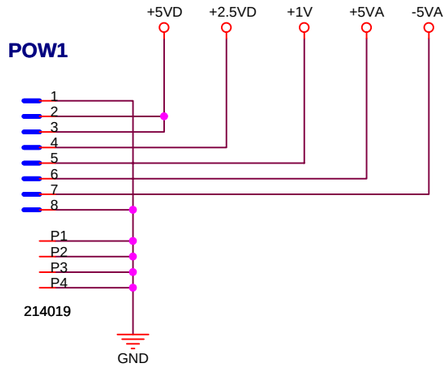
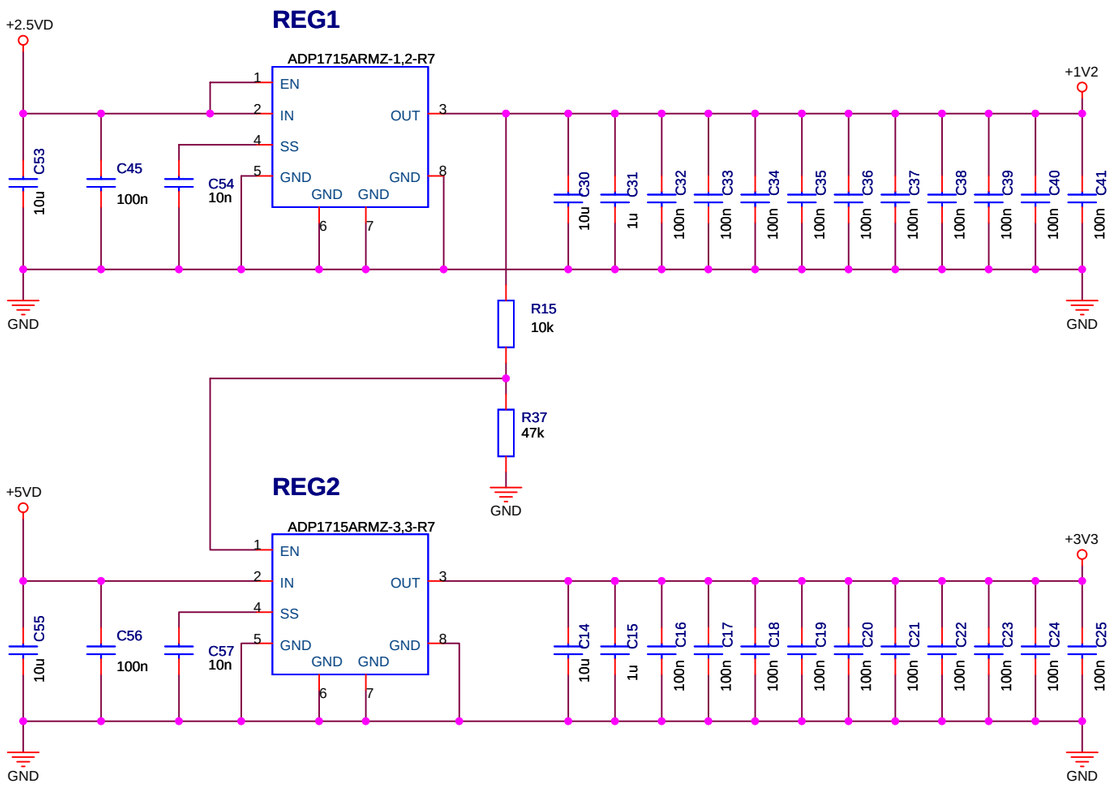
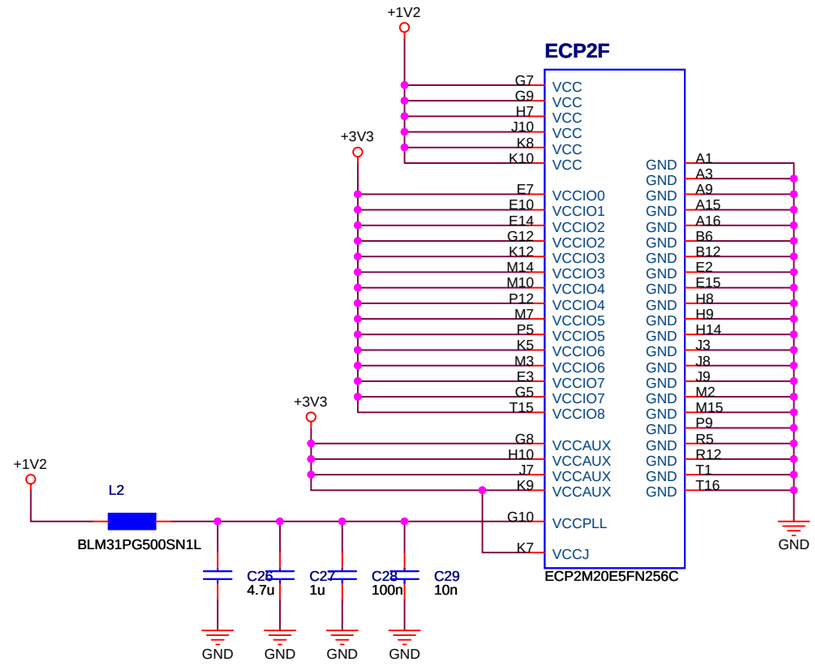
Modified: Wednesday, September 05, 2007	Size: A3 Page: 3 / 4
Designer: <Designer>	Layouter: <Layouter>

+1.5V is not used up to now. I a future version of this project,
this voltage should be used to make the 1.2V for the FPGA.







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Modified: Wednesday, September 05, 2007	Size: A3	Page: 4 / 4
Designer: <Designer>	Layouter: <Layouter>	