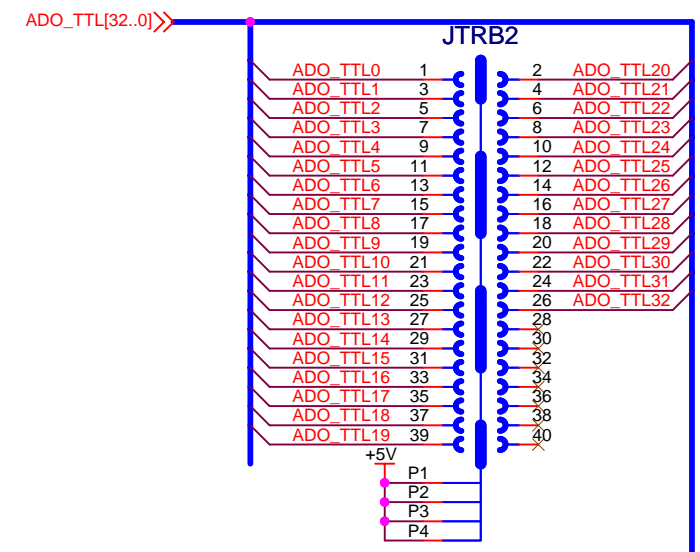
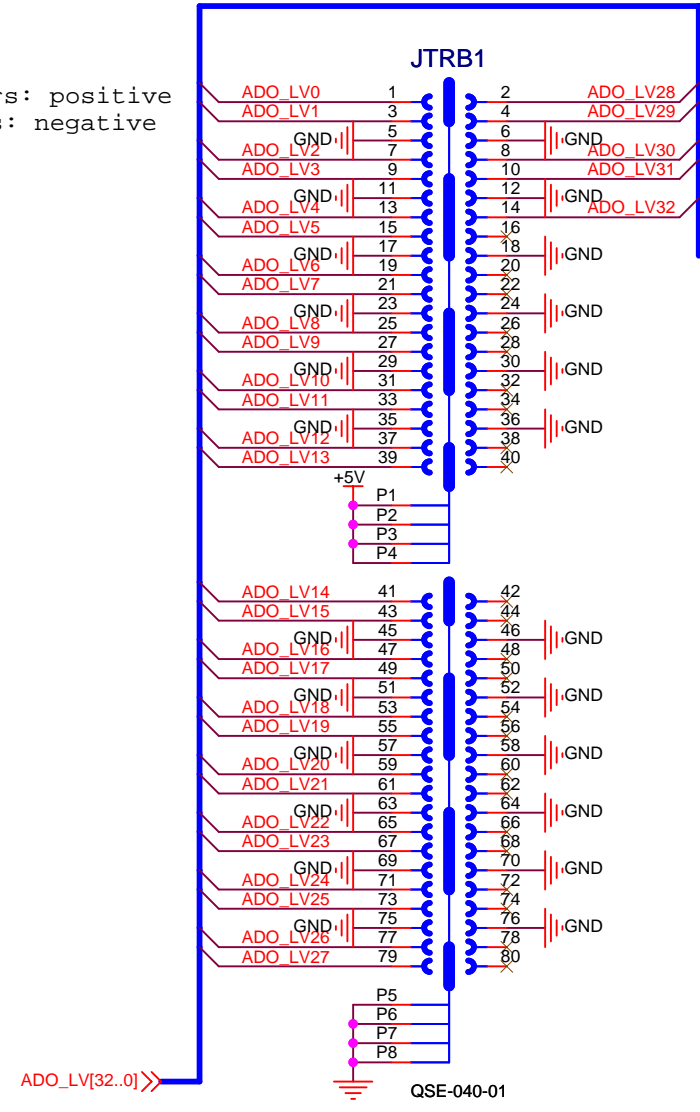
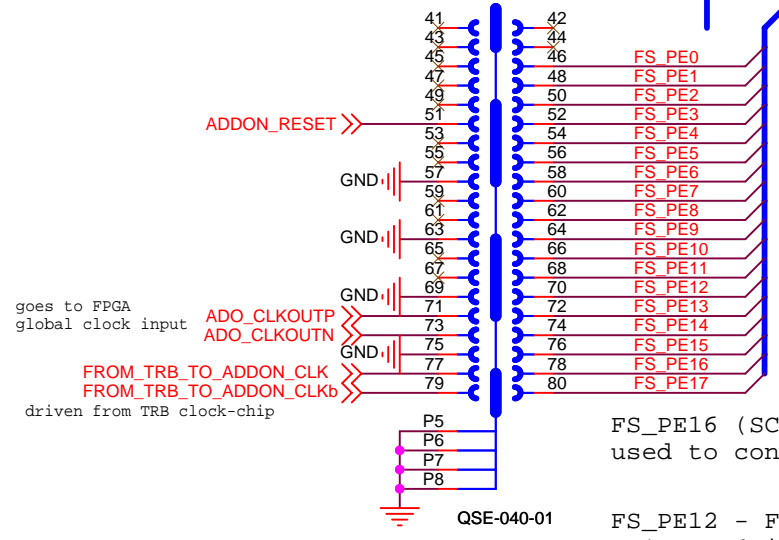


Even numbers: positive  
 Odd numbers: negative



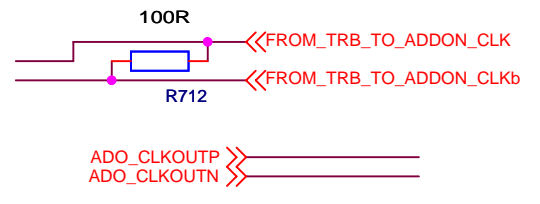
JTAG interface:  
 (seen from TRB)  
 TDI - TDO from FPGA on TRB (FS\_PE0 high Z)  
 TMS - FS\_PE1  
 TCK - FS\_PE2  
 TDO - FS\_PE4



FS\_PE16 (SCL) and FS\_PE17 (SDA)  
 used to control ispPAC-POWER chip

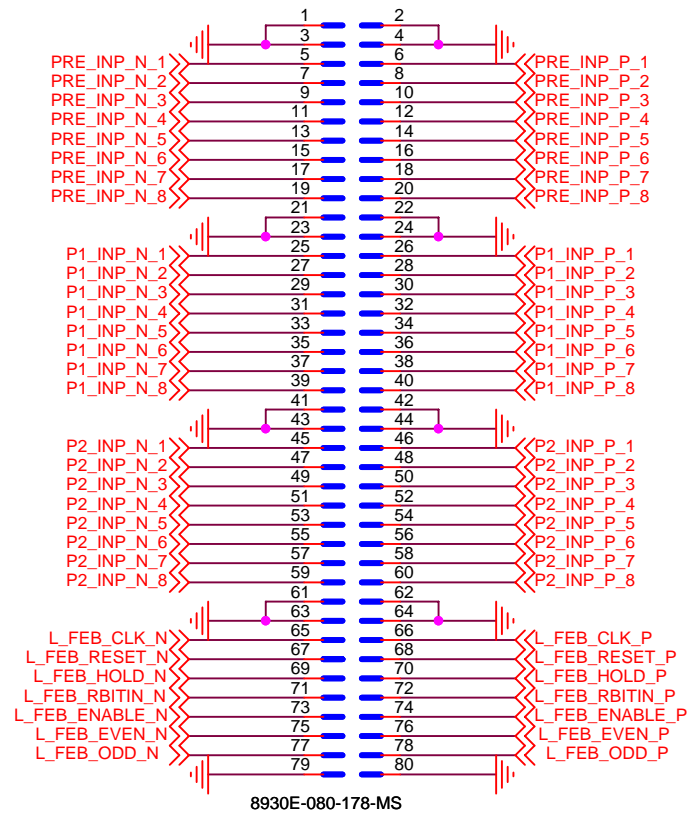
FS\_PE12 - FS\_PE15 connected to  
 IN1 - IN4 in ispPAC-POWER chip  
 general purpose inputs

FS\_PE11 - temperature control

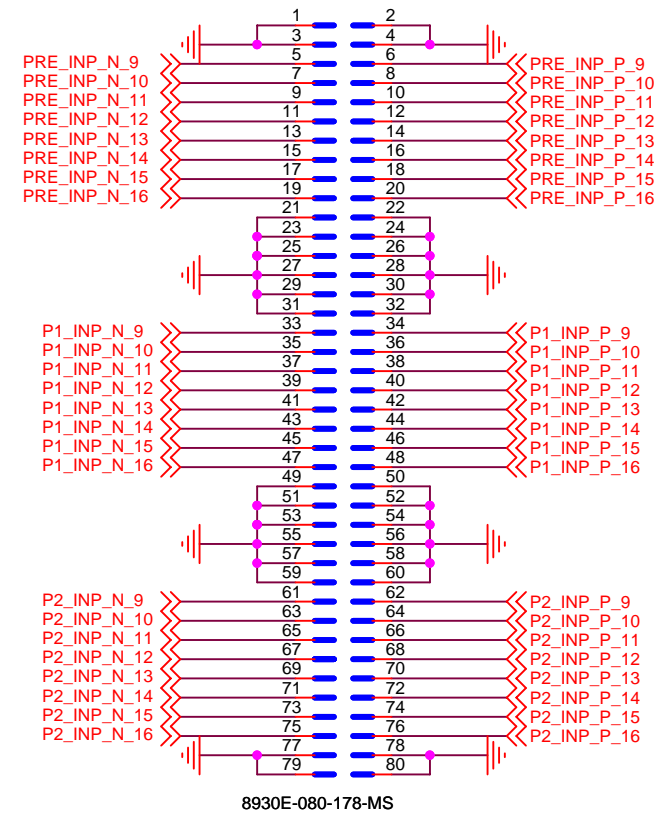


ADO\_LV[32..0]

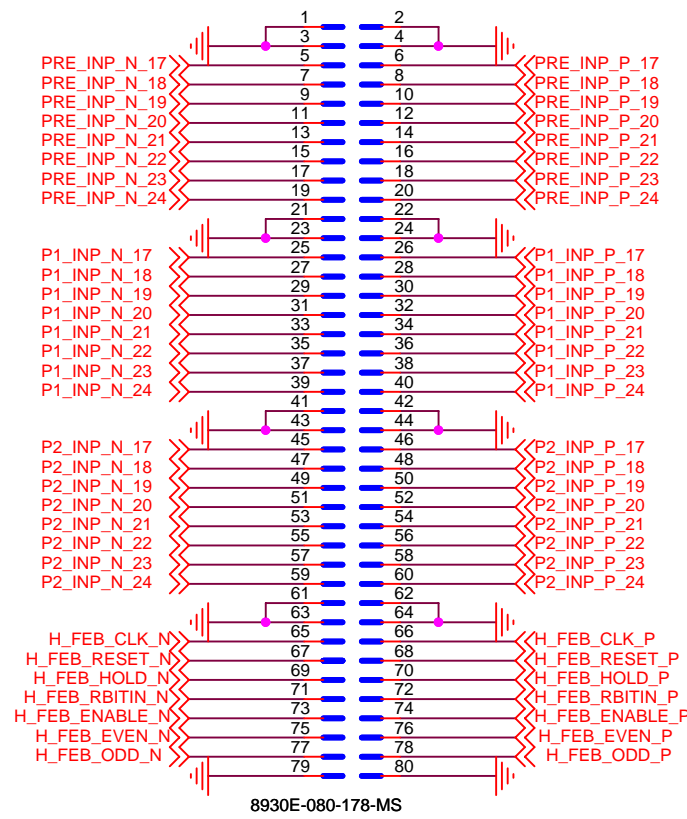
### DET\_LOW\_1-8



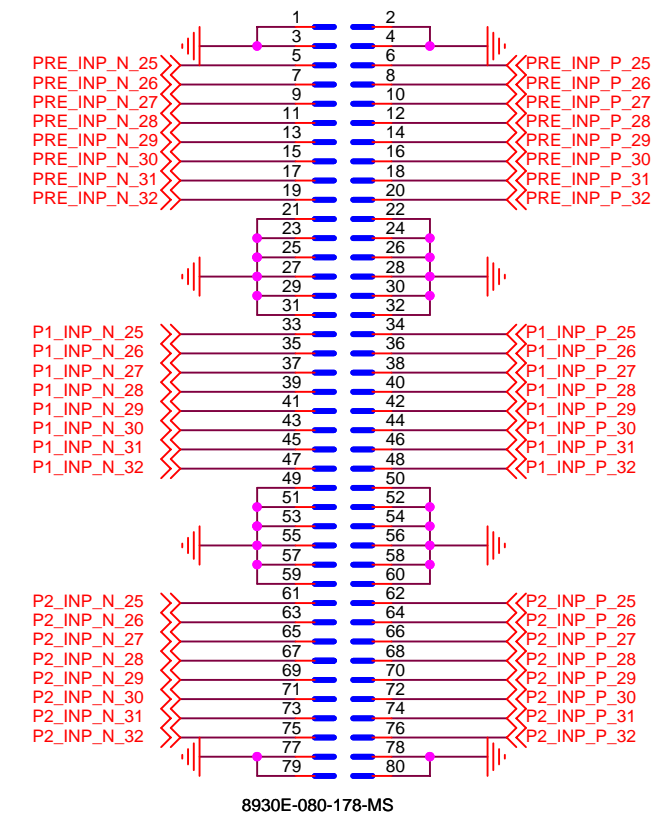
### DET\_LOW\_9-16

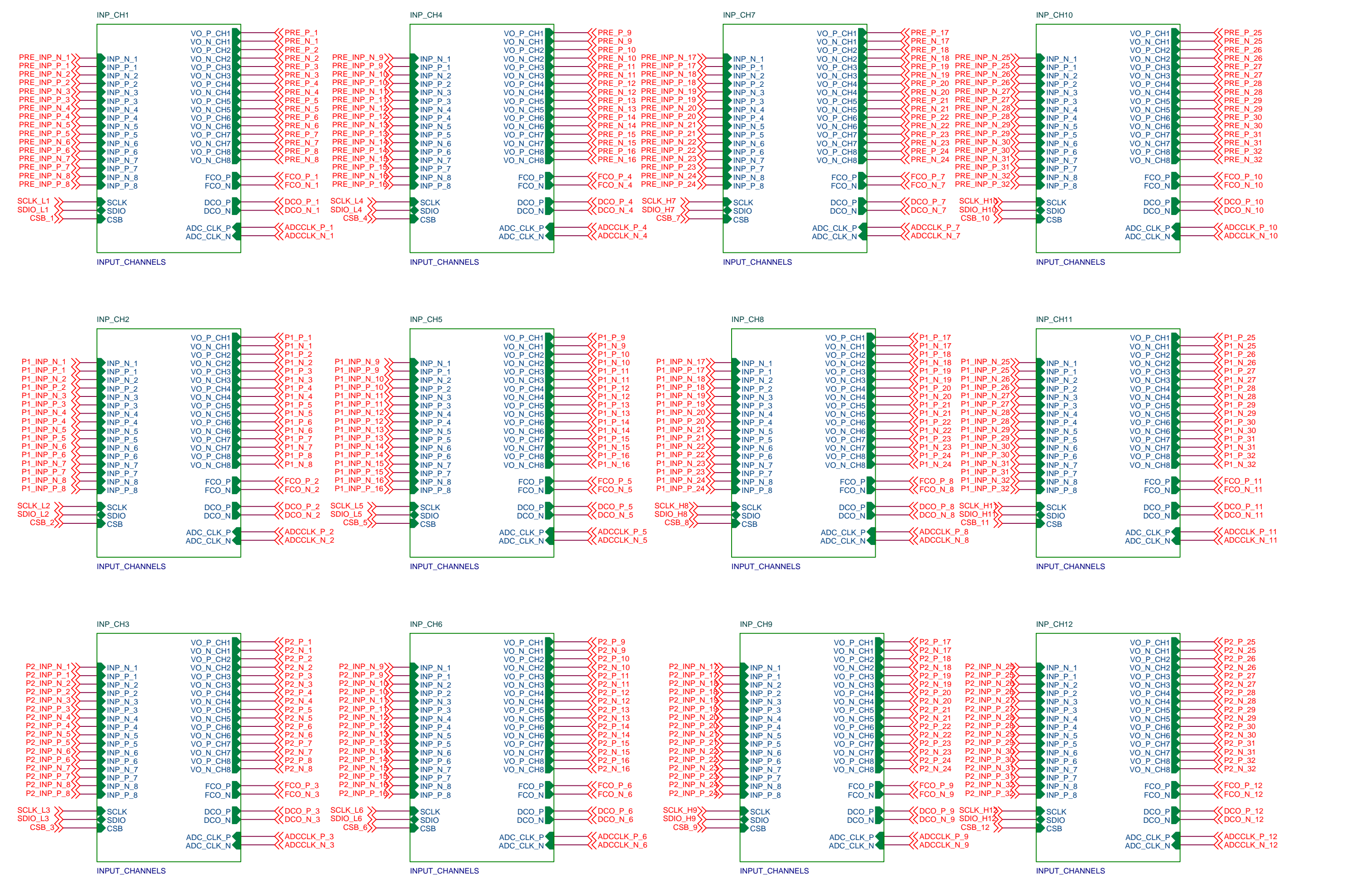


### DET\_HIGH\_17-24

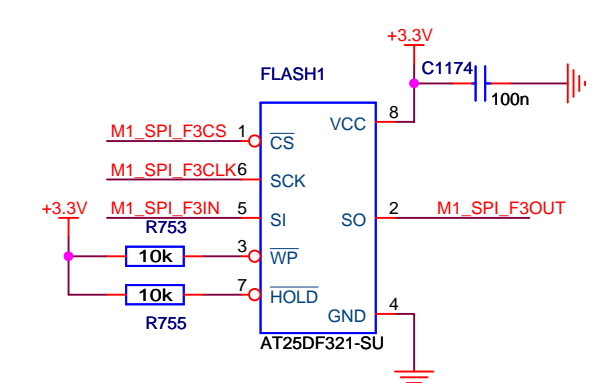
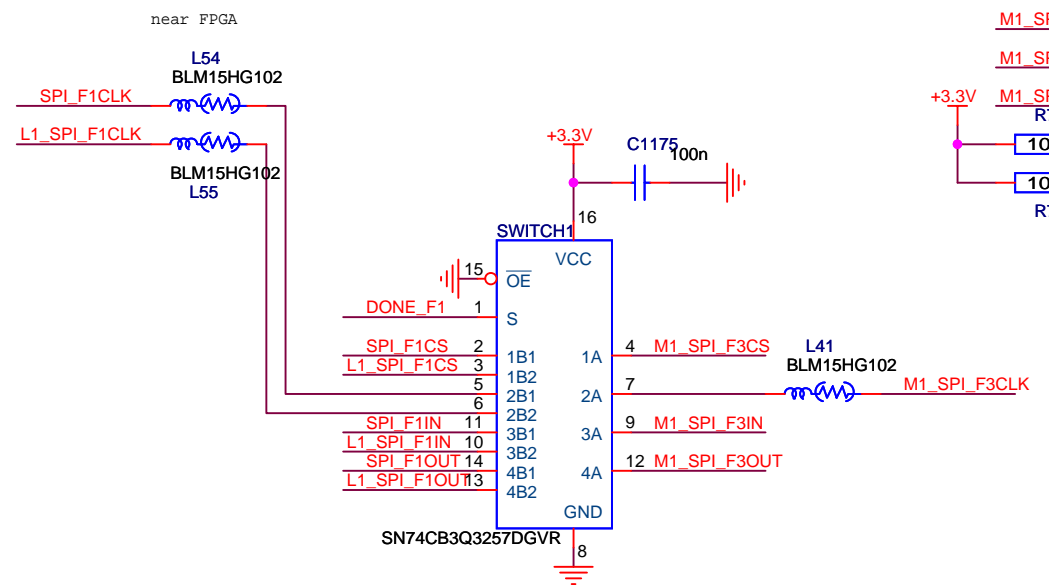
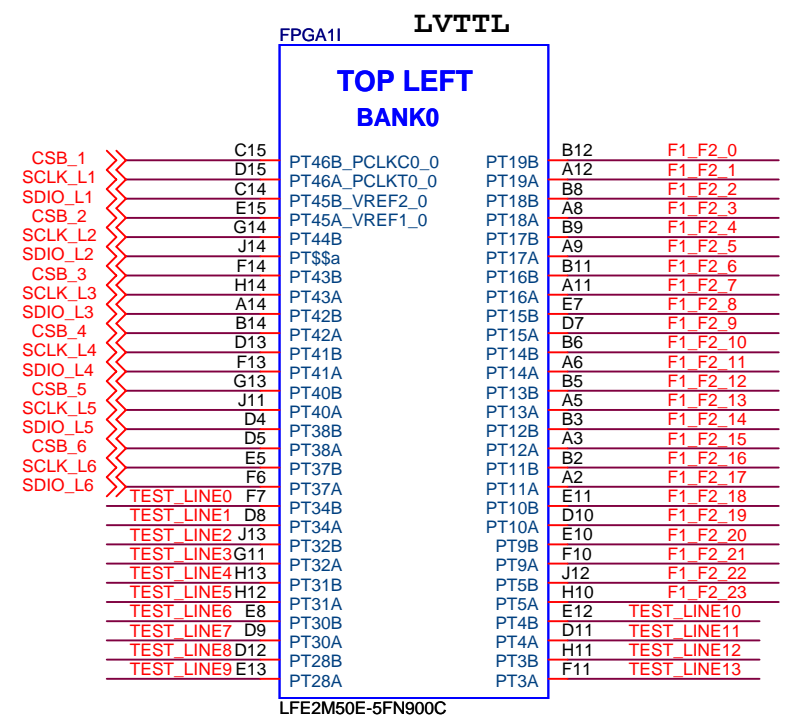


### DET\_HIGH\_25-32

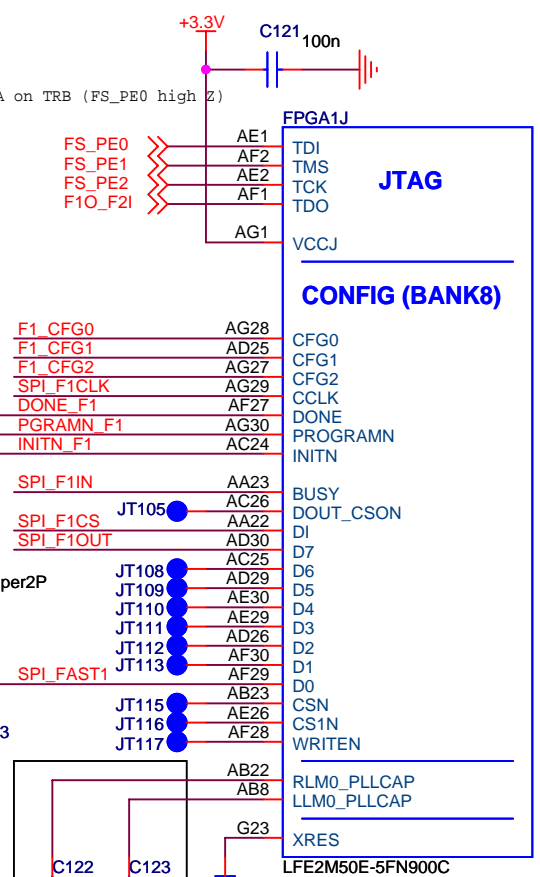




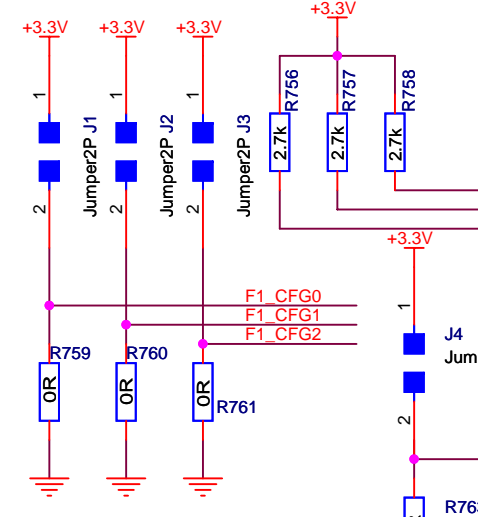
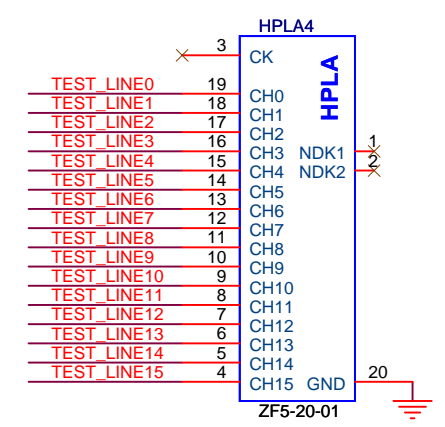
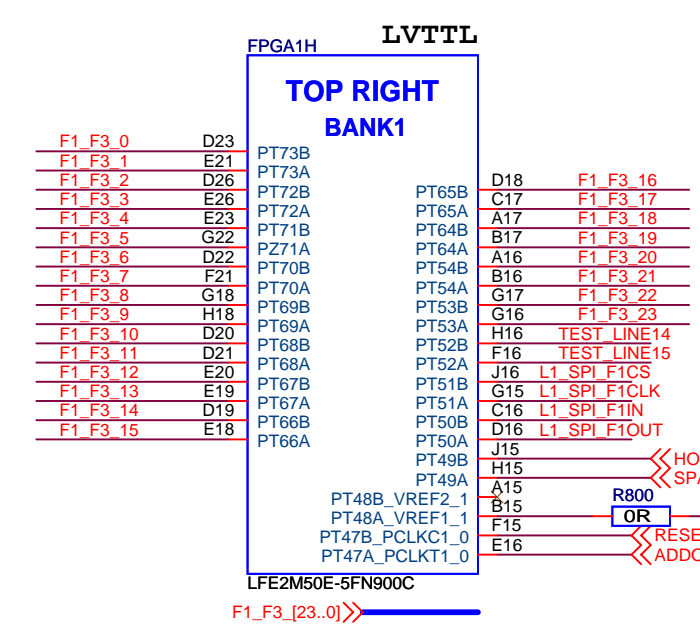
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Size	Document Number				Rev
A3	<Doc>				<RevC>
Date:	Tuesday, January 26, 2010	Sheet	4	of	35

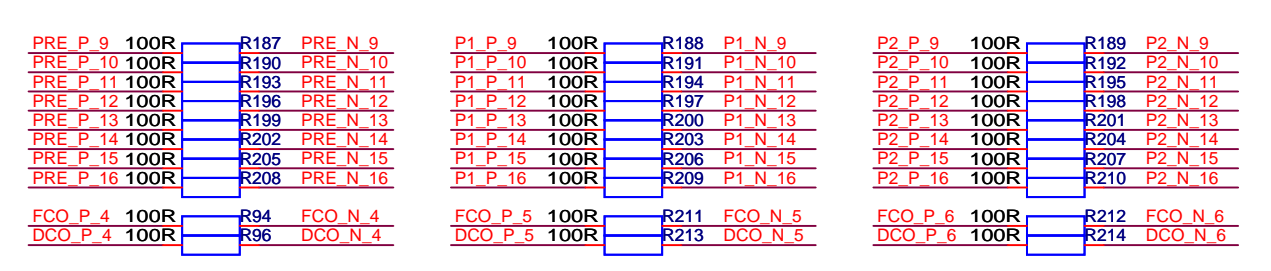
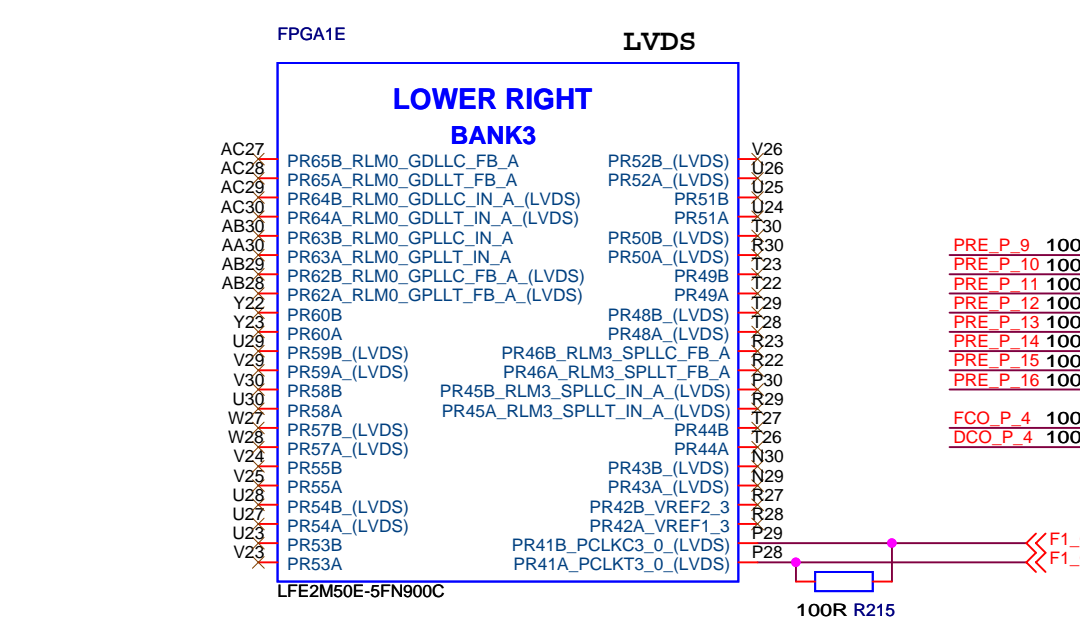
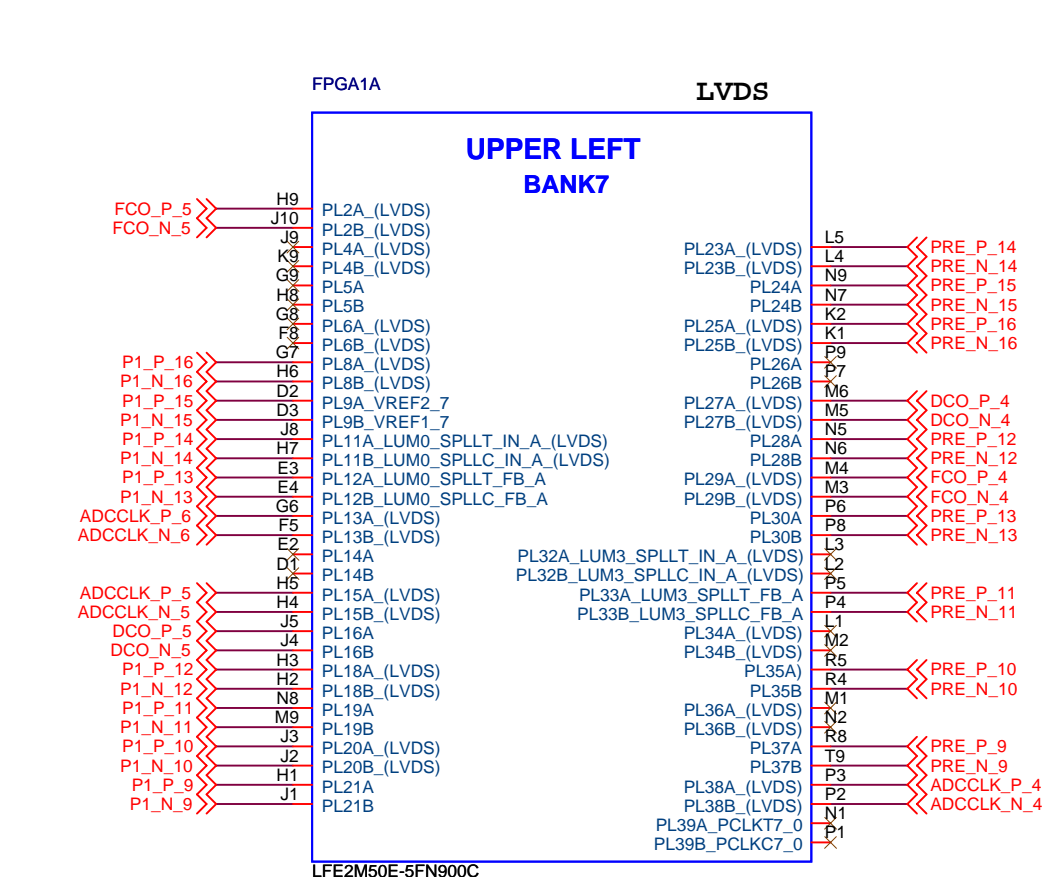
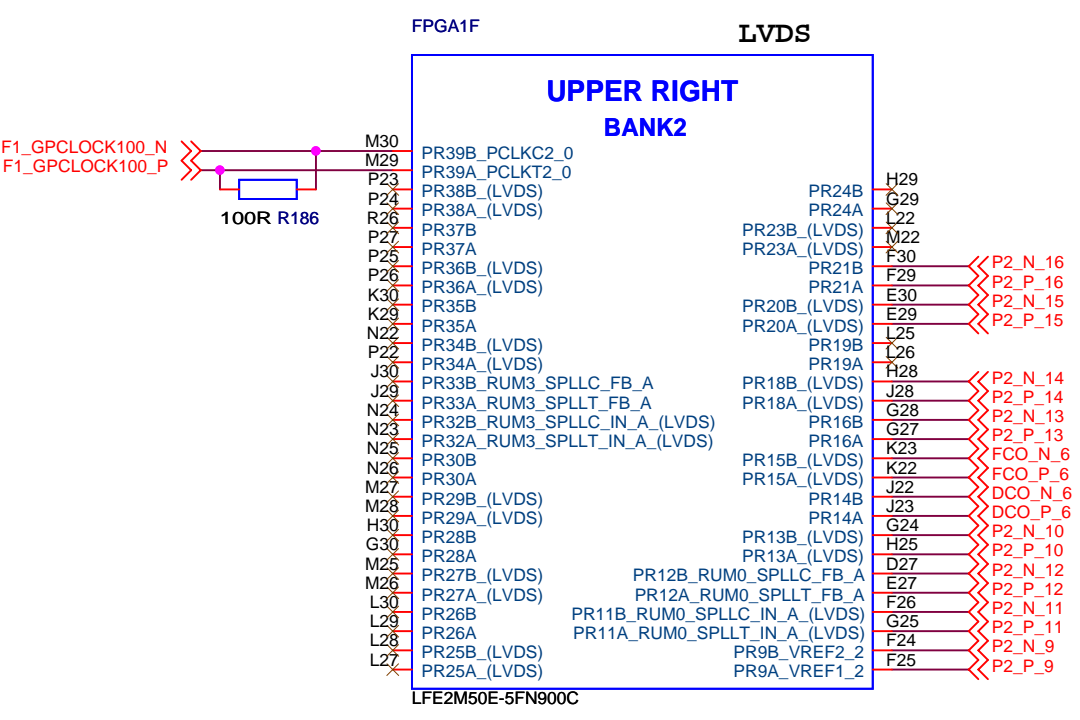


JTAG interface:  
(seen from TRB)  
TDI - TDO from FPGA on TRB (FS\_PE0 high Z)  
TMS - FS\_PE1  
TCK - FS\_PE2  
TDO - FS\_PE4



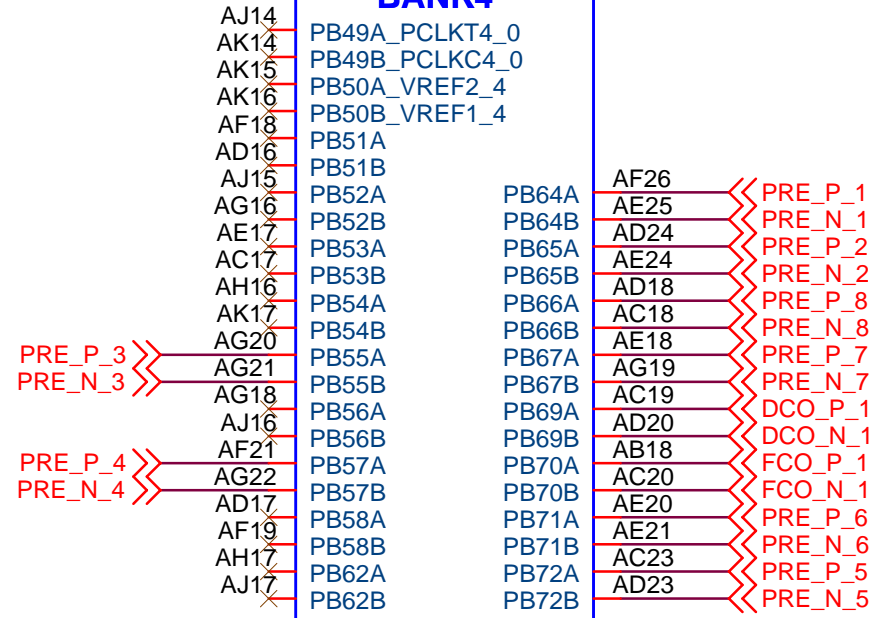
do not solder capacitors





FPGA1D LVDS

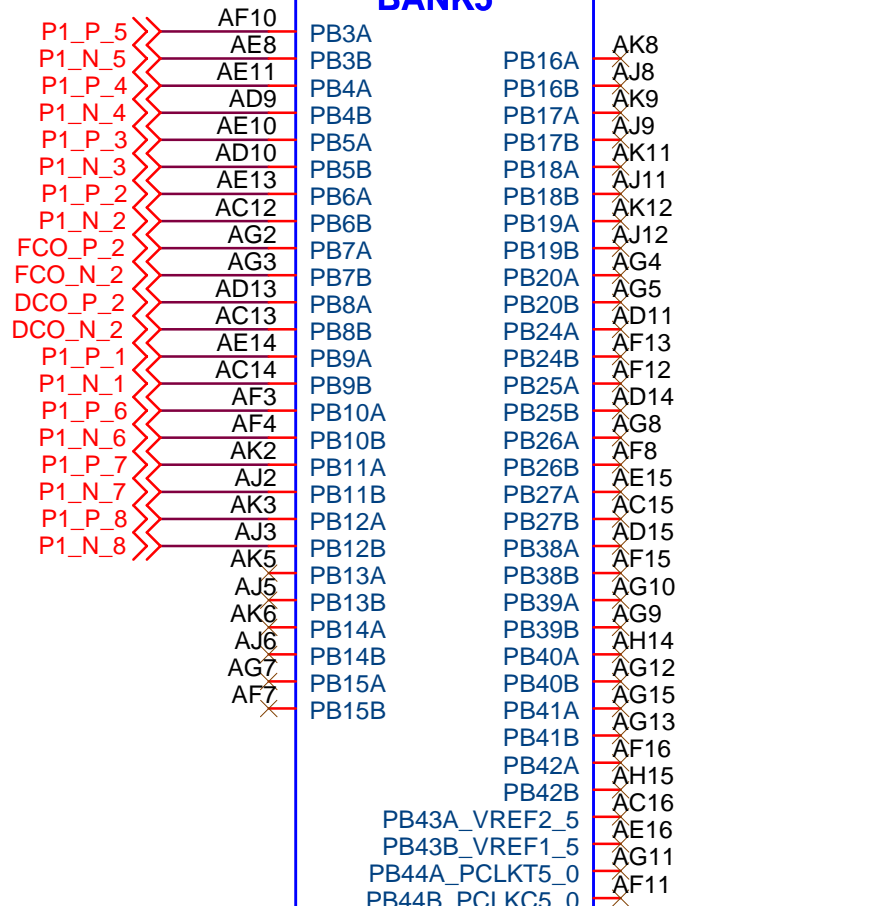
**BOTTOM RIGHT  
BANK4**



LFE2M50E-5FN900C

FPGA1C LVDS

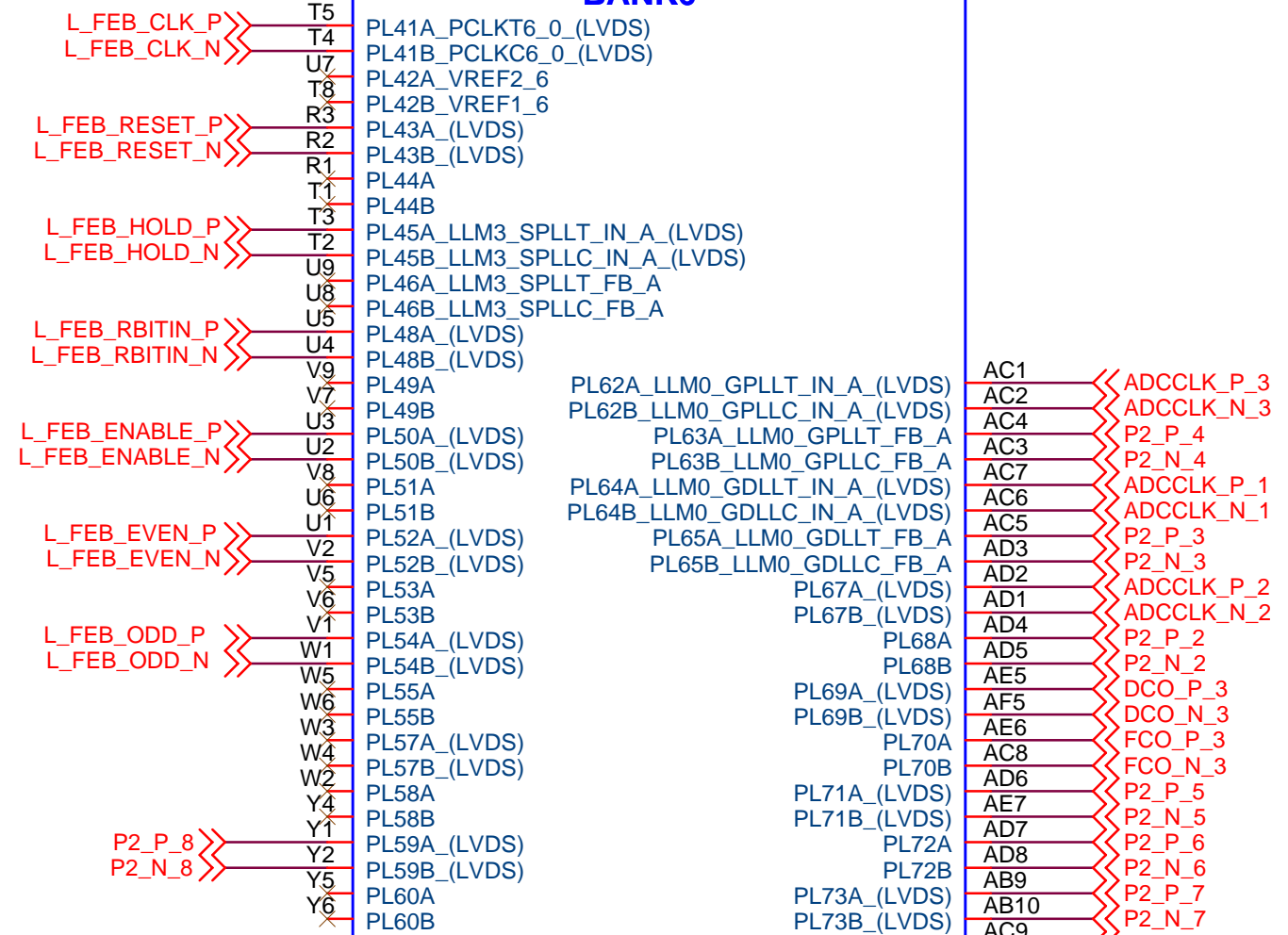
**BOTTOM LEFT  
BANK5**



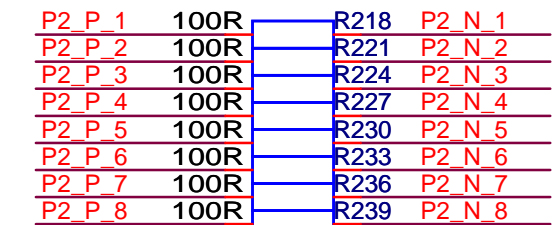
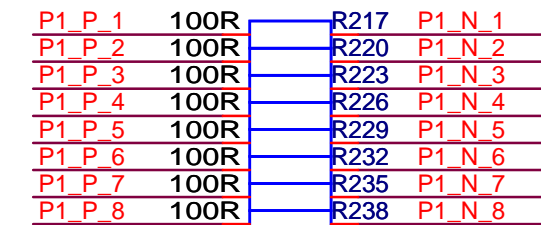
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FPGA1B LVDS

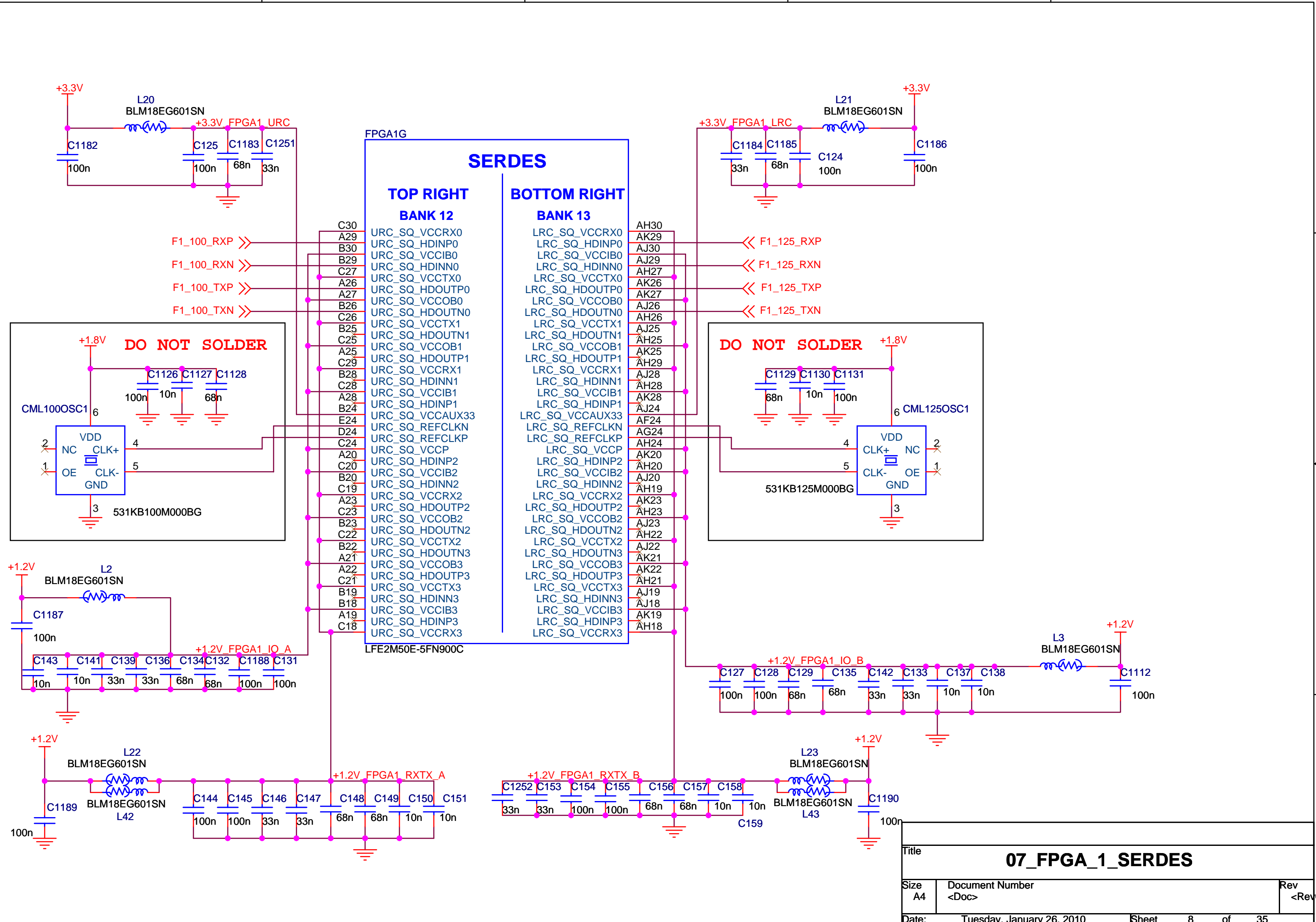
**LOWER LEFT  
BANK6**



LFE2M50E-5FN900C

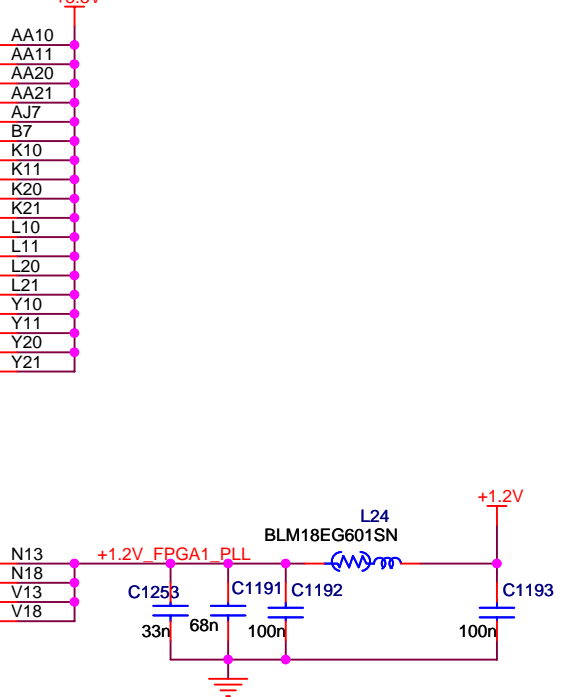
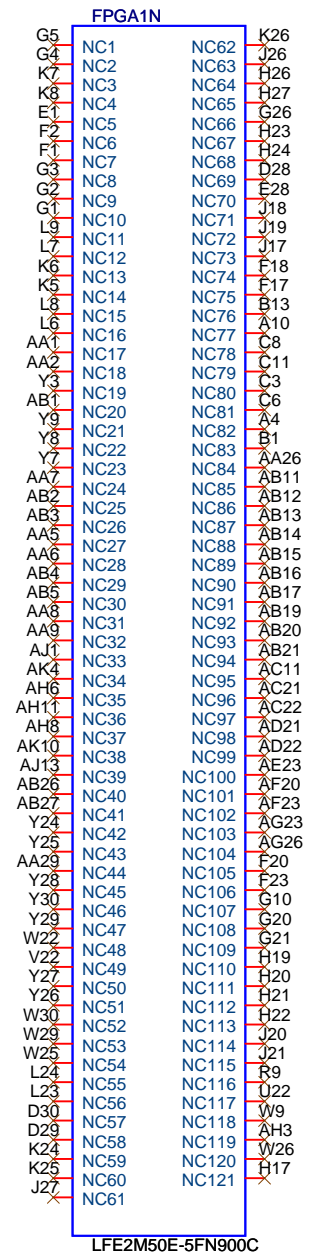
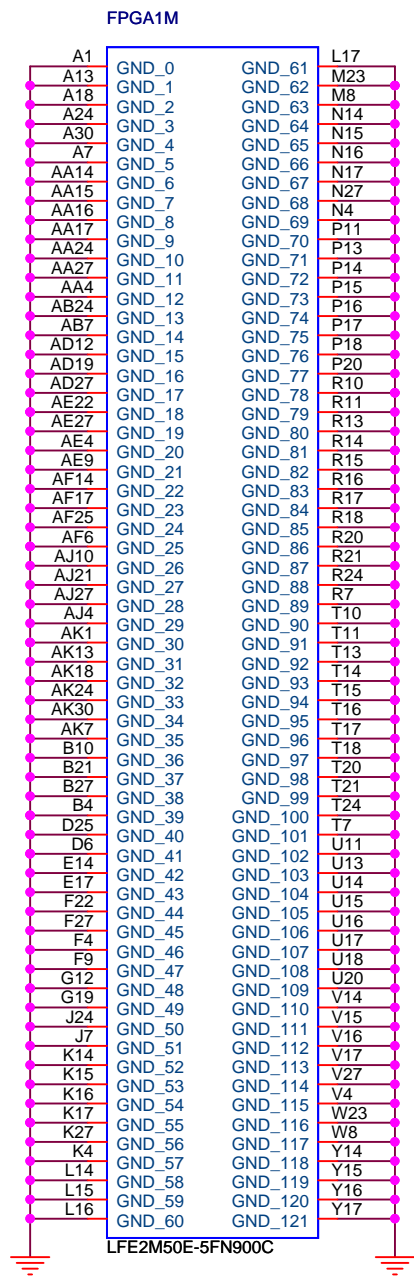
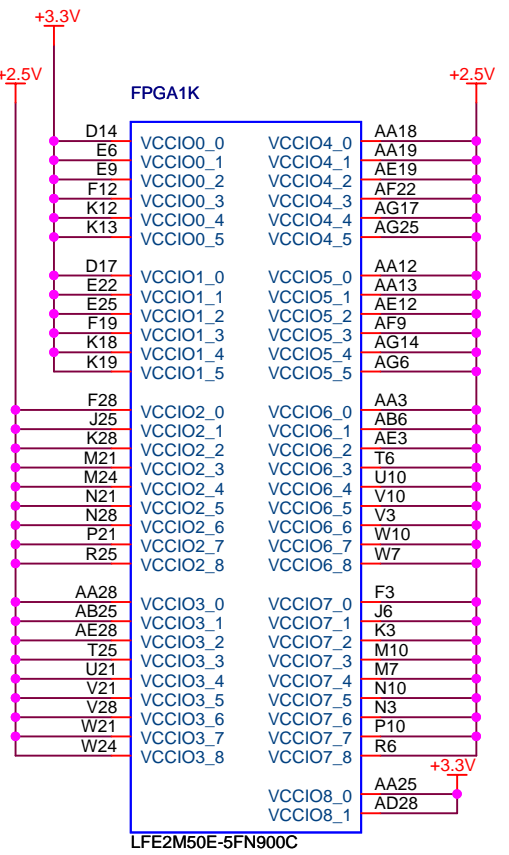
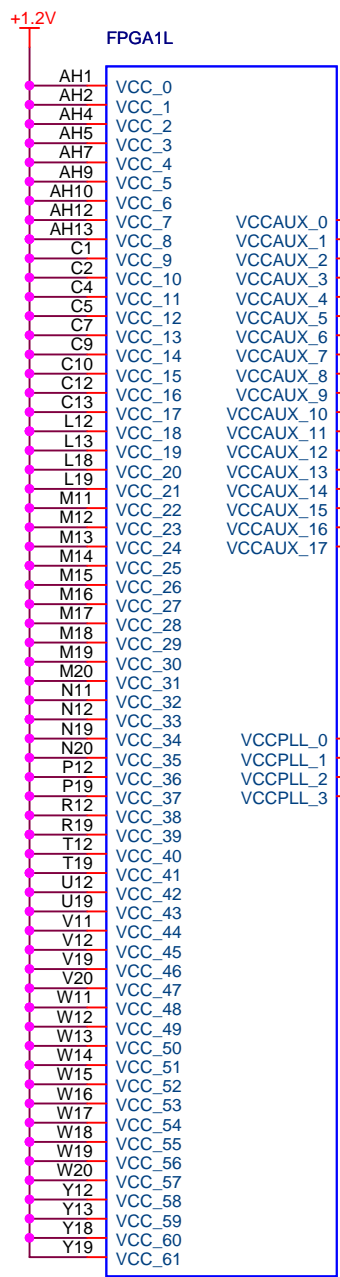


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Size	Document Number	Rev
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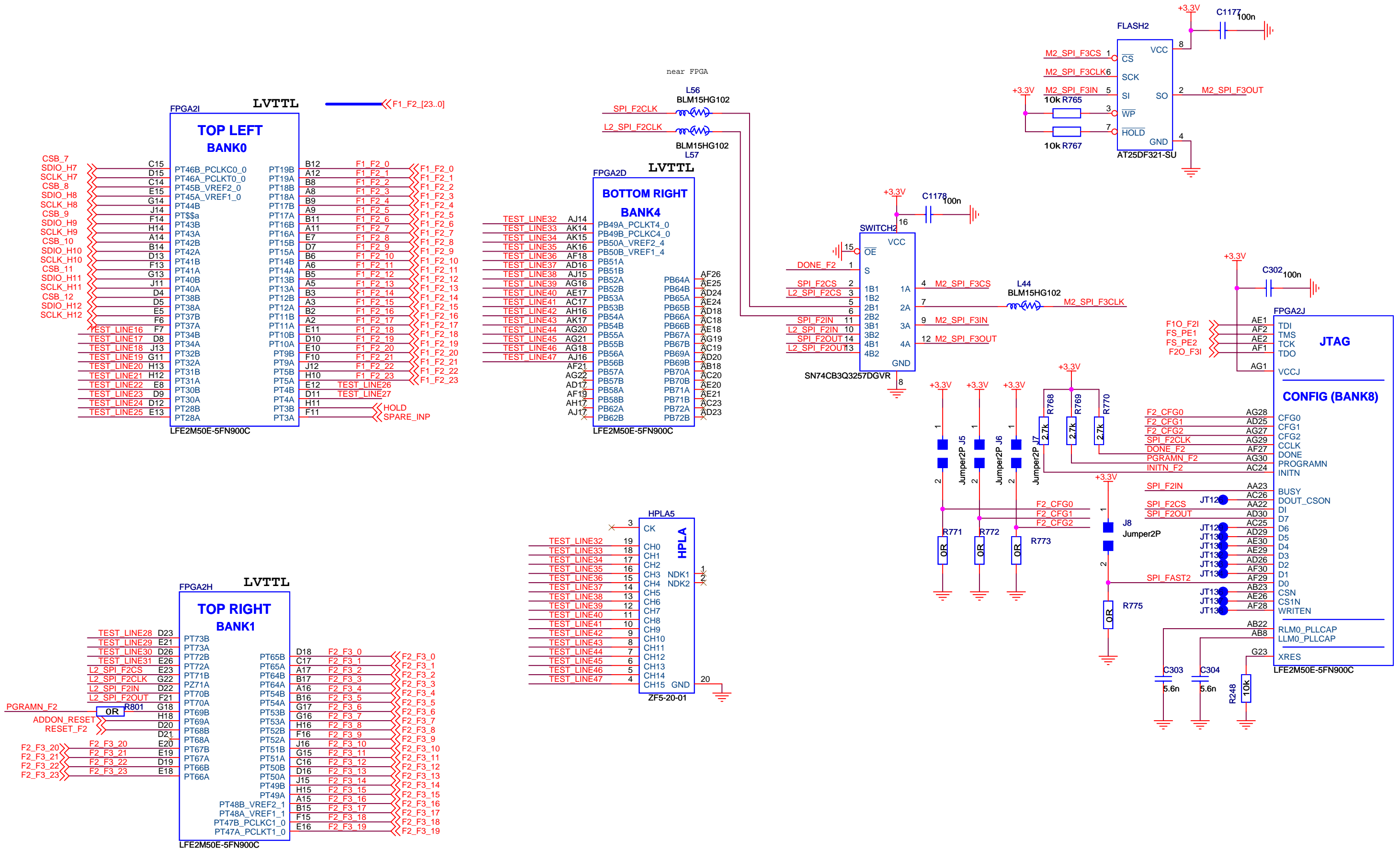


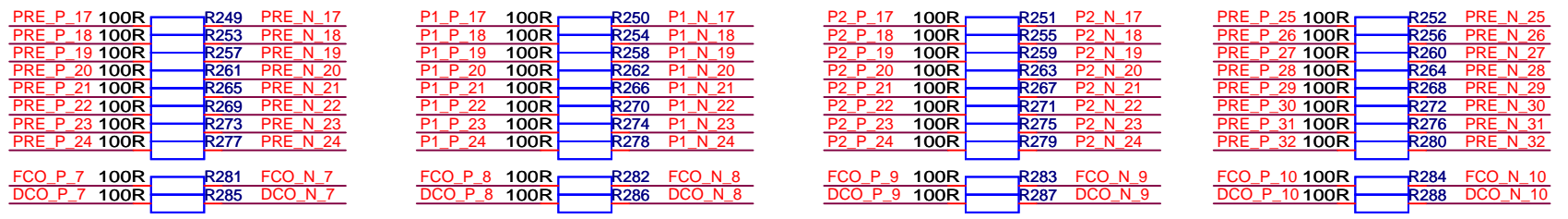
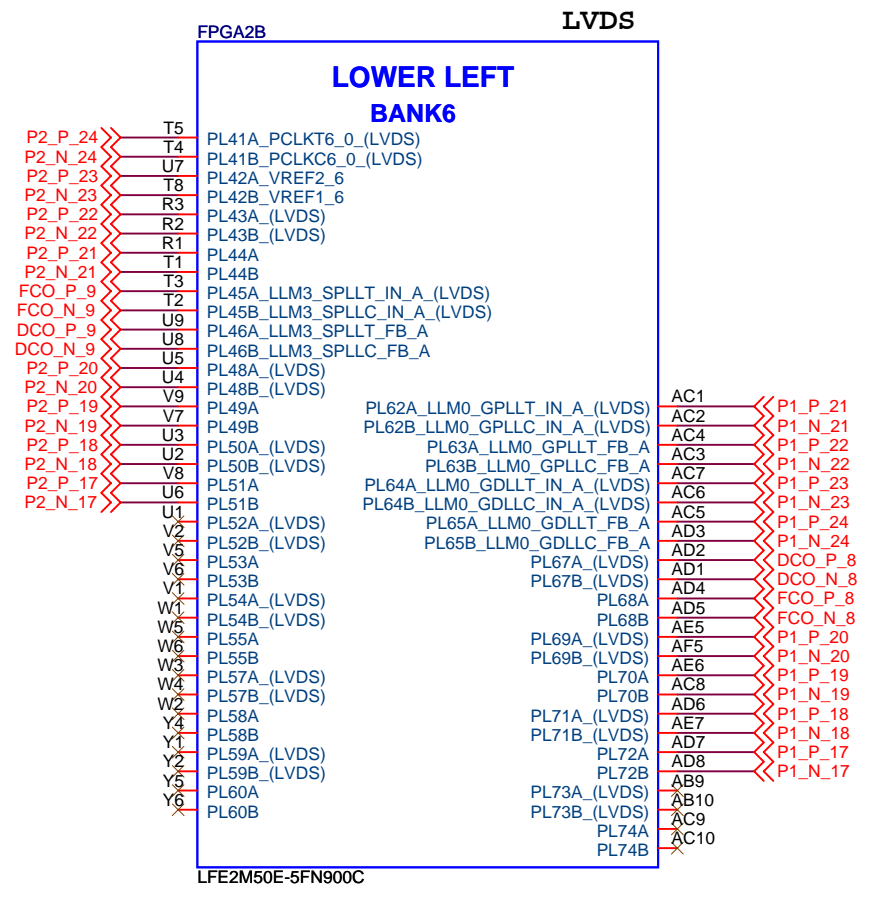
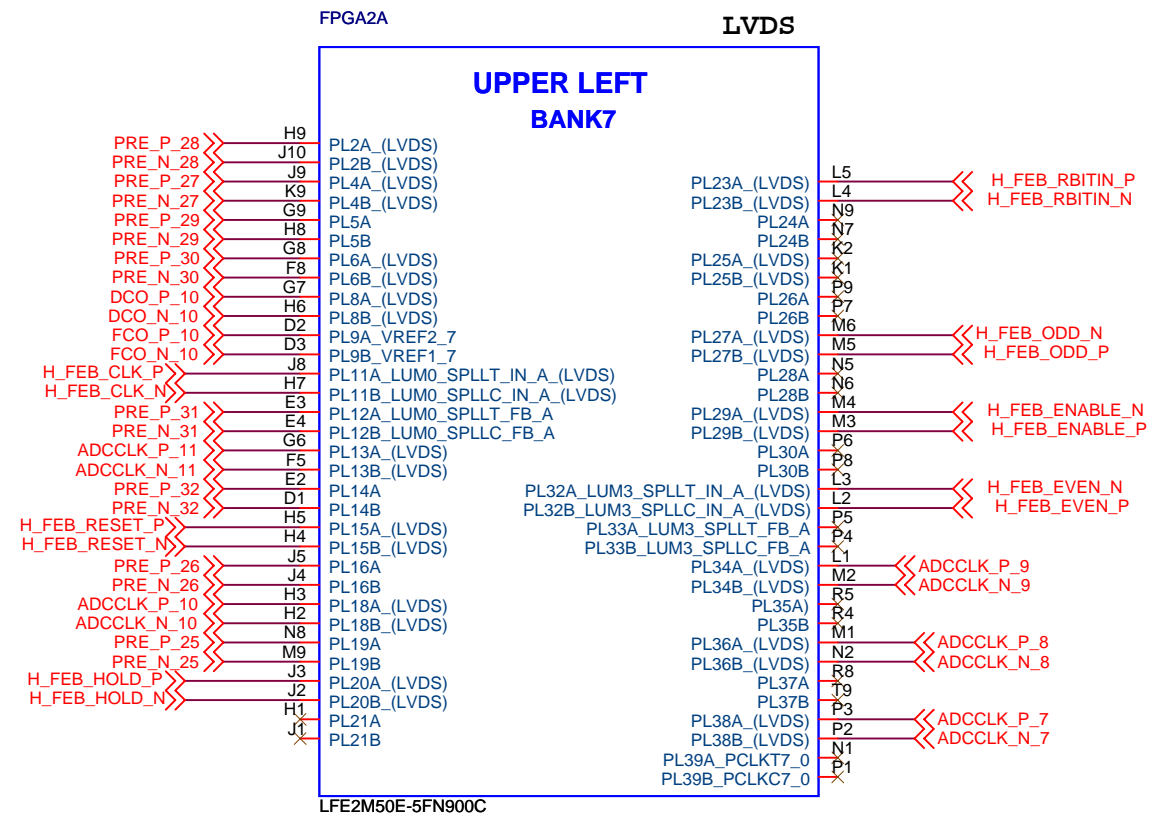
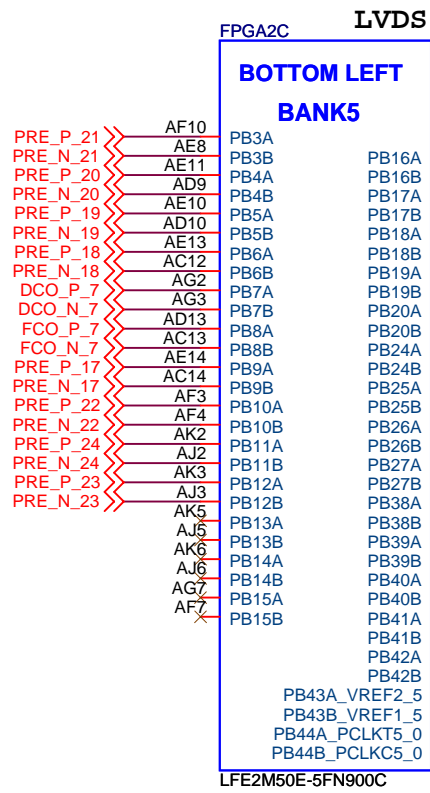
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Size	Document Number		Rev		
A4	<Doc>		<RevCo		<RevCo
Date:	Tuesday, January 26, 2010		Sheet	8	of 35

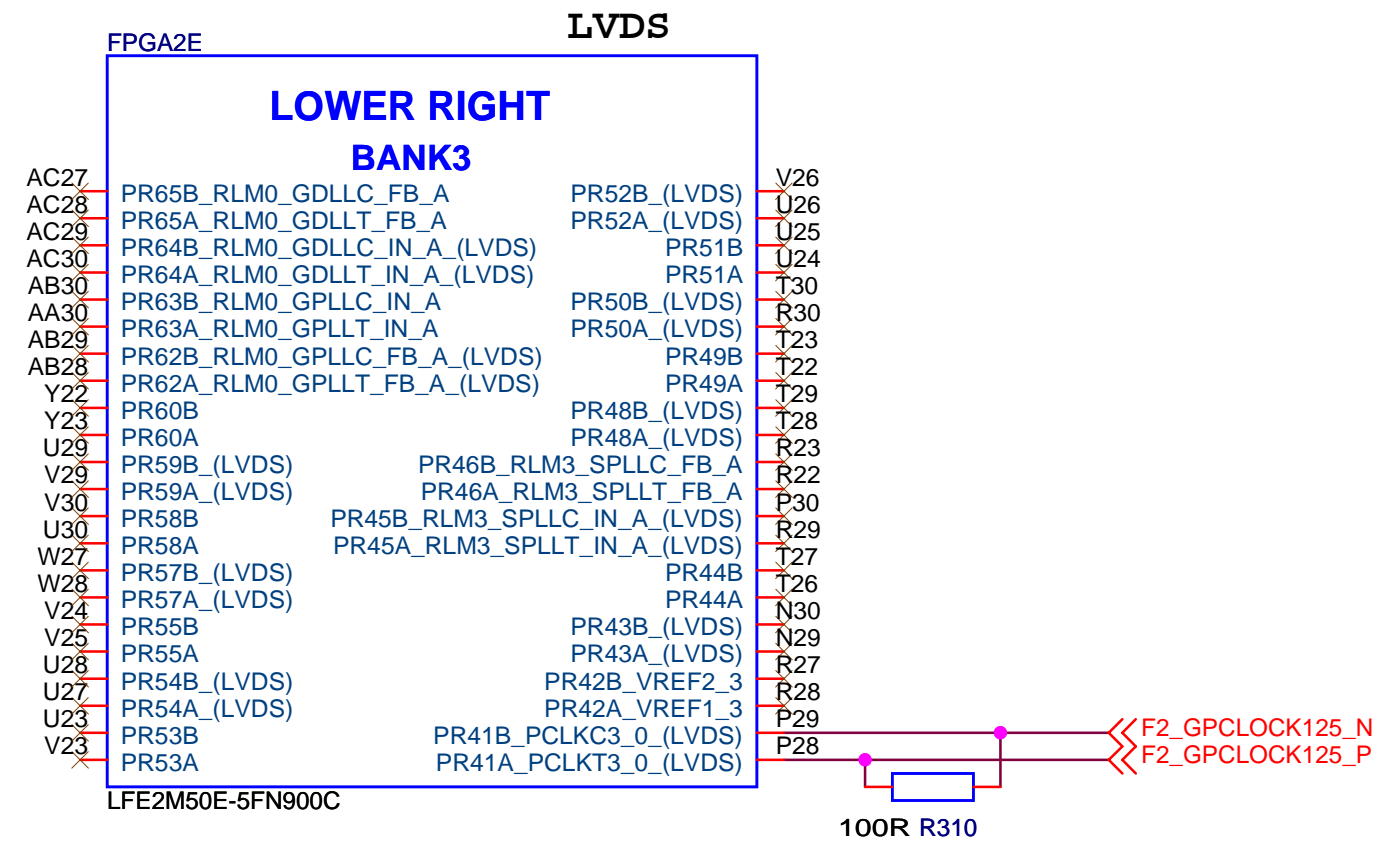
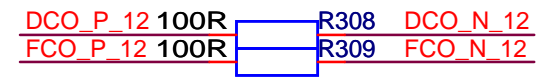
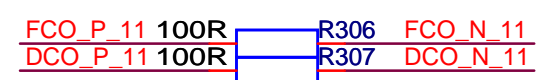
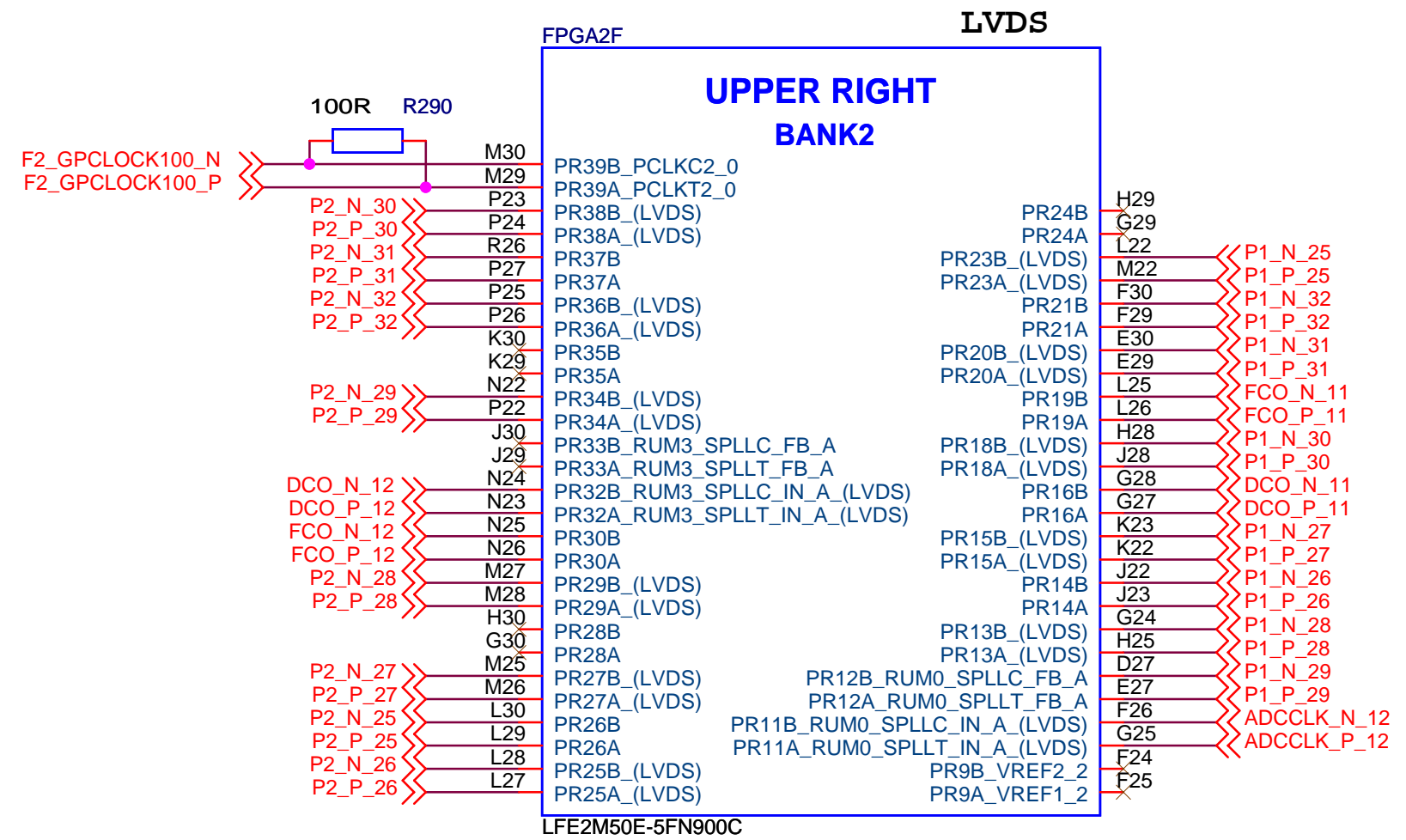




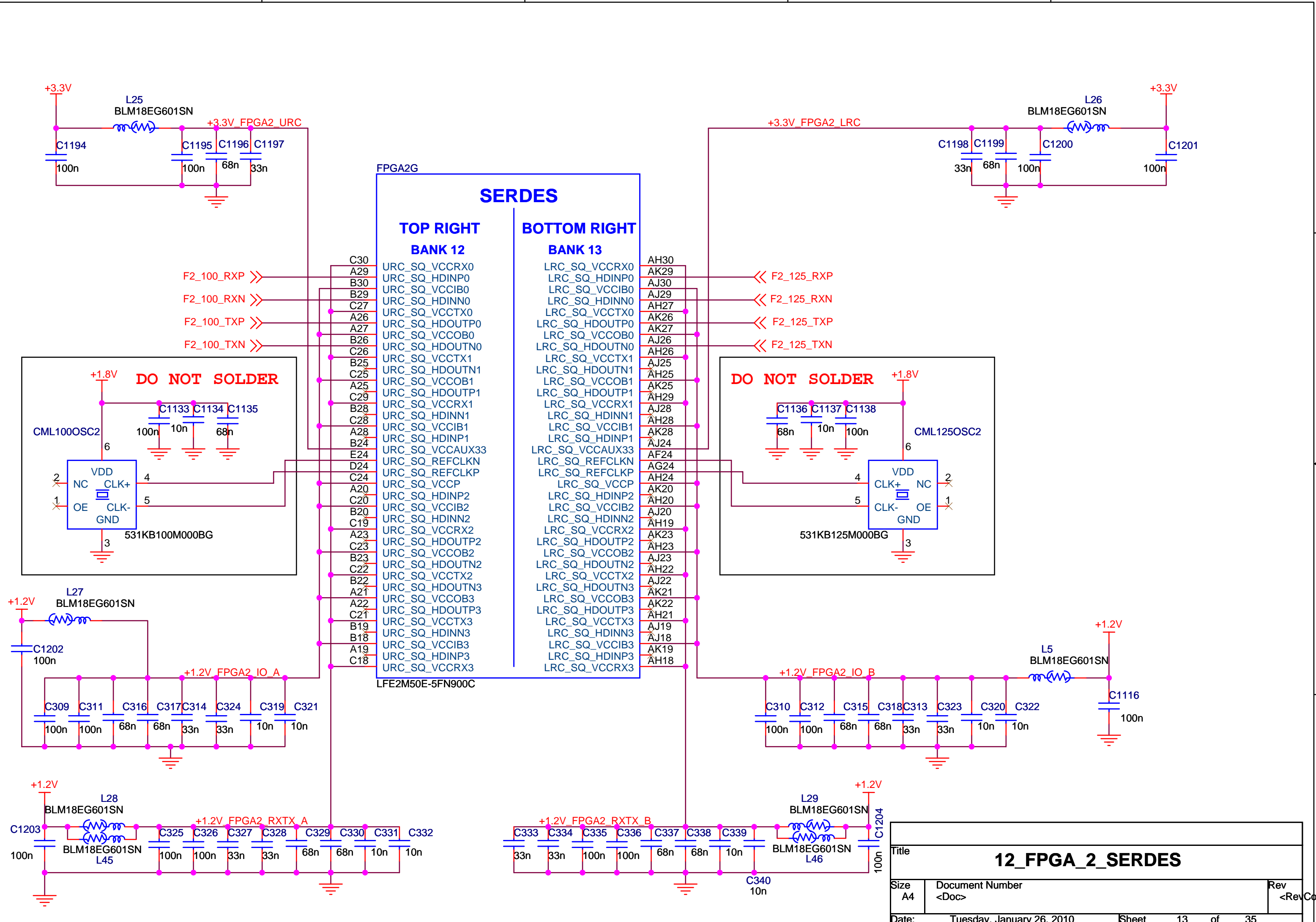
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<b>Title</b>		
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<b>Size</b>	<b>Document Number</b>	<b>Rev</b>
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<b>Date:</b> Tuesday, January 26, 2010		<b>Sheet</b> 12 <b>of</b> 35



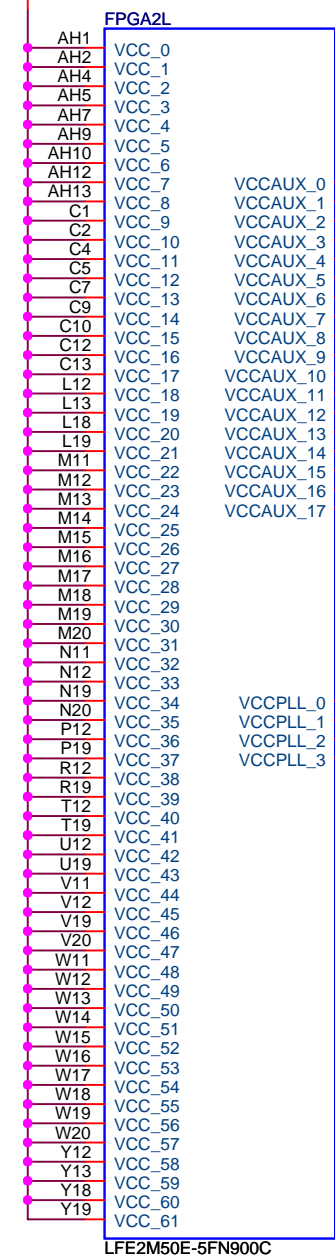
**SERDES**

TOP RIGHT BANK 12		BOTTOM RIGHT BANK 13	
C30	URC_SQ_VCCRX0	AH30	LRC_SQ_VCCRX0
A29	URC_SQ_HDINP0	AK29	LRC_SQ_HDINP0
B30	URC_SQ_VCCIB0	AJ30	LRC_SQ_VCCIB0
B29	URC_SQ_HDINN0	AJ29	LRC_SQ_HDINN0
C27	URC_SQ_VCCTX0	AH27	LRC_SQ_VCCTX0
A26	URC_SQ_HDOUTP0	AK26	LRC_SQ_HDOUTP0
A27	URC_SQ_VCCOB0	AK27	LRC_SQ_VCCOB0
B26	URC_SQ_HDOUTN0	AJ26	LRC_SQ_HDOUTN0
C26	URC_SQ_VCCTX1	AH26	LRC_SQ_VCCTX1
B25	URC_SQ_HDOUTN1	AJ25	LRC_SQ_HDOUTN1
C25	URC_SQ_VCCOB1	AH25	LRC_SQ_VCCOB1
A25	URC_SQ_HDOUTP1	AK25	LRC_SQ_HDOUTP1
C29	URC_SQ_VCCRX1	AH29	LRC_SQ_VCCRX1
B28	URC_SQ_HDINN1	AJ28	LRC_SQ_HDINN1
C28	URC_SQ_VCCIB1	AH28	LRC_SQ_VCCIB1
A28	URC_SQ_HDINP1	AK28	LRC_SQ_HDINP1
B24	URC_SQ_VCCAUX33	AJ24	LRC_SQ_VCCAUX33
E24	URC_SQ_REFCLKN	AF24	LRC_SQ_REFCLKN
D24	URC_SQ_REFCLKP	AG24	LRC_SQ_REFCLKP
C24	URC_SQ_VCCP	AH24	LRC_SQ_VCCP
A20	URC_SQ_HDINP2	AK20	LRC_SQ_HDINP2
C20	URC_SQ_VCCIB2	AH20	LRC_SQ_VCCIB2
B20	URC_SQ_HDINN2	AJ20	LRC_SQ_HDINN2
C19	URC_SQ_VCCRX2	AH19	LRC_SQ_VCCRX2
A23	URC_SQ_HDOUTP2	AK23	LRC_SQ_HDOUTP2
C23	URC_SQ_VCCOB2	AH23	LRC_SQ_VCCOB2
B23	URC_SQ_HDOUTN2	AJ23	LRC_SQ_HDOUTN2
C22	URC_SQ_VCCTX2	AH22	LRC_SQ_VCCTX2
B22	URC_SQ_HDOUTN3	AJ22	LRC_SQ_HDOUTN3
A21	URC_SQ_VCCOB3	AK21	LRC_SQ_VCCOB3
A22	URC_SQ_HDOUTP3	AH21	LRC_SQ_HDOUTP3
C21	URC_SQ_VCCTX3	AJ19	LRC_SQ_HDINN3
B19	URC_SQ_HDINN3	AJ18	LRC_SQ_VCCIB3
B18	URC_SQ_VCCIB3	AK19	LRC_SQ_HDINP3
A19	URC_SQ_HDINP3	AH18	LRC_SQ_VCCRX3
C18	URC_SQ_VCCRX3		

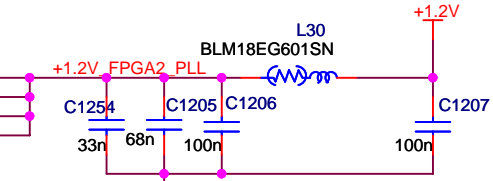
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Title			<b>12_FPGA_2_SERDES</b>		
Size	Document Number				Rev
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+1.2V

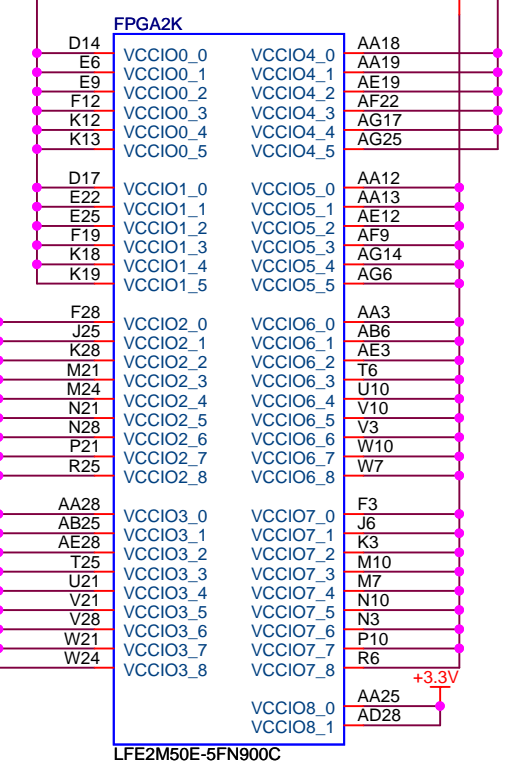


+3.3V



+3.3V

+2.5V

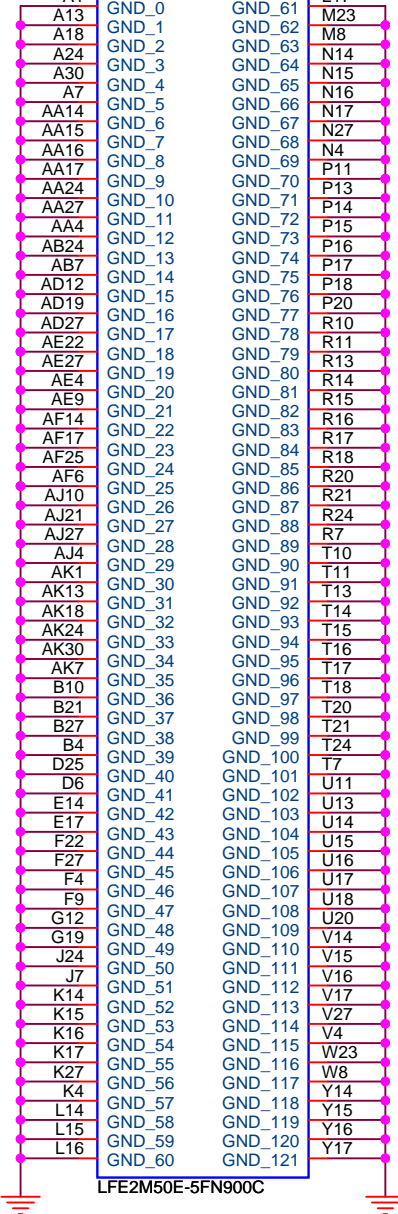


+3.3V

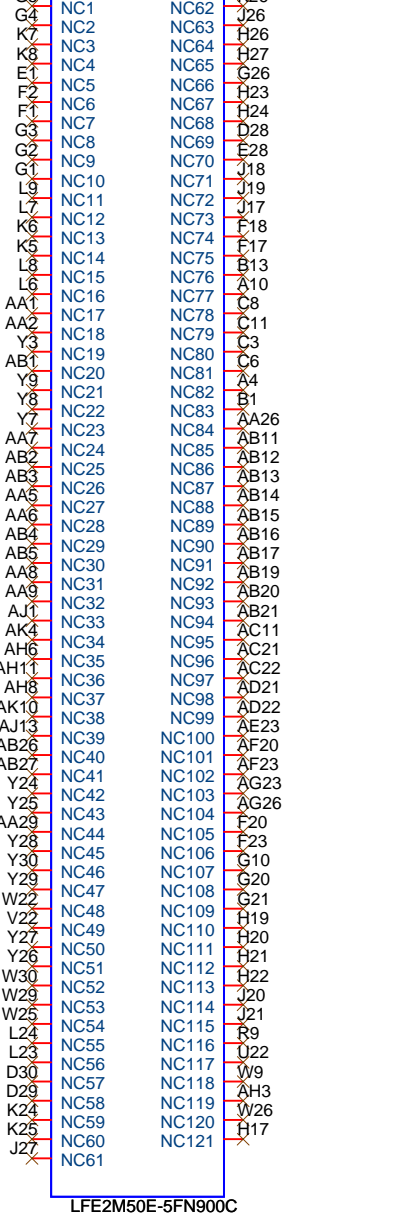
+2.5V

+3.3V

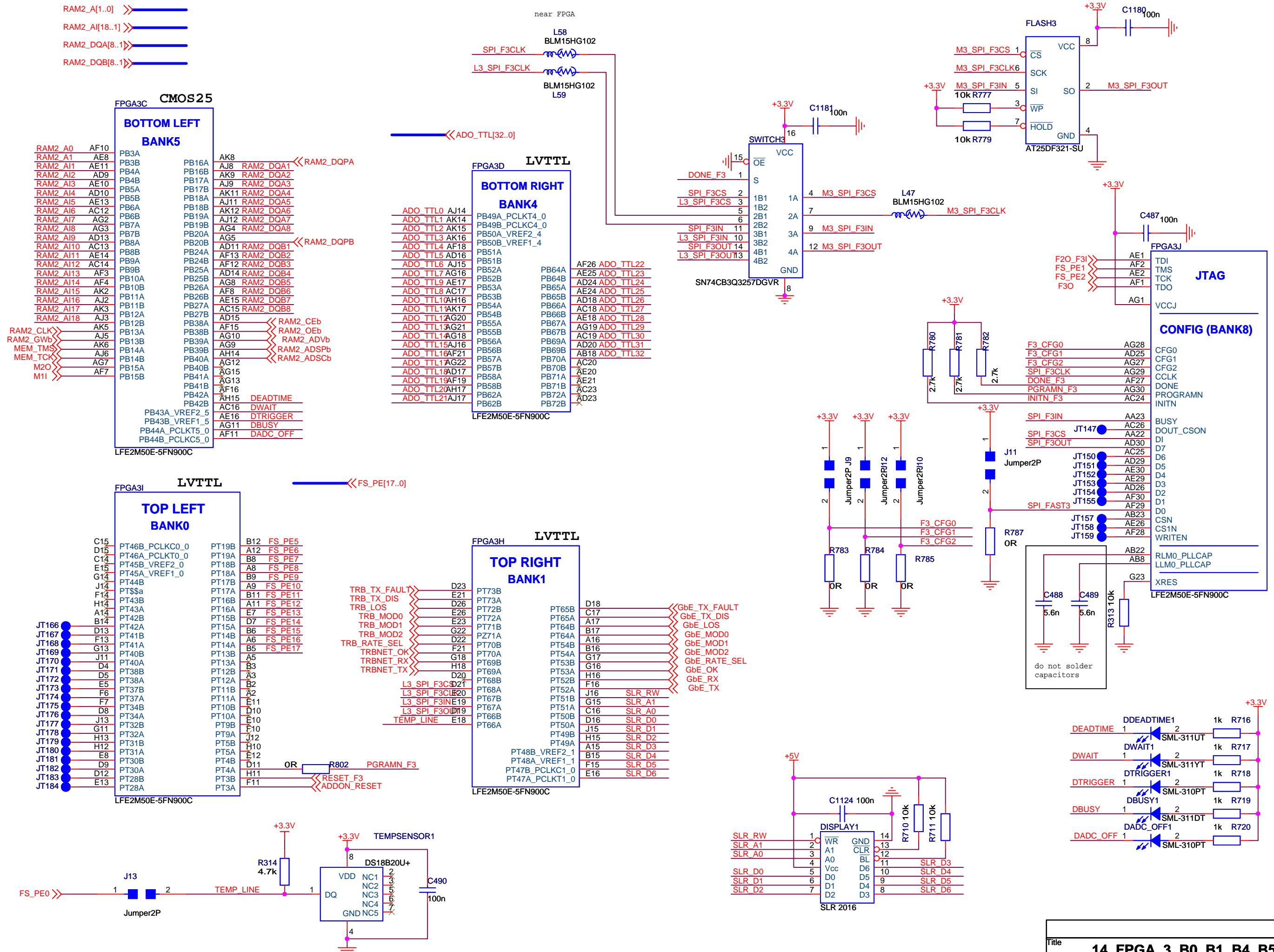
FPGA2M

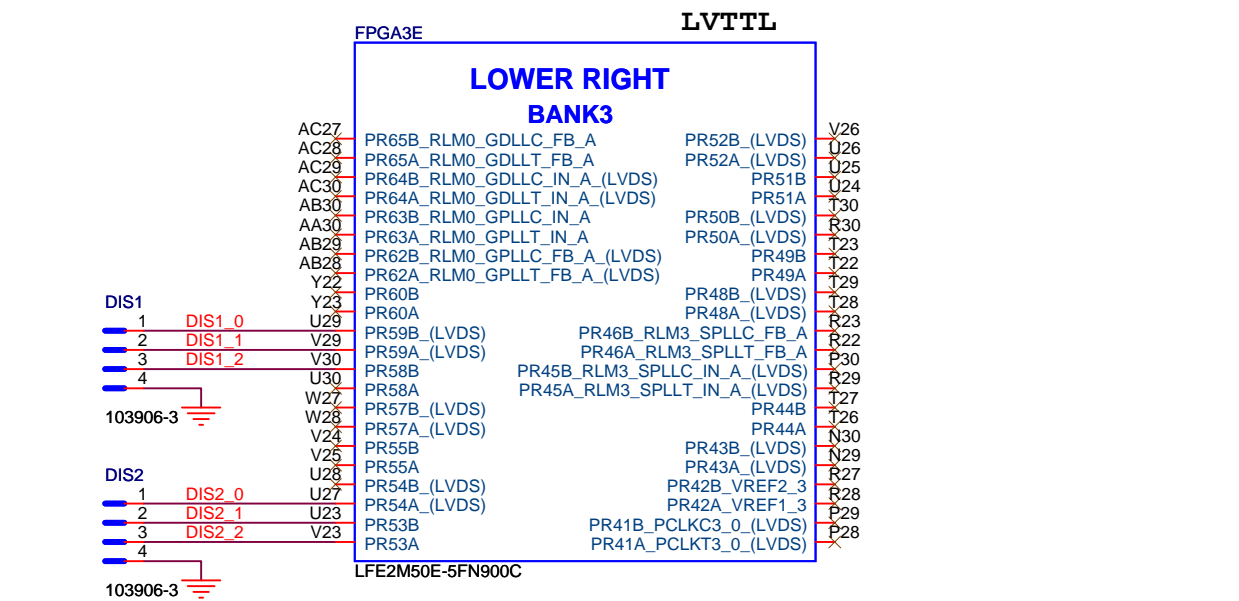
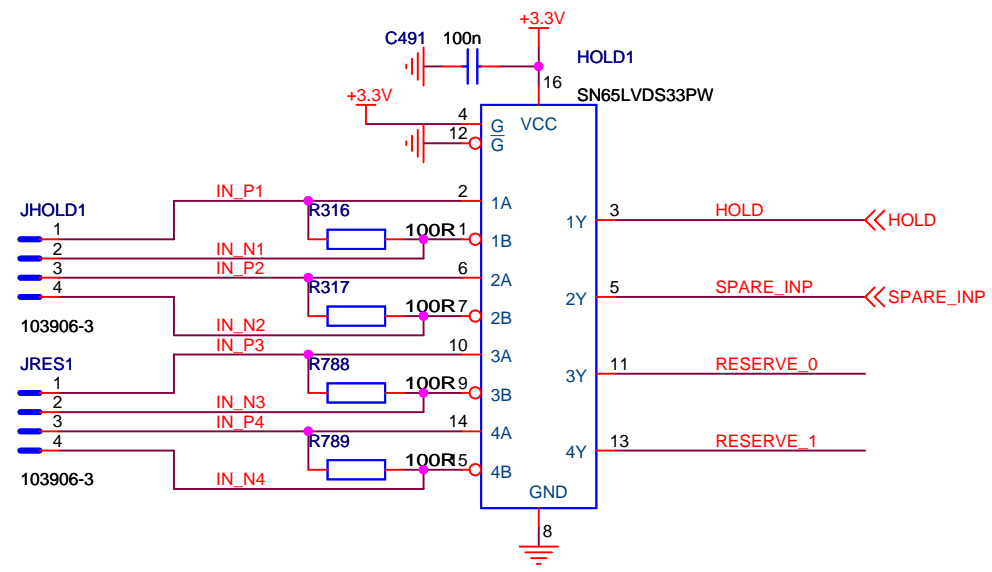
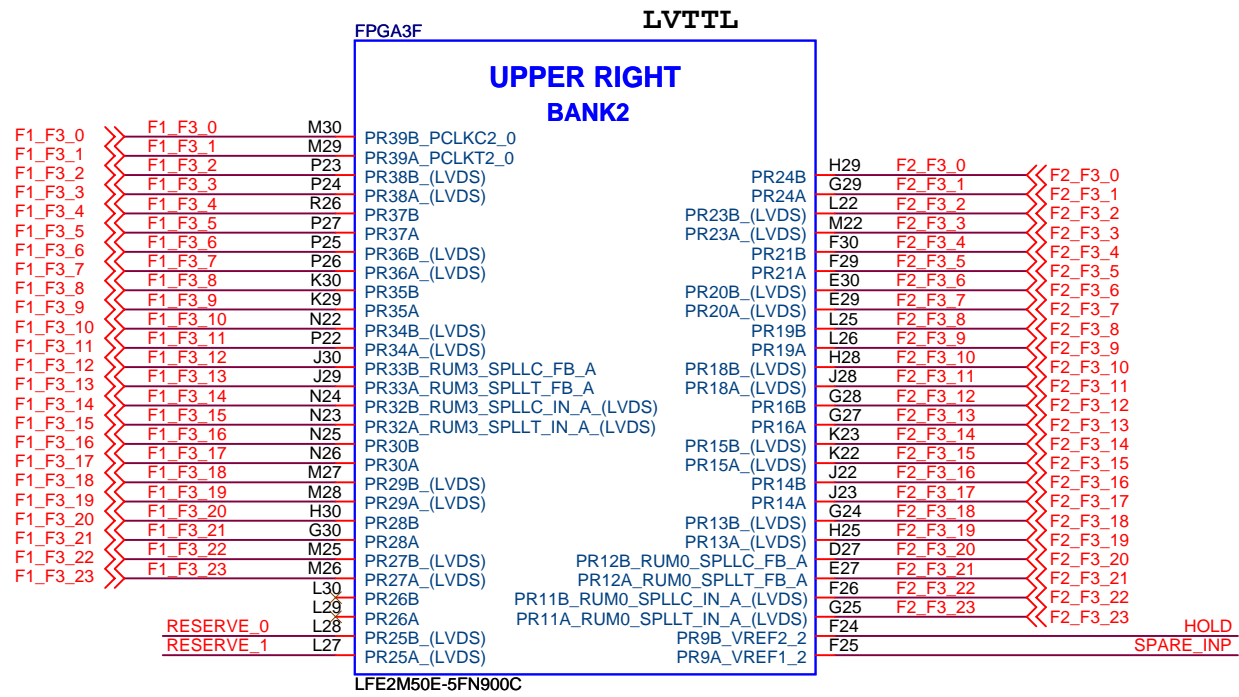


FPGA2N



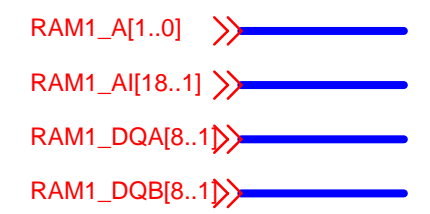
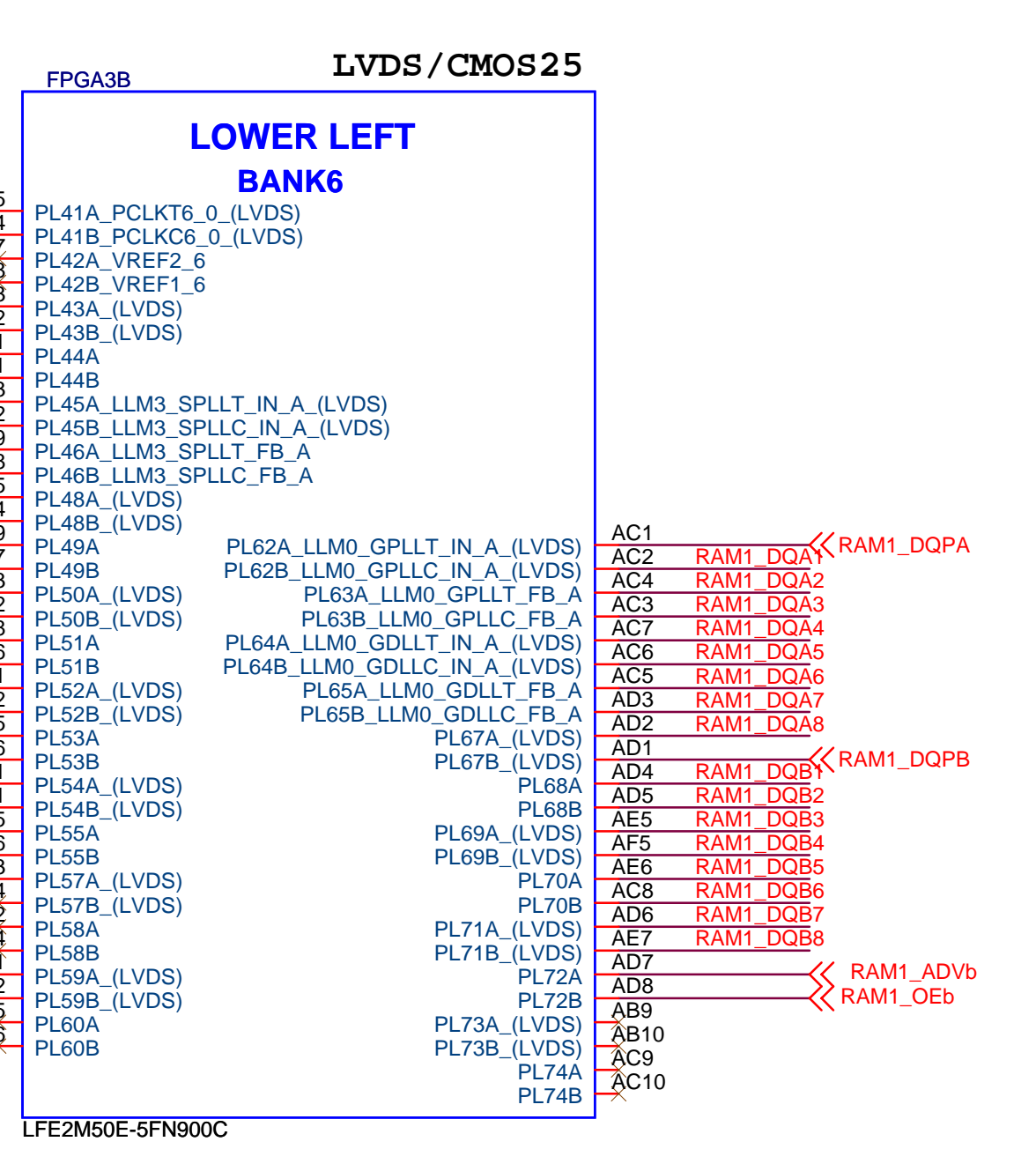
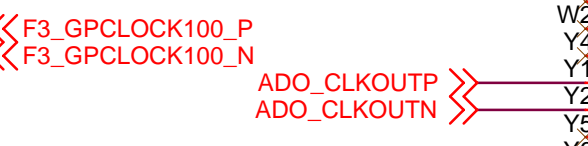
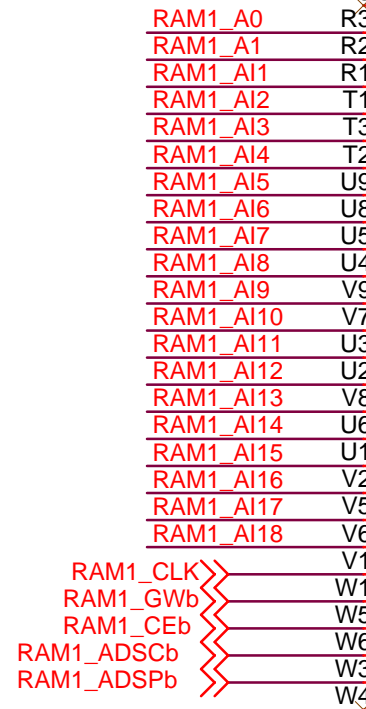
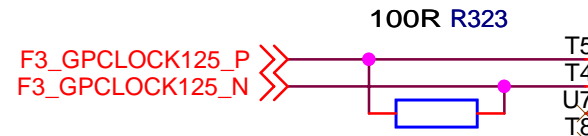
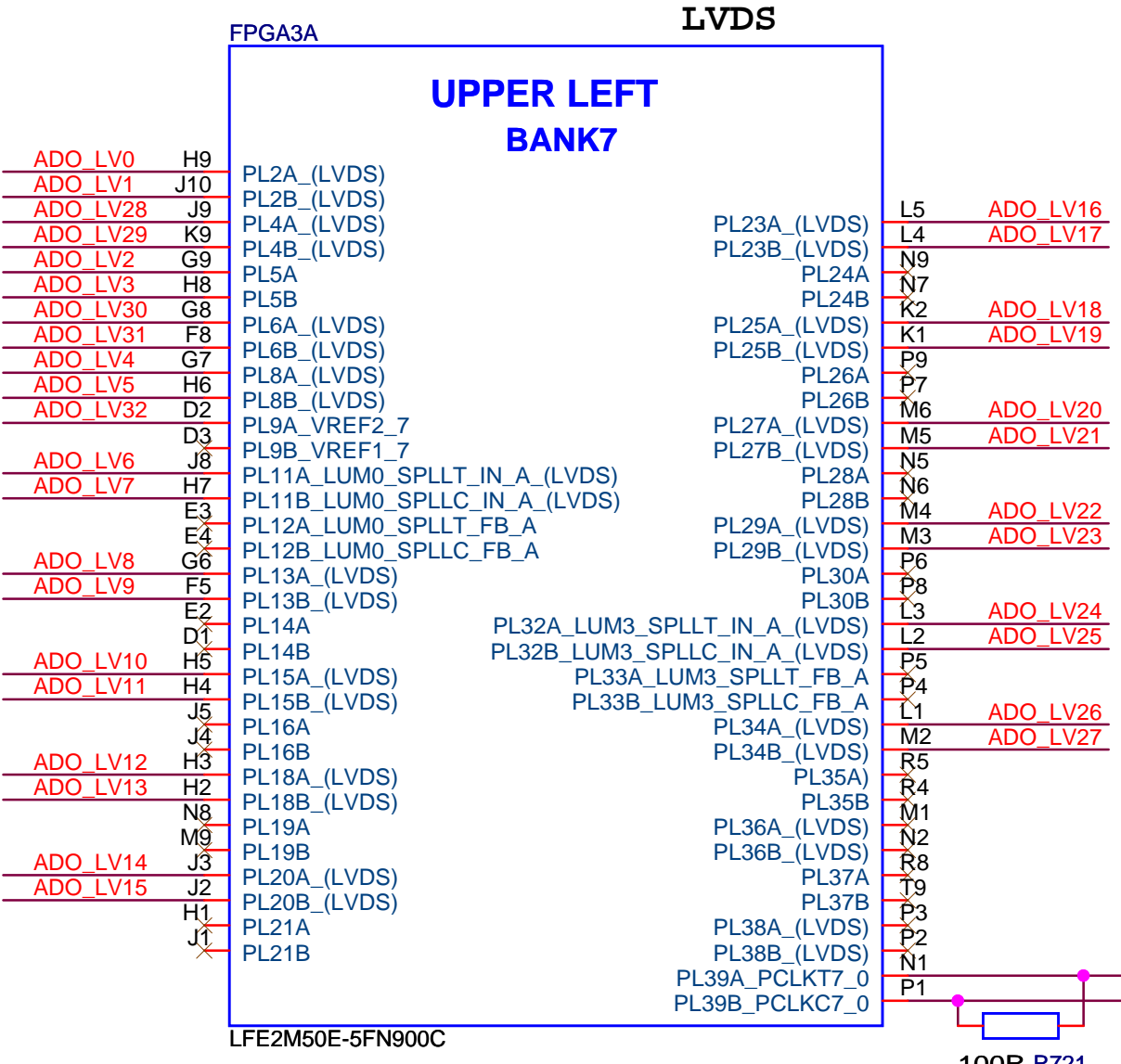
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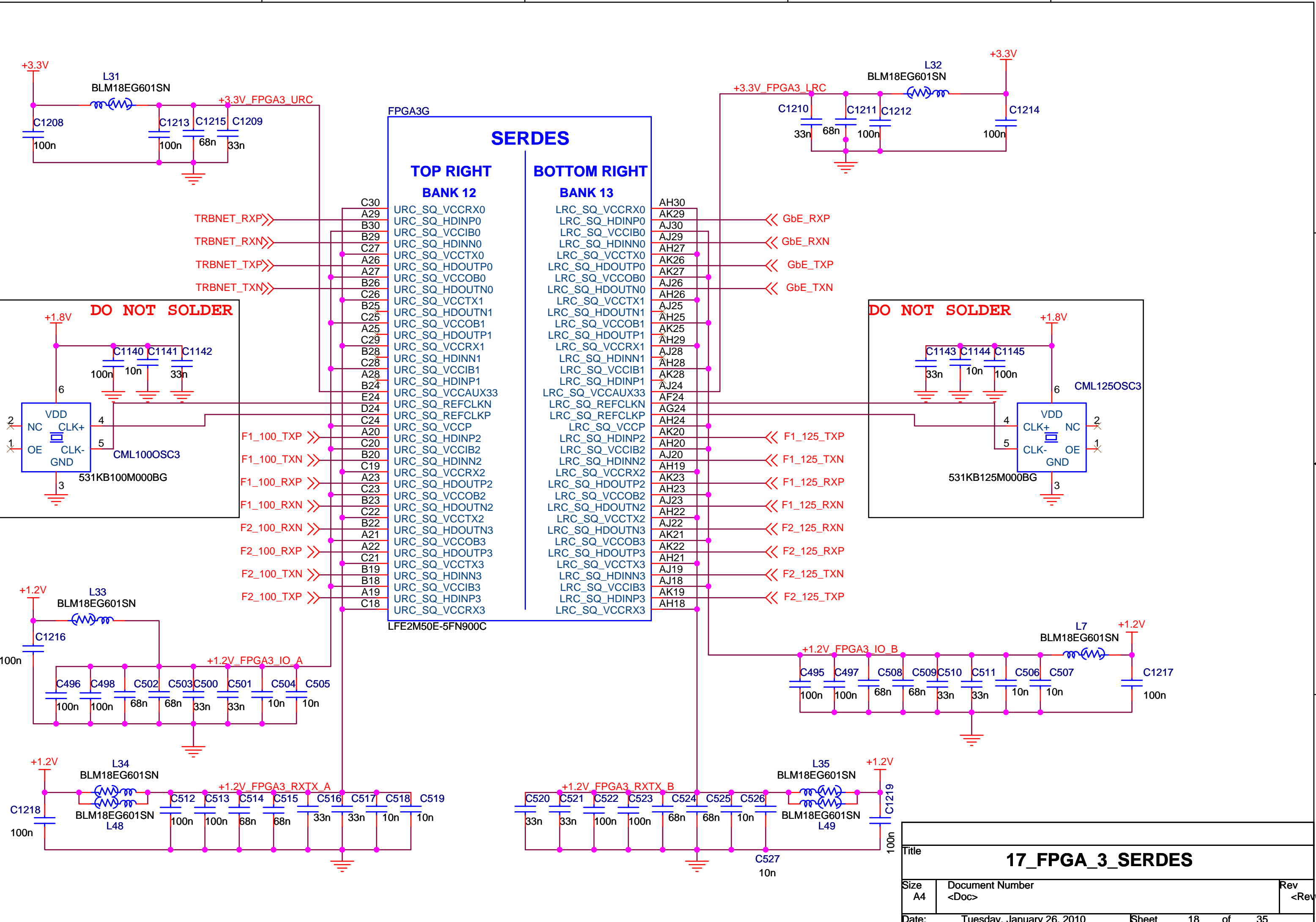




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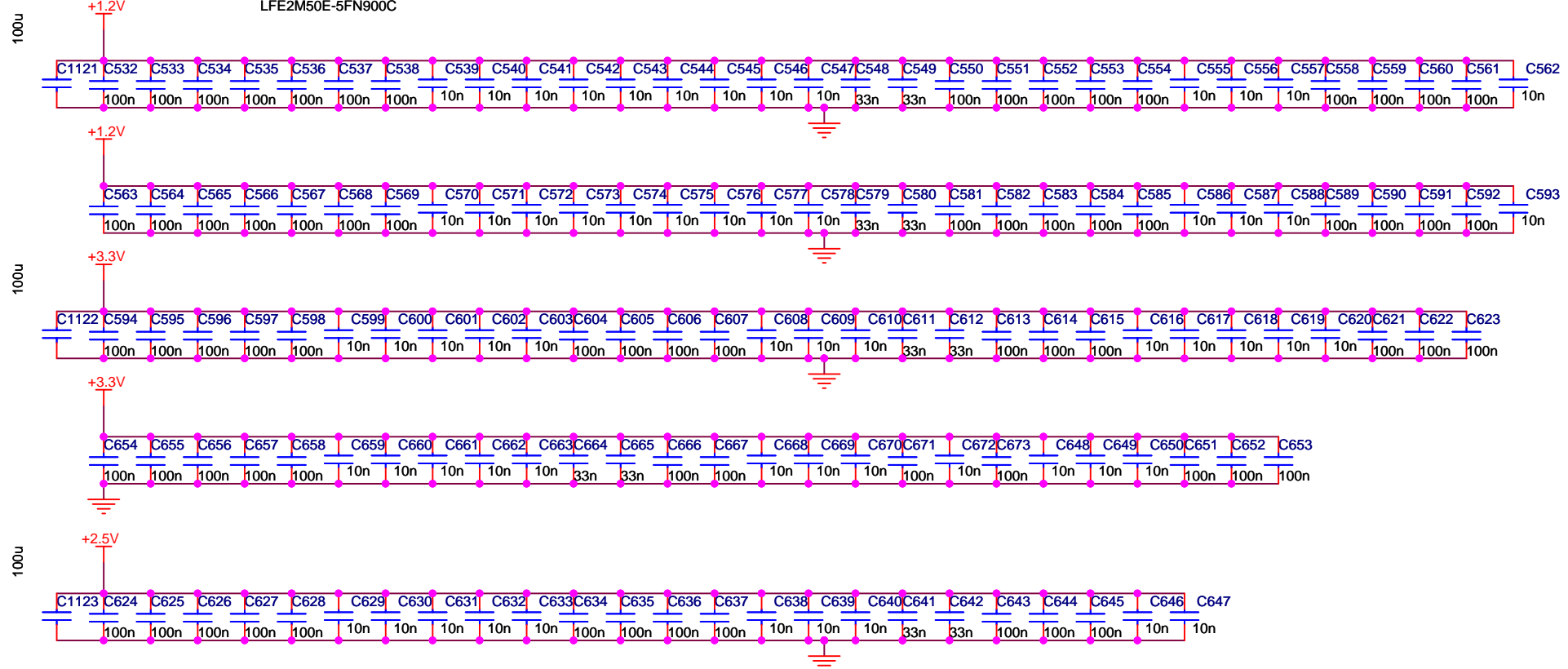
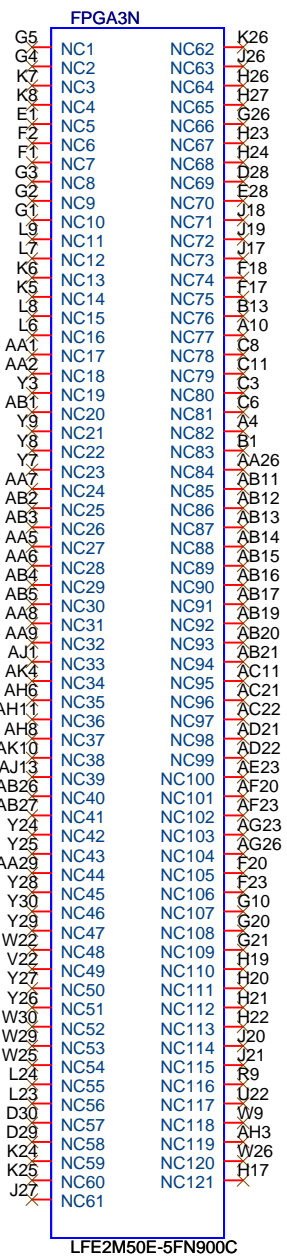
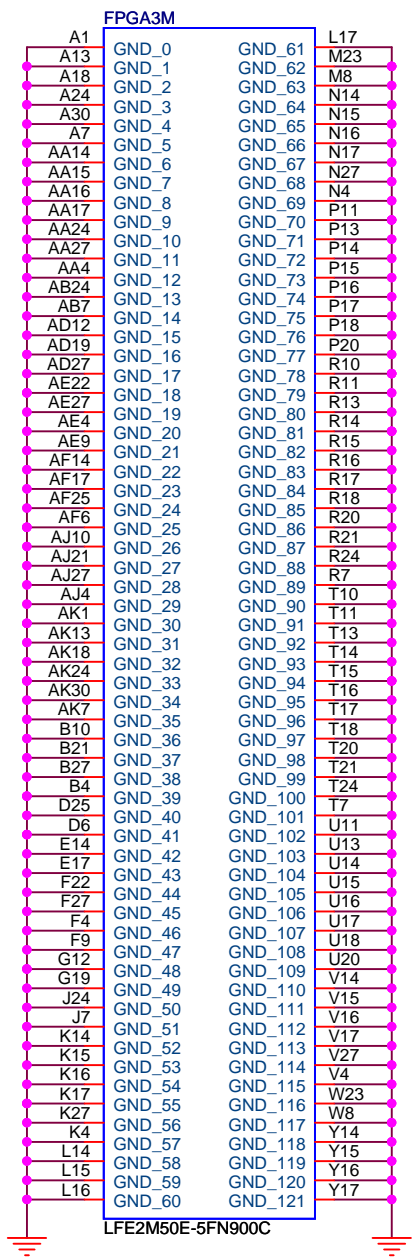
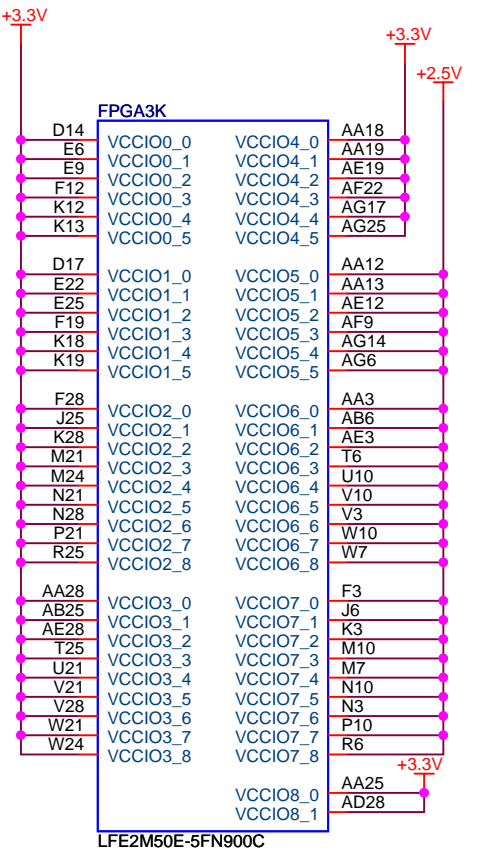
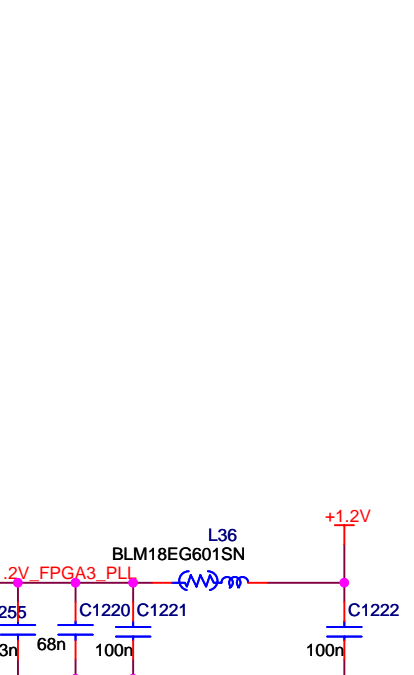
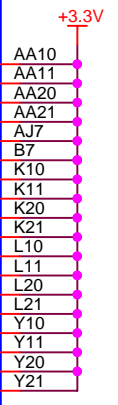
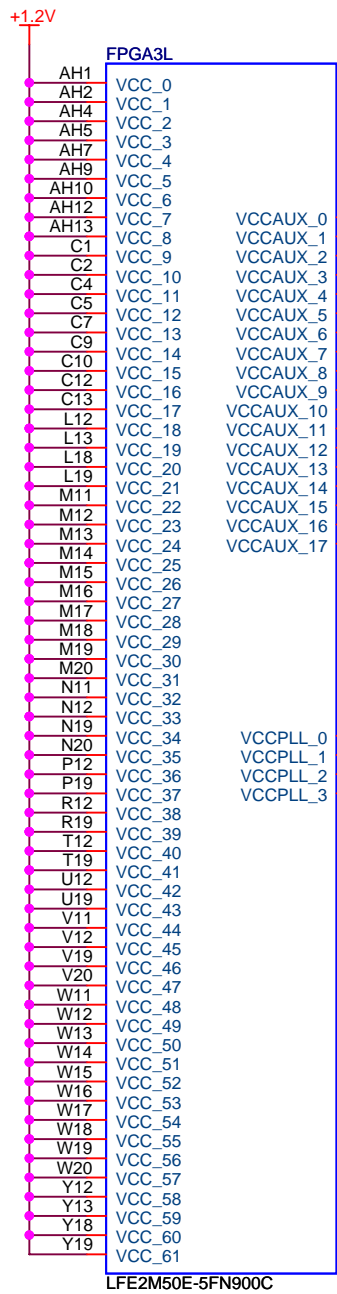
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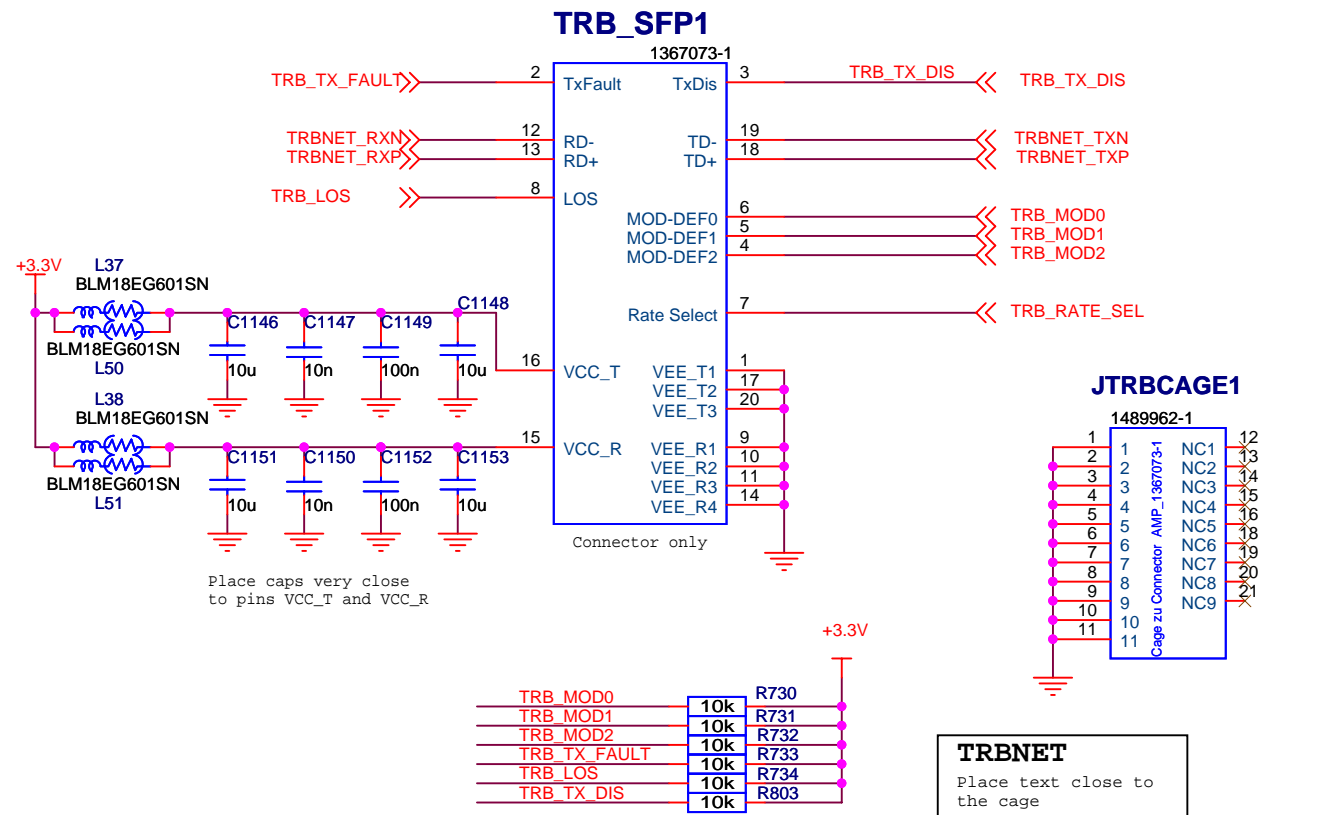


**SERDES**

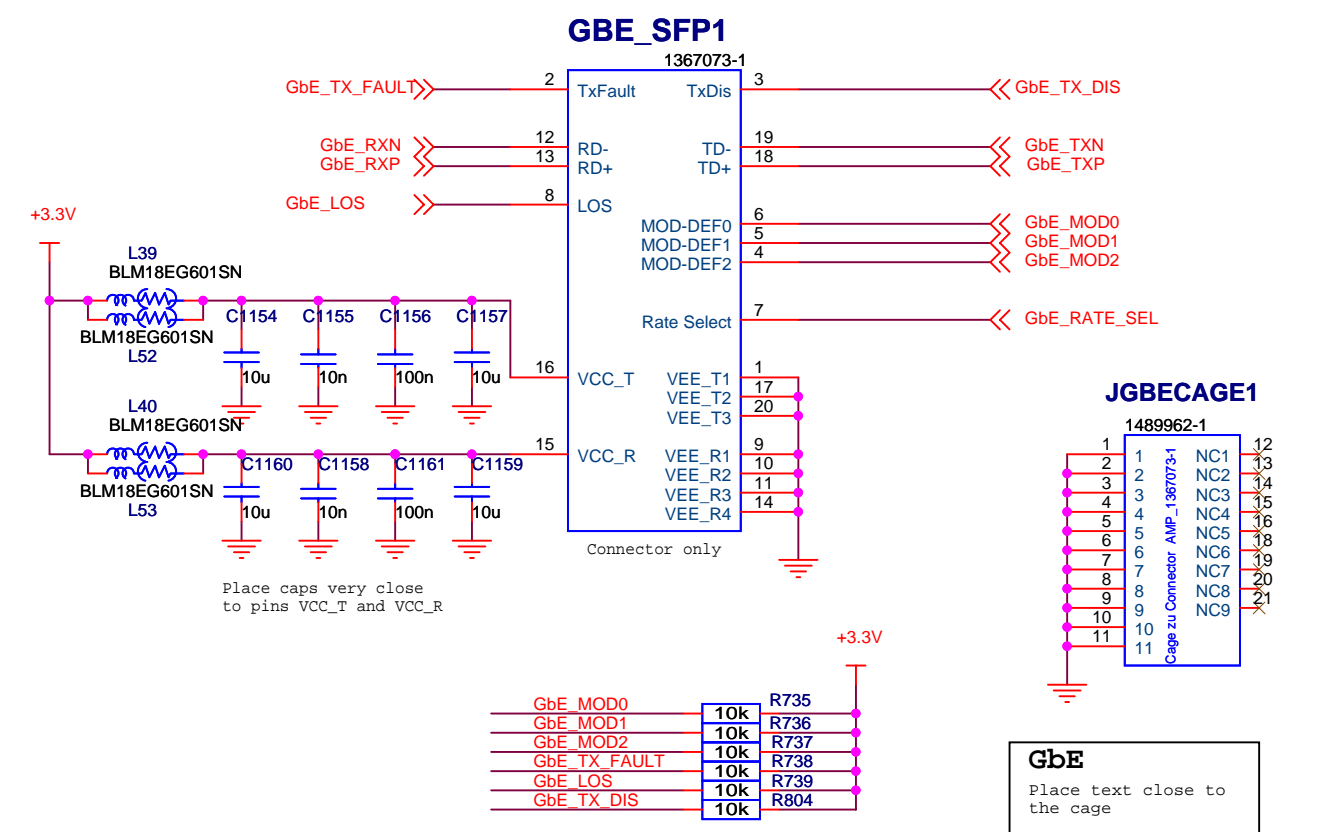
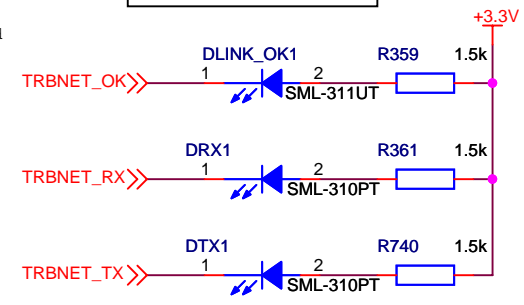
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C30	URC_SQ_VCCR0	AH30	
A29	URC_SQ_HDINP0	AK29	← GbE_RXP
B30	URC_SQ_VCCIB0	AJ30	← GbE_RXN
B29	URC_SQ_HDINN0	AH29	
C27	URC_SQ_VCCTX0	AK26	← GbE_TXP
A26	URC_SQ_HDOU0	AK27	← GbE_TXN
A27	URC_SQ_VCCOB0	AJ26	
B26	URC_SQ_HDOU1	AH26	
C26	URC_SQ_VCCTX1	AJ25	
B25	URC_SQ_HDOU2	AH25	
C25	URC_SQ_VCCOB1	AK25	
A25	URC_SQ_HDOU3	AH29	
C29	URC_SQ_VCCR1	AJ28	
B28	URC_SQ_HDINN1	AH28	
C28	URC_SQ_VCCIB1	AK28	
A28	URC_SQ_HDINP1	AK28	
B24	URC_SQ_HDINP33	AJ24	
E24	URC_SQ_VCCAUX33	AF24	
D24	URC_SQ_REFCLKN	AG24	
C24	URC_SQ_REFCLKP	AH24	
A20	URC_SQ_VCCP	AK20	← F1_125_TXP
C20	URC_SQ_HDINP2	AH20	← F1_125_TXN
B20	URC_SQ_VCCIB2	AJ20	← F1_125_RXN
C19	URC_SQ_HDINN2	AH19	← F1_125_RPN
A23	URC_SQ_VCCR2	AK23	← F1_125_RPN
C23	URC_SQ_HDOU2	AH23	← F1_125_RPN
B23	URC_SQ_VCCOB2	AJ23	← F1_125_RPN
C22	URC_SQ_HDOU2	AH22	← F2_125_RPN
B22	URC_SQ_VCCTX2	AJ22	← F2_125_RPN
A21	URC_SQ_HDOU3	AK21	← F2_125_RPN
A22	URC_SQ_VCCOB3	AK22	← F2_125_RPN
C21	URC_SQ_HDOU3	AH21	← F2_125_TPN
B19	URC_SQ_VCCTX3	AJ19	← F2_125_TPN
B18	URC_SQ_HDINN3	AJ18	← F2_125_TPN
A19	URC_SQ_VCCIB3	AK19	← F2_125_TPN
C18	URC_SQ_HDINP3	AH18	
	URC_SQ_VCCR3		
	URC_SQ_VCCR3		

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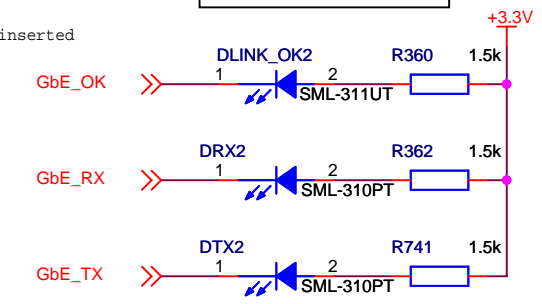


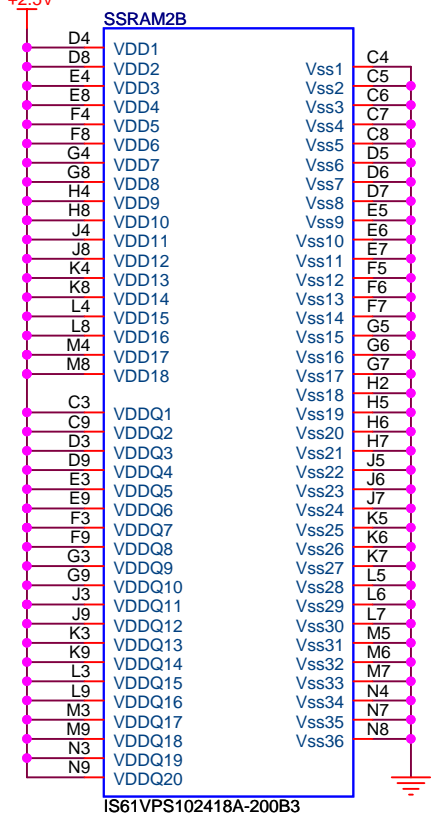
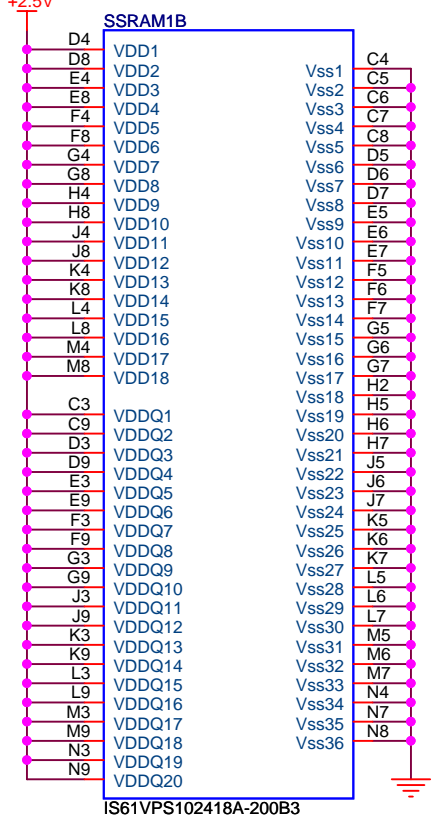
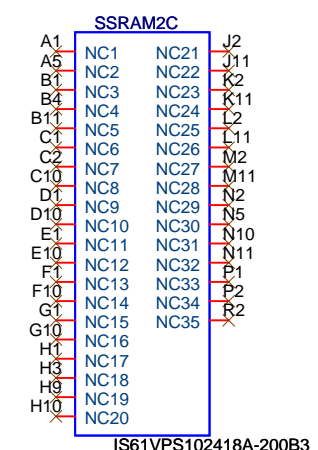
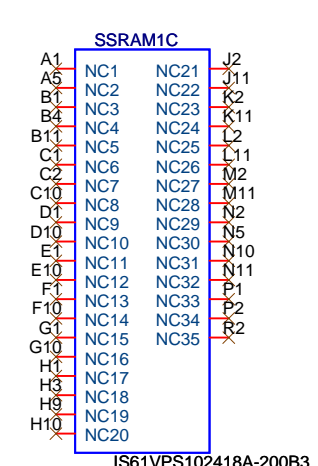
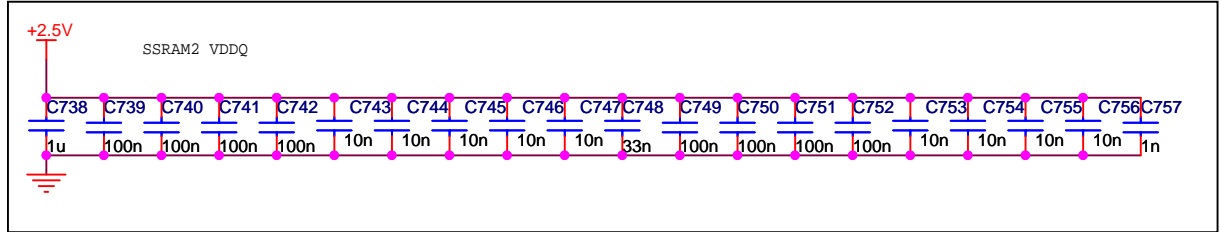
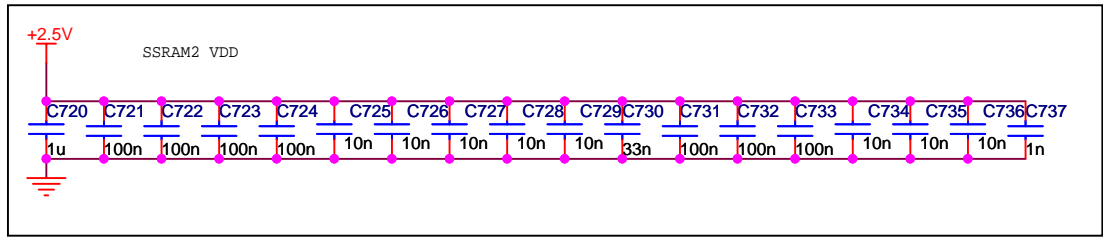
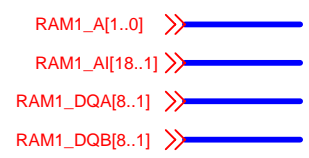
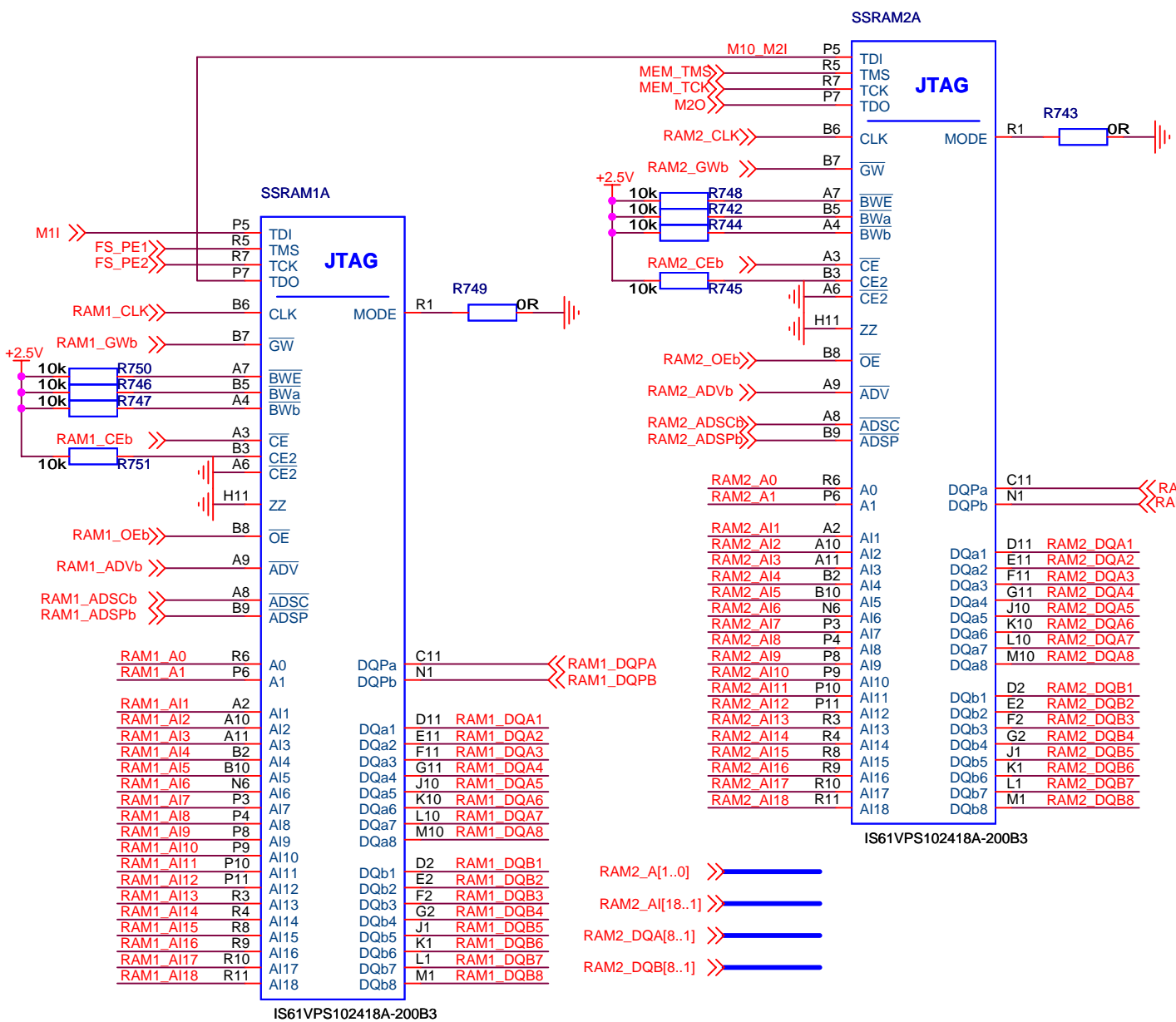
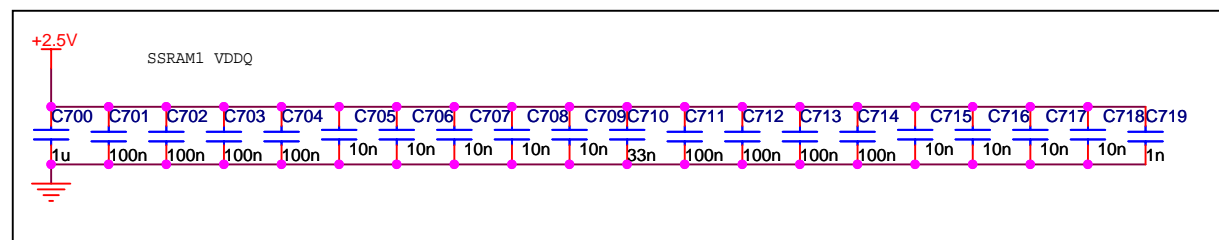
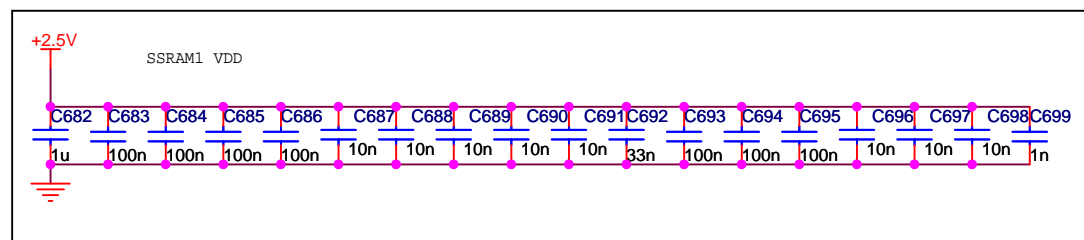


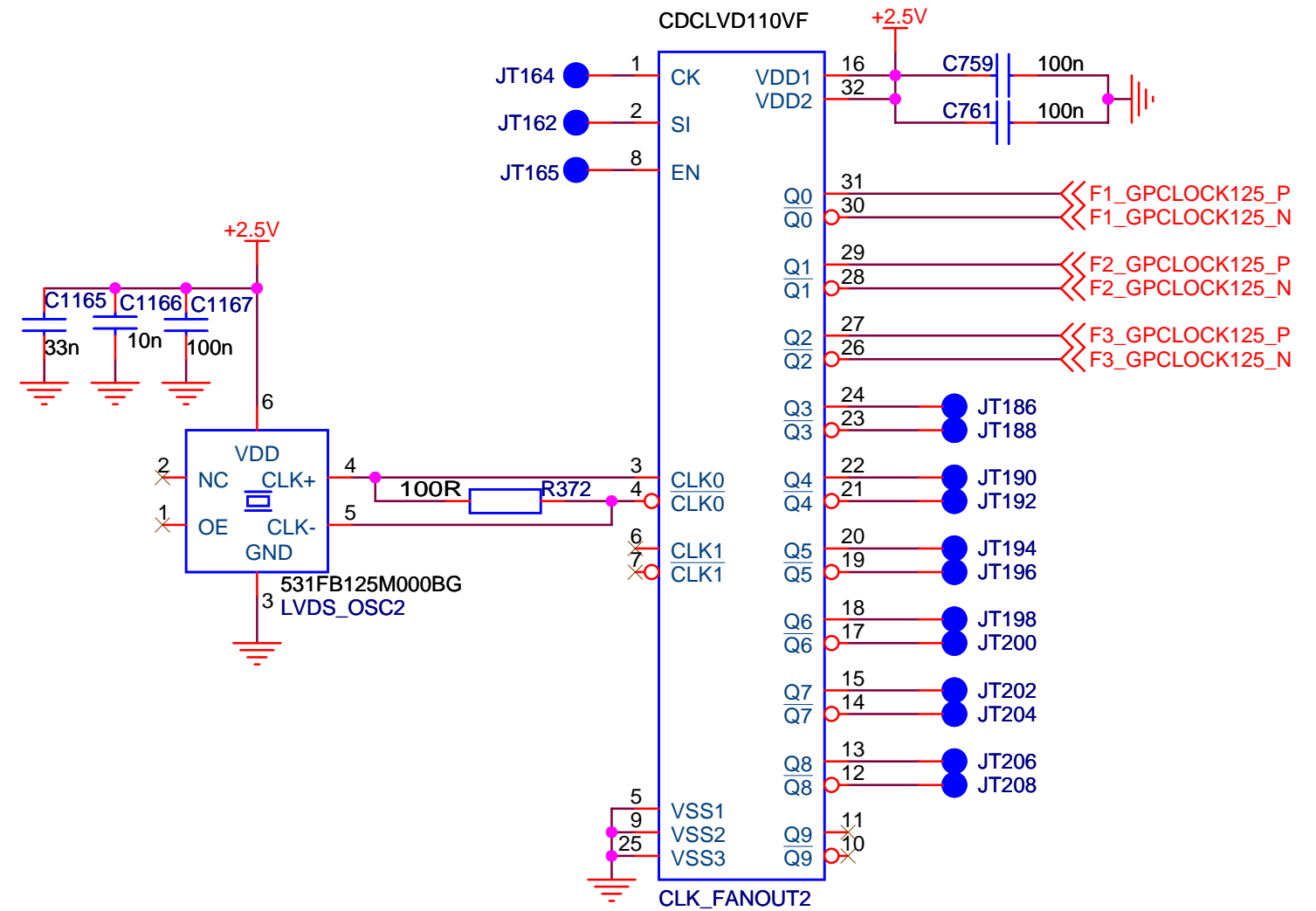
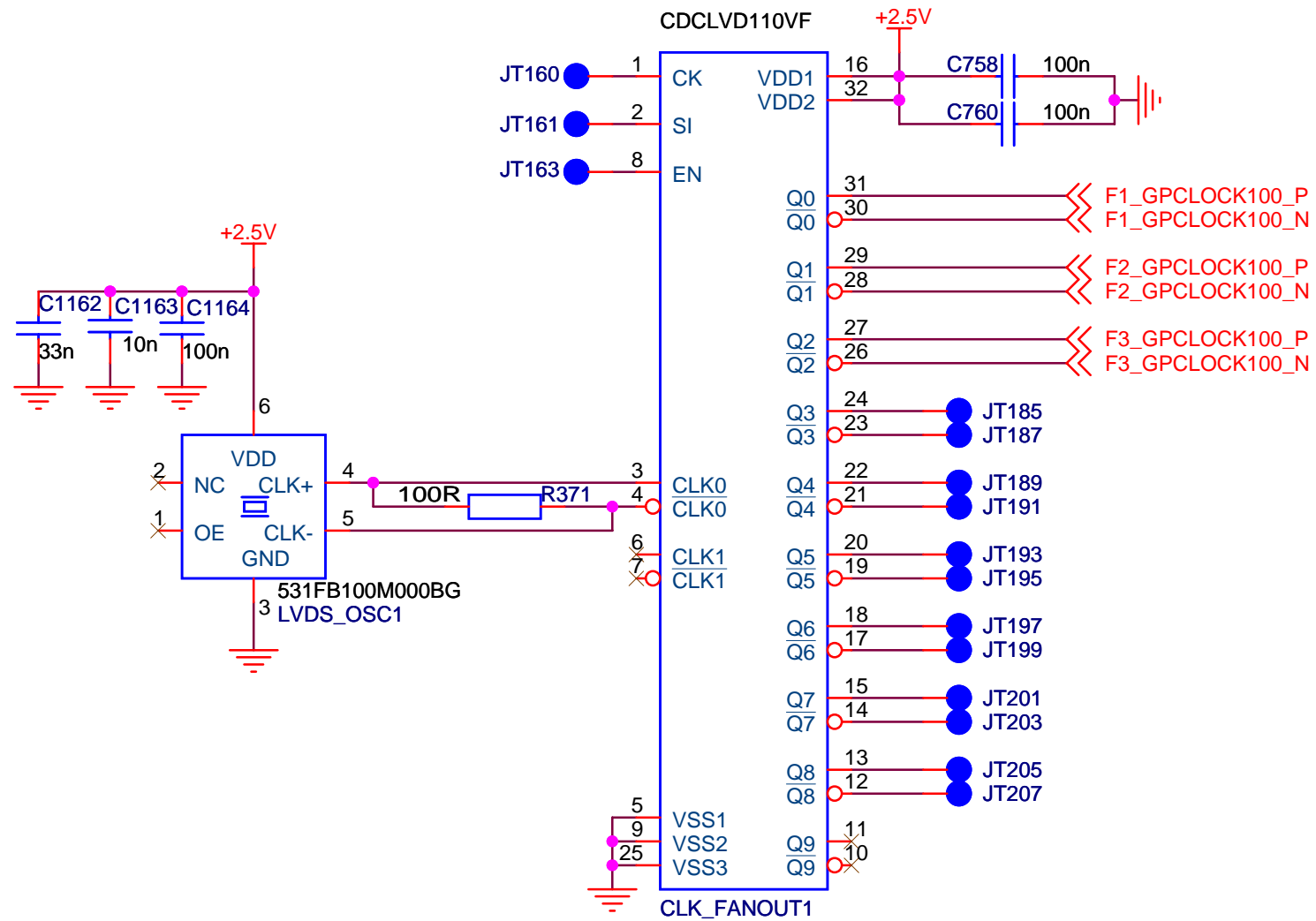
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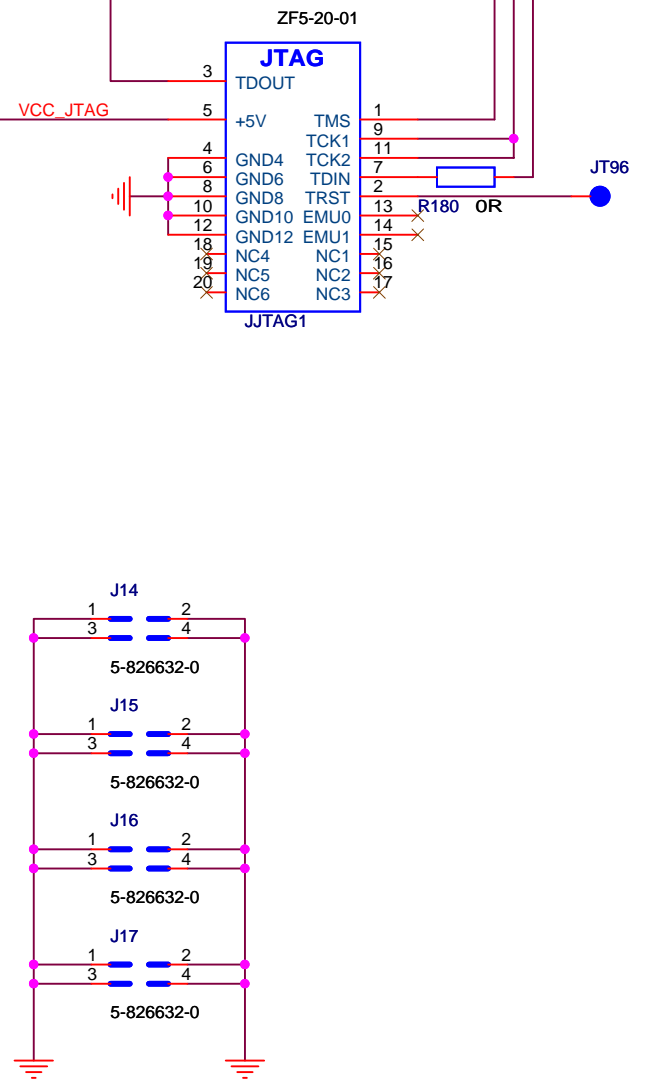
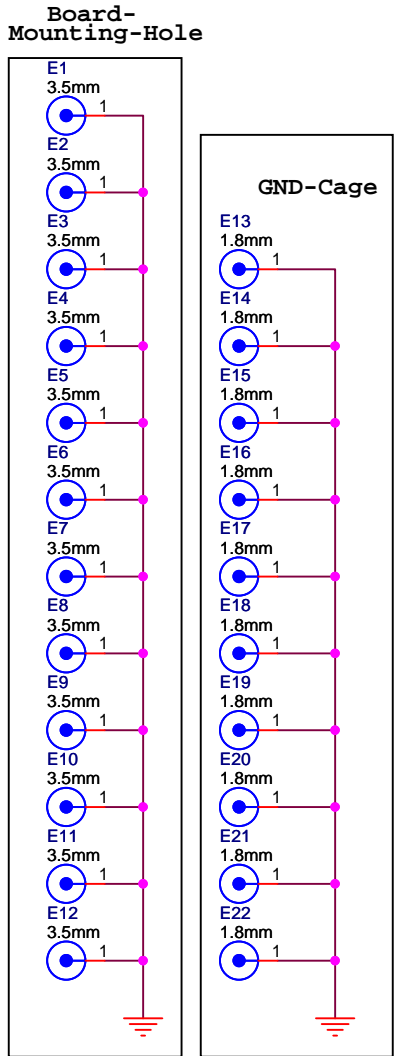
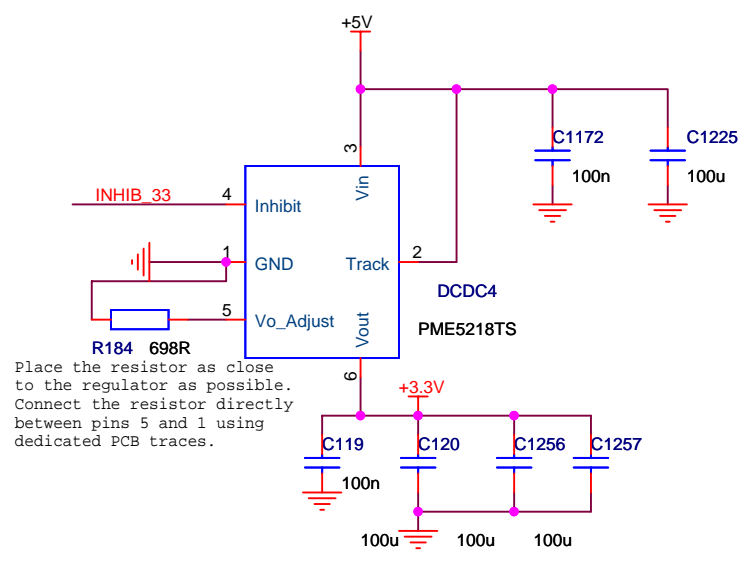
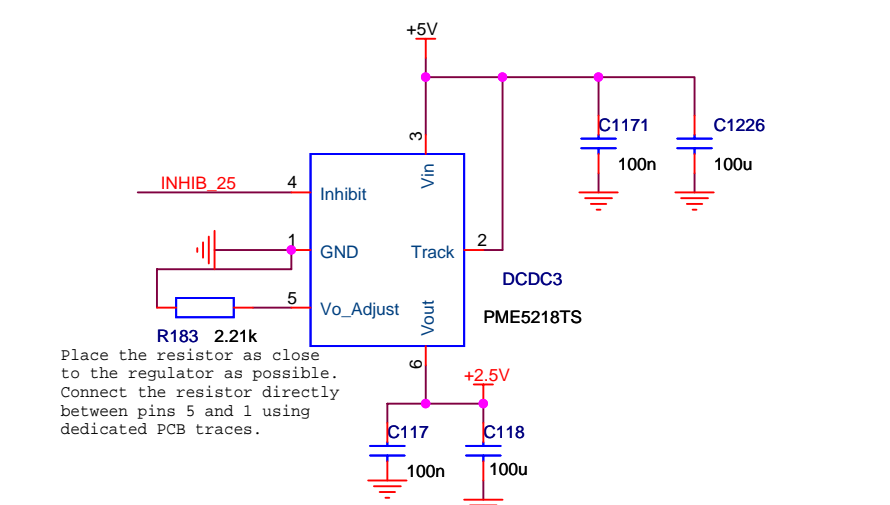
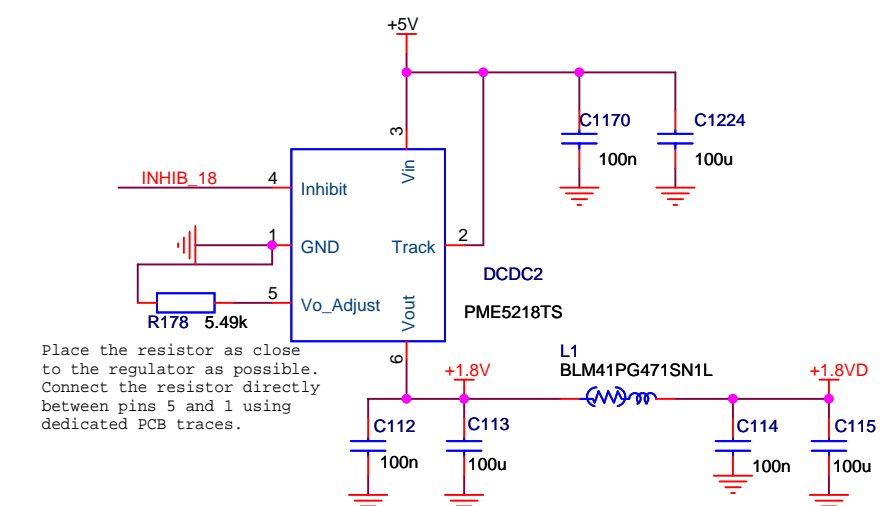
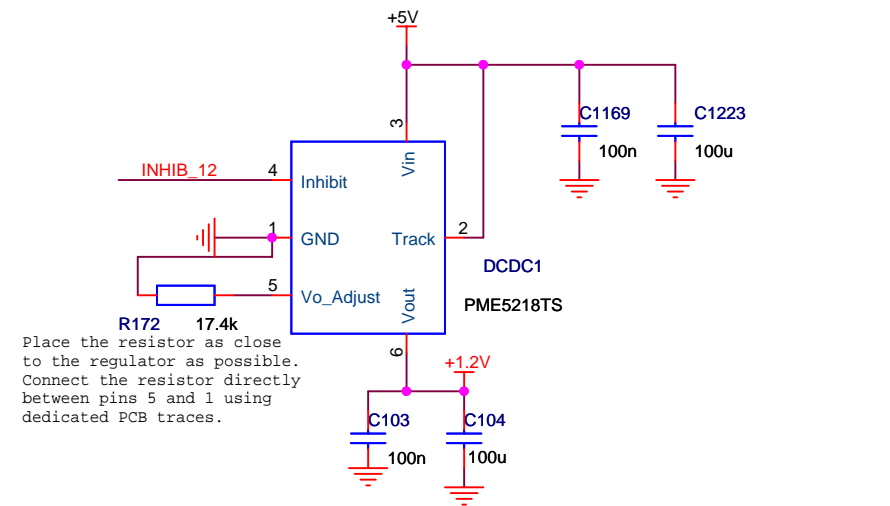
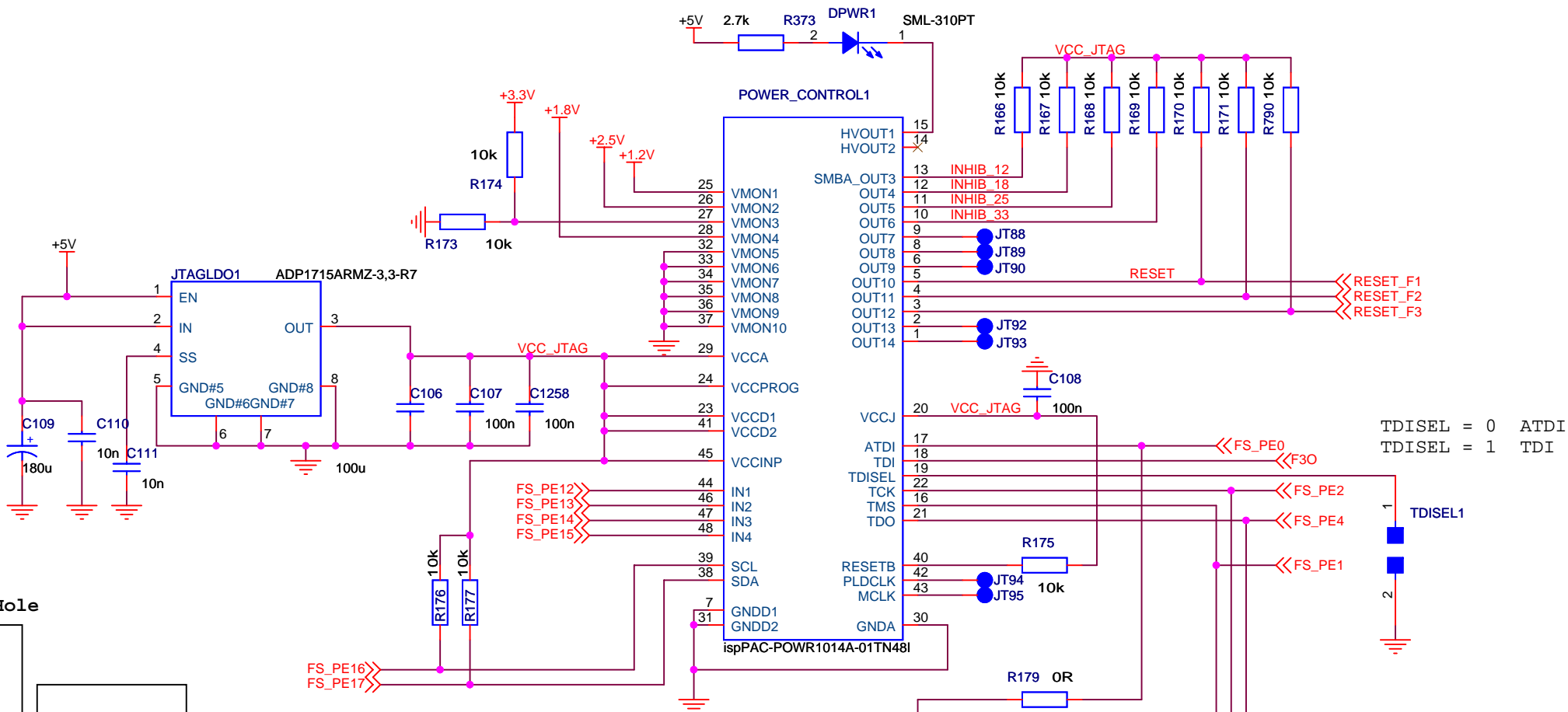
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ALL SIGNALS HERE ARE DIFFERENTIAL

LOCATE 100R RESISTOR CLOSE TO THE INPUT CONNECTOR

