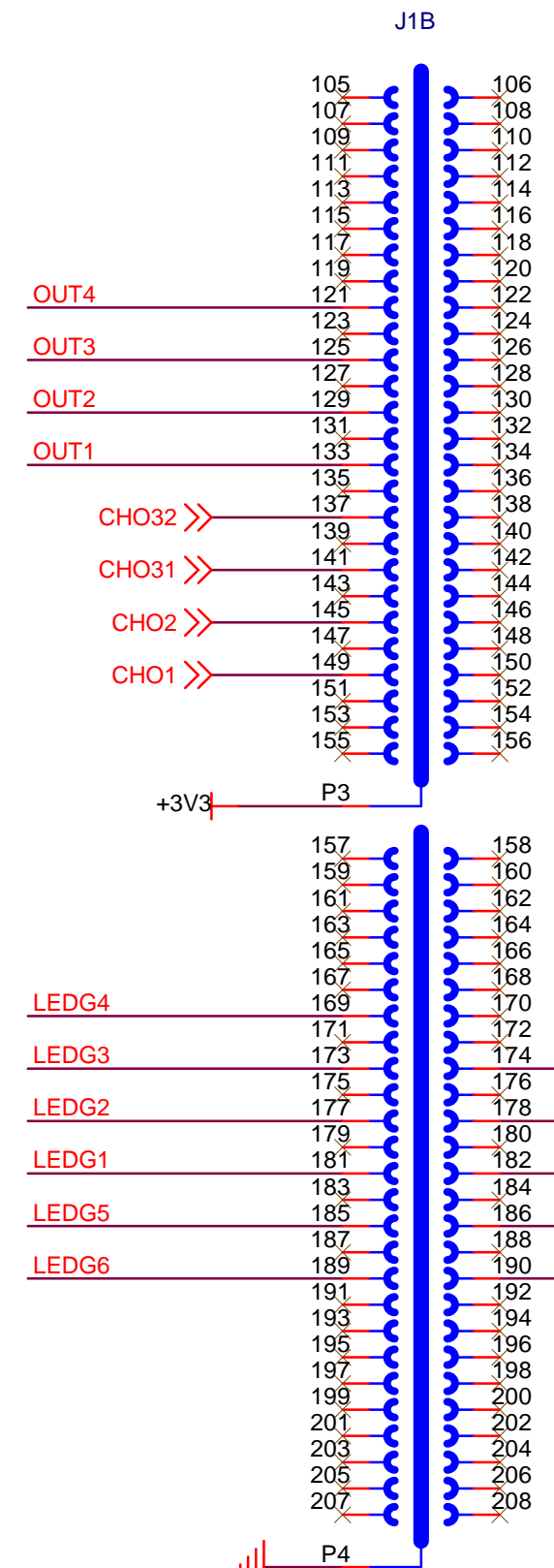
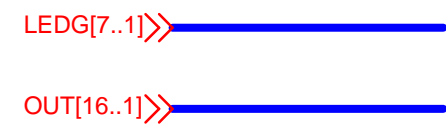
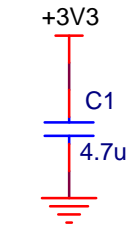
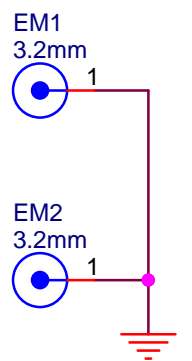


QFS-104-06.25-SL-D-A



QFS-104-06.25-SL-D-A

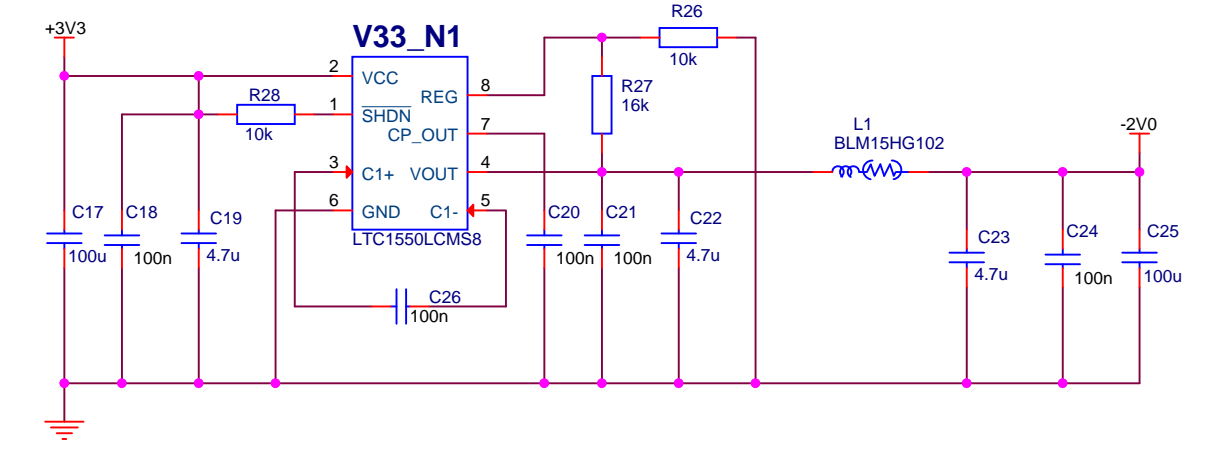
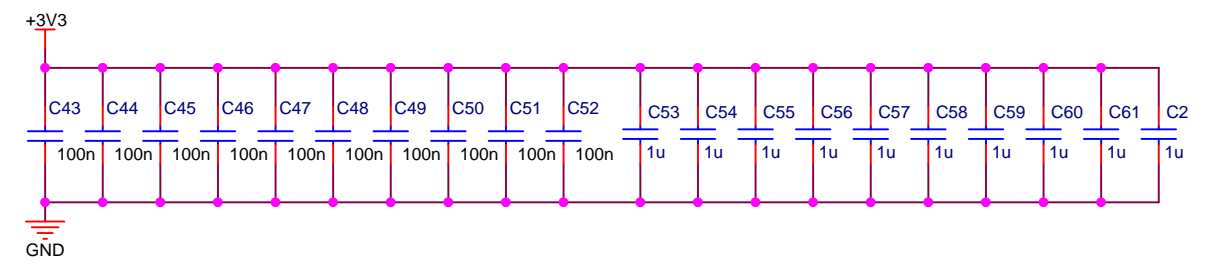
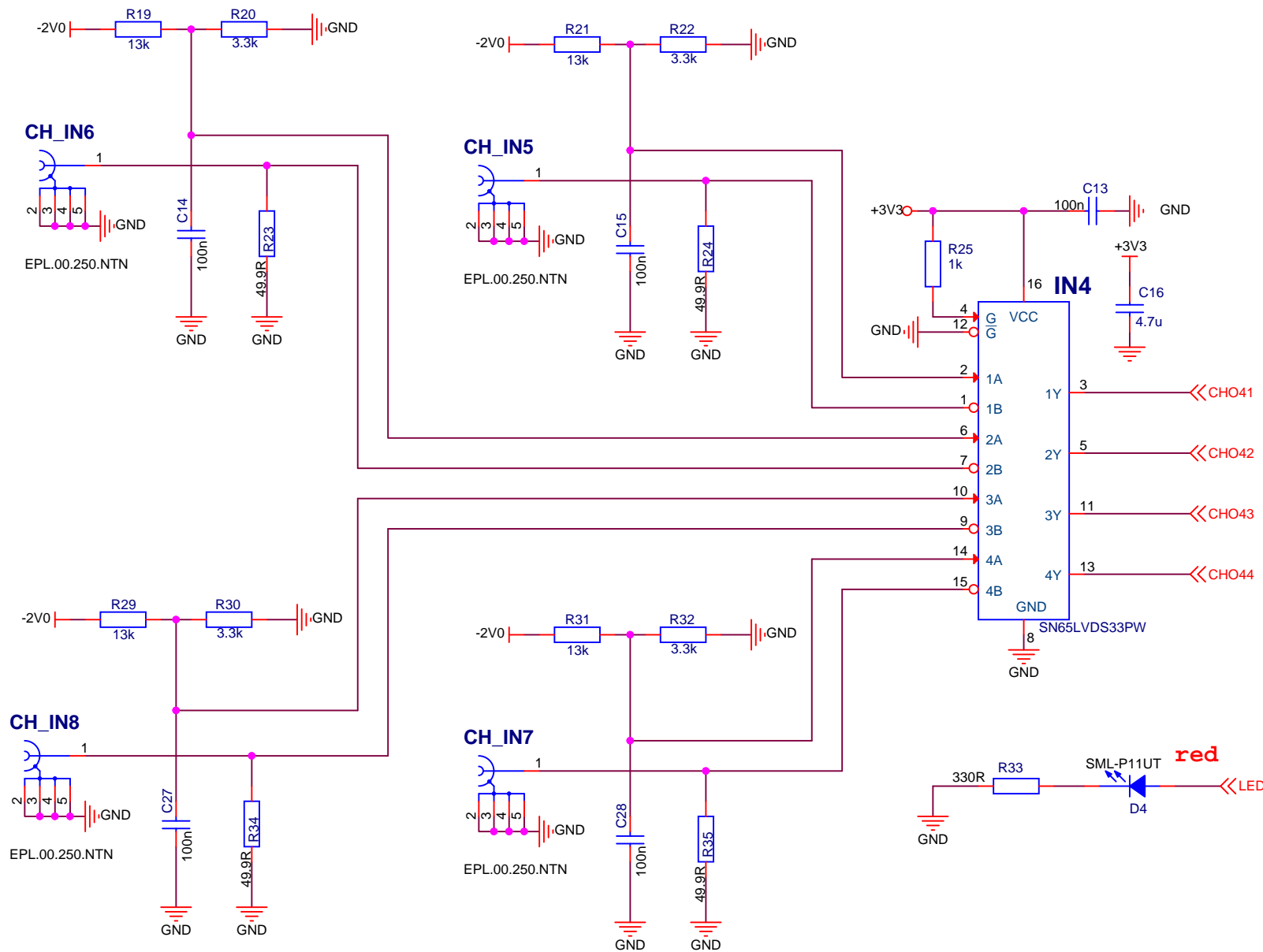
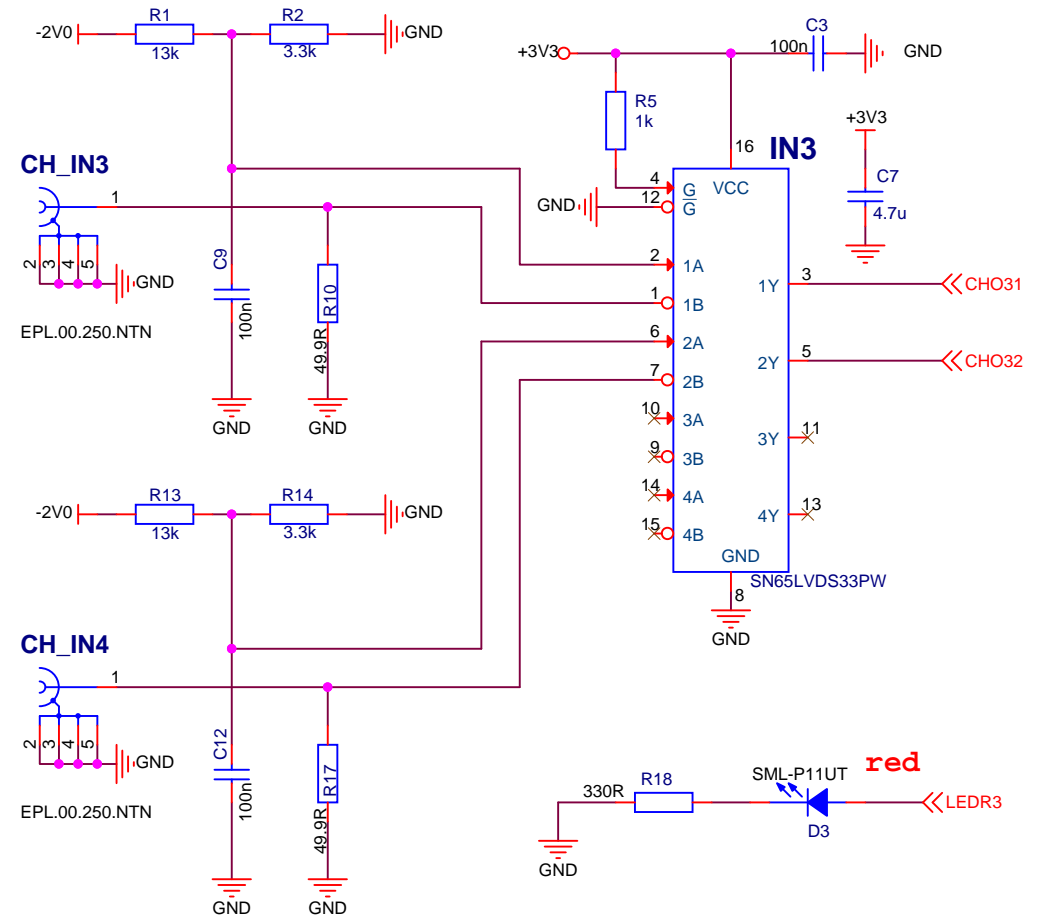
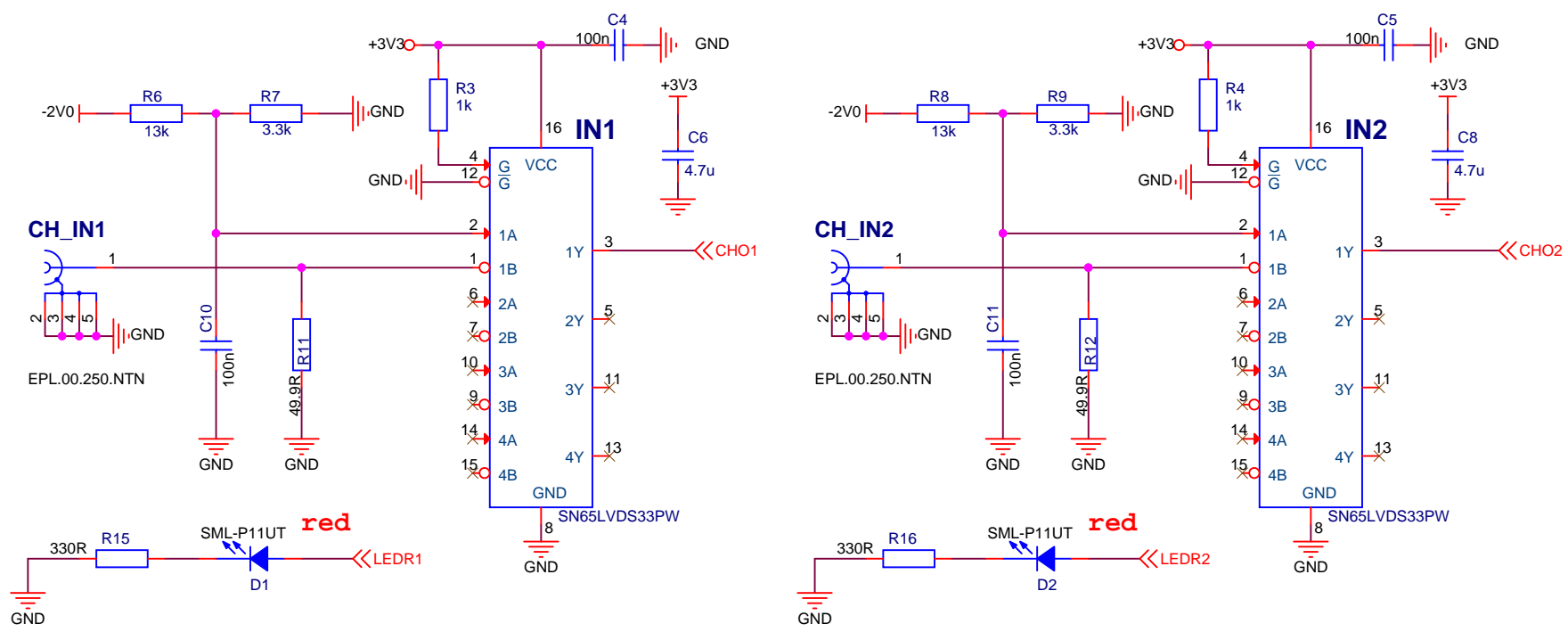




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TRB_SIDE

Design: K:\GSIJOB\HADES\TRBV3\GPIN_ADDON1\GPIN_ADDON1.DSN	
Modified: Friday, January 18, 2013	Size: A4 Page: 1 / 3
Designer: M.Traxler	Layouter: S.Voltz

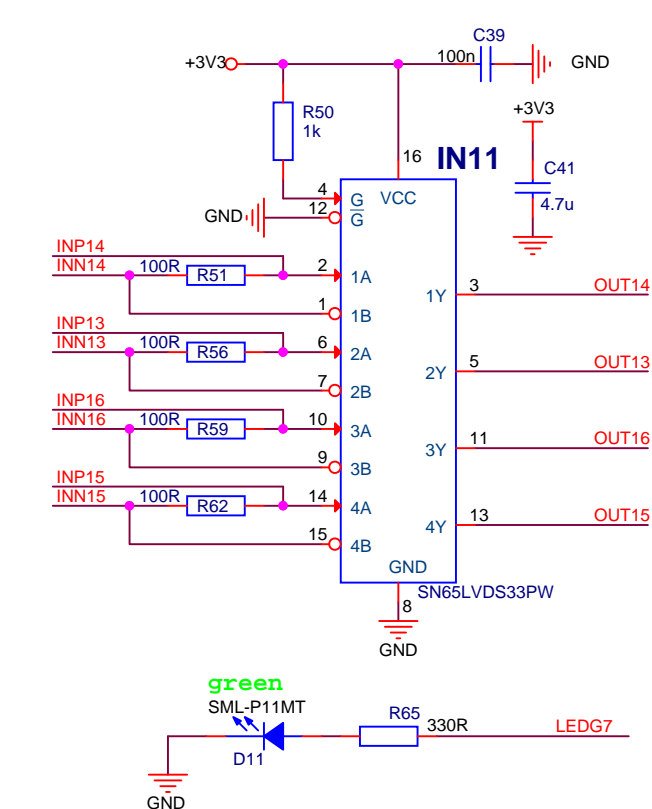
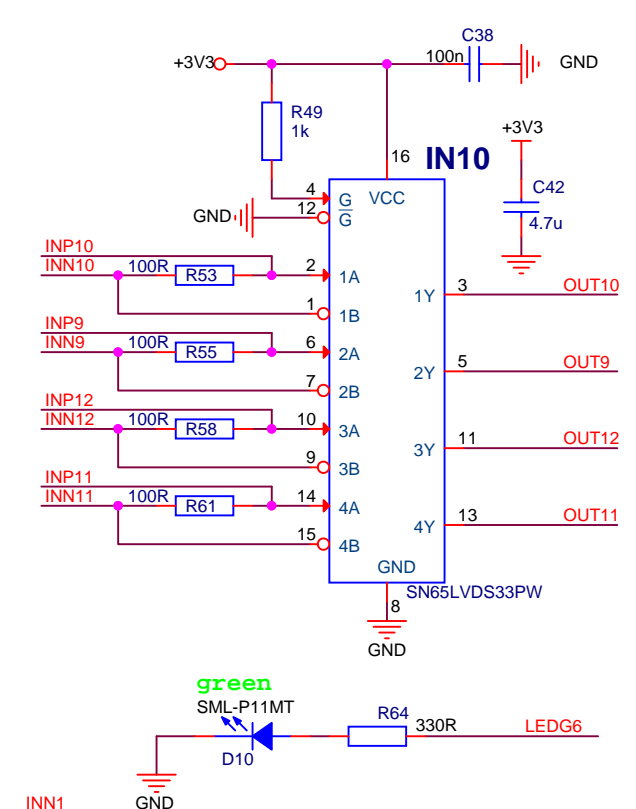
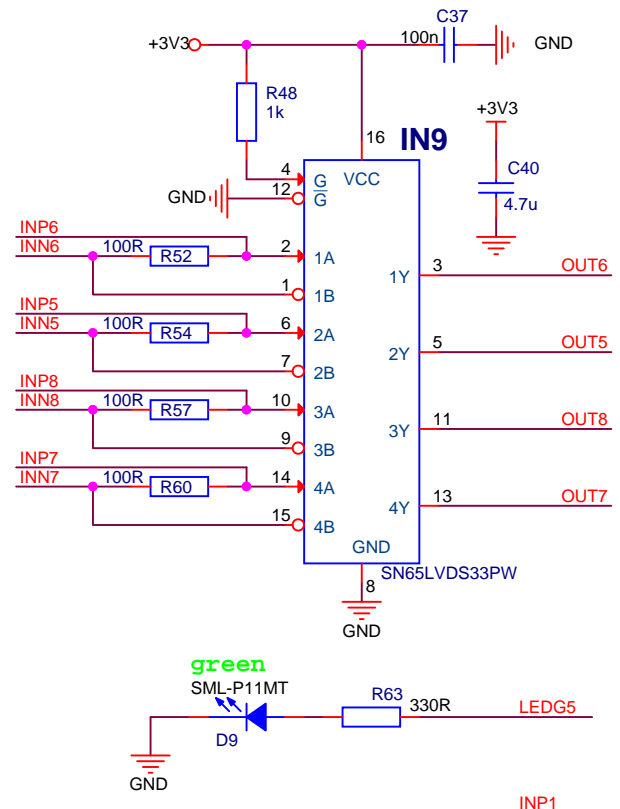
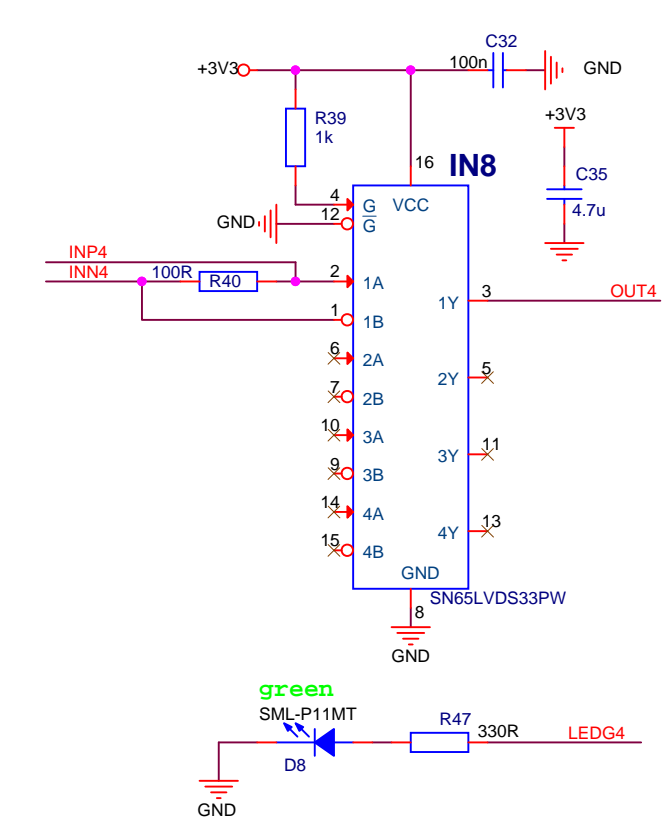
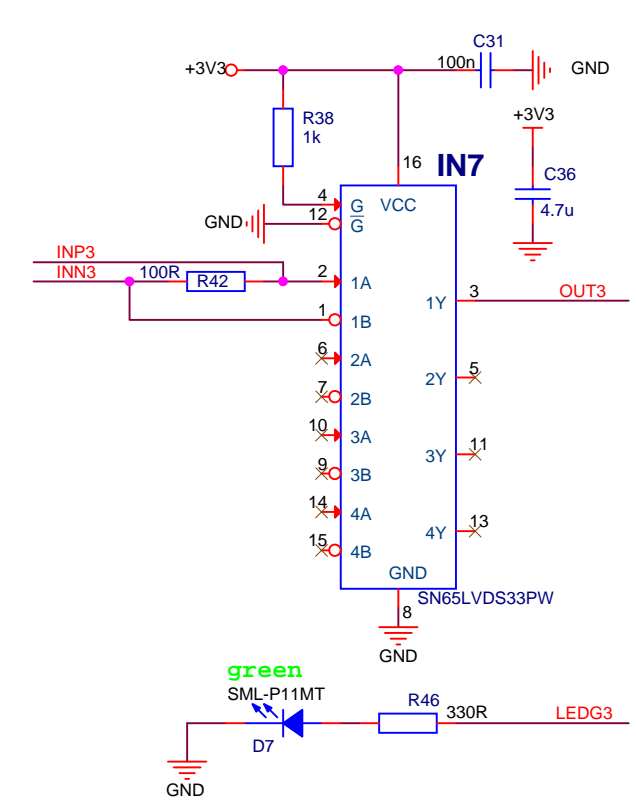
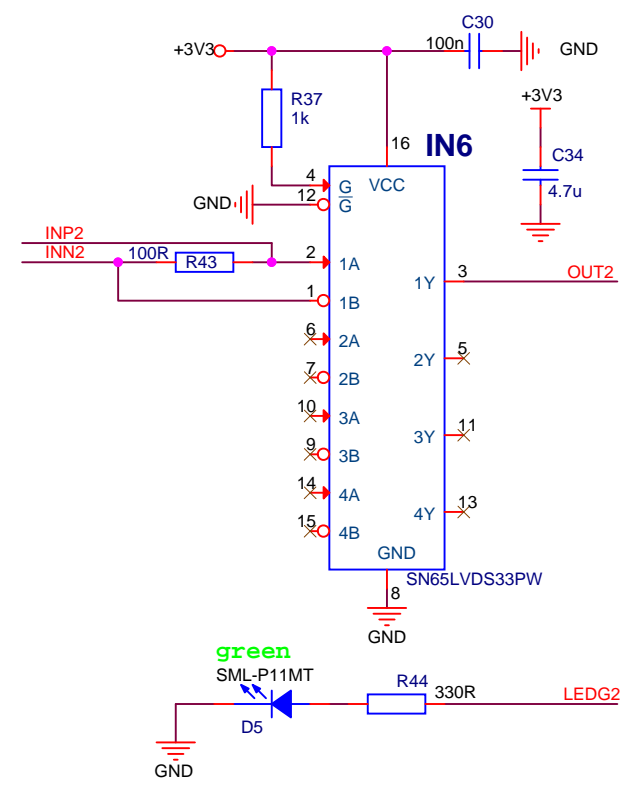
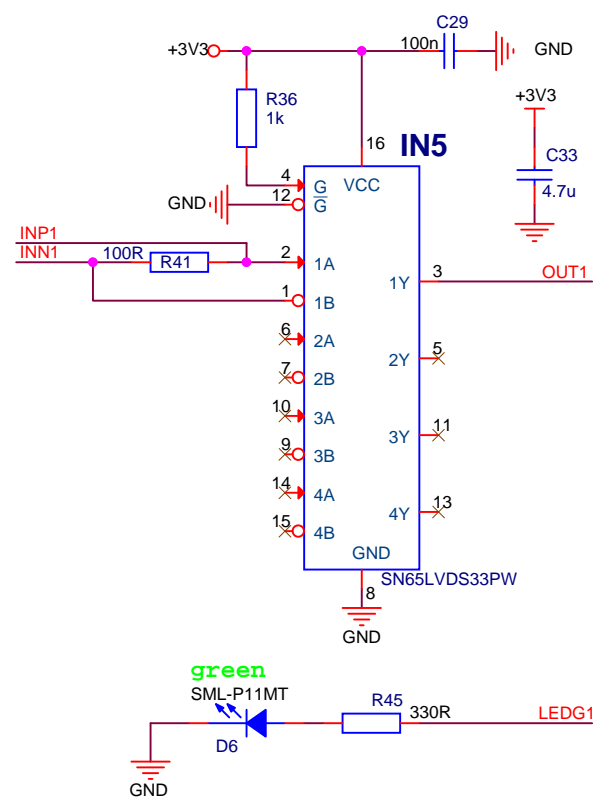


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LEMO

Design: K:\GSI\JOB\HADES\TRBV3\GPIN_ADDON1\GPIN_ADDON1.DSN
 Modified: Friday, January 18, 2013
 Designer: M. Traxler

Size: A3
 Page: 2 / 3
 Layouter: S.Voltz



JECL1

INP1	1	2	INN1
INP2	3	4	INN2
INP3	5	6	INN3
INP4	7	8	INN4
INP5	9	10	INN5
INP6	11	12	INN6
INP7	13	14	INN7
INP8	15	16	INN8
INP9	17	18	INN9
INP10	19	20	INN10
INP11	21	22	INN11
INP12	23	24	INN12
INP13	25	26	INN13
INP14	27	28	INN14
INP15	29	30	INN15
INP16	31	32	INN16
	33	34	

N3431-6202RB

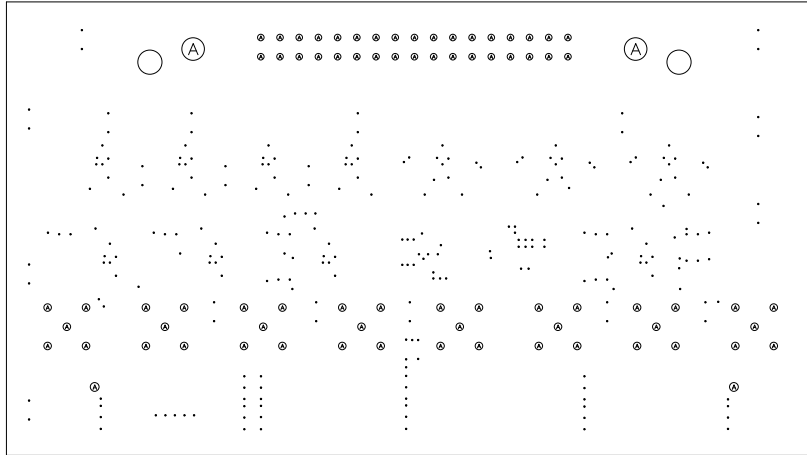
LEDG[7..1] >>> _____

OUT[16..1] >>> _____

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LEDs and Pin-header

Design: K:\GSI\JOB\HADES\TRBV3\GPIN_ADDON1\GPIN_ADDON1.DSN		
Modified: Friday, January 18, 2013	Size: A3	Page: 3 / 3
Designer: M.Traxler	Layouter: S.Voltz	



DRILL CHART: TOP to BOTTOM			
ALL UNITS ARE IN MILLIMETERS			
FIGURE	SIZE	PLATED	QTY
.	0.2	PLATED	253
.	0.4	PLATED	1
⊙	0.9	PLATED	34
⊙	1.0	PLATED	40
○	3.2	PLATED	2
⊙	1.2	NON-PLATED	2
⊙A	3.0	NON-PLATED	2

TOTAL HOLES: 334

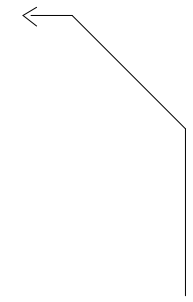
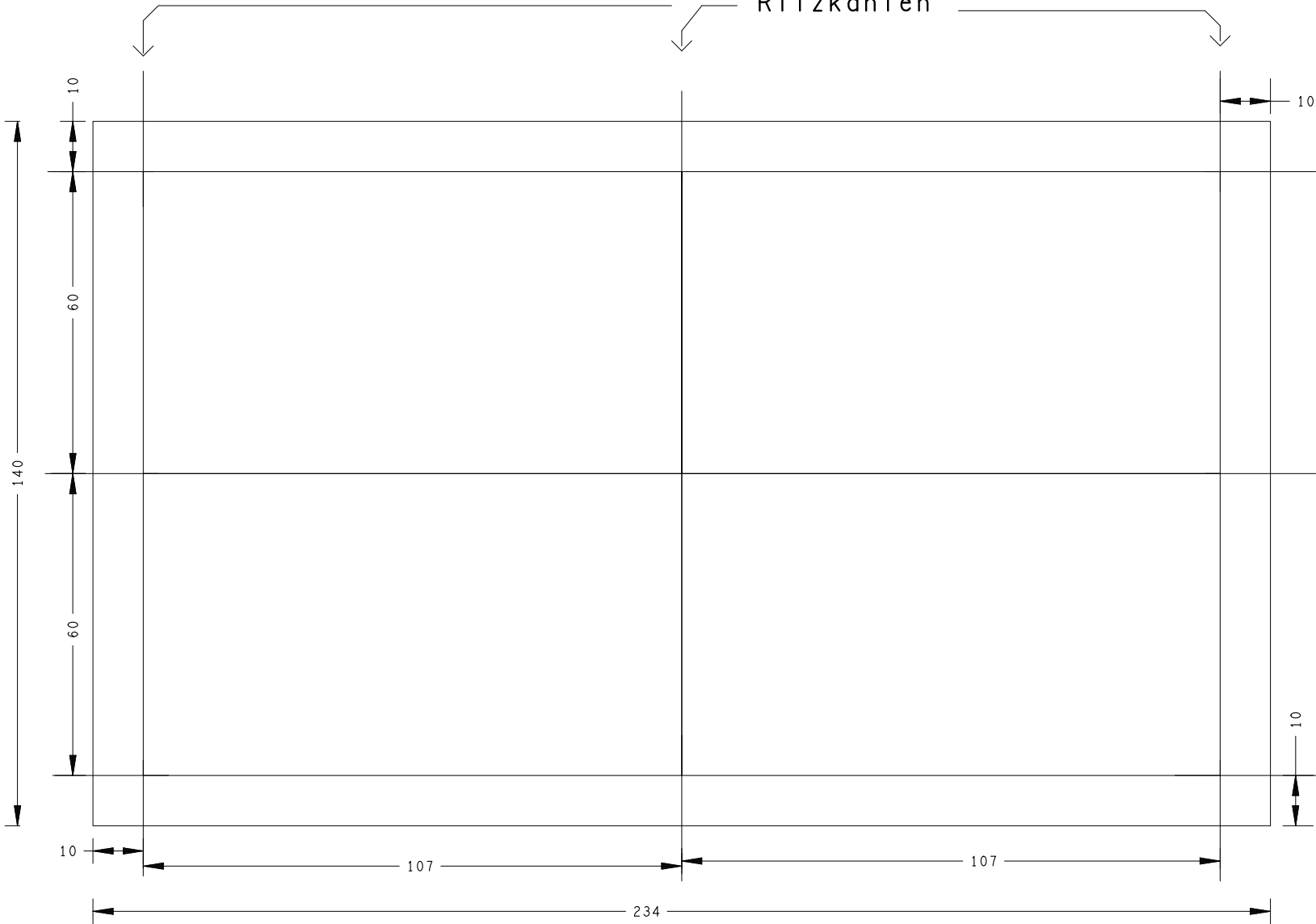


Jobname Date Designer Layouter
 GPIN_ADDON1 01.2013 M.Traxler S.Voltz

Layer Nickname

Drd

Ritzkanten



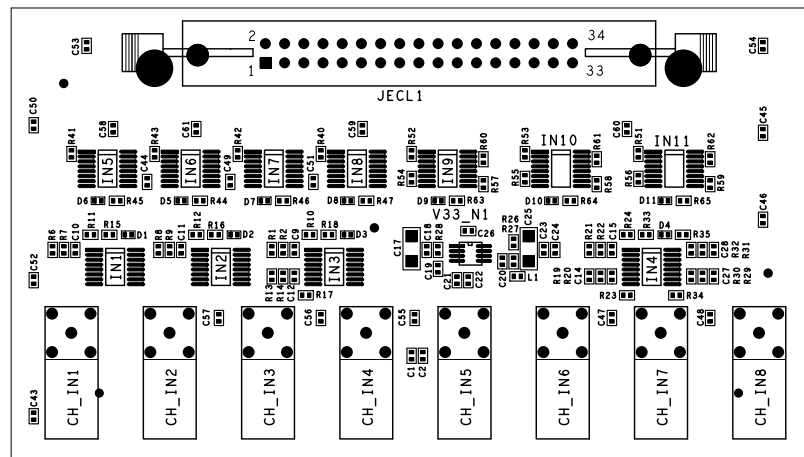
Ritzkanten



Jobname	Date	Designer	Layouter
GPIN_ADDON1	01.2013	M.Traxler	S.Voltz

Layer Nickname

Fab

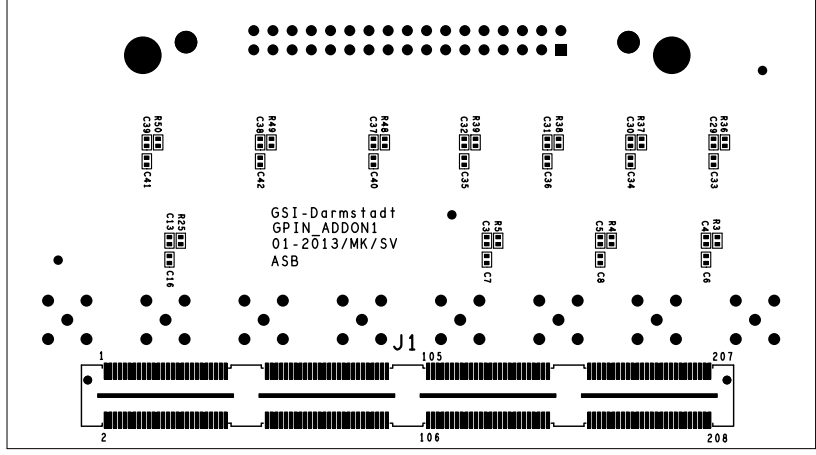


GSI-Darmstadt
 GPIN_AddOn1
 01-2013/MK/SV
 AST

Jobname	Date	Designer	Layouter
GPIN_ADDON1	01.2013	M.Traxler	S.Voltz

Layer Nickname

Ast



Jobname GPIN_ADDON1

Date 01.2013

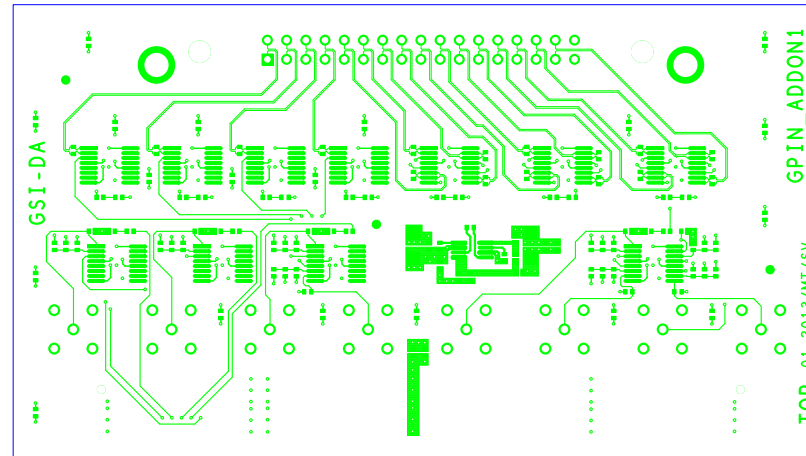
Designer M.Trautler

Laufwerk 2.Volfs

Asp

Asp

TOP- Signals

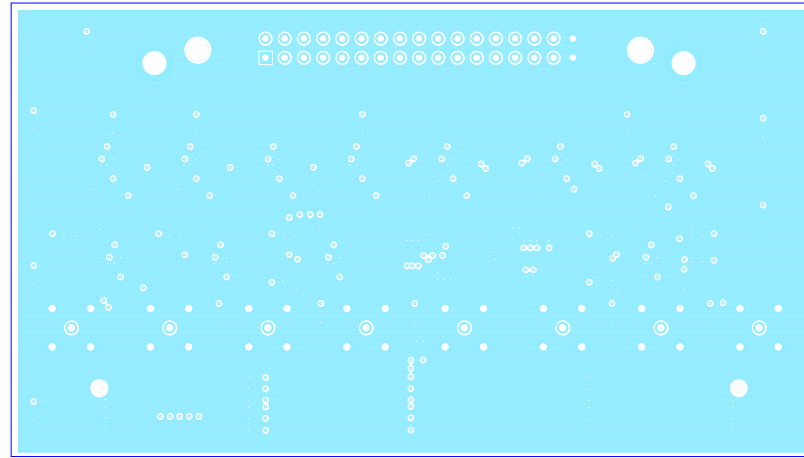


Jobname	Date	Designer	Layouter
GPIN_ADDON1	01.2013	M.Traxler	S.Voltz

Layer Nickname

Top

IN1- GND

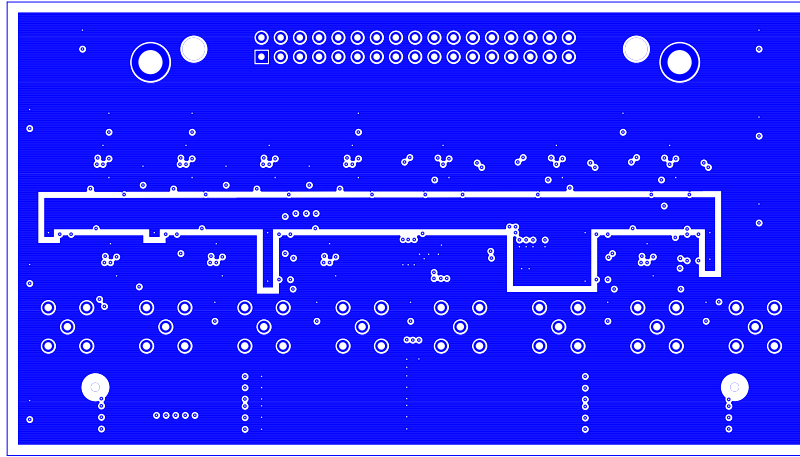


Jobname	Date	Designer	Layouter
GPIN_ADDON1	01.2013	M.Traxler	S.Voltz

Layer Nickname

I01

IN2- Planes: +3V3,-2.0V

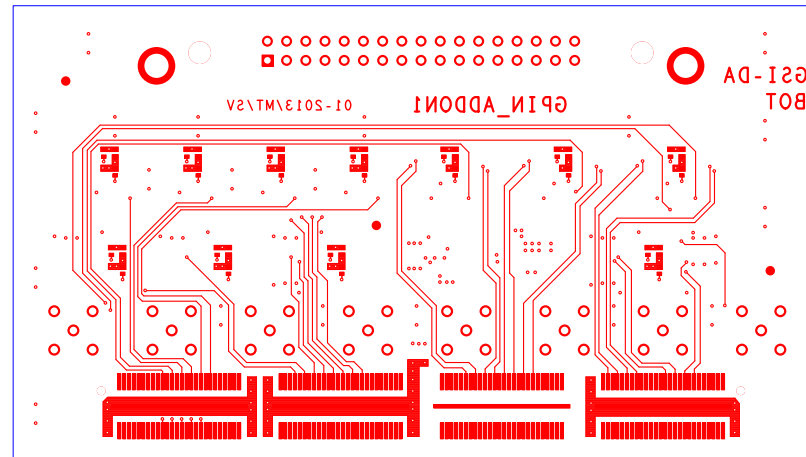


Jobname	Date	Designer	Layouter
GPIN_ADDON1	01.2013	M.Traxler	S.Voltz

Layer Nickname

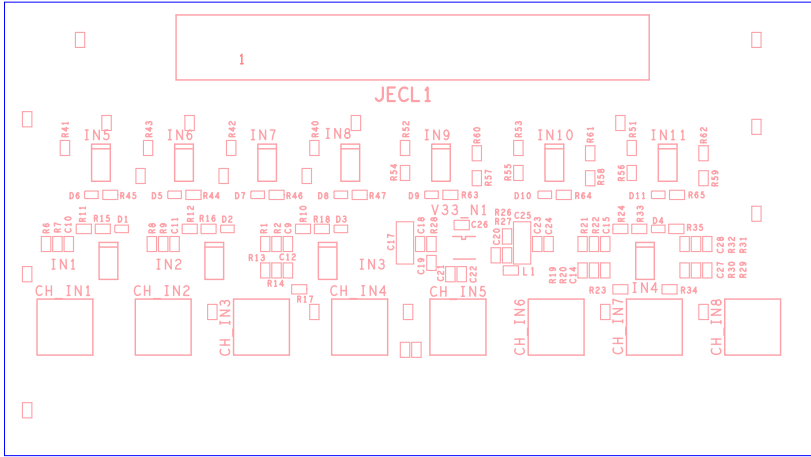
I02

BOT- Signals



Jobname	Date	Designer	Layouter
GPIN_ADDON1	01.2013	M.Traxler	S.Voltz

Layer Nickname
Bot



Jobname	Date	Designer	Layouter
GPIN_ADDON1	01.2013	M.Traxler	S.Voltz

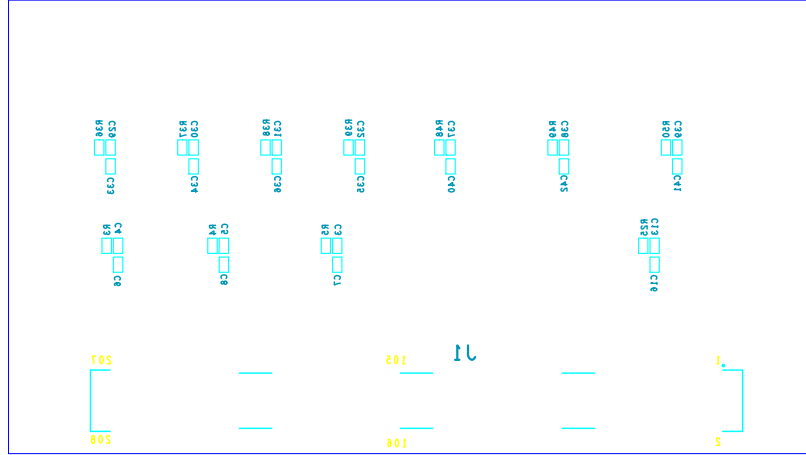
Layer Nickname

Sst

Jobname Date Designer Layouter
GPIN_ADDON1 01.2013 M.Traxler S.Voltz

Layer Nickname

Ssb



Lagenaufbau / Impedanzberechnung hmp für PCB PADIA1:

TOP: GND-Plane und impedanzkontr. Leitungen Ziel = 100 Ohm diff.

~~~~~  
 IN1: GND-Plane

#####

IN2: GND-Plane

~~~~~  
 BOT: Signale

Leiterplattendicke 1.6mm

Layer	Thickness (Millimeter)	Stackup Picture TopLayer L1 / LN	Family	Description	Type
ST1	0,0150		Stopplack	Stopplack	
L1	0,0390		Kupfer	12 + 27	Kupfer
	0,1452		IS410	1080	
			IS410	1080	
L2	0,0350		Kupfer	35	
	1,2000		IS410	1,200 mm	
L3	0,0350		Kupfer	35	
	0,1452		IS410	1080	
			IS410	1080	
LN	0,0390		Kupfer	12 + 27	Kupfer
STN	0,0150		Stopplack	Stopplack	
1,6685		Total Expected Thickness			
1,5500		After Lamination	+0,1300	-0,1300	
1,6000		Incl.Plating	+0,1600	-0,1600	

Drill/Rout Files: a: B1

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Empfehlung Leiterzugbreite und Separation 100µm für Ziel = 100 Ohm

Polar Scratch Pad
 Model: EdgeCoupledCoatedMicrostrip1B
 Length Unit: Micron

Name	Description	Value	Lock
W1	Lower Trace Width	100	<input checked="" type="checkbox"/>
W2	Upper Trace Width	90	<input checked="" type="checkbox"/>
T1	Trace Thickness	39	<input checked="" type="checkbox"/>
S1	Trace Separation	100	<input checked="" type="checkbox"/>
H1	Substrate 1 Height	145,25	<input checked="" type="checkbox"/>
Er1	Substrate 1 Dielectric	4,2	<input checked="" type="checkbox"/>
C1	Coating Above Substrate	30	<input checked="" type="checkbox"/>
C2	Coating Above Trace	15	<input checked="" type="checkbox"/>
C3	Coating Between Trace	30	<input checked="" type="checkbox"/>
CEr	Coating Dielectric	3,6	<input checked="" type="checkbox"/>
Impedance		100	<input type="checkbox"/>
Differential Calculation Mode		Differential	<input checked="" type="checkbox"/>
EtchFactor		10	<input checked="" type="checkbox"/>

Layer Assignment

Layer	L1
	H1
Layer	L2

Auto-fill Polar Values
 Er Calculation Method: Height-weighted Average

Polar returned: Impedance = 99,6590