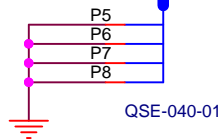
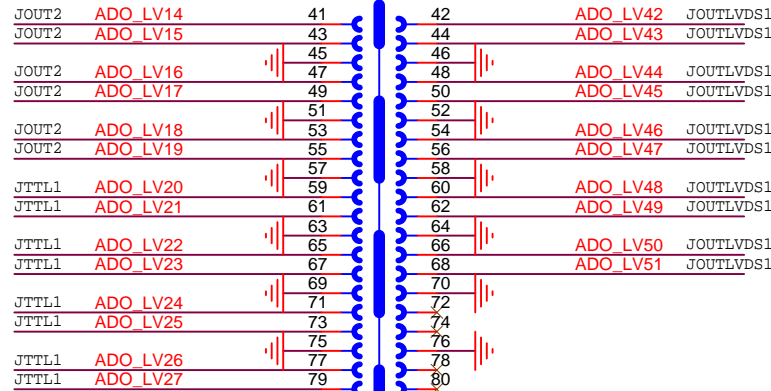
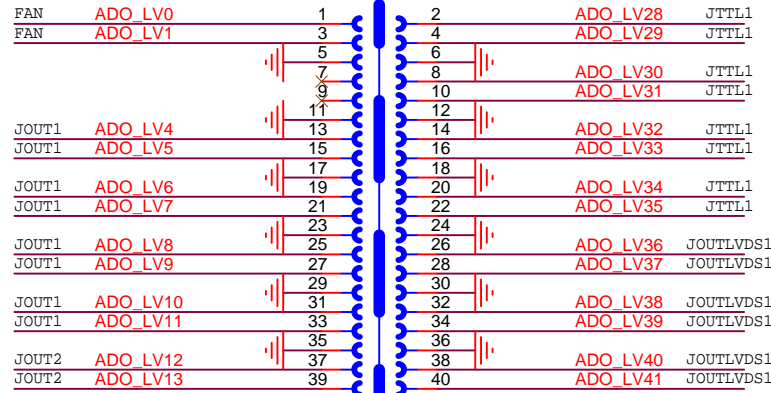


ADO_LV[1..0] >> 3
 ADO_LV[51..4] >> 2,4,5

ADO_TTL[33..0] >> 2,4,6
 ADO_TTL[40..35] >> 2,4,6
 ADO_TTL[46..43] >> 2,4,6

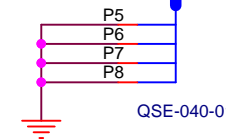
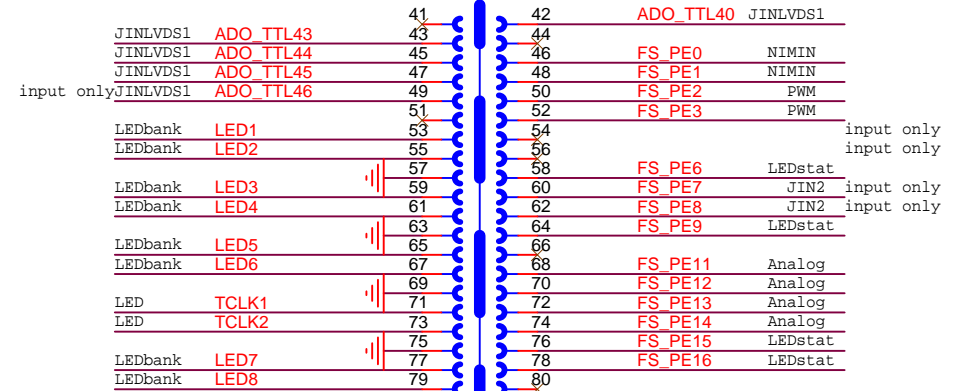
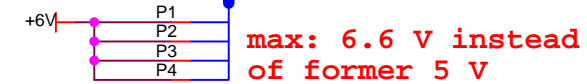
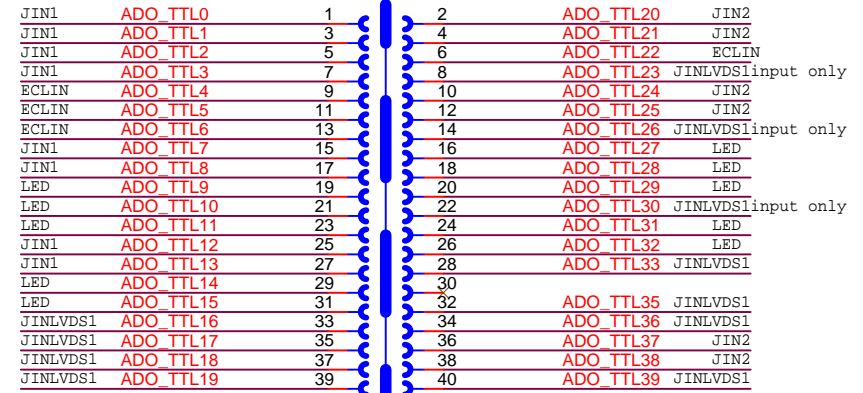
FS_PE[3..0] >> 2,3,5,6
 FS_PE[9..6] >> 2,3,5,6
 FS_PE[16..11] >> 2,3,5,6

JADDON1



TCLK[2..1] >> 2
 LED[8..1] >> 5

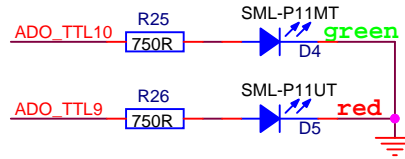
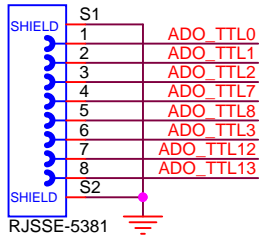
JADDON2



GSI Gesellschaft für Schwerionenforschung mbH
 Planckstrasse 1
 D-64291 Darmstadt
 GERMANY
 www.gsi.de

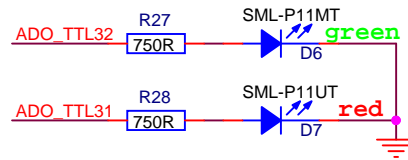
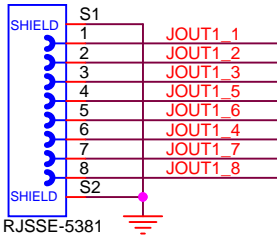
AddON-Connectors

JIN1

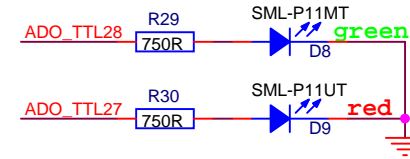
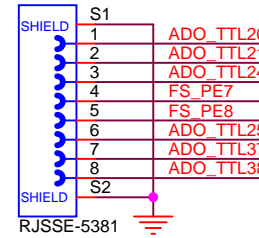


Place LEDs behind the RJ45

JOUT1

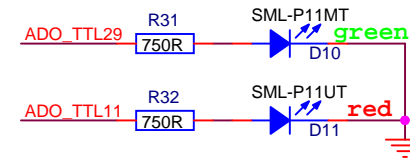
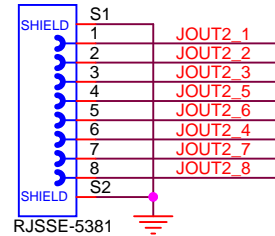


JIN2



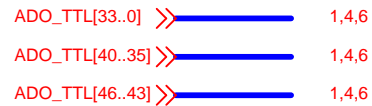
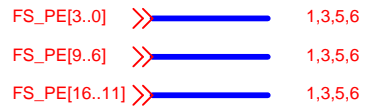
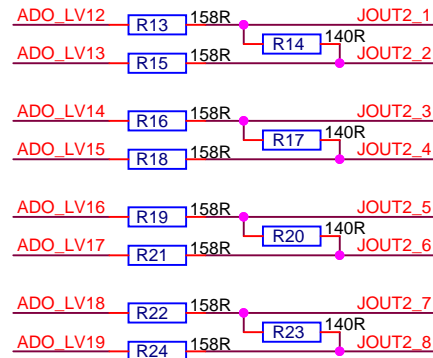
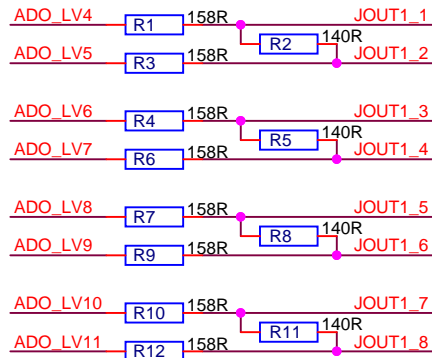
Place LEDs behind the RJ45

JOUT2



680R @ 2.5V = 0.89mA - normal
 330R @ 2.5V = 1.8mA - good for RJ-45 because of light guides through connector

1800R @ 3.3V = 0.75mA - dim for LED bar
 1500R @ 3.3V = 0.93mA - normal
 810R @ 3.3V = 1.7mA - RJ-45



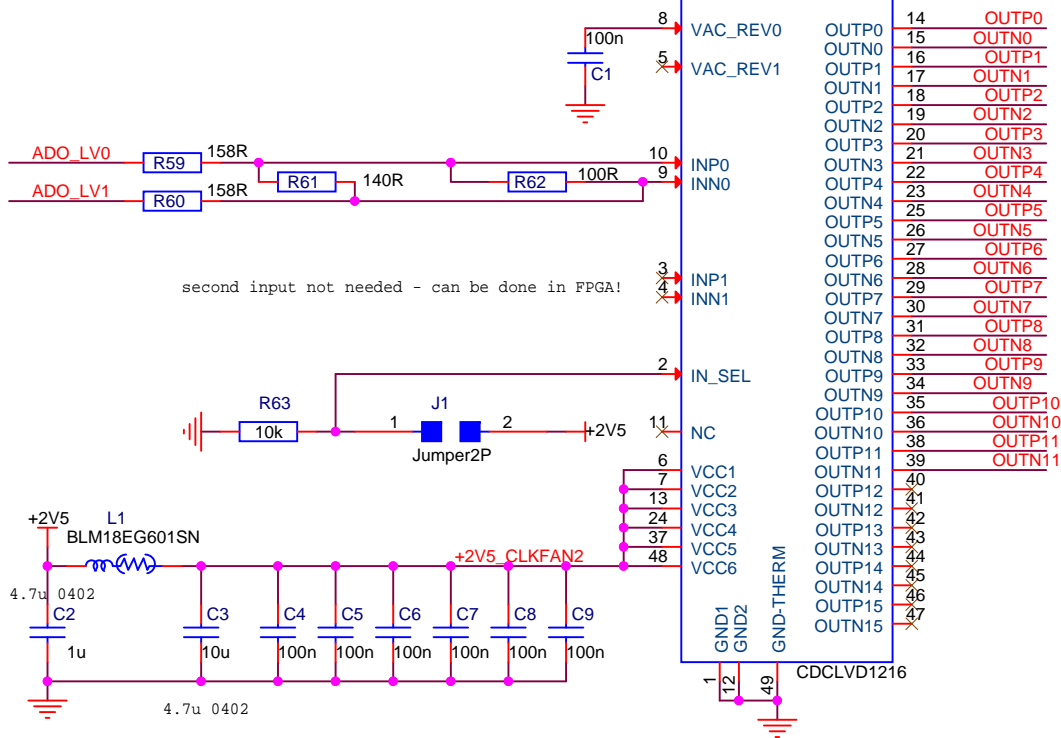
GSI Gesellschaft für Schwerionenforschung mbH
 Planckstrasse 1
 D-64291 Darmstadt
 GERMANY
 www.gsi.de

RJ45-Connectors

ADO_LV[1..0] >> 1

Is there nothing that can be operated at 3.3V?

TRIGGER_FAN1

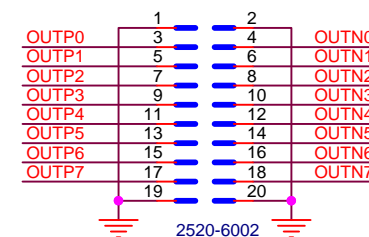


second input not needed - can be done in FPGA!

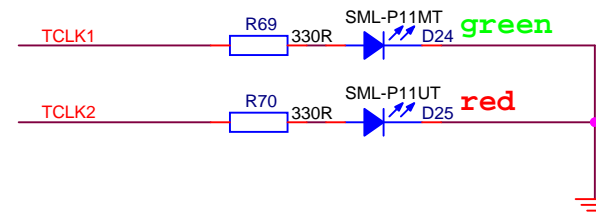
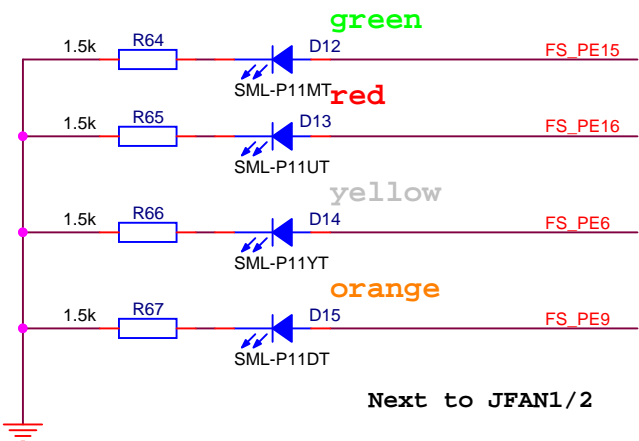
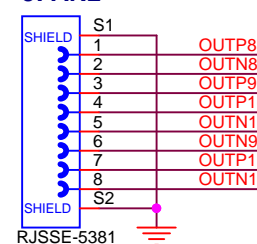
FS_PE[3..0] >> 1,2,4,6
 FS_PE[9..6] >> 1,2,4,6
 FS_PE[16..11] >> 1,2,4,6

TCLK[2..1] >> 1

JFAN1



JFAN2



Place LEDs behind the RJ45



Gesellschaft für Schwerionenforschung mbH
 Planckstrasse 1
 D-64291 Darmstadt
 GERMANY
 www.gsi.de

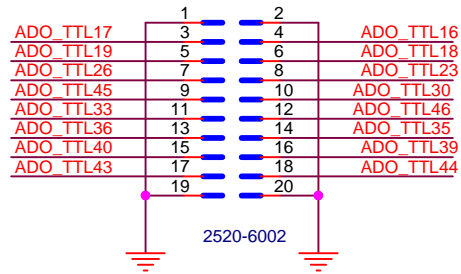
LVDS fan-out & Main Status LED

Design: K:\GSIJOB\HADES\TRBV3CTS_ADDON1\TRBV3CTS_ADDON1.DSN	
Modified: Tuesday, January 15, 2013	Size: A4 Page: 3 / 7
Designer: M. Traxler	Lavouter: S. Voltz

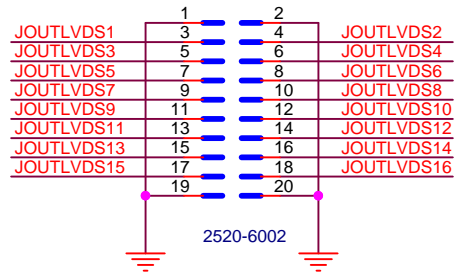
ADO_TTL[33..0] >> 1,2,6
 ADO_TTL[40..35] >> 1,2,6
 ADO_TTL[46..43] >> 1,2,6

ADO_LV[51..4] >> 1,2,5

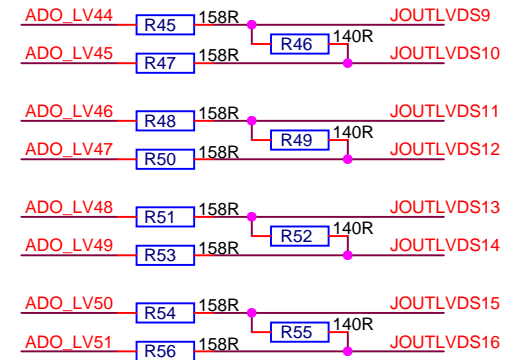
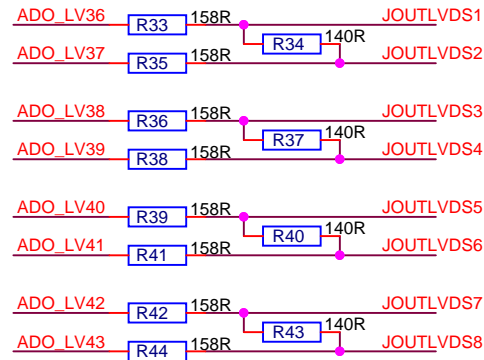
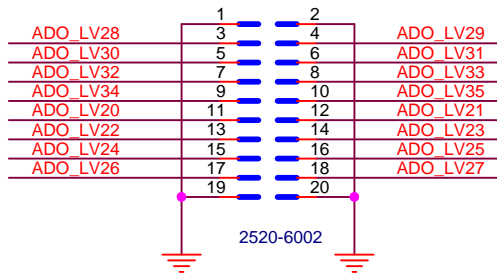
JINLVDS1



JOUTLVDS1



JTTL1

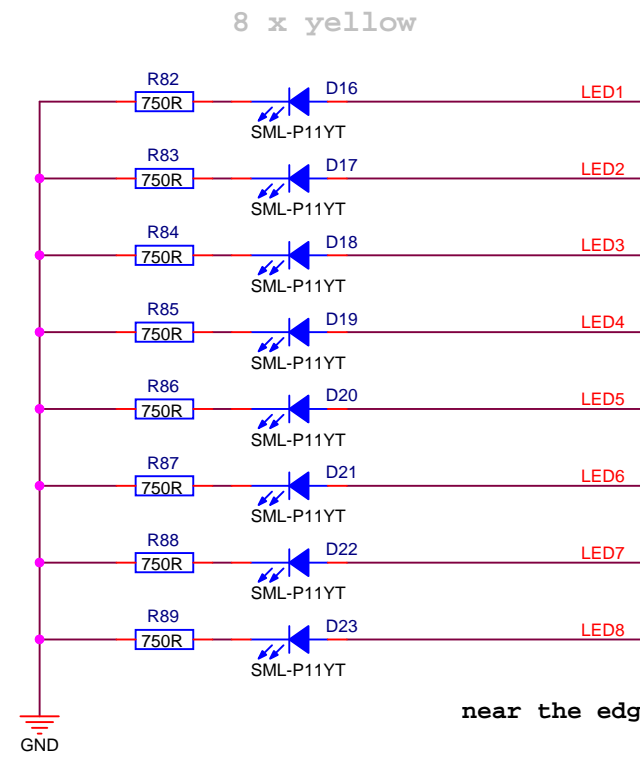
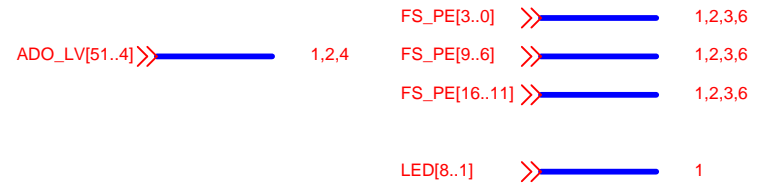
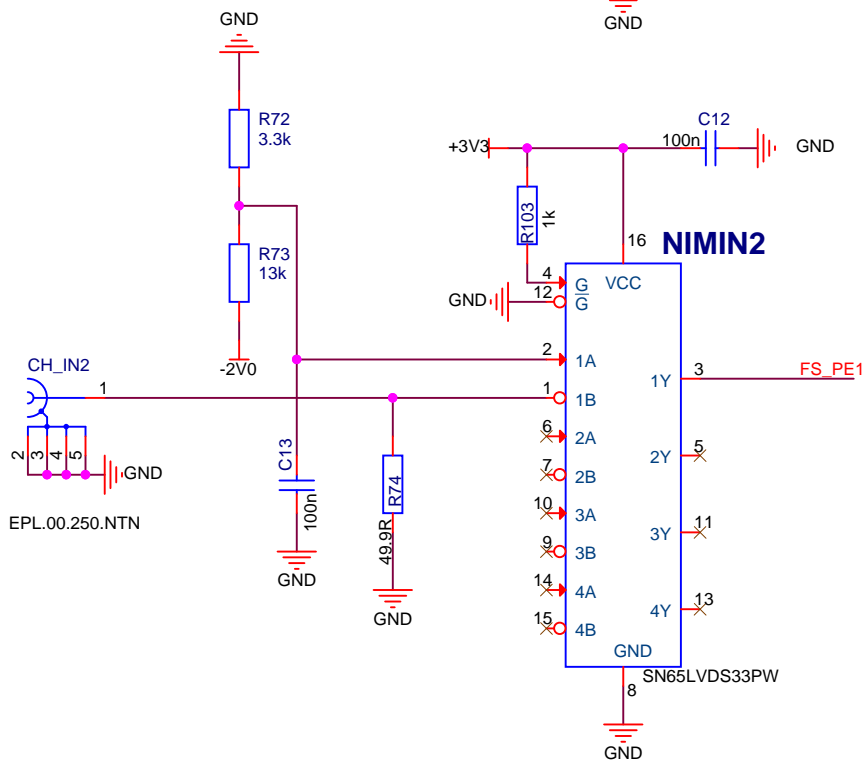
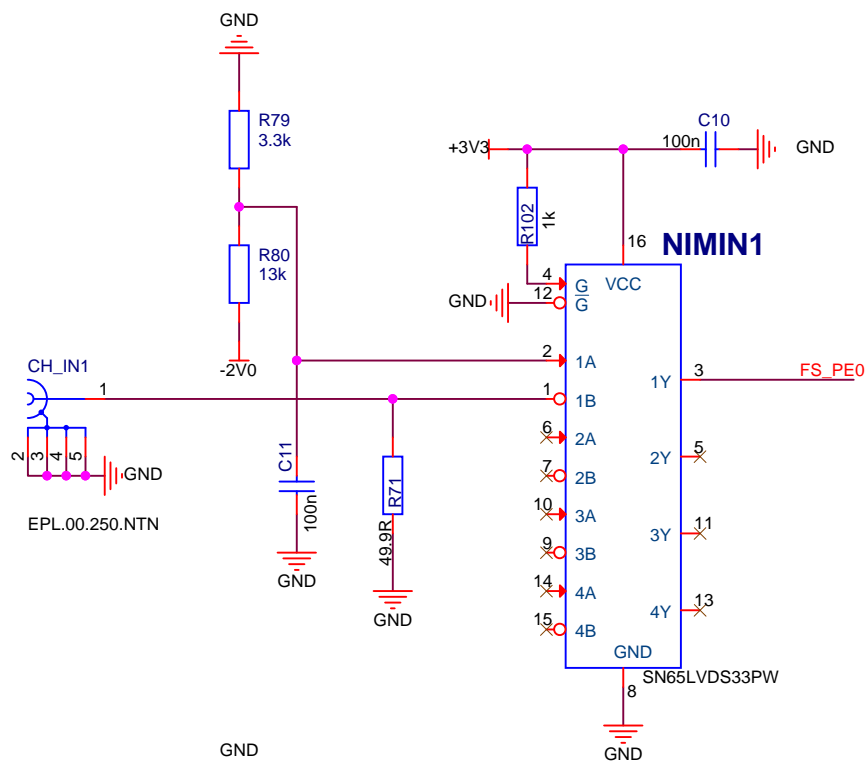




Gesellschaft für Schwerionenforschung mbH
 Planckstrasse 1
 D-64291 Darmstadt
 GERMANY
www.gsi.de

Pinheader I/O

Design: K:\GSIJOB\HADES\TRBV3\CTS_ADDON1\TRB3CTS_ADDON1.DSN	
Modified: Tuesday, January 15, 2013	Size: A4 Page: 4 / 7
Designer: M.Traxler	Lavouter: S.Voltz



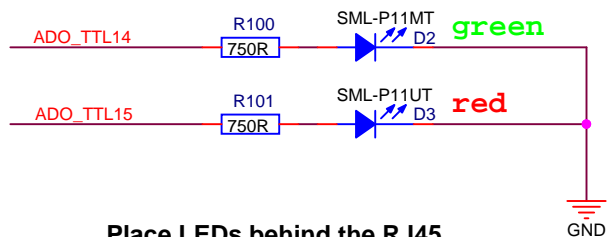


Gesellschaft für Schwerionenforschung mbH
Planckstrasse 1
D-64291 Darmstadt
GERMANY
www.gsi.de

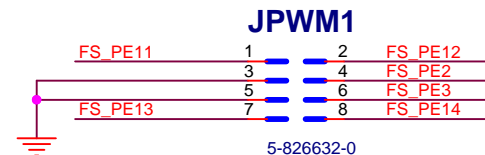
NIM LEMO Input and LEDs

Design: K:\GSIJOB\HADES\TRBV3\CTS_ADDON1\TRB3CTS_ADDON1.DSN	
Modified: Tuesday, January 15, 2013	Size: A4 Page: 5 / 7
Designer: M. Traxler	Layouter: S. Voltz

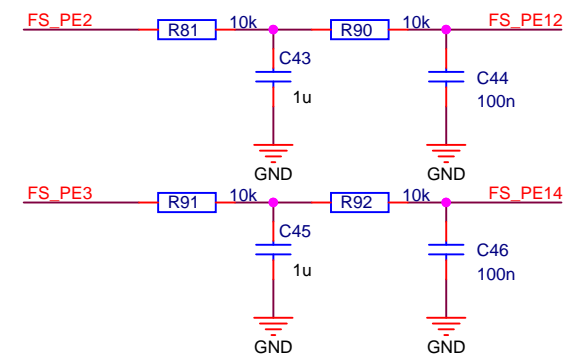
ADO_TTL[33..0] >> 1,2,4 FS_PE[3..0] >> 1,2,3,5
 ADO_TTL[40..35] >> 1,2,4 FS_PE[9..6] >> 1,2,3,5
 ADO_TTL[46..43] >> 1,2,4 FS_PE[16..11] >> 1,2,3,5



Place LEDs behind the RJ45



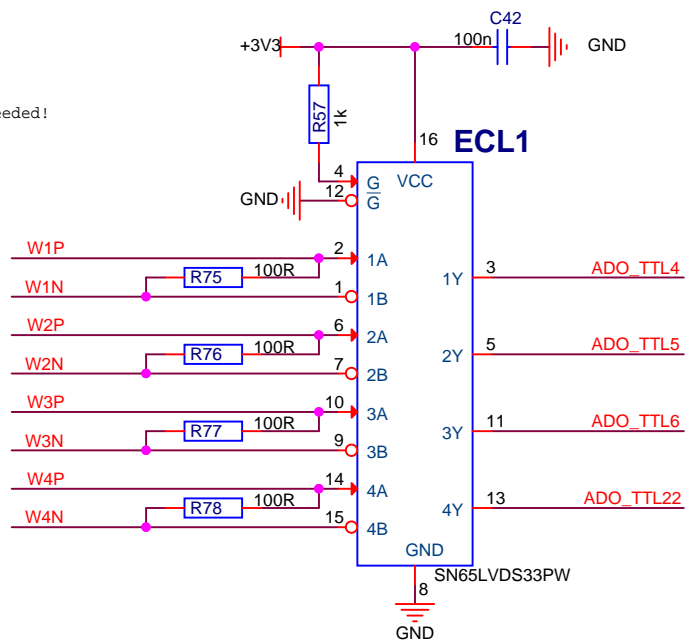
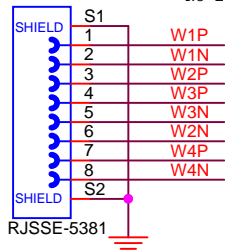
filtered and unfiltered PWM for possible external use,
 GND next to signals for simple pluggin of two pin connectors



Check values

JECLIN1

No ECL output, too much overhead needed!

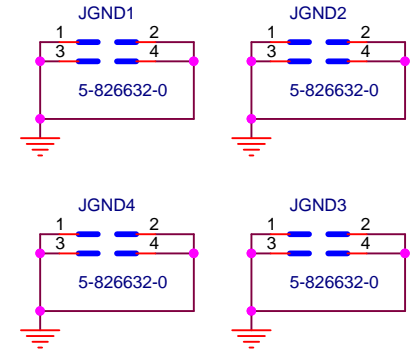
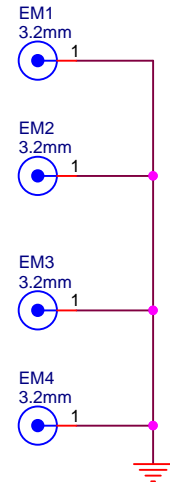
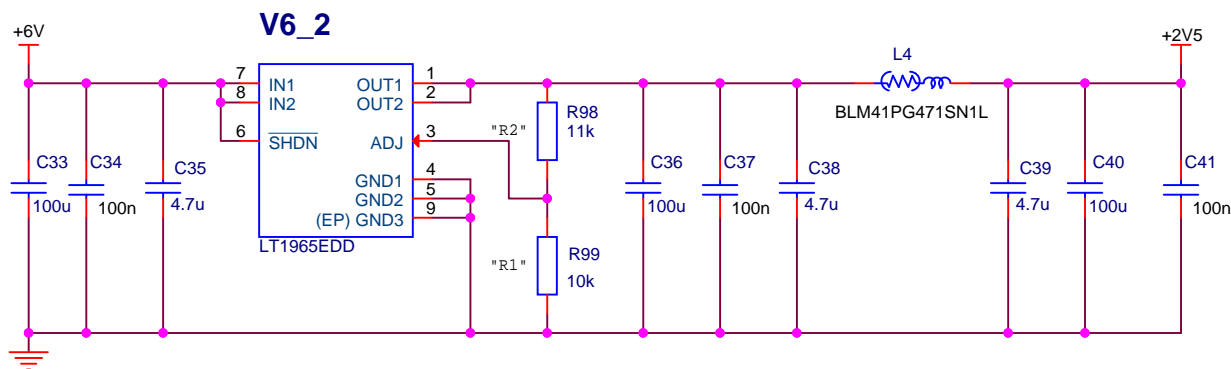
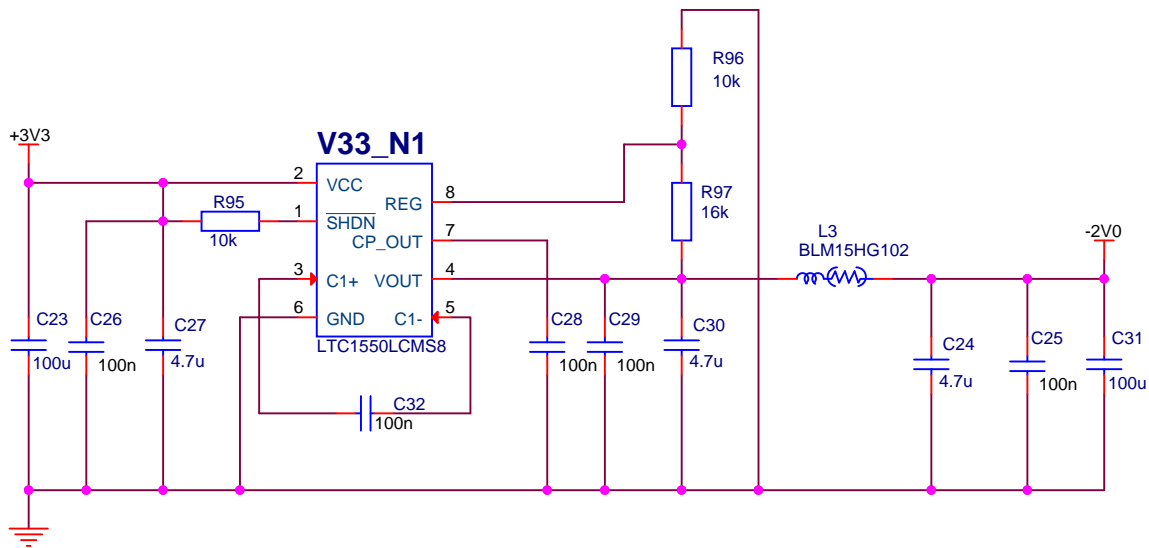
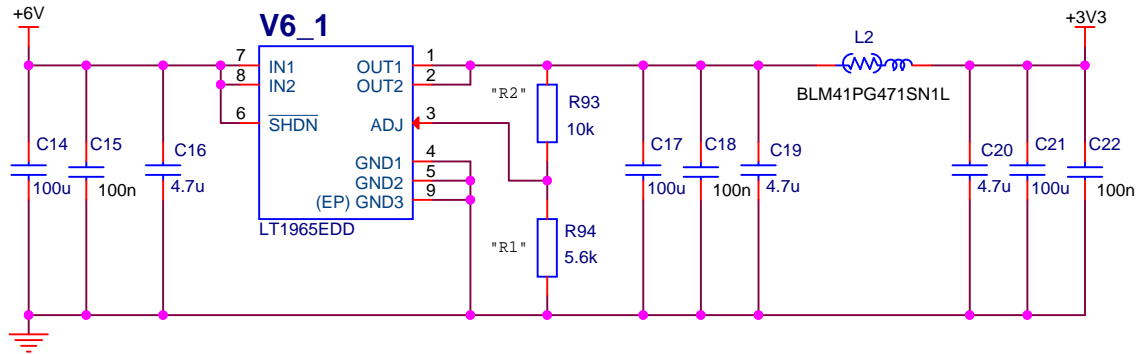




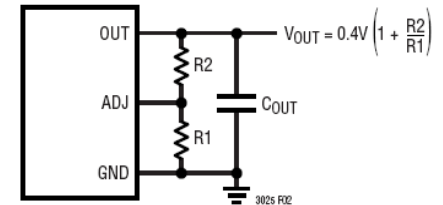
Gesellschaft für Schwerionenforschung mbH
 Planckstrasse 1
 D-64291 Darmstadt
 GERMANY
 www.gsi.de

ECL inputs & Discrimator/PWM Channels

Design: K:\GSIJOB\HADES\TRBV3\CTS_ADDON1\TRB3CTS_ADDON1.DSN	
Modified: Tuesday, January 15, 2013	Size: A4 Page: 6 / 7
Designer: M.Traxler	Lavouter: S.Voltz

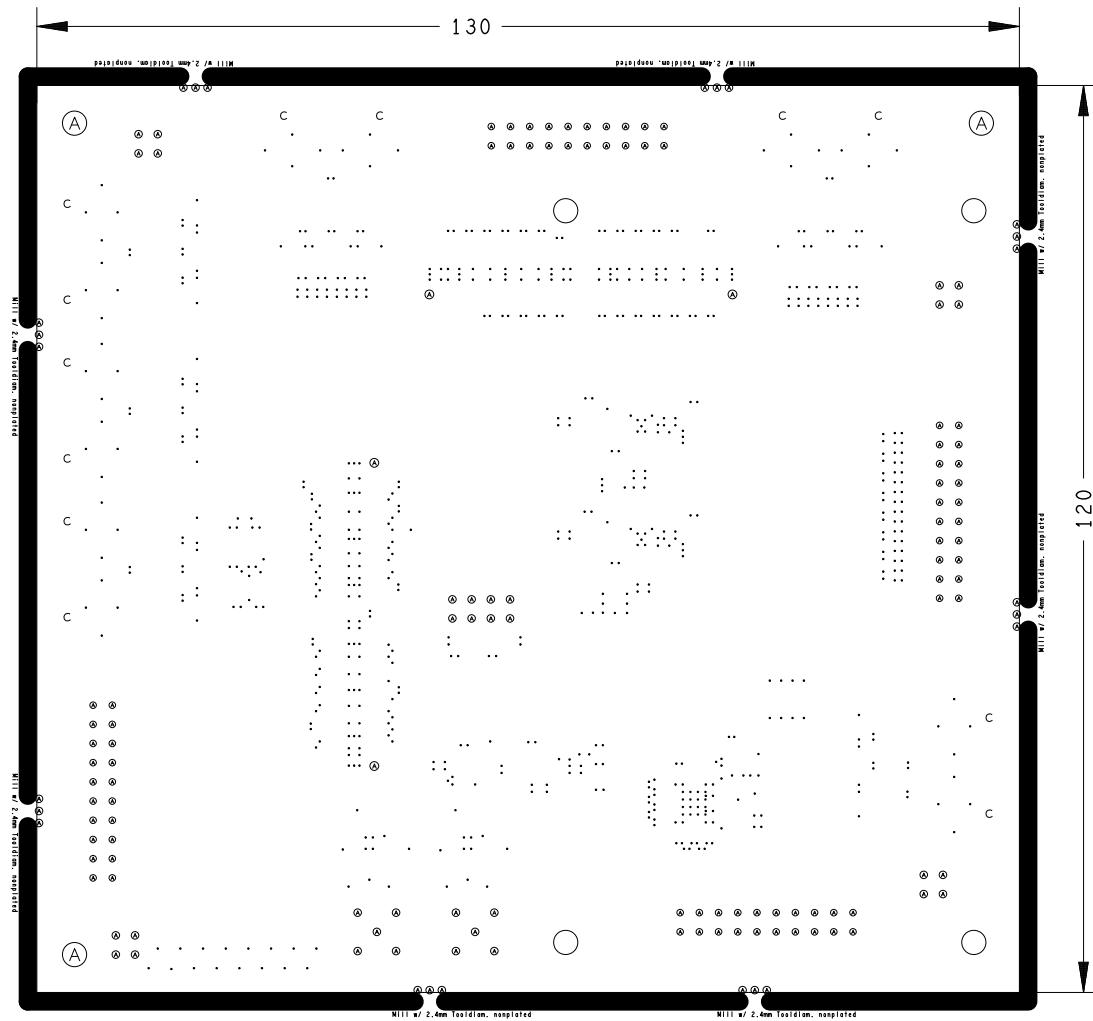


LTC3025: 300mA



GSI Gesellschaft für Schwerionenforschung mbH
 Planckstrasse 1
 D-64291 Darmstadt
 GERMANY
 www.gsi.de

Power



DRILL CHART: TOP to BOTTOM

ALL UNITS ARE IN MILLIMETERS

FIGURE	SIZE	PLATED	QTY
.	0.2	PLATED	16
.	0.2	PLATED	694
.	0.4	PLATED	1
o	0.9	PLATED	80
o	1.0	PLATED	34
o	3.2	PLATED	4
o	1.0	NON-PLATED	24
o	1.2	NON-PLATED	4
o	2.4	NON-PLATED	16
c	2.7	NON-PLATED	12
(A)	3.2	NON-PLATED	3

TOTAL HOLES: 888

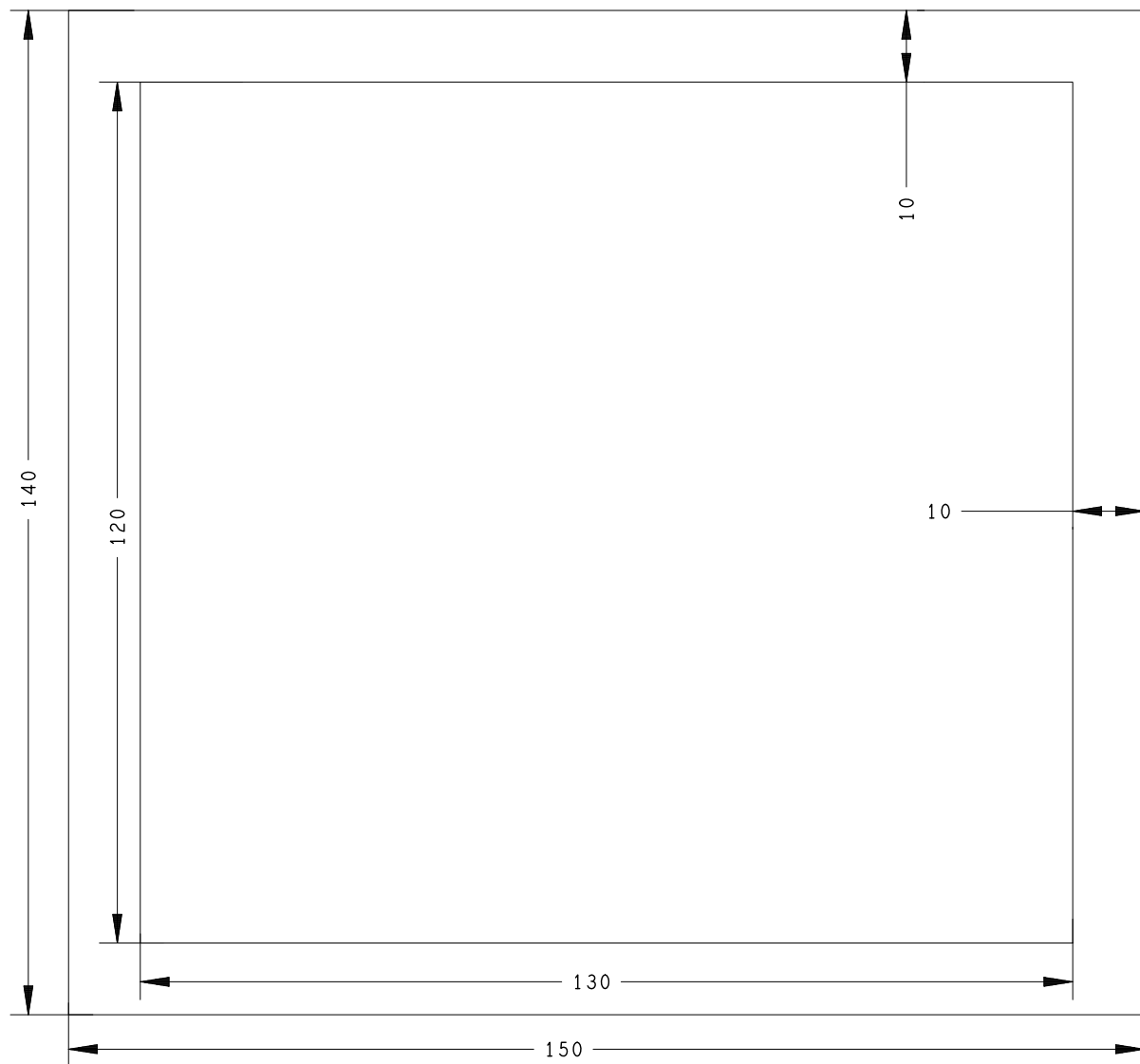
Jobname Date Designer Layouter
 TRB3CTS_AddOn1 01.2013 J.Michel/M.Traxler S.Voltz

Layer Nickname

Dr d



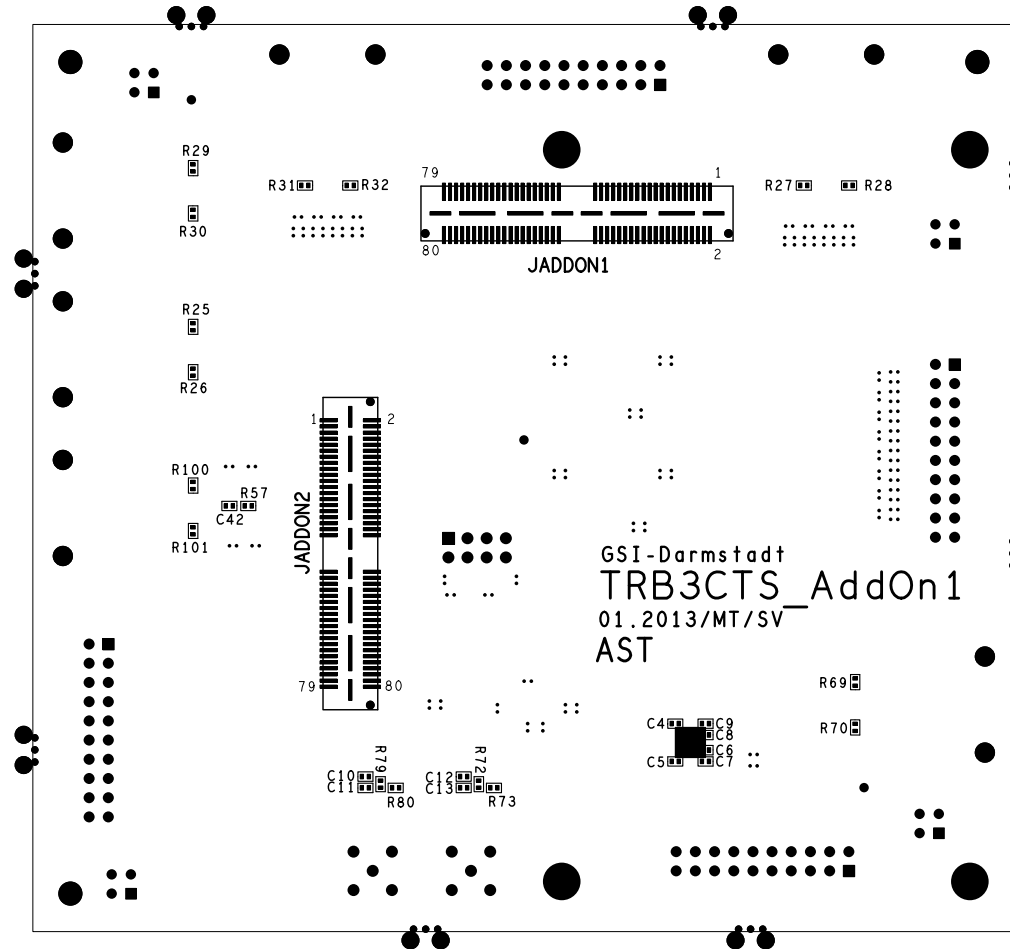
Bestueckungsrand umlaufend 10mm



Jobname	Date	Designer	Layouter
TRB3CTS_Add0n1	01.2013	J.Michel/M.Traxler	S.Voltz

Layer Nickname

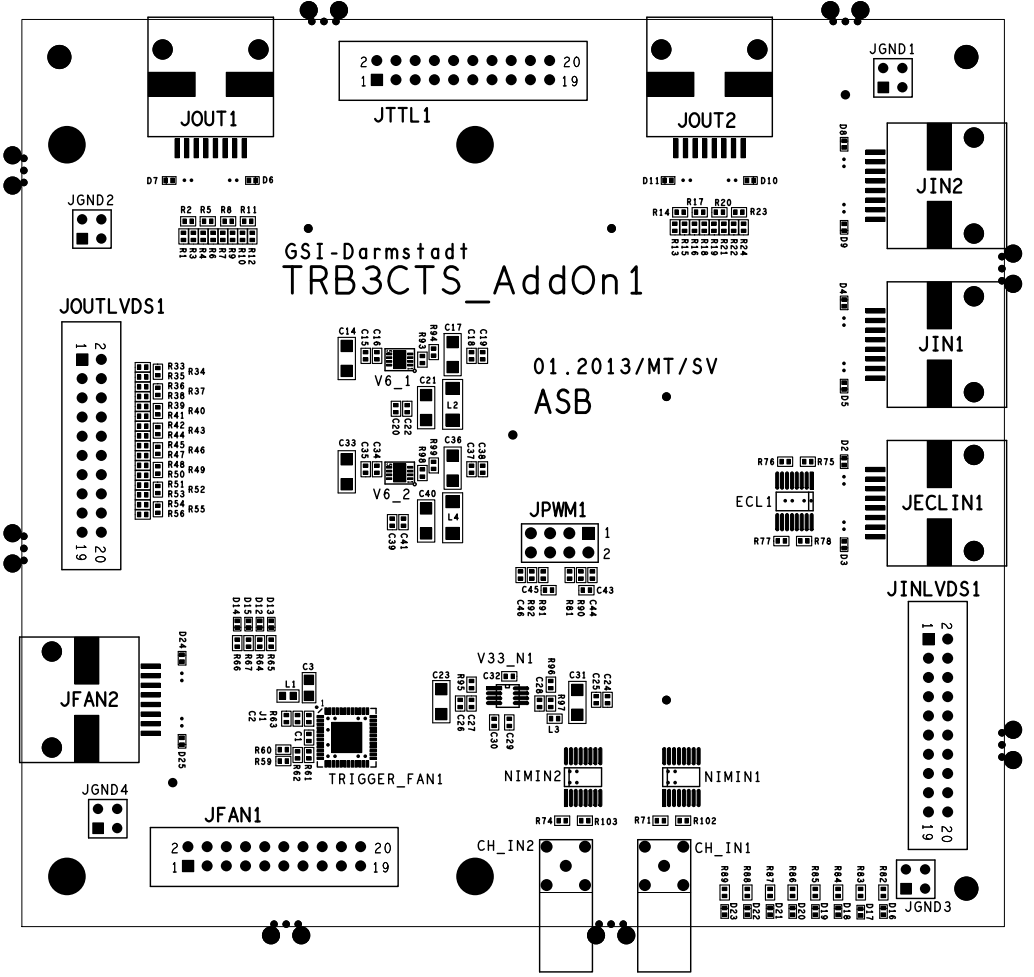
Fab



Jobname	Date	Designer	Layouter
TRB3CTS_AddOn1	01.2013	J.Michel/M.Traxler	S.Voltz

Layer Nickname

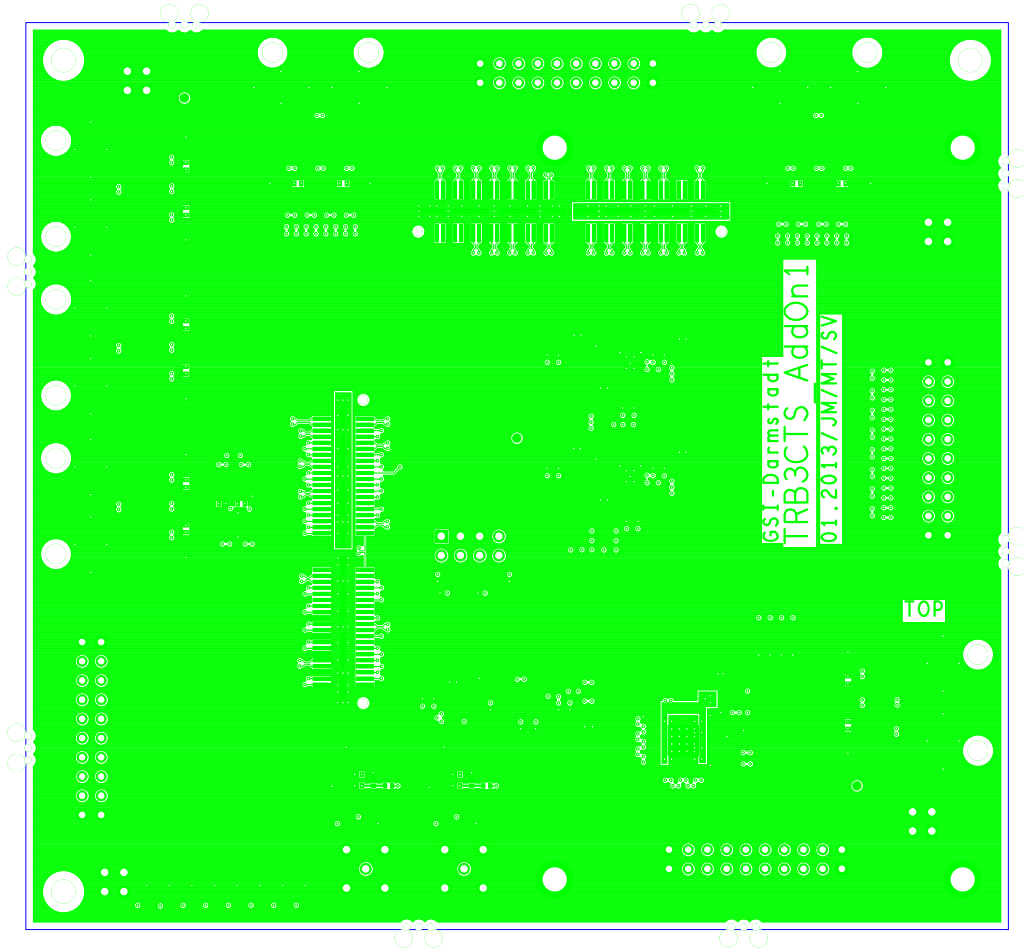
Ast



1. Michael Traxler
 Designer
 01.2013
 Date
 TRB3CTS_AddOn1
 Topname
 2. Volker
 Layouter

2x A

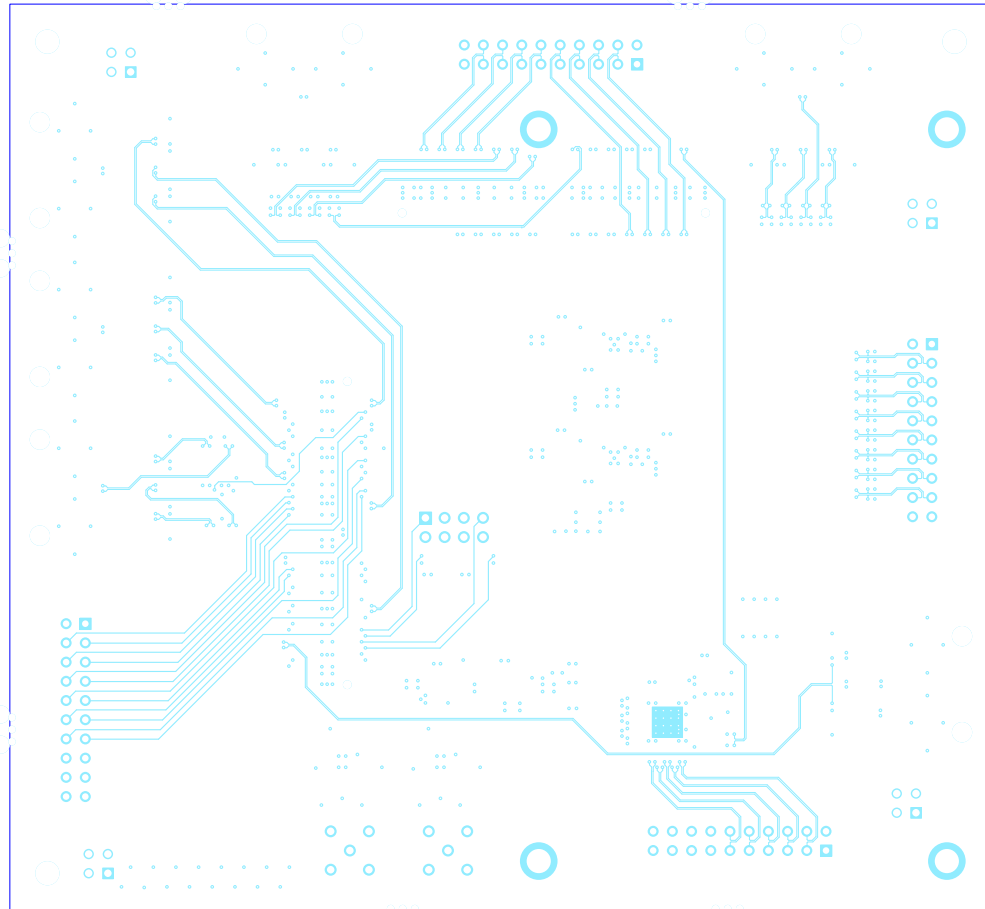
TOP- GND-Plane



Jobname	Date	Designer	Layouter
TRB3CTS_AddOn1	01.2013	J.Michel/M.Traxler	S.Voltz

Layer Nickname	Top
----------------	-----

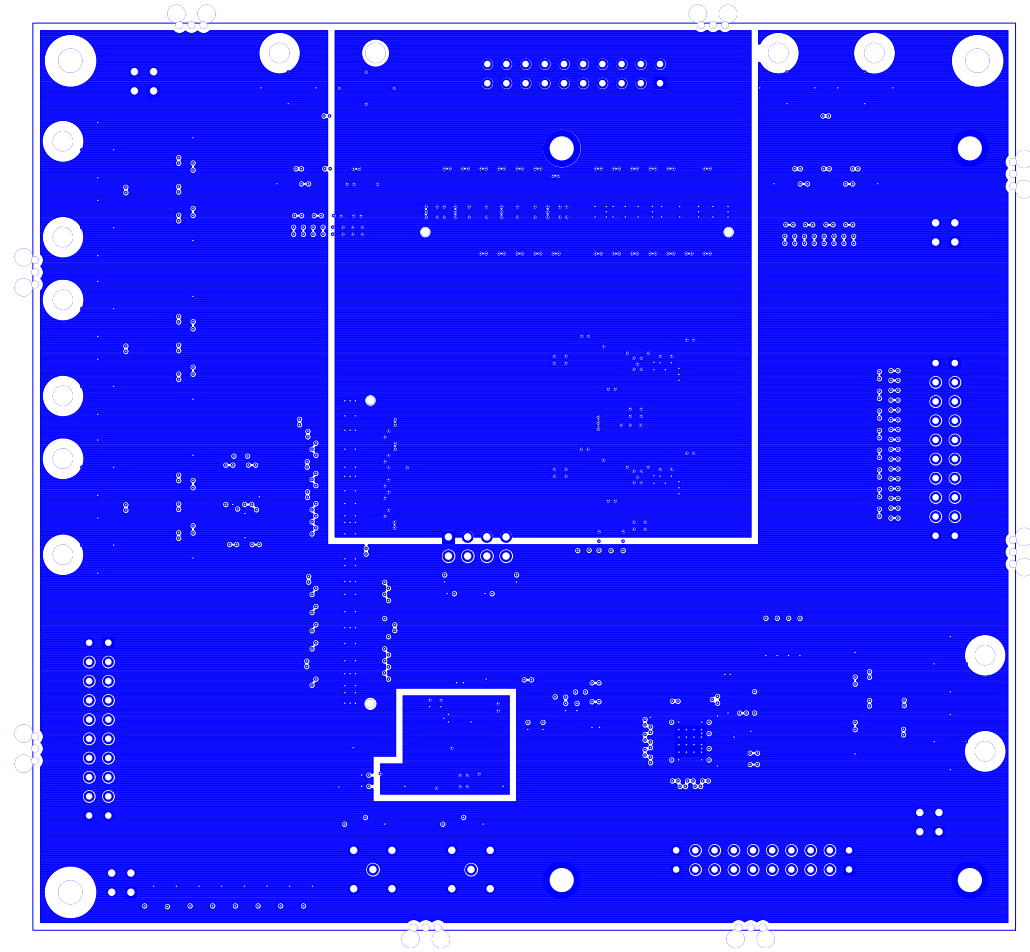
IN1- Diff



Jobname	Date	Designer	Layouter
TRB3CTS_AddOn1	01.2013	J.Michel/M.Traxler	S.Voltz

Layer Nickname
I01

IN2- Planes: +6V, -2V, GND

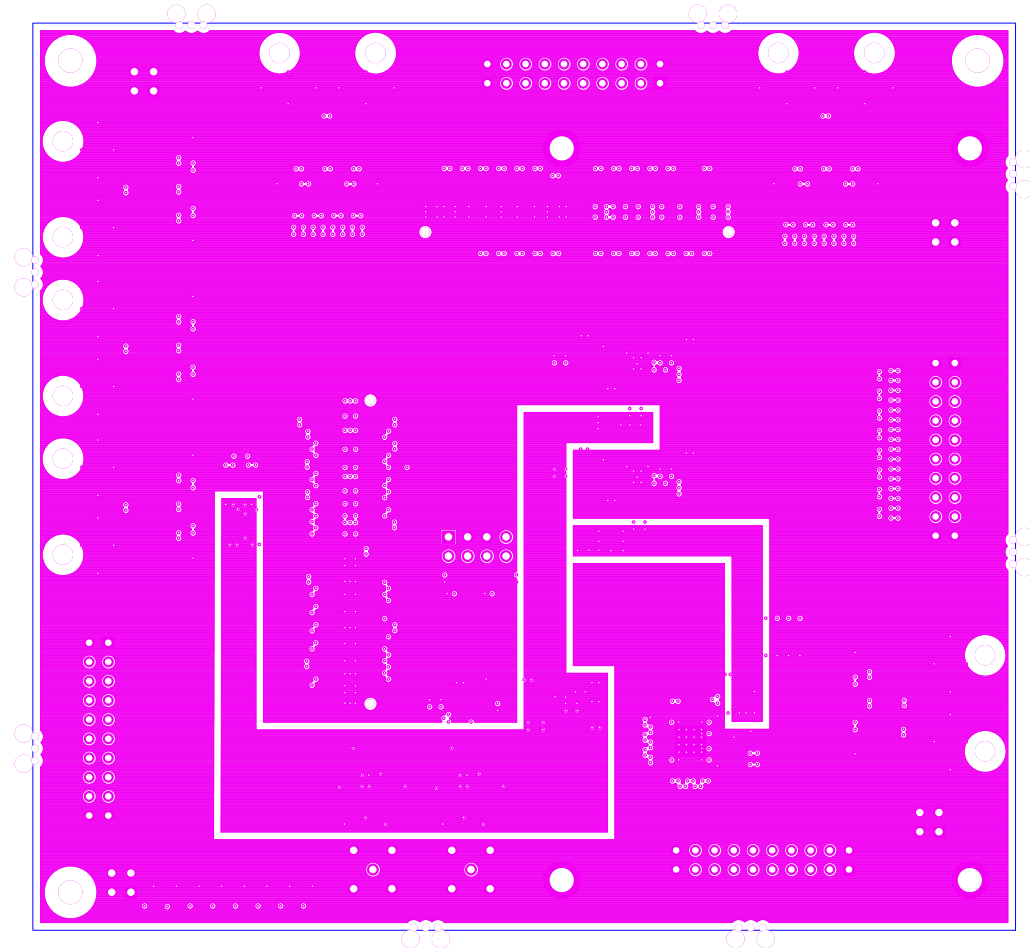


Jobname	Date	Designer	Layouter
TRB3CTS_AddOn1	01.2013	J.Michel/M.Traxler	S.Voltz

Layer Nickname

102

IN3- Planes: 3.3V, 2.5V, GND

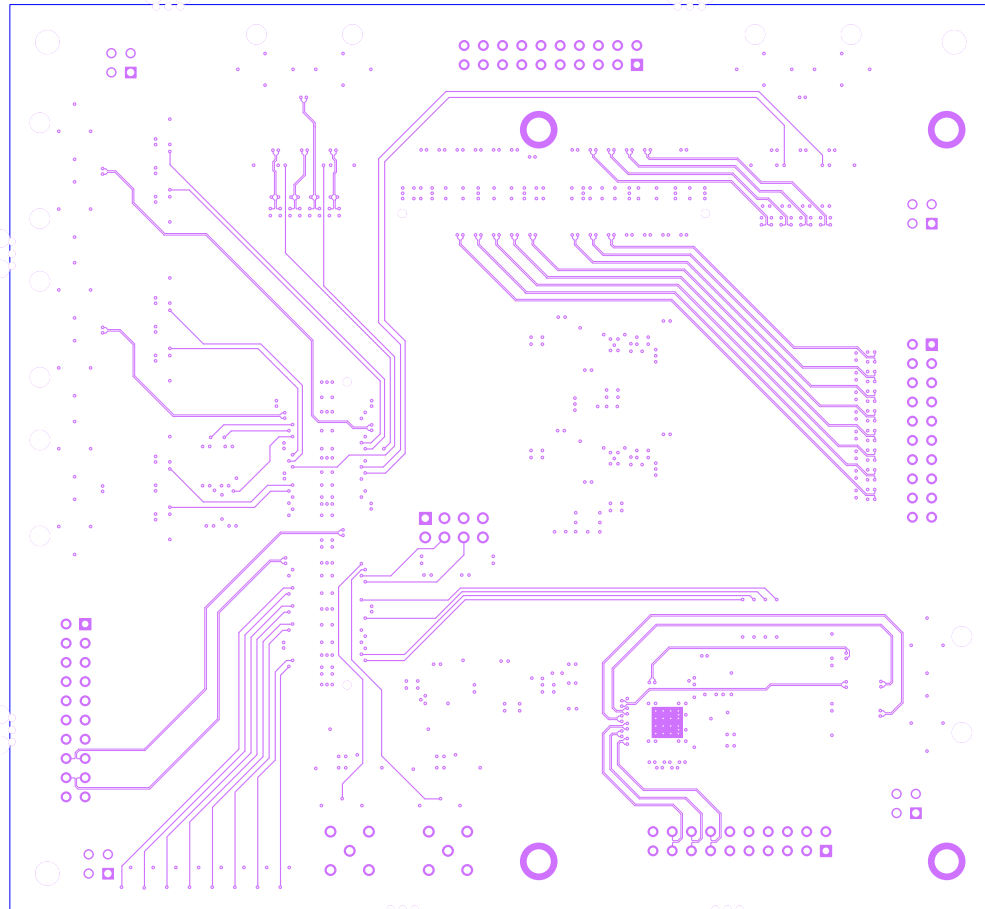


Jobname	Date	Designer	Layouter
TRB3CTS_AddOn1	01.2013	J.Michel/M.Traxler	S.Voltz

Layer Nickname

103

IN4- Diff

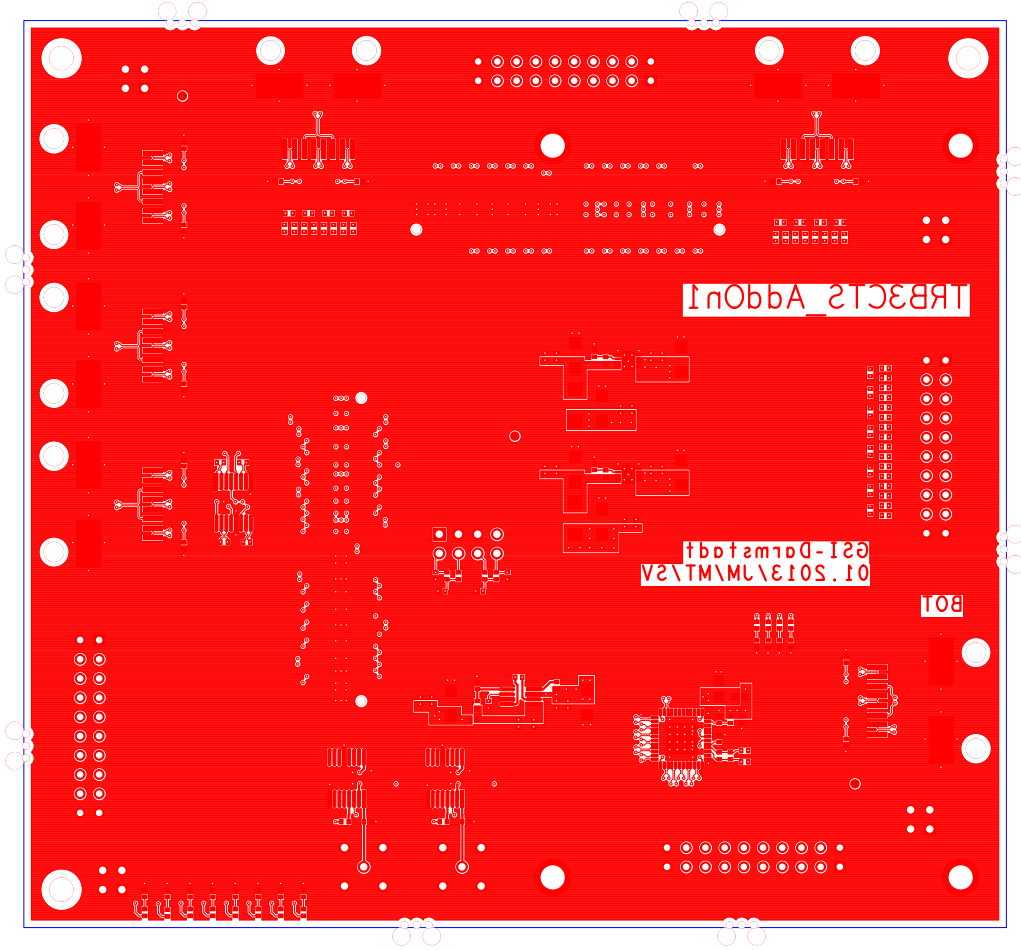


Jobname	Date	Designer	Layouter
TRB3CTS_AddOn1	01.2013	J.Michel/M.Traxler	S.Voltz

Layer Nickname

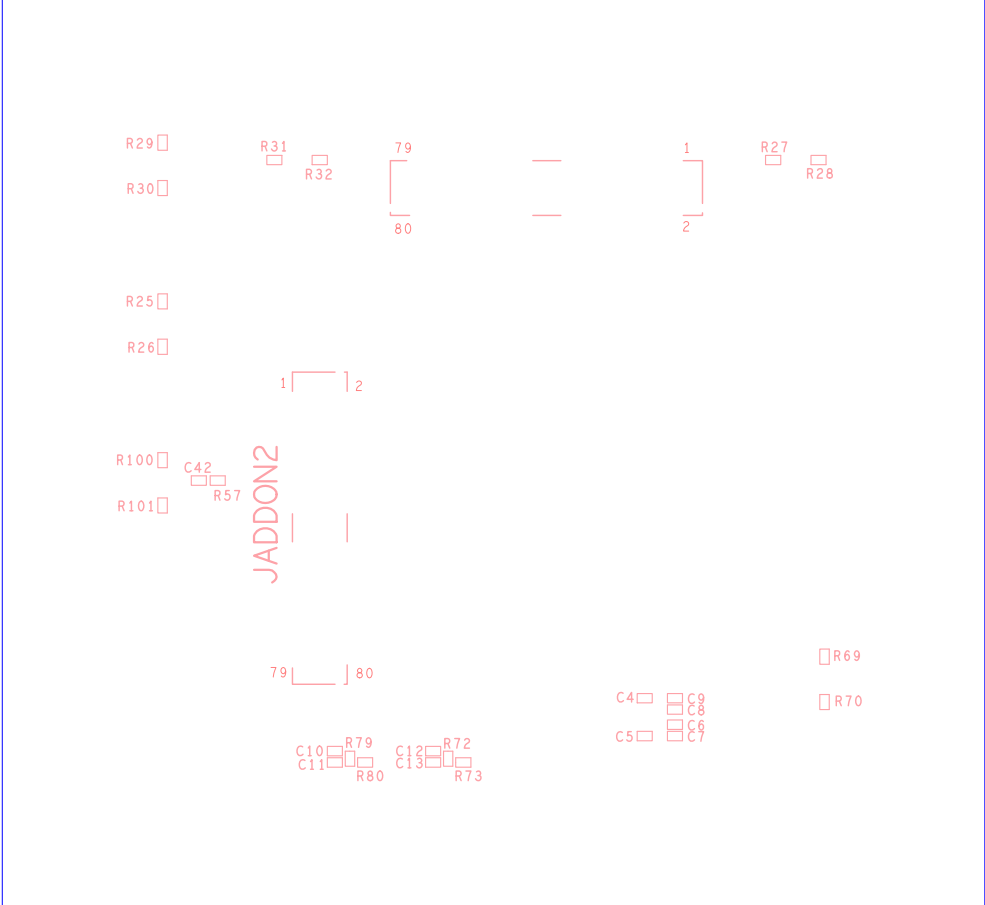
I04

BOT- GND-Plane



Jobname	Date	Designer	Layouter
TRB3CTS_AddOn1	01.2013	J.Michel/M.Traxler	S.Voltz

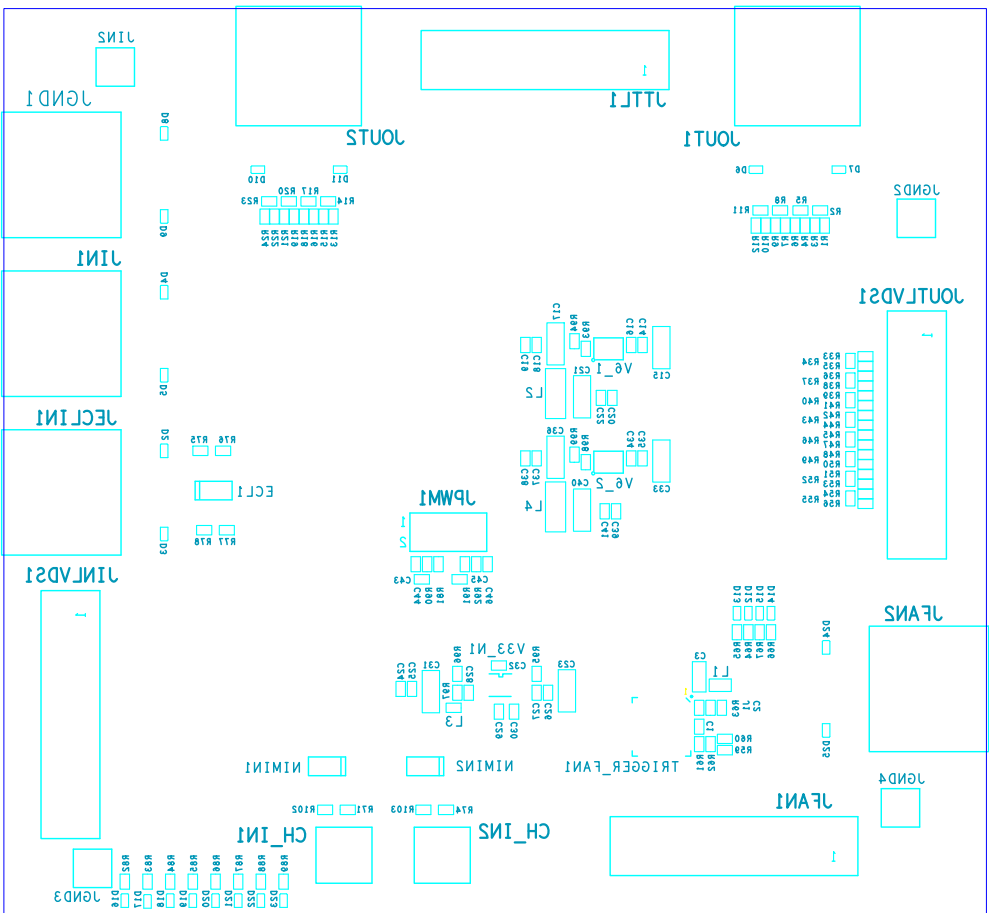
Layer Nickname	Bot
----------------	-----



Jobname	Date	Designer	Layouter
TRB3CTS_AddOn1	01.2013	J.Michel/M.Traxler	S.Voltz

Layer Nickname

Sst



Jobname TRB3CTS_AddOn1 Date 01.2013 Designer J.Michel/M.Traxler Layouter S.Voltz

Layer Nickname

Ssb

Material (µm)

Stack up

File

Assembly

25 Galvanic CU
9 Copper

107 NP-155F-B

98 NP-155F-B

17 Copper

400 NP-155F-TL

17 Copper

100 NP-155F-B

100 NP-155F-B

17 Copper

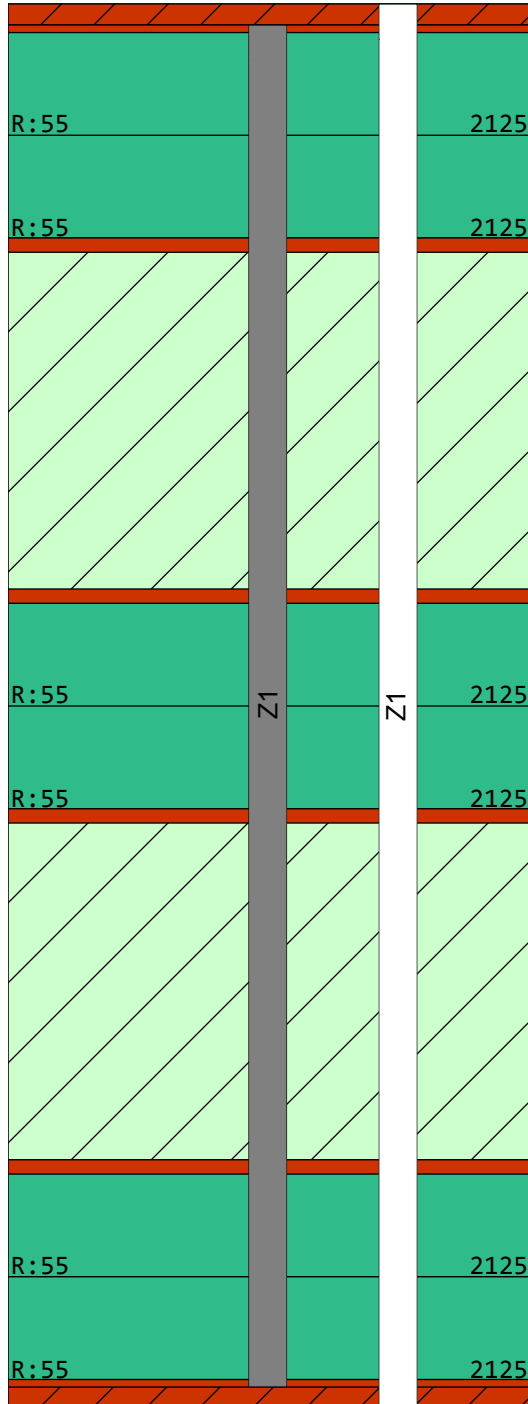
400 NP-155F-TL

17 Copper

98 NP-155F-B

107 NP-155F-B

9 Copper
25 Galvanic CU



BS

2125

2125

I2

I3

2125

2125

I4

I5

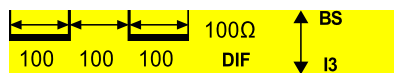
2125

2125

LS

A1

i2



i5

