Technical Information Manual

Revision n. 1

22 April 2002

MOD. V 878

32-CHANNEL TIME-TO-DIGITAL CONVERTER

NPO:
00103/99:V878x.MUTx/01

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

1. General description

1.1. Overview

The **Model V878** is a 1-unit wide VME 6U module housing 32 Time-to-Digital Conversion channels.

The board can operate both in COMMON START and COMMON STOP mode. It accepts 32 individual differential ECL inputs (one for each channel) and one COM input (ECL or NIM) common to all channels. Each time interval between the COM signal and the input channels is converted into a voltage level by the TAC sections. The outputs of the TAC sections are multiplexed and subsequently converted by a fast 12-bit ADC module (10 µs for all channels). The ADC module uses a sliding scale technique to reduce the differential non-linearity.

Programmable zero suppression, multievent buffer memory, trigger counter and test features complete the flexibility of the unit.

The module works in A24/A32 mode. The data transfer occurs in D16, D32, BLT32 or MBLT64 mode. The unit supports also the Chained Block Transfer and the Multicast commands.

The V878 module is live insertable, i.e. the user can insert (or remove) the board into (or from) the crate without switching it off.

The V878 board uses the VME P1 and P2 connectors and the auxiliary connector (PAUX) for the CERN V430 VMEbus crate.

1.2. Block diagram

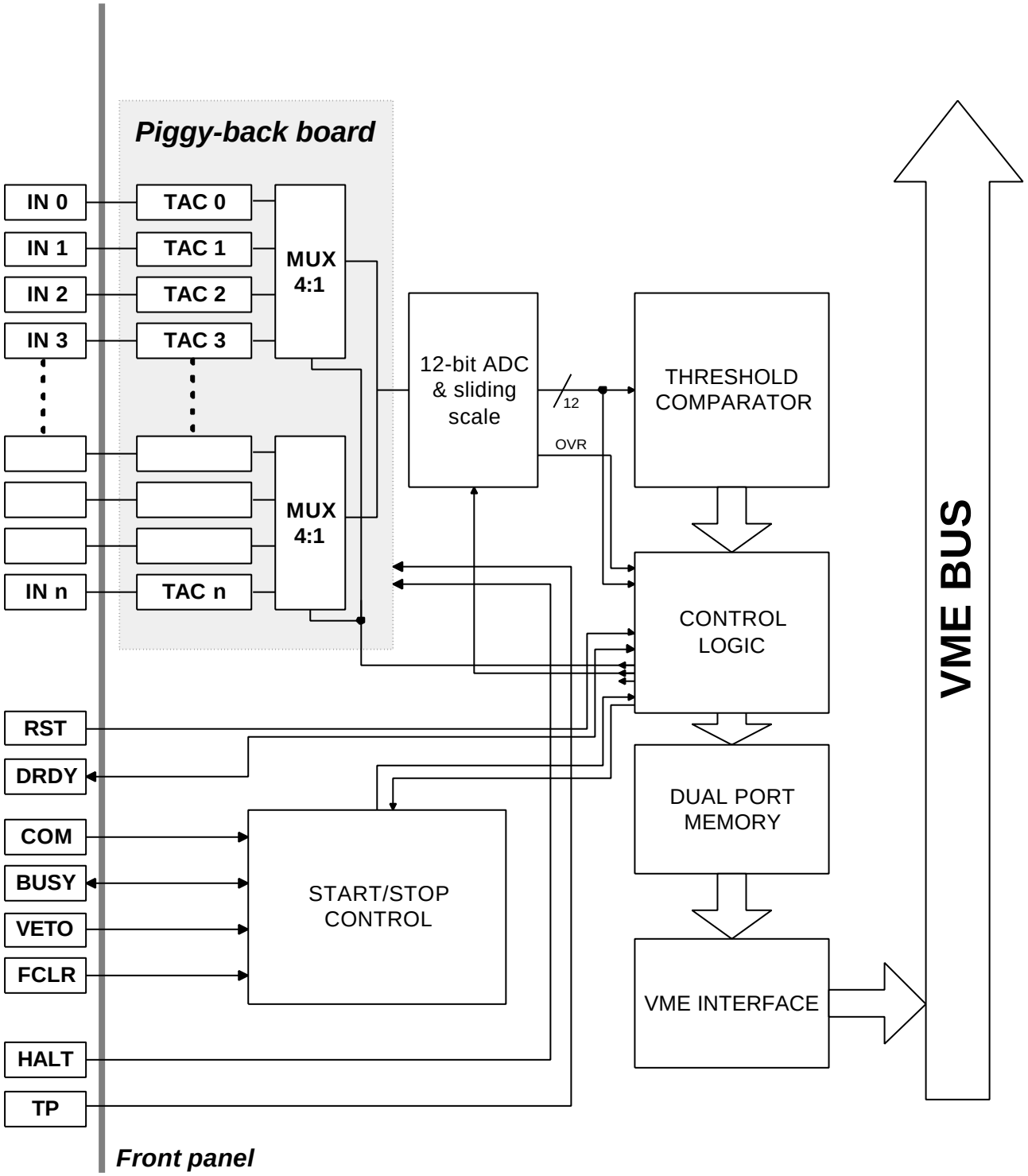

Fig. 1.1: Model V878 Block Diagram

1.3. Functional description

The board has 32 differential ECL inputs (one for each channel) and one differential ECL common input (COM input). The COM input can be also sent in as NIM signal through a couple of 00-type LEMO connectors which allow easy daisy-chaining of several modules.

The block diagram of the module is shown in Fig. 1.1.

The module can work both in COMMON START and in COMMON STOP mode, according to the operating mode selected by the user (bit 10 (COMM STOP) of the Bit Set 2 Register, see § 3.27).
Each time interval between the COM signal and the input channel signals is converted into a voltage level by the TAC sections. The outputs of the TAC sections are multiplexed and subsequently converted by a fast 12-bit ADC (10 µs for all channels).

The ADC adopts a sliding scale technique (see Ref. [1],[2]) to reduce the differential non-linearity of the measurement. Refer to § 5.2 for further details.

The module features zero and overflow suppression, i.e. only the values that are above a programmable level and do not cause overflow are stored in the dual port data memory accessible via VME. It is also possible to disable some channels via the KILL option (see § 5.3).

Besides COMMON START and COMMON STOP modes, some test modes are available and programmable via VME. Refer to § 6.3.2 for further details.

The unit accepts the following CONTROL signals (differential ECL, 110 Ω) in common to all channels (see Front Panel, Fig. 2.1):

- **COM**: input signal, common to all channels, acting as start/stop signal for data acquisition;
- **FCLR**: FAST CLEAR input signal, sent after the leading edge of the COM signal within a programmable window ending 10÷35 µs after the trailing-edge of the COM signal; it clears the TAC sections of the unit and aborts completely the conversion in progress;
- **RST**: clears the TAC sections, resets the Multi-Event Buffer status, stops pending ADC conversions and, depending on the user's settings (see §3.14), may reset the control registers;
- **VETO**: common input signal that inhibits the conversions of the signals from all channels;
- **HALT**: control input signal to the piggy-back;
- **TP**: input signal to the piggy-back;

Two special signals (**BUSY** and **DRDY**) are also available on the CONTROL bus.
The BUSY is a differential ECL signal corresponding to the wired-OR/NAND Global Busy signal of the boards connected to the same CONTROL bus. The Busy status indicates that the board is either full or converting or resetting or in MEMORY TEST mode.
The DRDY as well is a differential ECL signal corresponding to the wired-OR/NAND Global Data Ready signal of the boards connected to the same chain on the Control bus. A Data Ready status indicates the presence of data (at least one event, see §5.5) in the output buffer of the board.

All the above described control lines can be terminated on-board via internal DIP switches. Terminations must be inserted only on the last board in the bus. The status of the

terminations is available both on the front panel TERM LED and in an internal VME register (Status Register 1, see § 3.13).

Five front panel LEDs show the status of the unit (see Front Panel, Fig. 2.1):

- **DTACK** (green) lights up each time the module asserts the VME DTACK;
- **BUSY** (red) lights up each time the module is performing a conversion, when resetting the TAC section, when the Multi-Event Buffer is full or the module is in MEMORY TEST mode; it also lights up for a while at power-on to indicate that the board is configuring;
- **DRDY** (yellow) lights up when at least one event is present in the output buffer; it also lights up for a while at power-on to indicate that the board is configuring;
- **TERM** (orange/green/red) lights up green when all lines of the Control bus are terminated, red when no line of the control bus is terminated and does not light up when only some lines are terminated; it also lights up orange for a while at power-on to indicate that the board is configuring;
- **OVC/PWR** (green/orange) lights up orange to indicate an over-current situation and lights up green when the board is inserted into the crate and the crate is powered up;

Some of these LEDs light up at power-on to indicate that the board is configuring; after a little time these LEDs light off to indicate that the board is ready to operate. For details please refer to the Power-ON section (§ 6.1).

The board houses a 24-bit counter (Event Counter) that allows to count either the accepted Triggers, i.e. it is increased each time a pulse is sent through the COM input and accepted (VETO, FCLR and BUSY are not active), or all incoming Triggers. In the latter case the Event Counter acts also as an absolute time counter.
Via VME it is also possible to:

- Set a low threshold for the Zero suppression for each channel;
- Enable or disable the Zero/Overflow suppression;
- Disable some of the channels (KILL option);
- Increase the delay between the trailing edge of the COM signal and the start of conversion (Fast Clear window).

The module may be addressed in 3 different ways:

1. By Base Address;
2. By GEOgraphical address;
3. By Multicast/Chained Block Transfer addressing.

In the first case the module's Base Address can be fixed either by 4 rotary switches or by writing it in a couple of registers, the internal Address DEcoder Registers ADER HIGH and ADER LOW (see §3.15 and 3.16). Refer to §3.1.1 for further details on addressing via Base Address.

Geographical addressing can be used thanks to the PAUX connector: the geographical address is automatically read out at each RESET from the JAUX connector of the V430 VME crate and each slot is identified by a number (GEO) that is unique within the crate. This addressing mode is performed with the 0x2F Address Modifier code (i.e. only an A24 addressing mode is allowed). This addressing mode is recommended to perform module settings. Refer to § 3.1.2 for further details on addressing via geographical address.

Multicast/Chained Block Transfer addressing modes are also supported. Refer to § 3.1.4 for further details on this subject.

Data transfer occurs in D16, D32, BLT32 or MBLT64. The module supports also the Chained Block Transfer mechanism (CBLT) and the Multicast commands (MCST).

The V878 module is equipped with a special circuitry that allows the board to be removed from a powered crate without switching the crate off. Moreover, it is possible to switch the module off without cutting the interrupt chain off.

A detailed description of functional blocks and principles of operation can be found in § 5.

1.4. Technical specification table

Table 1.1 - Model V878 main technical specifications

Packaging	6U-high, 1U-wide VME unit (V430 backplane required)
Power requirements	• -2 V 800 mA • -5 V < 100 mA • +5 V < 100 mA • ±12 V 160 mA
Number of channels	32 differential ECL inputs, 110 Ω imp.
Power on time	140 ms
Internal clock frequency	32 MHz
Fast Clear intervention	< 500 ns + t_{clear}
Conversion time	10 µs + $t_{fastclear}$ for all channels (*)
Low Level Threshold	from 0 to 99% of FSR for each channel
Control inputs	active-high, diff. ECL input signals, 110 Ω imp.: **COM:** START/STOP signal for data acquisition (ECL/NIM). **RST:** resets TAC sections, MEB status and control registers. **VETO:** inhibits the conversion of the input values. **FCLR:** FAST CLEAR of the TAC sections and conversion. **HALT:** control signal to the piggy-back. **TP:** control signal to the piggy-back.
Control outputs	diff. ECL output signals: **BUSY:** wired-OR/NAND Global Busy. **DRDY:** wired-OR/NAND Global Data Ready.
Displays	**DTACK:** green LED; lights up at each VME access. **BUSY**: red LED; alight during conversion, reset or Memory Test mode or as the MEB is full. **DRDY**: yellow LED; alight as there is one event in the MEB. **TERM**: orange/green/red LED; alight according to line terminations status. **OVC/PWR**: green/orange LED; green at board insertion; if orange, it indicates that there is an over-current status.

(*) $t_{fastclear}$ *is VME programmable, see § 3.26.*

2. Technical specifications

2.1. Packaging

The Model V878 is housed in a 6U-high, 1U-wide VME unit. The board hosts the VME P1, P2 connectors and the PAUX connector.

The board requires the VME V430 backplane.

2.2. Power requirements

The power requirements of Mod.V878 are as follows:

-2 V	800 mA
-5 V	< 100 mA
+5 V	< 100 mA
±12 V	160 mA

2.3. Front Panel

The front panel of the Mod. V878 is shown in Fig. 2.1.

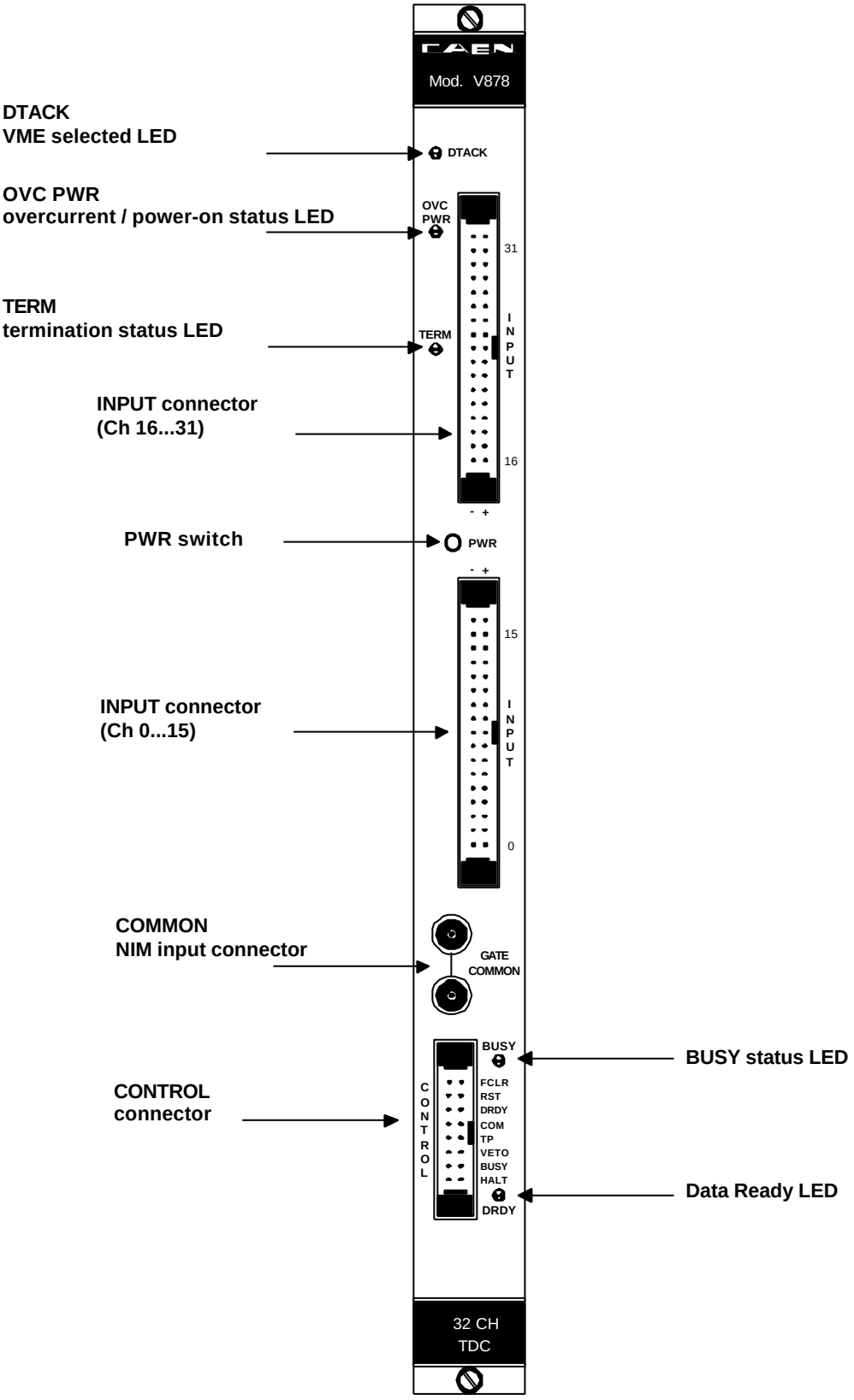

Fig. 2.1: Model V878 front panel

2.4. External connectors

The location of the connectors is shown in Fig. 2.1.
Their function and electro-mechanical specifications are listed in the following subsections.

2.4.1. INPUT connectors

Mechanical specifications:
two 17+17-pin, 3M 3431-5202 Header-type connectors.

Electrical specifications:
differential ECL input signals on 110-Ω impedance; min. width: 10 ns.

2.4.2. CONTROL connector

Mechanical specifications:
two 8+8-pin, 3M 3408-5202 Header-type connectors.

Electrical specifications:
differential ECL signals; 110-Ω impedance. Pin assignment is shown in Fig. 2.2.

FCLR: *Electrical specifications:* active-high, diff. ECL input signal, 110-Ω impedance; min. width: 10 ns.
Function: FAST CLEAR signal, accepted if sent within the so-called FAST CLEAR window (see Fig. 5.6). This window starts with the leading edge of the COM signal and ends with a programmable delay (10÷35 μs) with respect to the trailing-edge of the COM signal; it clears the TAC sections of the unit and aborts completely the conversion in progress. After a FAST CLEAR, a COM signal can occur only after 600 ns.

RST: *Electrical specifications:* active-high, diff. ECL input signal, 110-Ω impedance; min. width: 30 ns.
Function: clears the TAC sections, resets the Multi-Event Buffer status, stops pending ADC conversions and, depending on the user's settings (see PROG RESET, §3.14), may clear the control registers.

DRDY: *Electrical specifications:* diff. ECL output signal.
Function: wired-OR/NAND Global Data Ready signal from the boards belonging to the same chain on the CONTROL bus: DATA READY indicates the presence of data in the output buffer of the board.

COM: *Electrical specifications:* active-high, diff. ECL input signal; 110-Ω impedance.
Function: input pulse, common to all channels, to control data acquisition timing. If a FAST CLEAR signal is sent in, the following COM signal must occur at least about 600 ns after the FAST CLEAR signal.

TP: *Electrical specifications:* active-high, diff. ECL input signal, 110-Ω impedance.
Function: TEST PULSE control signal to the piggy-back board.

VETO: *Electrical specifications:* active-high, diff. ECL input signal, 110-Ω impedance; min. width: 30 ns.
Function: inhibits the conversion of the detected signals.

BUSY: *Electrical specifications:* diff. ECL output signal.
Function: wired-OR/NAND Global Busy signal from the boards belonging to the same chain on the CONTROL bus: a BUSY status indicates that the board is either converting or resetting or in MEMORY TEST mode or the MEB is full.

HALT: *Electrical specifications:* active-high, diff. ECL input signal, 110-Ω impedance.
Function: control signal to the piggy-back board.

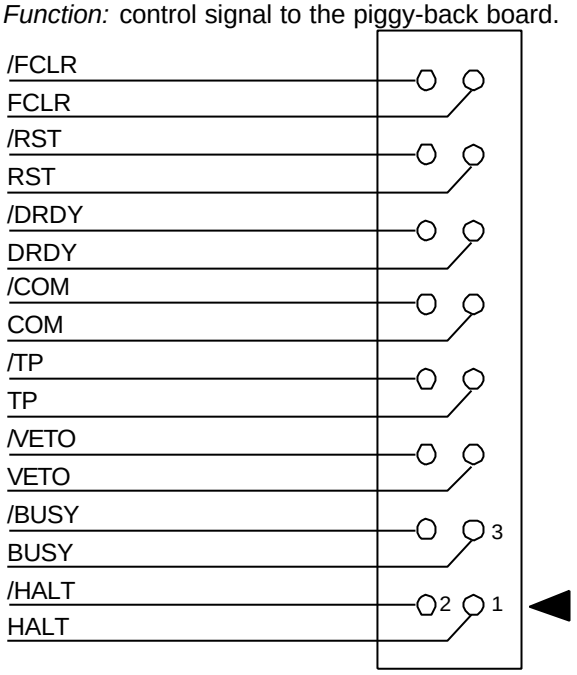

Fig. 2.2: CONTROL connector pin assignment

2.4.3. COMMON connectors

Mechanical specifications:
two 00-type LEMO connectors.
Electrical specifications:
NIM std. input signals; high impedance. If used in daisy-chain configuration, a 50-Ω termination must be inserted on the last board of the chain.

COMMON: *Function:* input signal, common to all channels, to control data acquisition timing. This signal is internally OR-wired with the COM of the CONTROL connector.

2.5. Other front panel components

2.5.1. Displays

The front panel (refer to Fig. 2.1) hosts the following LEDs:

DTACK: *Colour:* green.
Function: DATA ACKNOWLEDGE command; it lights up each time a VME access is performed.

BUSY: *Colour:* red.
Function: it lights up each time the module is performing a conversion or resetting the TAC section or in MEMORY TEST mode or when the Multi-Event Buffer is full; it also lights up for a while at power-on to indicate that the board is configuring.

DRDY: *Colour:* yellow.
Function: it lights up when at least one event is present in the output buffer; it also lights up for a while at power-on to indicate that the board is configuring.

TERM: *Colour:* orange/green/red.
Function: it lights up green when all the lines of the control bus are terminated, red when no line of the control bus is terminated. If only some lines are terminated, it is off. It also lights up orange for a while at power-on to indicate that the board is configuring.

OVC/PWR: *Colour:* green/orange.
Function: it lights up green when the board is inserted into the crate and the crate is powered up; when it is orange, it indicates that there is an over-current status: in this case, remove the overload source, switch the module off and then switch it on again.

2.5.2. Switches

PWR: *Type:* miniature flush plunger push-button switch.
Function: after the insertion of the board into the crate, it allows to turn the board on/off by pushing it with a pin. Refer to §6.1 for the power-on procedure.

2.6. Internal hardware components

The V878 board is constituted by a motherboard with a piggy-back board plugged into it (see also Fig. 1.1 where the functional blocks hosted on the piggy-back board are pointed out).
In the following some hardware setting components, located on the boards, are listed. Refer to Fig. 2.3 for their exact location on the PCB and their settings.

2.6.1. Switches

ROTARY SWITCHES: *Type:* 4 rotary switches.
Function: they allow the VME addressing of the module. Please refer to Fig. 2.3 for their settings.

TERM ON: *Type:* 14 DIP switches, a couple (positive and negative) for each control signal.
Function: they allow the insertion of the Bus termination on the relevant line. The 110 Ω-termination must be inserted on the lines of the last board of the chain. In order to insert the termination on a given line, both the positive and the negative DIP switches must be inserted. If the termination is inserted on all the lines of the board, the TERM LED is green; if none of the terminations is inserted, the TERM LED is red. If only some terminations are inserted, the LED is off. Please refer to Fig. 2.3 for their settings.

Right position (dot visible): the termination is inserted on the relevant line;

Left position (dot not visible): the termination is not inserted.

CAUTION

IN ORDER TO INSERT A TERMINATION ON A LINE, BOTH THE POSITIVE AND THE NEGATIVE DIP SWITCH MUST BE SET!

2.6.2. Jumpers

J9: *Function:* it allows to select board behaviour in response to a BUSY status:

Position A (high, INTBSY): data acquisition is stopped as the board is BUSY, independently from the status of the other boards on the CONTROL Bus;
Position B (low, EXTBSY): data acquisition is stopped as soon as any of the boards on the CONTROL Bus is BUSY.

Refer to Fig. 2.3 for the exact location of the jumper on the PCB and its setting.

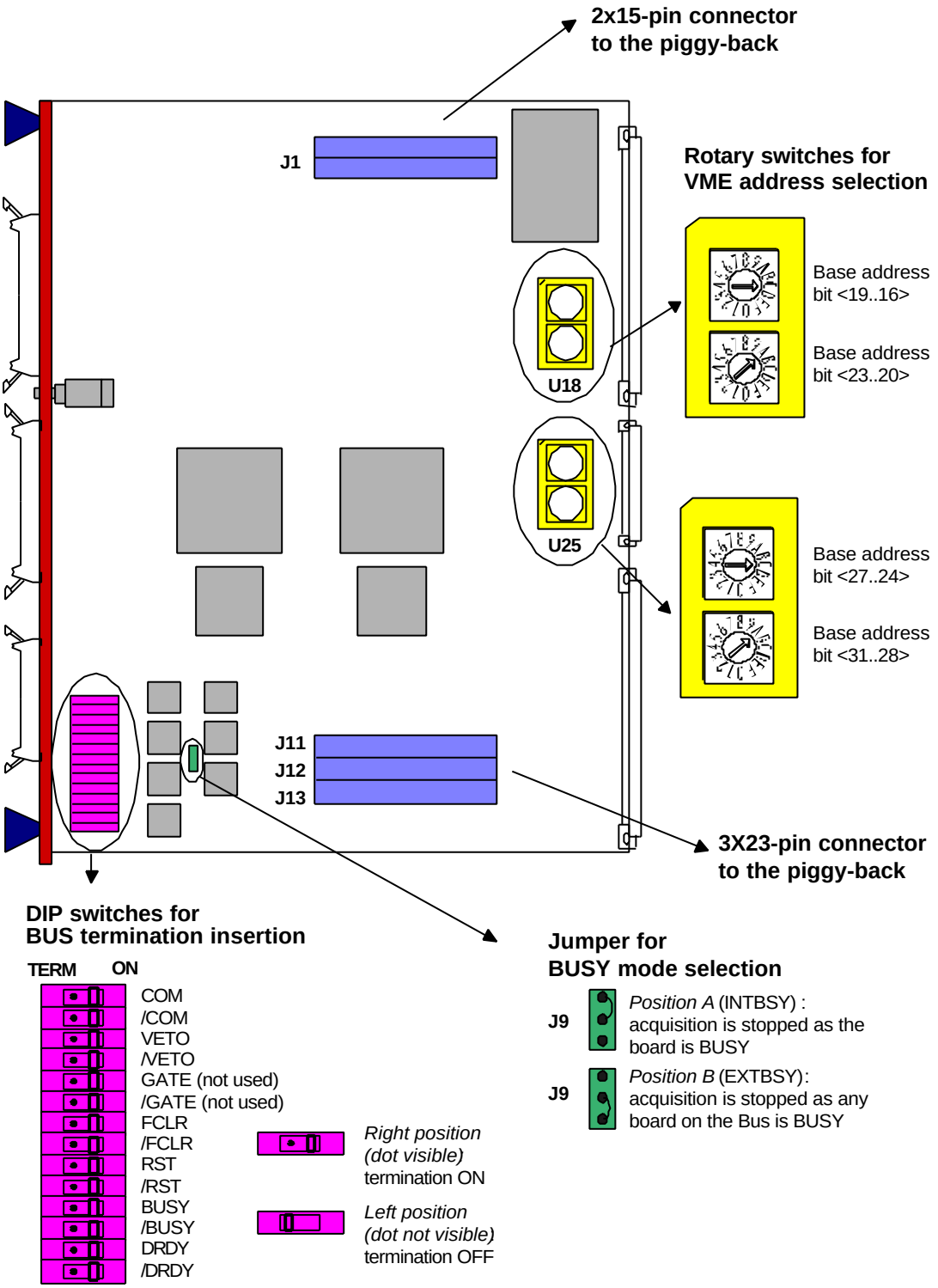

Fig. 2.3: Component Location (component side)

2.7. Performances and test results

Packaging	6U-high, 1U-wide VME unit (V430 backplane required)
Power requirements	• -2 V 800 mA • -5 V < 100 mA • +5 V < 100 mA • ±12 V 160 mA
Number of channels	32 differential ECL inputs
Power on time	140 ms
Internal clock frequency	32 MHz
Fast Clear intervention	< 500 ns + t_{clear}
Conversion time	10 µs + $t_{fastclear}$ for all channels
Low Level Threshold	from 0 to 99% of the full-scale range for each ch.

3. VME interface

3.1. Addressing capability

The modules can be addressed in three different ways, specifically:

1. via Base Address;
2. via GEOgraphical address;
3. via Multicast/Chained Block Transfer addressing mode.

3.1.1. Addressing via Base Address

The module works in A24/A32 mode. This implies that the module's address must be specified in a word of 24 or 32 bit. The Address Modifier codes recognised by the module are summarised in Table 3.1.

Table 3.1: Module recognised Address Modifier

A.M.	Description
0x3F	A24 supervisory block transfer (BLT)
0x3D	A24 supervisory data access
0x3C	A24 supervisory 64 bit block transfer (MBLT)
0x3B	A24 non privileged block transfer (BLT)
0x39	A24 non privileged user data access
0x38	A24 non privileged 64 bit block transfer (MBLT)
0x2F	Configuration ROM/Control & Status Register (CR/CSR)
0x0F	A32 supervisory block transfer (BLT)
0x0D	A32 supervisory data access
0x0C	A32 supervisory 64 bit block transfer (MBLT)
0x0B	A32 non privileged block transfer (BLT)
0x09	A32 non privileged data access
0x08	A32 non privileged 64 bit block transfer (MBLT)

The Base Address can be selected in the range:

0x000000	←→	0xFF0000	A24 mode
0x00000000	←→	0xFFFF0000	A32 mode

The Base Address of the module can be fixed in two ways:

- by four rotary switches;
- by writing the Base Address in the ADER_HIGH and ADER_LOW registers.

The 4 rotary switches for Base Address selection are housed on two piggy-back boards plugged into the main printed circuit board (see Fig. 2.3).

To use this addressing mode the bit 4 of the Bit Set 1 Register (see § 3.9) must be set to 0. This is also the default setting.

The module Base Address can be also fixed by using the Ader_High and Ader_Low Registers. These two registers set respectively the A[31:24] and the A[23:16] VME address bits (see § 3.15 and 3.16).
To use this addressing mode bit 4 of the Bit Set 1 Register (see § 3.9) must be set to 1.This must be the last operation to be done (if the GEO is not used).

3.1.2. Addressing via GEOgraphical address

The module works in A24 mode only. The Address Modifiers codes recognised by the module are:

AM=0x2F: A24 GEO access

All registers except for the Output Buffer (i.e. the CR/CSR area) can be accessed via geographical addressing.
The geographical address is automatically read out at each RESET from the SN5..SN1 lines of the PAUX connector. Each slot of the VME crate is identified by the status of the SN5...SN1 lines: for example, the slot #5 will have these lines respectively at 00101 and consequently the module inserted in the slot #5 will have a GEO address set to 00101 (see Fig. 3.1).
The complete address in A24 mode for geographical addressing is:

A[31:24]	**don't care**
A[23:19]	**GEO**
A[18:16]	**0**
A[15:0]	**offset**

The following two figures show the binary and the hexadecimal representation of, respectively, the board Address and a Register Address (Bit Set 1 Register) in GEO addressing mode.

23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
0	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	Binary representation
2				8				0				0				0				0				Hexadecimal representation

Fig. 3.1: Binary-Hexadecimal representation of the board Address in GEO mode

23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
0	0	1	0	1	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	1	1	0	Binary representation
2				8				1006(offset)																Hexadecimal representation

Fig. 3.2: Binary-Hexadecimal representation of Bit Set 1 Register Address in GEO mode

The geographical addressing mode is suggested to perform module settings.

3.1.3. Base/GEO addressing examples

The following is an example of Base/GEO Addressing for two V878 boards inserted in a VME crate.

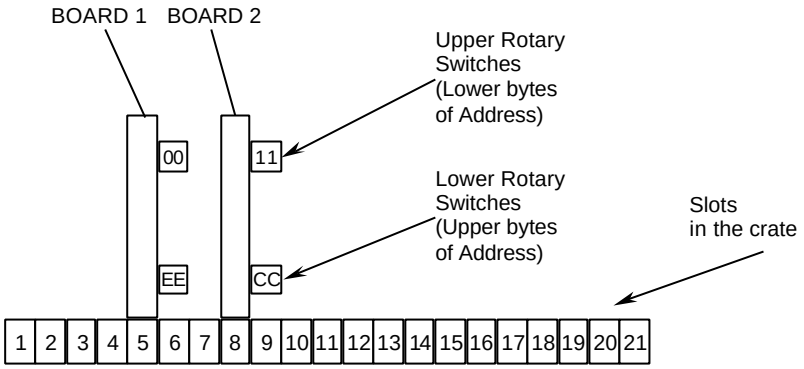

Fig. 3.3: Base/GEO Addressing: Example

If the board 1 and board 2 are respectively inserted in the slots 5 and 8 with the rotary switches for VME Base Addressing set as shown in the figure, the complete address of the registers of the two boards will be as follows:

Board 1:
Base addressing A32: 0xEE000000 + offset
Base addressing A24: 0x000000 + offset
GEO addressing A24: 0x280000 + offset (Output Buffer excluded).

Board 2:
Base addressing A32: 0xCC110000 + offset
Base addressing A24: 0x110000 + offset
GEO addressing A24: 0x400000 + offset (Output Buffer excluded).

3.1.4. MCST/CBLT addressing

When the Multicast/Chained Block Transfer addressing mode is adopted, the module works in A32 mode only. The Address Modifiers codes recognised by the module are:

AM=0x0F: A32 supervisory block transfer (CBLT)
AM=0x0D: A32 supervisory data access (MCST)
AM=0x0B: A32 user block transfer (CBLT)
AM=0x09: A32 user data access (MCST)

The boards can be accessed in Multicast Commands mode (MCST mode, see Ref. [4]), that allows to write in the registers of several boards at the same time by accessing the MCST Base Address in A32 only once.

The boards can be accessed in Chained Block Transfer mode (CBLT mode, see Ref. [4]) that allows to readout sequentially a certain number of contiguous boards in a VME crate. This access is allowed in BLT32 and BLT64 modes only to the MCST Base Address.

N.B.: The Base Address used for MCST and CBLT operations is the same, i.e. throughout this User's Manual the "MCST Base Address" identifies the same Address, used both for MCST commands (in Write only) and the CBLT Readout (in Read only, for the Output Buffer only).

The MCST Base Address must be set in a different way with respect to the ordinary Base Address. Its most significant byte (i.e. bits 31 through 24) must be written in the MCST/CBLT Address Register (see §3.8) and must be set in common to all boards belonging to the MCST/CBLT chain (i.e. all boards must have the same setting of the MCST/CBLT Base Address on bits 31 through 24). The default setting is 0xAA.

In CBLT and MCST operations, the IACKIN and IACKOUT VME lines are used for the control transfer from one board to the following. No empty slots must thus be left between the boards or, in alternative, empty slots can be left only in case VME crates with automatic IACKIN/IACKOUT short-circuiting are used.

Once the addresses have been set, the first and last board in a chain must have, respectively, only the FIRST_BOARD (F_B) and only the LAST_BOARD (L_B) bit set to 1 in the MCST Control Register (see § 3.18). On the contrary, all intermediate boards must have both the FIRST_BOARD and the LAST_BOARD bits set to 1 (active, intermediate) or both the FIRST_BOARD and the LAST_BOARD bits set to 0 (inactive). By default these bits are set to 0 (the board is inactive).

Board status	Board position in the chain	F_B bit	L_B bit
inactive	-	0	0
active	last	0	1
active	first	1	0
active	intermediate	1	1

Please note that in a chain there must be one (and only one) *first board* (i.e. a board with F_B bit set to 1 and the L_B bit set to 0) and one (and only one) *last board* (i.e. a board with F_B bit set to 0 and the L_B bit set to 1).

The complete address in A32 mode is:

A [31:24] MCST/CBLT Address
A [23:16] 00
A [15:0] offset

In MCST/CBLT operation it is possible to define more chains in the same crate, but each chain must have an address different from the other.

3.1.5. MCST/CBLT addressing examples

The following is an example of MCST and CBLT addressing for four V878 boards plugged into a VME crate. To access the boards the steps to perform are as follows:

1. Set the MCST address (see § 3.8) for all boards via VME Base Address or geographical addressing;
2. Set the bits F_B and L_B of the MCST Control Register (see § 3.18) according to the operational status (active or inactive) of each board and to its position in the chain (first, intermediate or last);
3. Write or read the boards via MCST/CBLT addressing.

An example of user procedures which can be used to perform a write access is:

vme_write *(address, data, addr_mode, data_mode),*

which contain the following parameters:

Address:	the complete address, i.e. Base Address + offset;
Data:	the data to be either written or read;
Addr_mode:	the addressing mode (A24 or A32);
Data_mode:	the data mode (D16, D32 or D64).

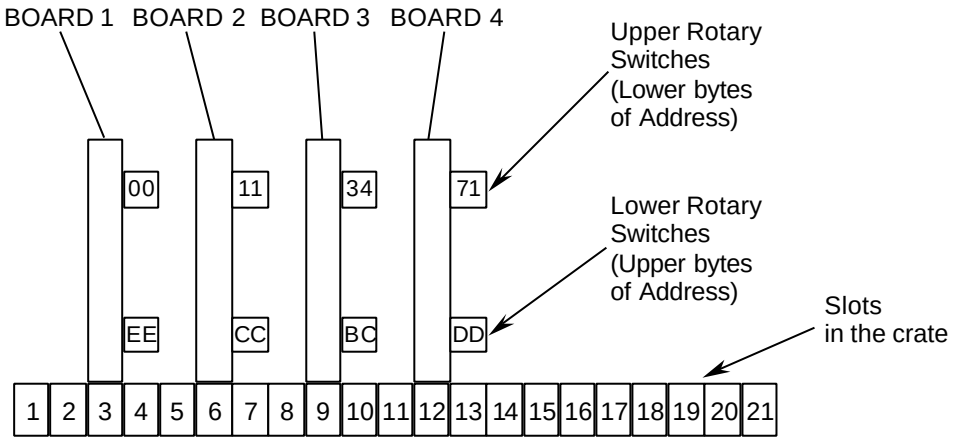

Fig. 3.4: MCST/CBLT Addressing Example

In the following two software examples using the above mentioned procedures are listed:

Example of Access via Base Address

```
vme_write (0xEE001004, 0xAA, A32, D16)    /* set MCST Address=0xAA for board 1 */
vme_write (0xCC111004, 0xAA, A32, D16)    /* set MCST Address=0xAA for board 2 */
vme_write (0xBC341004, 0xAA, A32, D16)    /* set MCST Address=0xAA for board 3 */
vme_write (0xDD711004, 0xAA, A32, D16)    /* set MCST Address=0xAA for board 4 */
vme_write (0xEE00101A, 0x02, A32, D16)    /* set  board 1 = First */
vme_write (0xCC11101A, 0x03, A32, D16)    /* set  board 2 = Active */
vme_write (0xBC34101A, 0x00, A32, D16)    /* set  board 3 = Inactive */
vme_write (0xDD71101A, 0x01, A32, D16)    /* set  board 4 = Last */
```

```
vme_write (0xAA001006, 0x80, A32, D16)    /* set RESET MODE for all the boards */
```

Example of Access via geographical address

```
vme_write (0x180016, 0xAA, A24, D16)      /* set MCST Address=0xAA for board 1 */
vme_write (0x300016, 0xAA, A24, D16)      /* set MCST Address=0xAA for board 2 */
vme_write (0x480016, 0xAA, A24, D16)      /* set MCST Address=0xAA for board 3 */
vme_write (0x510016, 0xAA, A24, D16)      /* set MCST Address=0xAA for board 4 */
vme_write (0x180040, 0x02, A24, D16)      /* set board 1 = First */
vme_write (0x300040, 0x03, A24, D16)      /* set board 2 = Active */
vme_write (0x480040, 0x00, A24, D16)      /* set board 3 = Inactive */
vme_write (0x510040, 0x01, A24, D16)      /* set board 4 = Last */
vme_write (0xAA001006, 0x80, A32, D16)    /* set RESET MODE for all the boards */
```

N.B.: there must be always one (and only one) FIRST BOARD and one (and only one) LAST BOARD.

3.2. Interrupter capability

The Mod. V878 houses a RORA-type VME INTERRUPTER which is generated when the number of events in the memory is equal to the value written in the Event Trigger Register at the VME address: Base Address + 0x1020 (see § 3.20). If the Event Trigger Register is set to 0 the interrupt is disabled (default setting).
The interrupt responds to 8 bit, 16 bit and 32 bit interrupt acknowledge cycles providing an 8-bit STATUS/ID on the VME data lines D00..D07 and removes its interrupt request when the condition mentioned above is FALSE.

3.2.1. Interrupt Status/ID

The interrupt STATUS/ID is 8-bit wide, and it is contained in the 8LSB of the Interrupt Vector Register (see § 3.12). The register is available at the VME address: Base Address + 0x100C.

3.2.2. Interrupt Level

The interrupt level corresponds to the value stored in the 3LSB of the Interrupt Level Register (see §3.11). The register is available at the VME address: Base Address + 0x100A. If the 3LSB of this register are set to 0, the Interrupt generation is disabled.

3.2.3. Interrupt Generation

The Interrupt Generation occurs as the number of events stored in the memory equals the value written in the Event Trigger Register (see § 3.20). This condition can be thus programmed via VME.

3.2.4. Interrupt Request Release

The INTERRUPTER removes its Interrupt request when a Read Access is performed to the Output Buffer so that the number of events stored in the memory decreases and becomes less than the value written in the Event Trigger Register.

3.3. Data transfer capability

The internal registers are accessible in D16 mode, unless otherwise specified. Access in D32, BLT32, MBLT64, CBLT32 and CBLT64 is available for the data buffer.

3.4. Register address map

The Address map for the Model V878 is listed in Table 3.2. All register addresses are referred to the Base Address of the board, i.e. the addresses reported in the Tables are the offsets to be added to the board Base Address.

The Table gives also information about the effects of RESET on the registers. In particular, column 2 through 4 refer to the following RESET operations:

- **D R → Data RESET;**
- **S R → Software RESET;**
- **H R → Hardware RESET.**

If a register has a mark in these columns, it means that the relevant RESET operation resets that register. For further details on the RESET Logic please refer to § 5.8.

Table 3.3 and Table 3.4 list register addresses (offset) in CBLT and MCST operations, respectively.

The ROM address map is reported in Table 3.5, p.54.

Table 3.2: Address Map for the Model V878

Register content	DR	SR	HR	Address	Type	Access mode
Output Buffer	✓	✓	✓	0x0000÷0x07FF	Read only	D32/D64
Firmware Revision				0x1000	Read only	D16
Geo Address				0x1002	Read only	D16
MCST/CBLT Address			✓	0x1004	Read/Write	D16
Bit Set 1		✓ (*)	✓ (*)	0x1006	Read/Write	D16
Bit Clear 1		✓ (*)	✓ (*)	0x1008	Read/Write	D16
Interrupt Level		✓	✓	0x100A	Read/Write	D16
Interrupt Vector		✓	✓	0x100C	Read/Write	D16
Status Register 1		✓	✓	0x100E	Read only	D16
Control Register 1		✓ (*)	✓ (*)	0x1010	Read/Write	D16
ADER High			✓	0x1012	Read/Write	D16
ADER Low			✓	0x1014	Read/Write	D16
Single Shot Reset				0x1016	Write only	D16
MCST/CBLT Ctrl			✓	0x101A	Read/Write	D16
SW Berr				0x101C	Write only	D16
Event Trigger Register		✓	✓	0x1020	Read/Write	D16
Status Register 2		✓	✓	0x1022	Read only	D16
Event Counter_L	✓ (*)	✓ (*)	✓ (*)	0x1024	Read only	D16
Event Counter_H	✓ (*)	✓ (*)	✓ (*)	0x1026	Read only	D16
Increment Event				0x1028	Write only	D16
Increment Offset				0x102A	Write only	D16
Load Test Register				0x102C	Read/Write	D16
FCLR Window		✓	✓	0x102E	Read/Write	D16
Bit Set 2		✓	✓	0x1032	Read/Write	D16
Bit Clear 2		✓	✓	0x1034	Write only	D16
W Memory Test Address		✓	✓	0x1036	Write only	D16
Memory Test Word_High		✓	✓	0x1038	Write only	D16
Memory Test Word_Low				0x103A	Write only	D16
Crate Select		✓	✓	0x103C	Read/Write	D16
Test Event Write				0x103E	Write only	D16
Event Counter Reset				0x1040	Write only	D16
Vset				0x1060	Write only	D16
Voff				0x1062	Write only	D16
R Test Address		✓	✓	0x1064	Write only	D16
Clear Time		✓	✓	0x1066	Read/Write	D16
SW Comm				0x1068	Write only	D16
Slide Constant		✓	✓	0x106A	Read/Write	D16
BAD				0x1072	Read only	D16

Thresholds				0x1080 ÷ 0x10BF	Read/Write	D16
AUX Bus				0x1200 ÷ 0x12FF	Read/Write	D16

(*) not all bits are reset with the same type of RESET: see the description of the relevant register for details.

The ROM address map is from 0x8000 to 0xFFFF: refer to § 3.43 for details.

Table 3.3: Address Map in CBLT operation

Register content	Address	Type	Access mode
Output Buffer	0x0000÷0x07FF	Read only	D32/D64

Table 3.4: Address Map in MCST operations

Register content	Address	Type	Access mode
Bit Set 1	0x1006	Write only	D16
Bit Clear 1	0x1008	Write only	D16
Interrupt Level	0x100A	Write only	D16
Interrupt Vector	0x100C	Write only	D16
Control Register 1	0x1010	Write only	D16
ADER High	0x1012	Write only	D16
ADER Low	0x1014	Write only	D16
Single Shot Reset	0x1016	Write only	D16
SW Berr	0x101C	Write only	D16
Event Trigger Register	0x1020	Write only	D16
Increment Event	0x1028	Write only	D16
Increment Offset	0x102A	Write only	D16
Load Test Register	0x102C	Write only	D16
Fast Clear Window	0x102E	Write only	D16
Bit Set 2	0x1032	Write only	D16
Bit Clear 2	0x1034	Write only	D16
W Memory Test Address	0x1036	Write only	D16
Memory Test Word_High	0x1038	Write only	D16
Memory Test Word_Low	0x103A	Write only	D16
Crate Select	0x103C	Write only	D16
Event Counter Reset	0x1040	Write only	D16
Vset	0x1060	Write only	D16
Voff	0x1062	Write only	D16
R Test Address	0x1064	Write only	D16
Clear Time	0x1066	Write only	D16
SW comm	0x1068	Write only	D16
Slide Constant	0x106A	Write only	D16
Thresholds	0x1080 ÷ 0x10BF	Write only	D16
AUX Bus	0x1200 ÷ 0x12FF	Write only	D16

3.5. Output Buffer Register

(Base Address + 0x0000 ÷ 0x07FC, read only)

This register allows the user to access the multiple event buffer to readout the converted values.

The output buffer contains the output data organised in 32-bit words.

The data in the buffer are organised in events.
Each event consists of:

- the **header**, that contains the geographical address, the crate number and the number of converted channels;
- one or more **data words**, each of which contains the geographical address, the number of the channel, the Under-Threshold (UN) bit, the Overflow (OV) bit and the 12-bit converted value;
- the **End Of Block** (EOB), which contains the geographical address and the event counter.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GEO[4:0]					0	1	0	CRATE[7:0]								0	0	CNT[5:0]														

Fig. 3.5: Output buffer: the Header

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GEO[4:0]					0	0	0	0	0	CHANNEL[5:0]						0	0	UN	OV	ADC[11:0]												

Fig. 3.6: Output buffer: the data word format

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GEO[4:0]					1	0	0	EVENT COUNTER[23:0]																								

Fig. 3.7: Output buffer: the End Of Block

Header content:

The bits[31…27] contains the GEO address.

The bits[26..24] identify the type of word (010 →header);

The bits[23..16] identify the crate number according to the content of the Crate Select Register (see § 3.32).

The bits[13…8] contain the number of memorised channels.

Datum content:

The bits[31…27] contains the GEO address.

The bits[26..24] identify the type of word (000 →datum);

The bits[21..16] identify the number of the channel which the data are coming from.

The bit[13] is the UNDERTHRESHOLD bit:
- = 0 → the datum is over the threshold fixed in the relevant register (see § 3.38);
- = 1 → the datum is under the threshold fixed in the relevant register; it is actually possible to make the datum be written in the buffer even if it is under the threshold by using the bits 3 and 4 of the Bit Set 2 Register (see § 3.27);

The bit[12] is the OVERFLOW bit:
- = 0 → ADC not in overflow condition;
- = 1 → ADC in overflow;

The bits[11…0] contain the converted datum.

EOB content:

The bits[31…27] contains the GEO address.

The bits[26..24] identify the type of word (100 → EOB);

The bits[23..0] contain the 24-bit event counter value (see § 3.22 and 0).

The bits[31…27] always contains the GEO address (except for the not valid datum, see Fig. 3.8).

The bits[26..24] identify the type of word, according to the following:

- 010 → header;
- 000 → valid datum;
- 100 → end of block;
- 110 → not valid datum.
- *others* → reserved.

If a read access is performed to the buffer when it is empty, the readout will provide a NOT VALID DATUM arranged as shown in Fig. 3.8.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
					1	1	0																								

Fig. 3.8: Output buffer: not valid datum

The sequence followed to store the data in the buffer is as follows:

CHANNEL 0
CHANNEL 1
CHANNEL 2
……
CHANNEL 30
CHANNEL 31

Please note that some of the above channel data may be missing in the sequence: this is due either to overflow or underthreshold conditions (which caused these data not to be stored), or to user's settings to kill some channels.

3.6. Firmware Revision Register

(Base Address + 0x1000, read only)

This register contains a 16-bit value identifying the firmware revision. The 16-bit value corresponds to 4 hexadecimal figures which give the firmware revision number. For example, in the figure is shown the register content for the firmware release:

Rev. 01.03

which presently is the latest one.

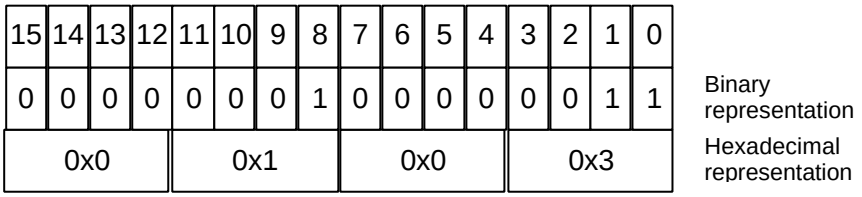

Fig. 3.9: Firmware Revision Register

3.7. GEO Address Register

(Base Address + 0x1002, read only)

This register contains the geographical address of the module, i.e. the slot number picked up from the JAUX connector on the VME backplane. The register is filled up upon arrival of a RESET. The register content is the following:

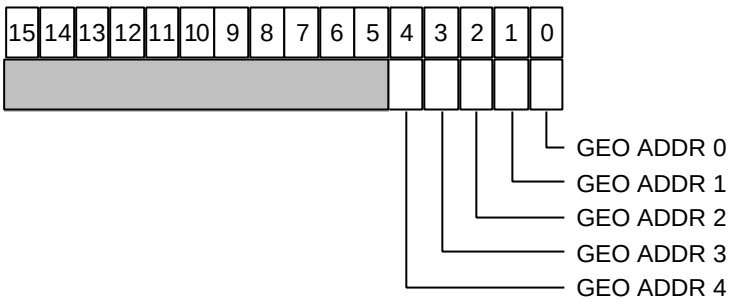

Fig. 3.10: Geographical address register

GEO [4...0] corresponds to A23...A19 in the address space of the CR/CSR area: each slot has a relevant number whose binary encoding consists of the GEO ADDR 4 to 0.

N.B.: after a write access to the GEO register, it is necessary to perform a reset to make the change active.

3.8. MCST/CBLT Address Register

(Base Address + 0x1004, read/write)

This register contains the most significant bits of the MCST/CBLT address of the module set via VME, i.e. the address used in MCST/CBLT operations. Refer to §3.1.4 for details about MCST/CBLT addressing mode.
The register content is the following:

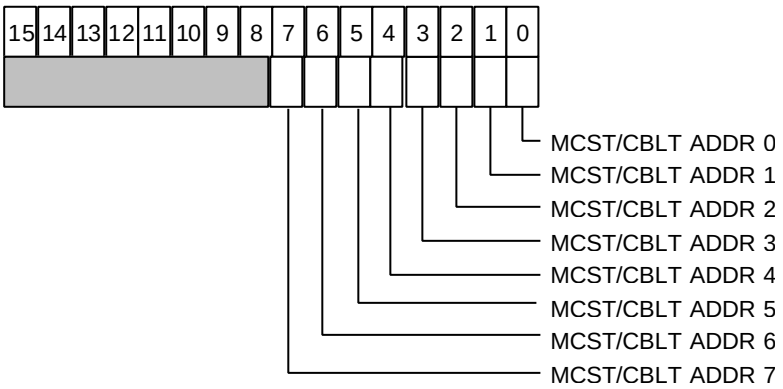

Fig. 3.11: MCST/CBLT address register

Default setting (i.e. at power-on or after hardware reset) is 0xAA.

3.9. Bit Set 1 Register

(Base Address + 0x1006, read/write)

This register allows to set the RESET logic of the module and to enable the change of the base address via VME.
A write access with the bits to 1 sets the relevant bits to 1 in the register (i.e. writing 0x10 to this register sets the SEL ADDR bit to 1). A write access with the bits set to 0 does NOT clear the register content: in order to clear the register content, the Bit Clear 1 Register must be used (see § 3.10).
A read access returns the status of this register.

The register content is the following:

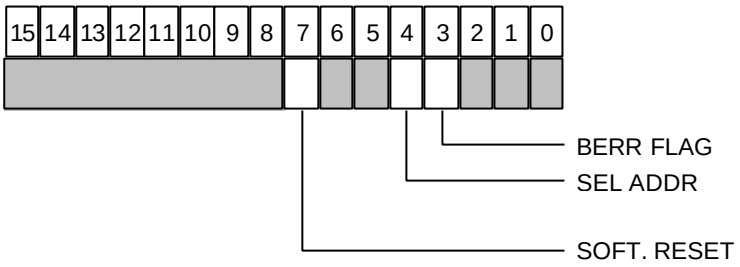

Fig. 3.12: Bit Set 1 Register

BERR FLAG: Bus Error Flag Bit (meaningful in BLT/CBLT modes only). The user may set this flag for test purposes only. Its content is cleared both via an hardware and via a software reset.
= 0 board has not generated a Bus Error (default);
= 1 board has generated a Bus Error.

SELECT ADDRESS: Select Address bit.
= 0 base address is selected via Rotary Switch (default);
= 1 base address is selected via internal ADER registers.

SOFTW. RESET: Sets the module to a permanent RESET status. The RESET is released only via write access with the relevant bit set to 1 in the Bit Clear Register, see § 3.10.

This register is reset via a hardware reset (see § 5.8). Only the bit 3 (BERR FLAG) is reset both via hardware reset and software reset.

3.10. Bit Clear 1 Register

(Base Address + 0x1008, read/write)

This register allows to clear the bits in the above described Bit Set 1 Register. A write access with a bit set to 1 resets that bit, e.g. writing 0x4 to this register resets the BERR FLAG bit. A write access with the bits set to 0 does NOT clear the register content. The

structure of the register is identical to the Bit Set 1 Register. A read access returns the status of the Bit Set/Clear 1 Register.

3.11. Interrupt Level Register

(Base Address + 0x100A, read/write)

The 3 LSB of this register contain the value of the interrupt level (Bits 3 to 15 are meaningless). Default setting is 0x0. In this case interrupt generation is disabled.

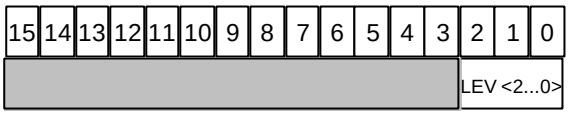

Fig. 3.13: Interrupt Level Register

3.12. Interrupt Vector Register

(Base Address + 0x100C, read/write)

This register contains the value of the Interrupt STATUS/ID that the V878 INTERRUPTER places on the VME data bus during the Interrupt Acknowledge cycle (Bits 8 to 15 are meaningless). Default setting is 0x00.

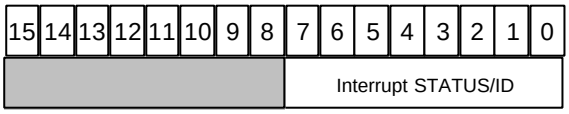

Fig. 3.14: Interrupt Vector Register

3.13. Status Register 1

(Base + 0x100E, read only)

This register contains information on the status of the module.
TERM ON and TERM OFF refer to the terminations of the CONTROL bus lines: the last module in a chain controlled via the front panel CONTROL connector must have these terminations ON, while all the others must have them OFF. The insertion or removal of the terminations is performed via internal DIP switches (see Fig. 2.3).
The BUSY and DATA READY signals are available both for the individually addressed module and as a global readout of a system of many units connected together via the CONTROL bus.

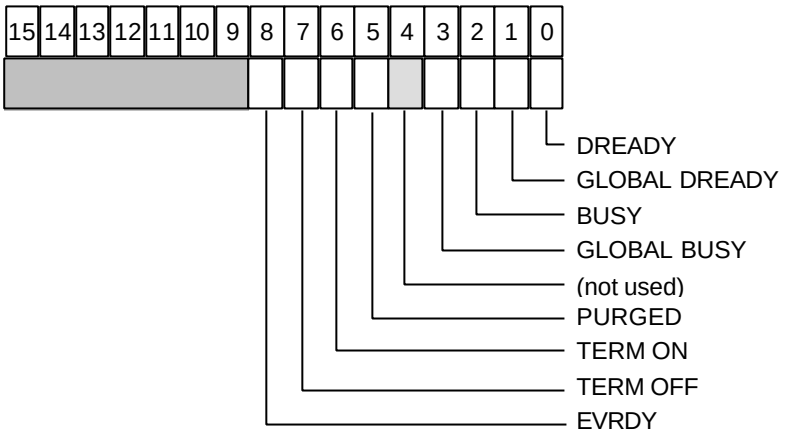

Fig. 3.15: Status Register 1

DREADY: Indicates that there are data (at least 1 event) in the Output Buffer.
= 0 No Data Ready;
= 1 Data Ready.

GLOBAL DREADY: Indicates that at least one module in the chain has data in the Output Buffer (wired “OR” of the READY signal of each module in the chain).
= 0 No Module has Data Ready;
= 1 At least one Module has Data Ready.

BUSY: Busy status indicates that either a conversion is in progress or the board is resetting or the Output Buffer is full or the board is in MEMORY TEST mode.
= 0 Module not Busy;
= 1 Module Busy.

GLOBAL BUSY: Indicates that at least a module in a chain is BUSY (wired “OR” of the BUSY signal of each module in the chain).
= 0 No Module is Busy;
= 1 At least a Module is Busy.

PURGED: during a CBLT operation it indicates that the board is purged, i.e. the board has finished to send data.
= 0 the board is not purged;
= 1 the board is purged.

TERM ON: Termination ON bit.
= 0 not all Control Bus Terminations are ON.
= 1 all Control Bus Terminations are ON.

TERM OFF: Termination OFF bit.
= 0 not all Control Bus Terminations are OFF
= 1 all Control Bus Terminations are OFF.

EVRDY: is a flag for the Event Trigger Register.

= 0 (default) indicates that the number in the Event Trigger Register (see § 3.20) is smaller than the number of events stored in the memory;
= 1 indicates that the number in the Event Trigger Register (see § 3.20) is greater than or equal to the number of events stored in the memory and an interrupt request has been generated with interrupt level different from 0 (see § 3.2.3).

N.B.: the condition in which both TERM ON and TERM OFF are equal to 0 means an uncommon termination status, e.g. some terminations are on and other are off.

3.14. Control Register 1

(Base Address + 01010, read/write)

This register allows performing some general settings of the module.

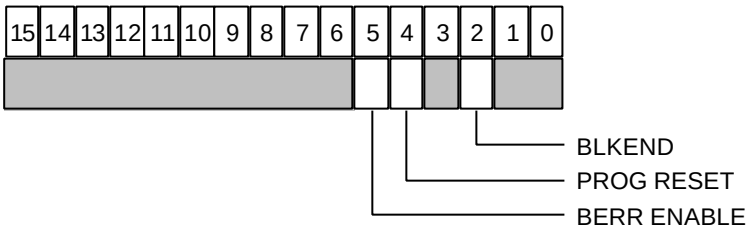

Fig. 3.16: Control Register 1

BLKEND: End of Block bit. Used in Block Transfer modes only.
= 0 The module sends all requested data to the CPU; when the Output Buffer is empty it will send no valid data. If BERR_VME is enabled (see bit 5 below, BERR ENABLE), a Bus Error is generated with the readout of the last word in the Output Buffer (default).
= 1 The module sends all data to the CPU until the first EOB word (end of first event) is reached; afterwards it will send no valid data. If BERR_VME is enabled, a Bus Error is generated at the readout of the EOB word.

PROG RESET: Programmable Reset Mode setting bit.
= 0 the front panel RESET acts only on data (data reset, default);
= 1 the front panel RESET acts on the module (software reset).
N.B. This bit is cleared only via hardware reset.

BERR ENABLE: Bus Error enable bit. Used in Block Transfer mode only.
= 0 the module sends a DTACK signal until the CPU inquires the module (default);
= 1 the module is enabled to generate a Bus error to finish a block transfer.

(Bits 6 to 15 are meaningless).

This register is reset both via software and via hardware reset (see §5.8), except for the bit 4 (PROG RESET) which is reset only via hardware reset.

3.15. Address Decoder High Register

(Base Address + 0x1012, read/write)

This register contains the A31...A24 bits of the address of the module: it can be set via VME for a relocation of the Base Address of the module, as described in Ref. [4]. The register content is the following:

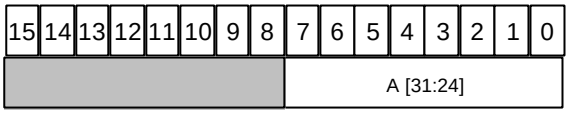

Fig. 3.17: ADER HIGH Register

3.16. Address Decoder Low Register

(Base Address + 0x1014 read/write)

This register contains the A23...A16 bits of the address of the module: it can be set via VME for a relocation of the Base Address of the module, as described in Ref. [4]. The register content is the following:

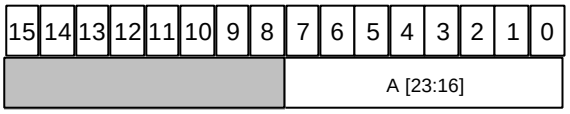

Fig. 3.18: ADER LOW Register

3.17. Single Shot Reset Register

(Base Address + 0x1016, write only)

A write access to this dummy register performs a module reset. This register must be used very carefully and for debugging purposes only. In order to reset the board, it is recommended to use the Bit Set 1 Register (see § 3.9).

3.18. MCST/CBLT Control Register

(Base Address + 0x101A, write only)

This register allows performing some general MCST/CBLT settings of the module.

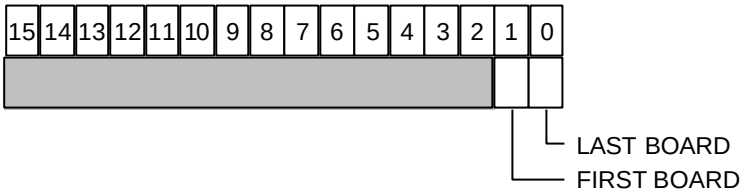

Fig. 3.19: MCST Address Register

LAST_BOARD	Last Board flag bit (valid in CBLT and MCST modes only)
FIRST_BOARD	First Board flag bit (valid in CBLT and MCST modes only)

The status of the boards according to the bit value is the following:

BOARD STATUS	FIRST BOARD bit	LAST BOARD bit
Board disabled in CBLT or MCST chain	0	0
First board in CBLT or MCST chain	1	0
Last board in CBLT or MCST chain	0	1
Active intermediate board in CBLT or MCST chain	1	1

(Bits 2 to 15 are meaningless).

3.19. SW Berr Register

(Base Address + 0x101C, write only)

A write access to this dummy register generates a bus error.

N.B.: this register allows the user to perform a non-standard CBLT access.

3.20. Event Trigger Register

(Base Address + 0x1020, read/write)

This register contains a 5-bit value set by the user: when the number of events stored in the memory equals this value and EVRDY is equal to 1 an interrupt request is generated. Default setting is 0: in this case the interrupt generation is disabled. See also § 3.2.

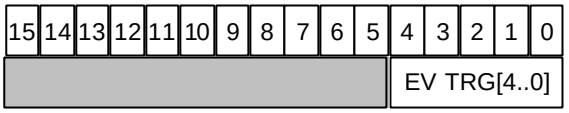

Fig. 3.20: Event Trigger Register

3.21. Status Register 2

(Base Address + 0x1022, read only)

This register contains further information on the status of the module output buffer and on the type of piggy back plugged into the main board.

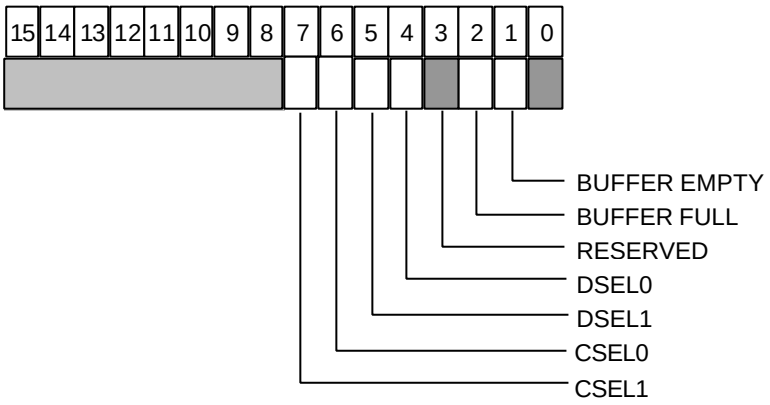

Fig. 3.21: Status Register 2

BUFFER EMPTY: Indicates if the output buffer is empty.
=0 buffer not empty;
=1 buffer empty.

BUFFER FULL: Indicates if the output buffer is full.
=0 buffer not full;
=1 buffer full.

CSEL1, CSEL0, DSEL1, DSEL0: Indicate the type of piggy-back plugged into the board. In the case of the Mod.V878, the value is: 0011 (32-channel time-to-digital converter).

3.22. Event Counter_Low Register

(Base Address + 0x1024, read only)

It contains the 16 LSBs of the event counter. The event counter can work in two different ways (see also § 5.6):

1. it counts all events;
2. it counts only the accepted events.

The two modes can be selected via the Bit 14 (ALL TRG) of the Bit Set 2 Register (see § 3.27).

EVENT CNT LOW: 16 LSB of the 24-bit Event Counter.

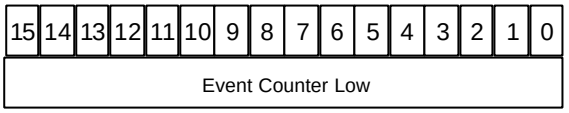

Fig. 3.22: Event Counter Low Register

This register is reset via the Event Counter Reset Register (see § 3.34) or via a software or hardware reset (see § 5.8). However, if the event counter is set so as to work as relative counter (i.e. it counts only the accepted events), this register is reset also with a data reset (see § 5.8).

3.23. Event Counter_High Register

(Base + 0x1026, read only)

It contains the 8 MSB of the 24-bit event counter. The event counter can work in two different ways (see also § 5.6):

1. it counts all events;
2. it counts only the accepted events.

The two modes can be selected via the Bit 14 (ALL TRG) of the Bit Set 2 Register (see § 3.27).

EVENT CNT HIGH: 8 MSB of the 24-bit Event Counter.

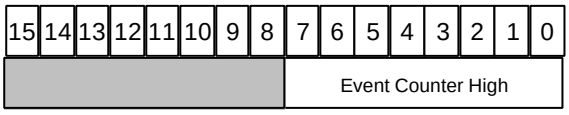

Fig. 3.23: Event Counter High Register

This register is reset via the Event Counter Reset Register (see § 3.34) or via a software or hardware reset (see § 5.8). However, if the event counter is set so as to work as relative counter (i.e. it counts only the accepted events), this register is reset also with a data reset (see § 5.8).

3.24. Increment Event Register

(Base Address + 0x1028, write only)

A write access to this dummy register sets the readout pointer on the next event in the output buffer (at the first address).
In particular, if the bit 11 (AUTO INCR) of the Bit Set 2 Register is set to 0 (see § 3.27), the readout pointer is no more automatically incremented, but it can be incremented via a write access to this register or to the Increment Offset Register (see below).

3.25. Increment Offset Register

(Base Address + 0x102A, write only)

A write access to this dummy register increments the readout pointer of one position (next word, same event if EOB is not encountered; next event if EOB is encountered).
In particular, if the bit 11 (AUTO INCR) of the Bit Set 2 Register is set to 0 (see § 3.27), the readout pointer is no more automatically incremented, but it can be incremented via a write access to this register or to the Increment Event Register (see above).

3.26. Fast Clear Window Register

(Base Address + 0x102E, read/write)

Sets the delay time (expressed as number of 32-MHz clock cycles) with respect to the trailing edge of COM signal in order to define the Fast Clear window. For the definition of the Fast Clear window refer to Fig. 5.6.

3.27. Bit Set 2 Register

(Base Address + 0x1032, read/write)

This register allows to set the operation mode of the module. A write access with a bit to 1 sets the relevant bit to 1 in the register. A write access with the bit set to 0 does not clear the register content, the Bit Clear 2 Register must be used (see § 3.28). A read access returns the status of the register. The register content is the following:

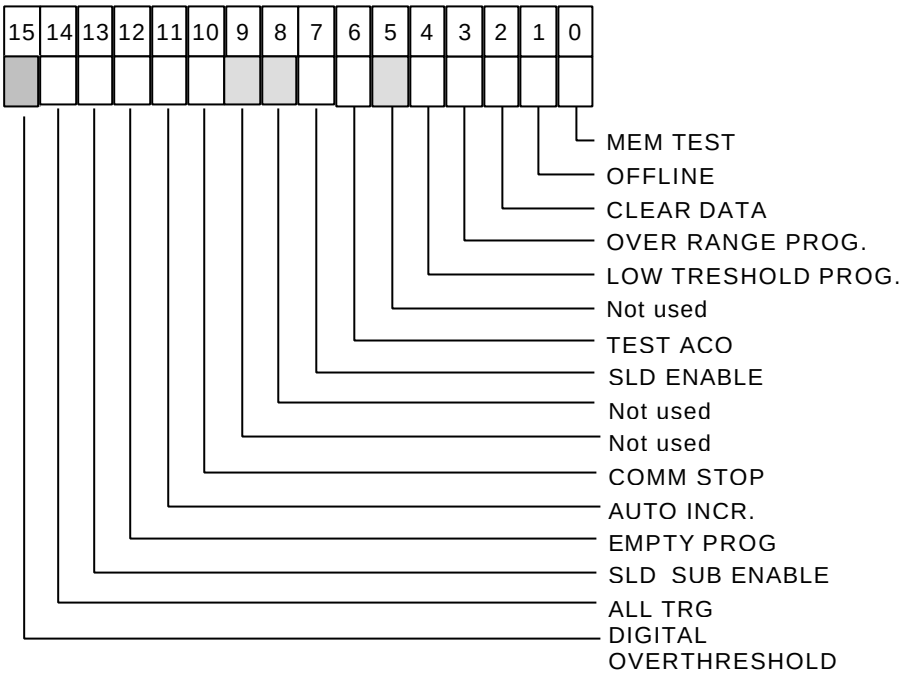

Fig. 3.24: Bit set 2 register

MEM TEST: Test bit: allows to select the Random Memory Access Test Mode (see § 6.4.1).
- =0 normal mode (default);
- =1 Random Memory Access Test Mode selected: it is possible to write directly into the memory.

OFFLINE: Offline bit: allows to select the ADC controller's status.
- =0 ADC controller online (default);
- =1 ADC controller offline: no conversion is performed.

CLEAR DATA: Allows to generate a reset signal which clears the data, the write and read pointers, the event counter and the analog sections.
- =0 no data reset is generated (default);
- =1 a data reset signal is generated.

OVER RANGE: Allows to disable overflow suppression (see also § 5.4).
- =0 over range check enabled: only the data not causing the ADC overflow are written into the output buffer (overflow suppression; default);
- =1 over range check disabled: all the data are written into the output buffer (no overflow suppression).

LOW THRESHOLD: Allows to disable zero suppression (see also § 5.3).
- =0 low threshold check enabled: only data above the threshold are written into the output buffer (zero suppression; default);
- =1 low threshold check disabled: all the data are written into the output buffer (no zero suppression).

TEST ACQ: Allows to select the Acquisition Test Mode (see § 6.4.2).
- =0 normal operation mode, i.e. the data to be stored in the buffer are the real data (default);
- =1 Acquisition Test Mode selected, i.e. the data to be stored in the buffer are taken from an internal FIFO (Test Event Write Register, see § 3.33).

SLIDE ENABLE: Allows to enable/disable the sliding scale.
- =0 the sliding scale is disabled and the DAC of the sliding scale is set with a constant value (Slide Constant, see § 3.40);
- =1 the sliding scale is enabled (default).

COMM STOP: Allows to select the operation mode for the module. The status of this bit corresponds to the level of the SSB pin of the J13 connector to the piggy-back board (see Fig. 2.3).
- =0 COMMON START mode selected (default, see § 6);
- =1 COMMON STOP mode selected (see § 6).

AUTO INCR: Allows to enable/disable the automatic increment of the readout pointer.
- =0 the read pointer is not incremented automatically but only by a write access to the Increment Event or Increment Offset Registers (see § 3.24 and 3.25);
- =1 the read pointer is incremented automatically (default).

EMPTY PROG: Allows to choose if writing the header and EOB when there are no accepted channels.
- =0 when there are no accepted channels, nothing is written in the output buffer (default).
- =1 when there are no accepted channels, the Header and the EOB are anyway written in the output buffer.

SLIDE_SUB ENABLE: Allows to change operation mode for the sliding scale.
- =0 the sliding scale works normally (default);
- =1 the subtraction section of the sliding scale is disabled (test purposes only).

ALL TRG: Allows to choose how to increment the event counter.
- =0 event counter incremented only on accepted triggers.
- =1 event counter incremented on all triggers (default).

DIGITAL OTD: Allows to enable the Digital Overthreshold operation.
- =0 no suppression
- =1 up to 3840 counts stored in memory, the subsequent are neglected

3.28. Bit Clear 2 Register

(Base Address + 0x1034 write only)

This register allows clearing the bits of the Bit Set 2 Register (§ 3.27). A write access with a bit set to 1 resets that bit, e.g. writing 0x4 to this register resets the CLEAR DATA bit. A write access with the bits set to 0 does NOT clear the register content. The structure of the register is identical to the Bit Set 2 Register. A read access returns the status of Bit Set/Clear 2 Register.

3.29. W Memory Test Address Register

(Base Address + 0x1036 write only)

This register contains the address of the memory on which data can be written for the memory test.

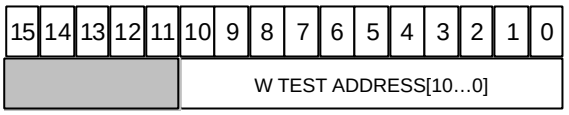

Fig. 3.25: W Memory Test Address Register

N.B.: The output buffer is a FIFO, so the read address (R Test Address Register) must be different from the write address (W Test Address Register).

3.30. Memory Test Word_High Register

(Base Address + 0x1038 write only)

The Memory Test Word is a 32-bit word used for the memory test. The higher 16 bits are set via this register, while the lower 16 bits are set via the Test Word_Low Register.

These registers are used in TEST mode as follows:

1. set the module in test mode (bit 0 of the Bit Set 2 Register, see § 3.27);
2. write the memory address (see § 3.29),
3. write the 16 MSBs in the TESTWORD_HIGH register;
4. write the 16 LSBs in the TESTWORD_LOW register;

With the latter operation, the 32-bit pattern is transferred to the memory. If operations 3. and 4. are inverted, the content of the 16 MSBs may be meaningless.

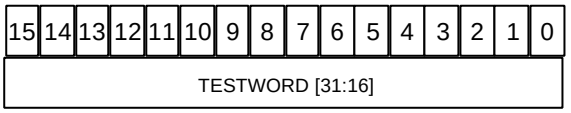

Fig. 3.26: Test Word_High Register

3.31. Memory Test Word_Low Register

(Base Address + 0x103A write only)

This register allows to set the lower 16 bits of the Test Word (see above).

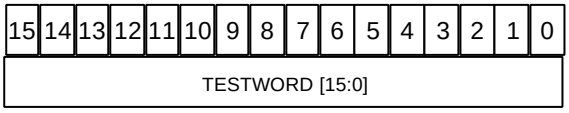

Fig. 3.27: Test Word_Low Register

3.32. Crate Select Register

(Base Address + 0x103C read/write)

This register contains the number of the crate which the board is plugged into. This register must be filled at board initialisation and will be part of the data word (see § 3.5).

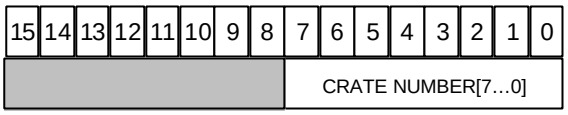

Fig. 3.28: Crate Select Register

3.33. Test Event Write Register

(Base Address + 0x103E write only)

This register is used in Acquisition Test Mode and its content constitutes the test event to be written in the output buffer.
A write access to this register allows the user to write a set of 32 data into a 32-word FIFO. As the Bit 6 (TEST ACQ) of the Bit Set 2 Register (see §3.27) is set to 1 and the Acquisition Test Mode is consequently selected, these data are directly written in the output buffer constituting an event which can be used to test the module and/or the acquisition software.
Each 16-bit test word (see the figure below) contains a 12-bit value, acting as the ADC converted value, and an OV bit which indicates the possible overflow.
The 32 test data, corresponding to the data from the 32 channels, must be written in this FIFO in the same order as they are read from the output buffer, that is:

- test datum for the channel 0
- test datum for the channel 1
- …….
- test datum for the channel 29
- test datum for the channel 30
- test datum for the channel 31

For further details on the use of this register in Acquisition Test Mode please refer to § 6.4.2.

N.B.: please note that the user must write at least and not more than 32 test words. Actually, since the words are written in a FIFO, if the user writes less than 32 words, some words will be not defined; on the other hand, if the user writes more than 32 words, some words will be overwritten.

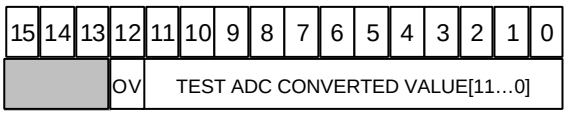

Fig. 3.29: Test Event Write Register

3.34. Event Counter Reset Register

(Base Address + 0x1040 write only)

A VME write access to this dummy register clears the Event Counter.

3.35. Vset Register

(Base Address + 0x1060 write only)

This 8-bit register contains the DAC value to set the slope of the ramp (i.e. to select the range). The register content can be set from 0 to 255 corresponding to a Vset value ranging from 0 to -11 V.
Default status is not defined.

3.36. Voff Register

(Base Address + 0x1062 write only)

This 8-bit register contains the DAC value to set the offset of the ramp. The register content can be set from 0 to 255 corresponding to a Voff value ranging from 0 to 4 V.
Default status is not defined.

3.37. R Memory Test Address Register

(Base Address + 0x1064 write only)

This register contains the address of the output buffer from which data can be read for the memory test.

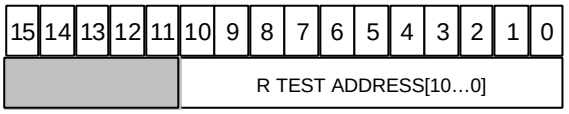

Fig. 3.30: R Memory Test Address Register

N.B.: The output buffer is a FIFO, so the read address (R Test Address Register) must be different from the write address (W Test Address Register).

3.38. Clear Time Register

(Base Address + 0x1066 read/write)

The 10 LSB of this 16-bit register contain the t_{clear} value (expressed in clock cycles) which allows to set the duration of the clear operation of the analog section. The total time required for the clear operation is:

$$T_{clear}\ (total) = 500\ ns + t_{clear}$$

It can be varied from 500 ns to 32 µs. Default setting is 0x0000

The 6 MSB contain the Busy Release Time (expressed in clock cycles), which allows to set how long the module will remain in Busy status after that the clear operation has been completed.
It can be varied from 0 to 2000 ns. Default setting is 0x0000

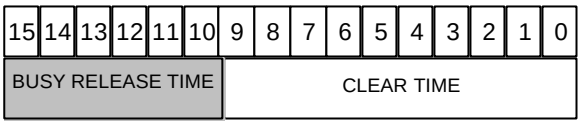

Fig. 3.31: R Memory Test Address Register

3.39. SW Comm Register

(Base Address + 0x1068 write only)

A write access to this dummy register causes a conversion for test purposes.

3.40. Slide constant Register

(Base Address + 0x106A read/write only)

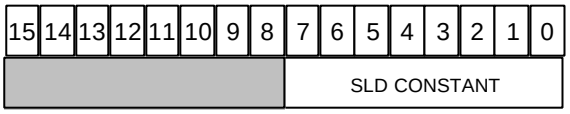

Fig. 3.32: Slide Constant Register

This register contains a 8-bit value corresponding to the constant to which is set the sliding scale DAC when the sliding scale is disabled by means of the SLD_ENABLE bit of the Bit Set 2 Register (refer to § 3.27).

3.41. BAD Register

(Base Address + 0x1072 read only)

This register contains the value converted by the ADC.

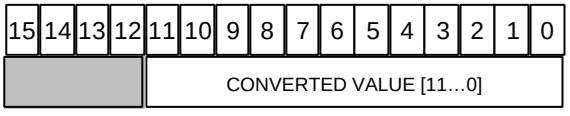

Fig. 3.33: BAD Register

3.42. Thresholds Memory

(Base Address + 0x1080 ÷ 0x10BE read/write)

This register contains the low threshold and kill option for each channel. The address is different for each channel (ch0 → 0x1080, ch1 → 0x1082, …, ch30 → 0x10BA, ch31 → 0x10BE).

Each threshold is as shown in the figure:

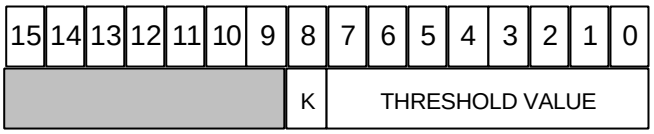

Fig. 3.34: Threshold Register

KILL (K): allows to abort memorisation of the data from the relevant channel.
= 0 channel data are memorised;
= 1 channel data memorisation is aborted.

THRESHOLD VALUE: this is a 8-bit value which is compared with the 8MSB of the 12-bit value to be memorised.

Default settings are not defined.

Please note that the KILL option can be used to disable some channels.

N.B.: the threshold values are reset only when the board is switched off.

3.43. AUX Bus

(Base Address + 0x1200 ÷ 0x12FE read/write)

This 8-bit register allows access to an auxiliary 8-bit bus connecting the VME to the piggy-back board.

3.44. ROM memory

(Base Address + 0x8000 ÷ 0xFFFE, read only)

It contains some useful information according to the table below, such as:

- **OUI**: manufacturer identifier (IEEE OUI);
- **Version**: purchased version (vers. 0);
- **Board ID**: Board identifier (Mod. V878);
- **Revision**: hardware revision identifier;
- **Serial MSB**: serial number (MSB);
- **Serial LSB**: serial number (LSB).

Table 3.5: ROM Address Map for the Model V878

Description	Address	Content (*)
OUI	0x8026	**0x00**
OUI	0x802A	**0x40**
OUI	0x002E	**0xE6**
Version	0x0032	**0x00**
BOARD ID	0x0036	**0x00**
BOARD ID	0x003A	**0x03**
BOARD ID	0x003E	**0x6E**
Revision	0x004E	**0x00**
Serial MSB	0x0F02	**0x00**
Serial LSB	0x0F06	**0x02**

(*) the example of content for the relevant register refers to the Mod.V878 (version: 0; serial number: 2; hardware revision: 0).

4. Hardware set-up and installation

4.1. Safety information

This section contains the fundamental safety rules for the installation and operation of the module.
Read thoroughly this section before starting any procedure of installation or operation of the product.

4.1.1. General safety precautions

Review the following safety precautions to avoid injury and prevent damage to this product or any products connected to it. To avoid potential hazards, use the product only as specified.

Only qualified personnel should perform service procedures.

4.1.1.1. Injury Precautions

Avoid Electric Overload.
To avoid electric shock or fire hazard, do not apply a voltage to a load that is outside the range specified for that load.

Avoid Electric Shock.
To avoid injury or loss of life, do not connect or disconnect cables while they are connected to a voltage source.

Do Not Operate Without Covers.
To avoid electric shock or fire hazard, do not operate this product with covers or panels removed.

Do Not Operate in Wet/Damp Conditions.
To avoid electric shock, do not operate this product in wet or damp conditions.

Do Not Operate in an Explosive Atmosphere.
To avoid injury or fire hazard, do not operate this product in an explosive atmosphere.

4.1.1.2. Product Damage Precautions

Use Proper Power Source.
Do not operate this product from a power source that applies more than the voltage specified.

Provide Proper Ventilation.
To prevent product overheating, provide proper ventilation.

Do Not Operate With Suspected Failures.
If you suspect there is damage to this product, have it inspected by qualified service personnel.

4.1.1.3. EC Certifications and Compliance

Use in conformity of the definition with fully equipped mainframe with fully closed slots by boards or dummy panels. Sufficient cooling and mains connection must be secured according to regulations. Signal lines length during all tests was less than 3 m. Admitted for powering by industrial mains only.

4.1.1.4. Terms in this Manual

The user is requested to pay particular attention to the parts of the document containing the following terms:

WARNING:
Warning statements identify conditions or practices that could result in injury or loss of life.

CAUTION:
Caution statements identify conditions or practices that could result in damage to this product or other property.

Please pay particular attention to the grey areas where warning and caution statements are emphasised, as shown in the following examples:

CAUTION

PROVIDE PROPER VENTILATION!

WARNING

DO NOT OPERATE IN AN EXPLOSIVE ATMOSPHERE!

4.1.2. Terms and Symbols on the Product

These terms may appear on the product:

- **DANGER** indicates an injury hazard immediately accessible as you read the marking.
- **WARNING** indicates an injury hazard not immediately accessible as you read the marking.
- **CAUTION** indicates a hazard to property including the product.

The following symbols may appear on the product:

DANGER

High Voltage

ATTENTION

Refer to Manual

4.2. Hardware settings

Specific internal hardware components allow to perform the settings concerning the following:

- Selection of the VME Base Address of the board (refer to § 2.6.1 for details);
- Insertion of 110 Ω-termination on one or more lines of the board (refer to §2.6.1 for details);
- Selection of the board behaviour in response to a BUSY signal (refer to §2.6.2 for details);

Details on these settings are given in the relevant sections mentioned above.

4.3. Installation

The V878 board must be inserted in a V430 VME 6U crate.

Please note that the board supports live insertion/extraction into/from the crate, i.e. it is possible to insert or extract it from the crate without turning the crate off. Moreover, it is possible to switch the board off by the relevant PWR switch (see §2.5.2) without cutting the interrupt chain off.

CAUTION: all cables connected to the front panel of the board must be removed before extracting/inserting the board from/into the crate.

CAUTION

ALL CABLES MUST BE REMOVED FROM THE FRONT PANEL

BEFORE EXTRACTING THE BOARD FROM THE CRATE!

5. Principles of operation

The board has 32 individual differential ECL inputs and one COM input (ECL/NIM), common to all channels, which is used to control data acquisition timing according to the selected operating mode (COMMON START/ COMMON STOP).

Each time interval between the COM signal and the input channel signals is converted into a voltage level by the TAC sections.
If the COMMON START mode is selected (default, see § 3.27), the time intervals will start with the leading-edge of the COM pulse and will end at the occurrence of the relevant channel signal (leading edge) which acts as STOP signal.
If the COMMON STOP mode is selected (see § 3.27), the time intervals will start with the leading-edge of the relevant input channel ECL signal and will end with the leading edge of the COM pulse which now acts as STOP signal.

The outputs of the TAC sections are multiplexed and subsequently converted by a fast 12-bit ADC (10 µs for all channels).
Only the values that are above a programmable threshold (see § 5.3), do not cause overflow (see §5.4) and are not killed (see §5.3) will be stored in a dual port data memory accessible via VME.

In the following functional sections and operation principles of the module are described in some detail. The block diagram of the module can be found in Fig. 1.1.

5.1. TAC sections

The time to amplitude conversion is based on the charging of a capacitor at constant current. A schematic view of the TAC section is reported in Fig. 5.1.

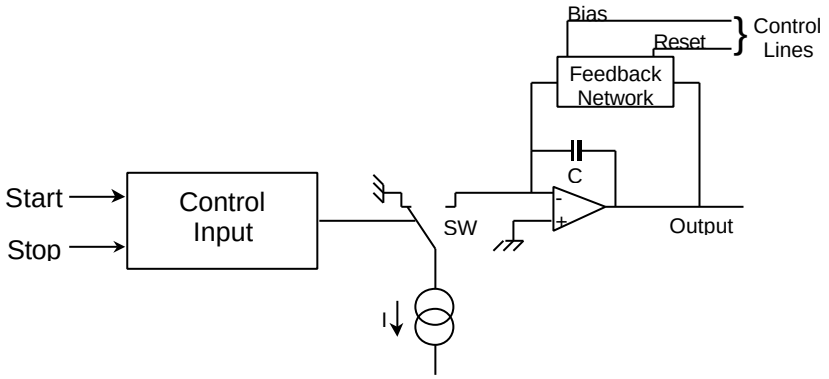

Fig. 5.1: Simplified block diagram of the Time to Amplitude Converter section

The start pulse closes the switch SW and allows the capacitor C to be charged at the current I. The control of the front panel signals and of the START and STOP signals is

performed by the *Control Input* section according to the selected operating mode (COMMON START or COMMON STOP, see § 3.27).

The timing of the signals involved in the conversion of data is shown in

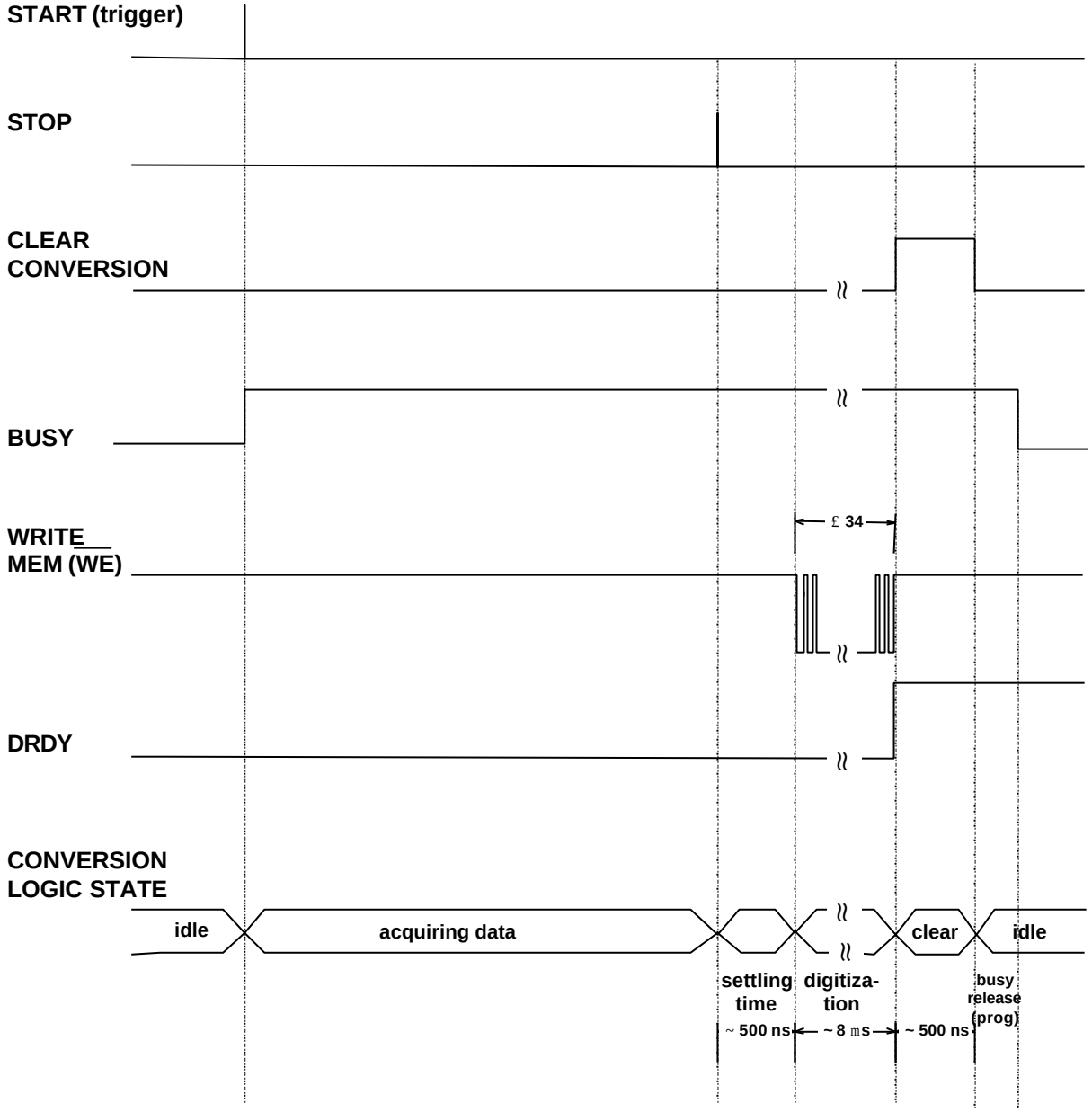

Fig. 5.1.

The diagram includes four different temporal phases: idle, data acquisition, settling time, digitization and clear.
While the conversion logic is ***idle*** the *feedback network* keeps the TAC output at V_{off}: at the occurrence of a START signal the ***acquiring data*** phase starts up, during which the TAC output increases linearly until the stop signal arrival (V_{out}). As the STOP signal occurs, the *feedback network* acts as a high level impedance to hold the capacitor charge until the end of the digital conversion (***digitisation***). The latter starts about 500 ns (***settling time***) after the STOP signal and takes about 8 µs. After the digital conversion, the ***clear*** phase

takes place by a fast capacitor discharge (about 500 ns) which makes the conversion logic idle again.
The relationship between V_{out} and the time difference $T=t_{stop}-t_{start}$ is:

$$V_{out} = V_{off} + \frac{I}{C}T \quad .$$

The input signals which act as START and STOP for the conversion of the single channel are different according to the selected operating mode.
If the COMMON START mode is selected (default, see §3.27), the leading-edge of the COM pulse starts the conversion, while the leading edge of the relevant channel signal acts as STOP signal.
If the COMMON STOP mode is selected (see §3.27), the conversion will start with the leading-edge of the relevant input channel ECL signal and will end with the leading edge of the COM pulse which now acts as COMMON STOP signal.

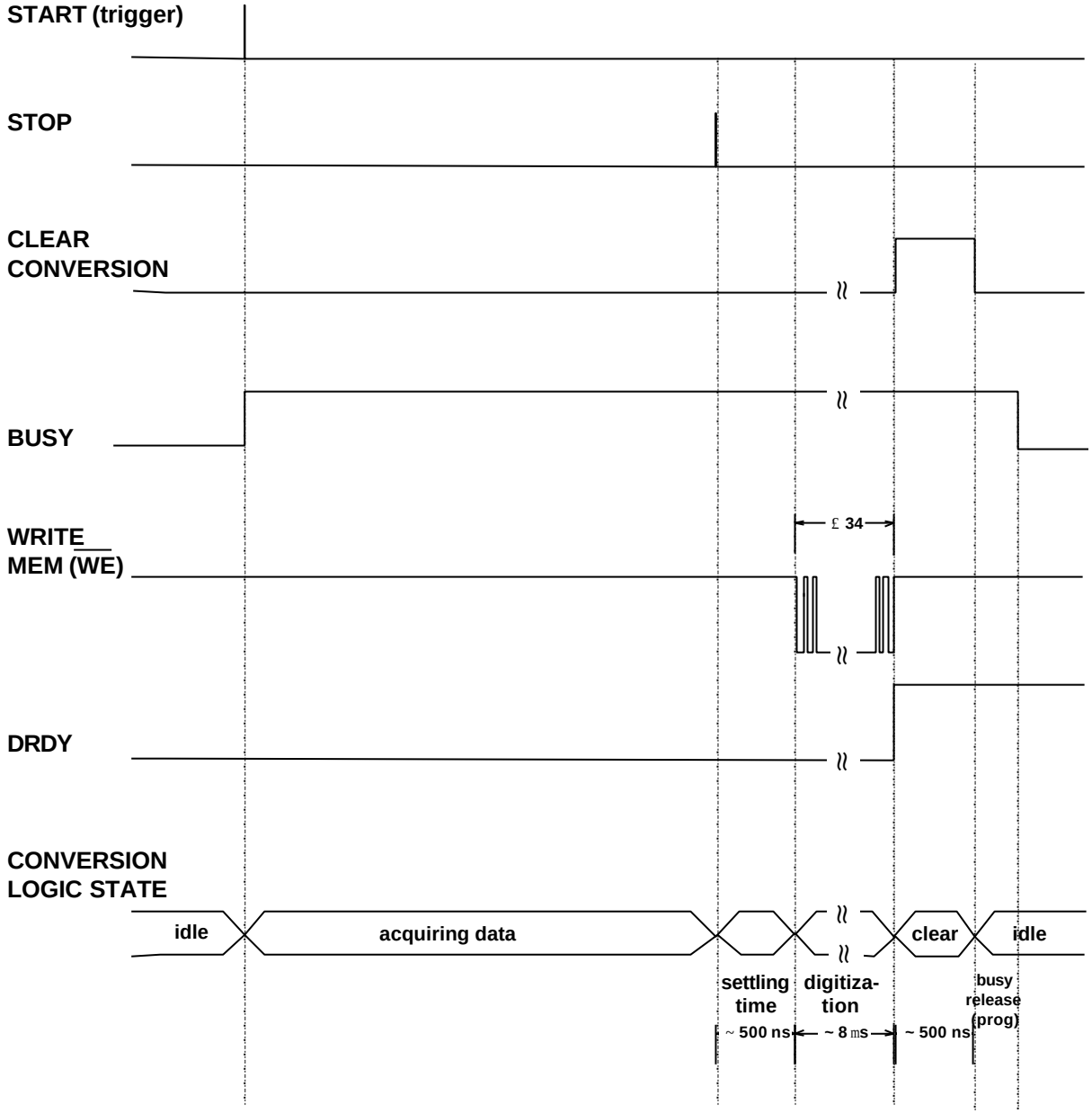

Fig. 5.1: Signal timing for conversion sequence

5.2. Analog to digital conversion

The output of each TAC section is multiplexed, by group of 4 channels, and subsequently converted by a fast 12-bit ADC. The ADC supports the sliding scale technique to reduce the differential non-linearity (see references [1], [2]). This technique (see Fig. 5.2) consists in adding a known value to the analog level to be converted, thus spanning different ADC conversion regions with the same analog value. The known level is then digitally subtracted after the conversion and the final value is sent to the threshold comparator.
If the sliding scale is enabled, it reduces slightly the dynamic range of the ADC: the 12-bit digital output is valid from 0 to 3840, while the values from 3841 to 4095 are not correct.

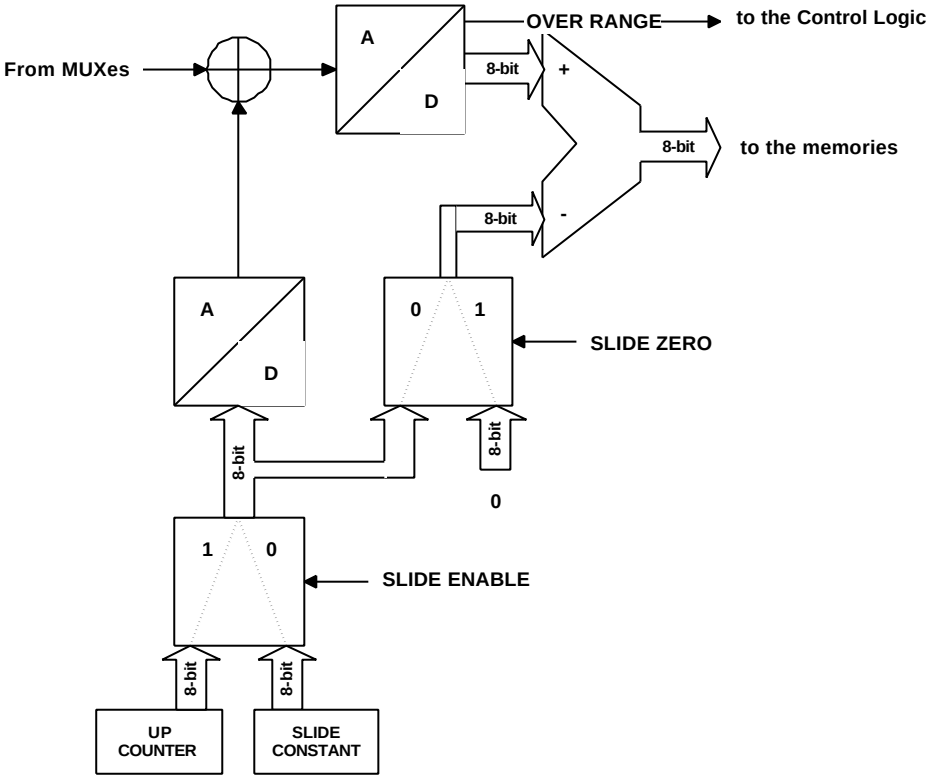

Fig. 5.2: Block diagram of the sliding scale section

5.3. Zero suppression

The output of the ADC is fed to a threshold comparator to perform the zero suppression.
If the converted value from a channel is greater than (or equal to) the relevant low threshold value set via VME in the Thresholds memory (Base Address + 0x1080 ÷ 0x10BF, see § 3.42), the result is fed to the dual port memory and will be available for the readout.
If the converted value is lower than the threshold, the value is stored in the memory only if the LOW TRESHOLD PROG. bit of the Bit Set 2 Register is set to 1 (see § 3.27). The fact that the converted value was under the threshold is also flagged in the datum stored in the memory, where the bit 13 (UNDERTHRESHOLD) of the 16-bit data word is set to 1 (see § 3.5).

The Thresholds memory allows for the setting of one low threshold value for each channel. Default setting corresponds to thresholds not defined.

The comparison is performed between the 8MSB of each 12-bit converted value and the 8-bit threshold value which is stored in the relevant register, as illustrated in the figure.

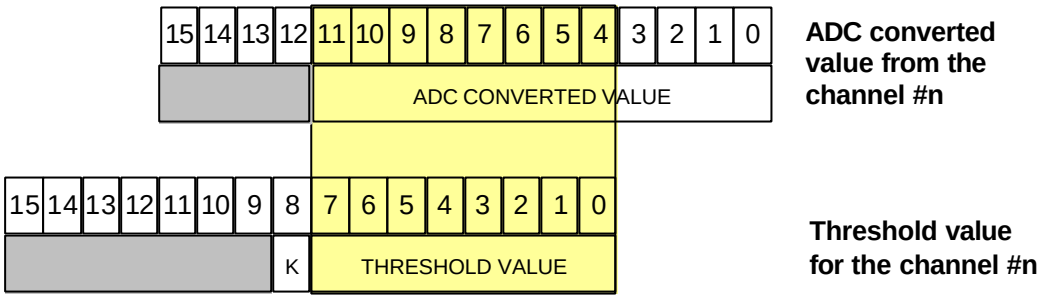

Fig. 5.3: Zero suppression

The content of the Threshold Register includes also a KILL bit, which allows to abort the memorisation of the datum even if it is higher than the threshold set in the register. This bit can thus be used to disable some channels. Refer to § 3.42 for further details.

The threshold values are lost only after switching the board off (a reset operation does not affect the threshold values).

5.4. Overflow suppression

The overflow suppression allows to abort the memorisation of data which originated an ADC overflow. The control logic provides to check if the output of the ADC is in overflow and, in the case, the value is not stored in the memory.
The overflow suppression can be disabled by means of the OVER RANGE PROG bit of the Bit Set 2 Register (see § 3.27): if this bit is set to 1, all the data, independently from the fact that they caused ADC overflow or not, are stored in the memory. In this case, the 16-bit word stored in the memory will have the bit 12 (OVERFLOW) set to 1 (see § 3.5).

5.5. Multiple Event Buffer (MEB)

After the conversion, if there is at least one converted value above the programmed threshold, not causing overflow and not killed, the control logic stores it in the Multi-Event Buffer (MEB).

The Multi-Event Buffer is a Dual Port Memory (34 Words/event) which can store up to 32 events. It is available at the VME address: Base Address + 0x0000÷0x07FF (see also § 3.5).

In order to trace the event flow, two pointers (Read and Write pointer) are employed.
The Read Pointer points to the active read buffer.

The Write pointer is incremented automatically via hardware at the end of the channels conversion, while the Read pointer can be either incremented automatically (AUTO INCR. bit of the Bit Set 2 Register set to 1; see § 3.27) or via write access to one of two dummy registers, Increment Event and Increment Offset Registers (see §3.24 and 3.25). These allow to move the readout pointer to the next event in the output buffer or to the next word, respectively.

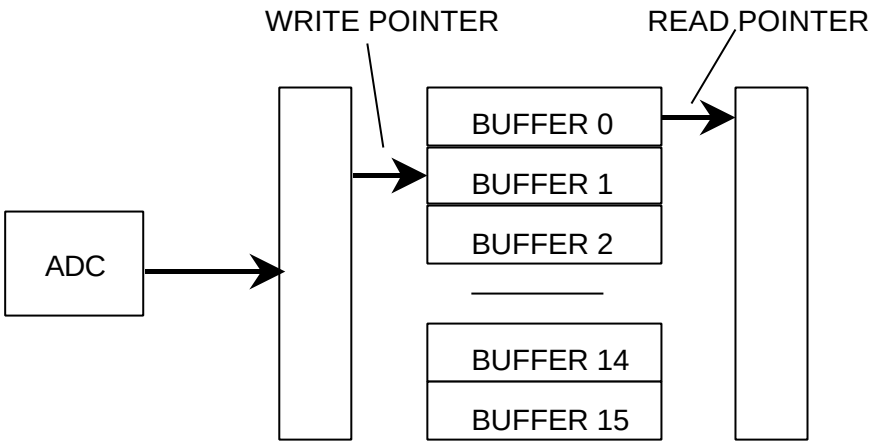

Fig. 5.4: Multi-Event Buffer: Write pointer and Read pointer

The MEB can be either in a "Full", a "Not empty" or an "Empty" status.
When the 5MSB of the Read pointer and the 5MSB of the Write pointer are different (i.e. point to different events), the MEB is in a "Not empty" status.
When the Read pointer and the Write pointer are equal, the MEB can be either in a "Full" or an "Empty" status. The MEB is full or empty according to the last increment pointer operation performed: if the last increment is the one of the Write pointer, the MEB is Full; if the last increment is the one of the Read pointer, the MEB is Empty.
The status of the MEB is monitored via two Registers, the Status Register 1 and the Status Register 2 (see § 3.13 and § 3.21, respectively).

After the conversion, the accepted data (i.e. the converted values above the programmed threshold, not causing overflow and not killed) are stored in the active event buffer (i.e. the one pointed by the write pointer) in subsequent 32-bit words. These are organised in events. Each event consists of a Header (see Fig. 3.5), a block of data words (Fig. 3.6) and an End-Of-Block (EOB) word (Fig. 3.7).
Each event contains thus from a minimum of 3 32-bit words (Header, one data word and EOB) to a maximum of 34 32-bit words (Header, 32 data words and EOB).

In case there are no accepted data, the user can choose to store anyway in the MEB the Header and the EOB relative to the event (see EMPTY PROG bit of the Bit Set 2 Register, see § 3.27): in this case the event is constituted by 2 32-bit words only.

The **Header** content is as follows:

- GEO address (bits[31…27])
- Type of word (bits[26..24]; 010 →header)
- Crate number (bits[23..16])
- 00 (bits[15, 14])
- Number of memorised channels (bits[13…8])
- Reserved (bits[7…0]).

The **Data Word** content is as follows:

- GEO address (bits[31…27])
- Type of word (bits[26..24]; 000 →datum)
- 00 (bits[23, 22])
- Number of the channel which the datum comes from (bits[21..16])
- 00 (bits[15, 14])
- UNDERTHRESHOLD flag (bit[13])
- OVERFLOW flag (bit[12])
- Converted datum (bits[11..0]).

The **End-Of-Block** content is as follows:

- GEO address (bits[31…27])
- Type of word (bits[26..24]; 100 →EOB)
- Event Counter (bits[23..0]).

The MEB may contain a not valid datum as well. In a not valid datum only the bits[26..24], which mark it as not valid datum, are meaningful.

The **Not Valid Datum** content is as follows:

- Type of word (bits[26..24]; 110 →not valid datum).

The meaning of the bits[26…24] to identify the type of word stored in the buffer is summarised in Table 5.1.

Table 5.1: Word type in the multi-event buffer

	Bit 26	Bit 25	Bit24
Header	0	1	0
Datum	0	0	0
End of Block	1	0	0
Not valid datum	1	1	0
Reserved	X	X	1

The converted data, relative to each event, are stored in the active write buffer (i.e. the buffer pointed by the Write Pointer) in the following order:

- **Channel 0**
- **Channel 1**
- **Channel 2**

…..

- **Channel 30**
- **Channel 31**

However, because of possible user's settings (e.g. Zero/Overflow suppression), some channels can be missing. In any case, each data word contains the converted datum together with its relevant channel number.

Fig. 5.5 shows an example of the Multi-Event Buffer structure in case of zero suppression enabled and with event counter set so as to count all events (see § 5.6).
The first event written in the active Event Buffer (Write pointer = n) is that relative to the COM n.5 pulse causing the conversion of two channels (2 and 5) which were over the programmed threshold: the stored event is constituted by a Header, the data relative to the two channels and the End of Block word at the end of all converted data of the relevant Event.
During COM n.6 and n. 7 no channels were in the selected range.
The next event written in the following active Event Buffer (Write pointer = n+1) is that relative to the COM n.8 pulse: it consists of the Header, the data relative to three channels (0, 17 and 3) and the End of Block word at the end of all converted data.

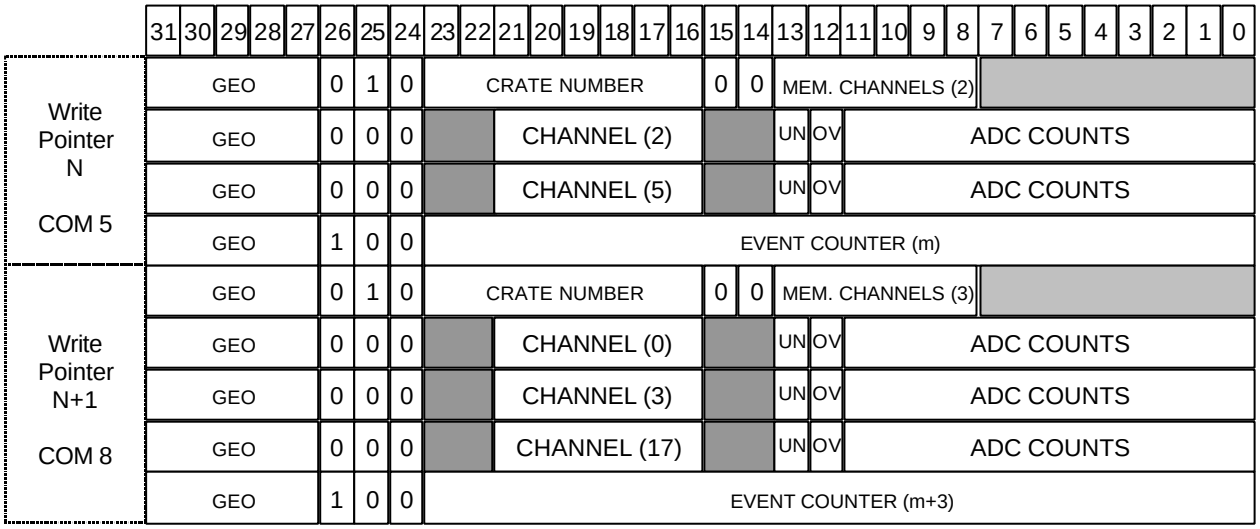

Fig. 5.5: Multi-Event Buffer: data structure example

5.6. Event Counter

The module houses a 24-bit counter that counts the number of COM signals that the module has received.

The Event Counter can work in two different modes, which can be selected via the Bit 14 (ALL TRG) of the Bit Set 2 Register (see § 3.27):

Mode A (ALL TRG = 1): it counts all events (default);
Mode B (ALL TRG = 0): it counts only the accepted events.

In the first case (Mode A), the Event Counter is increased each time a pulse is sent through the COM input and acts also as an absolute time counter.
In the second case (Mode B), the Event Counter is increased each time a pulse, sent through the COM input, is accepted (i.e. VETO, FCLR and BUSY are not active).

The value of the Event Counter is stored in the EOB of the Multi-Event Buffer (see §3.5). The Event Counter is also stored in two registers, the Event Counter_Low and Event Counter_High Registers, which respectively contain the 16LSBs and the 8MSBs of the Event Counter (see § 3.22 and § 3.23).

5.7. Busy Logic

The board is BUSY either during the conversion sequence or during the reset of the TAC section or when the MEB is not ready to accept data (MEB Full) or when the board is in Random Memory Access Test mode (see § 6.4.1).
On the occurrence of one of these conditions the front panel BUSY signal (CONTROL bus) is active, the red BUSY LED is on and the bit 2 (BUSY) and bit 3 (GLOBAL BUSY) of the Status Register 1 are set to 1 (see § 3.13).
The BUSY LED lights up also while the board is configuring (power-on).

The BUSY signal on the CONTROL bus allows to obtain a wired-OR/NAND GLOBAL BUSY signal of a chain of many units connected together via the CONTROL bus.
Actually, each module sets to 1 its BUSY output at the occurrence of the leading-edge of the START signal and drops it at the end of the conversion sequence. When the module is busy, it does not accept another START. If many units are connected via the COM and BUSY signals of the CONTROL bus, after the START leading edge the GLOBAL BUSY signal is set to 1 and it is dropped only when all the modules in the chain have completed the conversion sequence and the system is ready to accept another START input.
The jumper J9 placed on the PCB (see Fig. 2.3) allows to select board behaviour in response to a BUSY/GLOBAL BUSY status: if this jumper is set to EXTBSY, the acquisition is stopped as soon as any of the boards on the Control bus is BUSY; if the jumper is set to INTBSY, acquisition is stopped as the board is BUSY.

The GLOBAL BUSY condition is also flagged by the bit 3 (GLOBAL BUSY) of the Status Register 1 set to 1 (see § 3.13).

5.8. Reset Logic

Three different types of RESET operations can be distinguished, according to the effects they have on the module and particularly on the registers. These are:

- *Type A*: Data RESET
- *Type B*: Software RESET
- *Type C*: Hardware RESET

The **Data RESET** clears the data in the output buffer, resets the read and write pointers, the event counter and the TAC sections. It does not affect the registers.
This type of RESET can be forwarded in two ways:

1. setting the Bit 2 (CLEAR DATA) of the Bit Set 2 Register to 1 (see §3.27). the Reset is released via the Bit Clear 2 Register (see § 3.28);
2. sending a RESET pulse from the front panel with the Bit 4 (PROG RESET) of the Control Register 1 set to 0 (see § 3.14).

The **Software RESET** performs the same actions as the data RESET and, moreover, it resets the registers marked in the column SR (Software Reset) in Table 3.2.
This type of RESET can be forwarded in three ways:

1. setting the Bit 7 (SOFTWARE RESET) of the Bit Set 1 Register to 1 (see § 3.9): this sets the module to a permanent RESET status which is released only via write access, with the relevant bit set to 1, to the Bit Clear Register;
2. sending a RESET pulse from the front panel with the Bit 4 (PROG RESET) of the Control Register 1 set to 1 (see § 3.14);
3. performing a write access to the Single Shot Reset Register (see §3.17): the RESET lasts as long as the write access itself.

The **Hardware RESET** performs the same actions as the Software RESET and, moreover, it resets further registers. All the registers reset by a Hardware RESET are marked in the column HR (Hardware Reset) in Table 3.2.
This type of RESET is performed:

1. at Power-On of the module;
2. via a VME RESET (SYS_RES).

At power on or after a reset the module must thus be initialised.

5.9. FAST CLEAR

The FAST CLEAR of the module can be performed via the relevant front panel signal on the CONTROL connector (see § 2.4.2). A FAST CLEAR signal, generated at any time within the FAST CLEAR window, i.e. between the leading edge of the COM signal and the end of

the programmable time value set in the Fast Clear Window Register (see §3.26), aborts the conversion. Its minimum width must be 10 ns.

N.B.: since a FAST CLEAR operation implies a CLEAR CONVERSION cycle, a new COM signal is accepted only if it occurs at least 600 ns after the leading-edge of the FAST CLEAR signal.

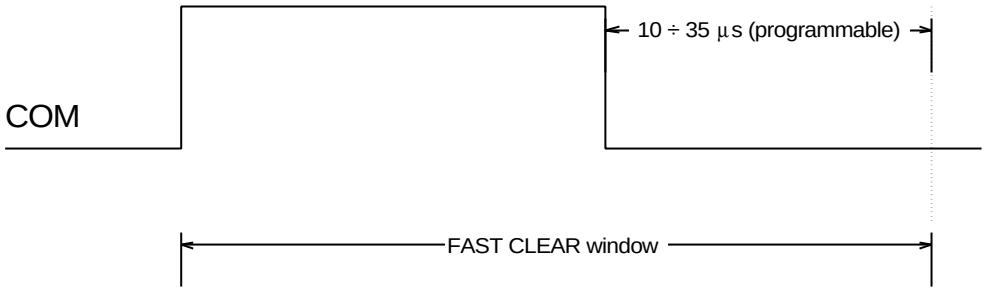

Fig. 5.6: Fast Clear window

6. Operating modes

6.1. Power-on sequence

To power-on the board follow this procedure:

1. insert the V878 board into the crate: as the board is inserted, the OVC PWR green LED lights up indicating that the board is powered;
2. if the TERM LED, BUSY LED and DRDY LED are off, press the flush plunger PWR micro-switch on the front panel by inserting into it a pin: as this switch is pressed, the TERM LED lights up orange, the BUSY LED becomes red and the DRDY LED becomes yellow; this indicates that the board is turned on and is configuring;
   if the TERM LED, BUSY LED and DRDY LED are on, it means that the board is already on and is configuring (the board can be ON or OFF as it is inserted into the crate, depending on how it was when it was extracted);
3. after a short time the BUSY and DRDY LEDs will light off and the TERM LED will become either red or green or off, according to the status of the terminations on the PCB of the board: this indicates that the board is ready to acquire data.

N.B.: if the OVC PWR LED becomes orange instead of being green, there is an overload and the over-current protection is now running. In order to acquire data, it is necessary to remove the overload source, then turn the board off and switch it on again. Sometimes, it may happen that the OVC PWR LED is orange as soon as the board is inserted in the crate: this is due to the fact that the board has been just misplaced into the crate. In this case, extract the board and insert it again into the crate.

6.2. Power-on status

At power-on the module is in the following status:

- the Event Counter is set to 0;
- the Output buffer is cleared;
- the Read and Write Pointer are cleared (i.e. Buffer 0 is pointed);
- the Interrupt Level is set to 0x0 (in this case interrupt generation is disabled) and the Interrupt Vector is set to 0x0;
- the values in the threshold memory are not defined (see § 3.42);
- the MCST/CBLT address is set to 0xAA.

Moreover, all other registers marked in the column HR (Hardware RESET) in Table 3.2 are cleared or set to the default value.

At power on or after a hardware reset (see § 5.8) the module must thus be initialised.

6.3. Operation sequence

After the power-on sequence the module is in the status described above.

Please note that the threshold values are not defined after power-on and consequently before starting the operation of the module it is necessary to set a threshold value for each channel in the Threshold memory (refer to § 3.42).

The module can work either in COMMON START or COMMON STOP mode. The operating mode can be selected via the relevant bit (bit 10, COMM STOP) of the Bit Set 2 Register (see § 3.27).

6.3.1. COMMON START mode

To select the COMMON START mode, set the bit 10 of the Bit Set2 Register to 0, (default setting). Refer to § 3.27 for further details on operating mode selection.

If the module is not BUSY, an ECL pulse on the COM input causes the following:

1. starts the TAC acquisition;
2. increments the event counter according to the user's settings (see § 5.6);
3. sets the BUSY output signal to 1.

The control logic waits for the time necessary for the maximum TAC range; during this time an ECL pulse on any input stops the corresponding TAC section. If neither RESET nor FAST CLEAR (refer to § 5.8 and § 5.9) occur during this time to abort the conversion, the control logic starts the following conversion sequence:

1. The outputs of the TAC sections are multiplexed and sampled;

2. The control logic checks if there are accepted data among the converted values, according to the user's settings (zero suppression, overflow suppression and KILL option: see § 5.3 and § 5.4):
    a) if there are accepted data, these are stored in the active event buffer together with a Header and an EOB;
    b) if there are no accepted data and the EMPTY PROG bit of the Bit Set 2 Register is set to 0 (default setting, see § 3.27), no data will be written in the output buffer.
    c) if there are no accepted data and the EMPTY PROG bit of the Bit Set 2 Register is set to 1 (see § 3.27), the Header and EOB only will be written in the output buffer.

3. The TAC sections are cleared and the BUSY is removed and the module is ready for the next acquisition.

6.3.2. COMMON STOP mode

To select the COMMON STOP mode, set the bit 10 of the Bit Set 2 Register to 1. Refer to § 3.27 for further details on operating mode selection.

If the module is not BUSY, an ECL pulse on any input starts the TAC conversion of the corresponding TAC section. An ECL input on the COM input causes the following:

1. stops the TAC acquisition;
2. increments the event counter according to the user's settings (see § 5.6);
3. sets the BUSY output signal to 1.

If neither RESET nor FAST CLEAR (refer to § 5.8 and § 5.9) occur to abort the conversion, the control logic starts the following conversion sequence:

1. The outputs of the TAC sections are multiplexed and sampled;
2. The control logic checks if there are accepted data among the converted values, according to the user's settings (zero suppression, overflow suppression and KILL option: see § 5.3 and § 5.4):
   a) if there are accepted data, these are stored in the active event buffer together with a Header and an EOB;
   b) if there are no accepted data and the EMPTY PROG bit of the Bit Set 2 Register is set to 0 (default setting, see § 3.27), no data will be written in the output buffer.
   c) if there are no accepted data and the EMPTY PROG bit of the Bit Set 2 Register is set to 1 (see § 3.27), the Header and EOB only will be written in the output buffer.
3. The TAC sections are cleared and the BUSY is removed and the module is ready for the next acquisition.

6.4. Test Modes

Two different test modes can be enabled:

- **Random Memory Access Test Mode,**
- **Acquisition Test Mode,**

The first test mode operation is enabled via the Bit 0 of the Bit Set 2 Register and allows to write directly into the buffer.
The second test mode is enabled via the Bit 6 of the Bit Set 2 Register and allows to test the whole acquisition system by writing a set of 32 data in an internal FIFO which are then transferred to the output buffer at each COM pulse for the readout.

The test modes will be described in detail in the following subsections.

6.4.1. Random Memory Access Test Mode

This test mode allows the user to write and read a word in the output buffer.

To perform such test follow these steps:

1. Set to 1 the Bit 0 of the Bit Set 2 Register (see § 3.27);
2. Write into the W Memory Test Address Register (see § 3.29) the 11-bit address where to write the test word;
3. Write the high and low part of the 32-bit test word respectively in the Testword_High and Testword_Low Registers (see § 3.30 and § 3.31). As the Testword_Low register is accessed, the whole test word is written into the memory;
4. Write in the R Test Address Register (see § 3.35) the 11-bit reading memory address and read out the buffer; please note that this address must be different from the write address written in the W Memory Test Address Register.

N.B.: please note that the R Memory Test Address must be different from the W Memory Test Address at any step of the procedure. If the user tries to write an address in one of these registers that is equal to the address contained in the other register, write cycles (step 3. above) will not write the correct value.

6.4.2. Acquisition Test Mode

This test mode allows the user to simulate the real operation of the board without using any channel input signals but just writing the data into a FIFO via an appropriate register (Test Event Write Register, see § 3.33) and reading them after a COM signal.

To operate the acquisition test follow these steps:

1. Set to 1 the Bit 6 (TEST ACQ) of the Bit Set 2 Register (see §3.27); this action selects the Acquisition Test Mode and resets the write pointer in the FIFO;
2. Set to 0 the Bit 6 (TEST ACQ) of the Bit Set 2 Register (see § 3.27); this action resets the read pointer in the FIFO and releases the write pointer;

3. Write 32 data words (each word consisting of a 13-bit word, corresponding to the ADC converted value, + the overflow bit, see §3.33) in the Test Event Write Register (Base Address + 0x103E). These 32 data constitute the event to obtain as output of the 32 channels. The 32 test data must be written in this FIFO in the same order as they will be read from the output buffer, that is:

    - test datum for the channel 0
    - test datum for the channel 1
    - test datum for the channel 2
    - …….
    - test datum for the channel 29
    - test datum for the channel 30
    - test datum for the channel 31

    N.B.: please note that the user must write at least and not more than 32 test words. Actually, since the words are written in a circular FIFO, if the user writes less than 32 words, some words will be not defined; on the other hand, if the user writes more than 32 words, some words will be overwritten.

4. Set to 1 the Bit 6 (TEST ACQ) of the Bit Set 2 Register (see §3.27); this action resets again the write pointer in the FIFO and releases the read pointer;
5. at each COM signal an event, based on the data previously written in the FIFO, will be transferred to the output buffer. The data will be read via VME in the same order as they were written into the FIFO:

    - test data word for the channel 0
    - test data word for the channel 1
    - test data word for the channel 2
    - …….
    - test data word for the channel 29
    - test data word for the channel 30
    - test data word for the channel 31

N.B.: To operate in normal mode again, the Bit 6 of the Bit Set 2 Register must be set again to 0.

6.5. Block Transfer Mode

The module supports the Standard BLT32 and MBLT64 modes.

A standard readout in Block Transfer mode, for example, consists of a readout of the Header for the relevant event and a Block Transfer readout of the number of data words relative to the event (the number of data words referring to the event is the CNT number in the Header, see § 3.5).

A more efficient readout in Block Transfer mode can be performed by using the BLOCK END and BERR-ENABLE bits of the Control Register 1 (see § 3.14).

Some examples of this type of readout in Block Transfer mode are as follows:

Example A: BLOCK END = 0, BERR_ENABLE = 0;
A Block Transfer readout of 32x34 words (32 events max., each event 34 words max.) allows the readout of all data stored in the buffer: as the buffer is empty, the module will send only not valid data.

Example B: BLOCK END = 0, BERR_ENABLE = 1;
A Block Transfer readout of 32x34 words (32 events max., each event 34 words max.) allows the readout of all events stored in the buffer: as the buffer is empty, a BERR is generated.

Example C: BLOCK END = 1, BERR_ENABLE = 0;
A Block Transfer readout of 34 words (each event 34 words max.) allows the readout of one complete event: after the readout of the EOB the module will send only not valid data.

Example D: BLOCK END = 1, BERR_ENABLE = 1;
A Block Transfer readout of 34 words (each event 34 words max.) allows the readout of one complete event: as the EOB is encountered, a BERR is generated.

The use of the BERR_ENABLE bit (Examples B and D above) is suggested only if the VME CPU can handle the Bus Error (BERR) in an effective way.

N.B.: Please note that, according to the VME standard, a Block Transfer readout can be performed with 256 read cycles maximum: as a consequence, a readout with a greater number of read cycles may require more BLT operations.
This limit is not due to the board itself but only to the VME standard: if it is possible to disable or delay the timeout of the BUS Timer (BTO(x)), a Block Transfer readout with more than 256 read cycles can be performed as well.

6.6. Advanced Setting and Readout Modes

Chained Block Transfer (CBLT) and Multicast (MCST) operations allow to enhance the set and readout time of the 32 channels. These operations allow accessing several boards at the same time: CBLT operations are used for reading cycles only, while MCST operations are used for write cycles only.

CBLT and MCST modes use the IACKIN and IACKOUT VME lines for the control transfer from one board to the following one: the interrupt daisy-chain is used to pass the token from one board to the following one (see Ref. [4]). The board which has received the token stores/sends the data from/to the master via MCST/CBLT accesses.
No empty slots must thus be left in the chain or, in alternative, empty slots can be left only in case VME crates with automatic IACKIN/IACKOUT short-circuiting are used.

In order to perform CBLT and MCST operations, the higher Base Address bits of all the involved modules (i.e. bits 31 to 24) must be set in common to all boards via the MCST/CBLT Address Register (see § 3.8). This means that all boards must have the same setting on bits 31 to 24.
The resulting MCST (CBLT) Base Address for all boards is:

MCST (CBLT) Base Address = %NN000000,

Once the addresses have been set, the first and last board in a chain must have, respectively, only the FIRST_BOARD and only the LAST_BOARD bit set to 1 in the MCST Control Register (see § 3.8). Conversely, all intermediate boards must have both the FIRST_BOARD and the LAST_BOARD bits set either to 1 or to 0.

For further details on the CBLT/MCST addressing mode please refer to § 3.1.4 and § 3.1.5.

6.6.1. Chained Block Transfer Mode

Once set the address of the boards as described in the above section, the boards can be accessed in Chained Block Transfer mode (CBLT, see Ref. [4]). This mode allows for sequential readout of a certain number of contiguous boards in a VME crate. A CBLT access is allowed with the BLT32 and MBLT64 address modifiers only (CBLT32 and CBLT64 accesses respectively).

N.B.: The CBLT operation can be performed only for the readout of the Multi-Event Buffer: its address in CBLT mode corresponds to the set of offsets listed in Table 3.3 to be added to the address, common to all boards, set by the user via the MCST/CBLT Address Register which contains the most significant bits of the address (see § 3.8).

The CBLT uses the VME Bus Error (BERR) generated by the last board in the chain as a data readout completion flag. This feature is very useful if the VME CPU handles the Bus Error in an efficient way. For a correct board operation, it is MANDATORY that a VME Bus Error is generated.
The user must thus perform a number of CBLT accesses that allows for the readout of all data in all boards of the chain in all possible occupancy conditions. E.g.: if the user has a chain of 10 boards, the total number of words for a given event lies between 0 (i.e. no data) and 34x10=340 32-bit words (i.e. each board has an event, each event consists of a Header

+ 32 data + End of Block). In order to be sure that a BERR is generated, the user must thus perform 11 CBLT accesses of 34-word each.

In CBLT32 mode the first board of the chain starts sending data (if there are any, i.e. if it is not purged, see § 3.13); as it has sent all data and the EOB is met, the board becomes purged, i.e. the relevant bit (PURGED) of the Status Register 1 is set to 1. This implies that the board will not be involved in the CBLT access any more since it has already sent all the required data. At this point the IACKOUT line is asserted and the next board, if not purged, starts sending data. As the last board receives the token and is purged, it asserts a BERR which acts as a data readout completion flag.
In CBLT64 mode the accesses work as in the CBLT32 one, except for the fact that the address is acknowledged during the first cycle and consequently a DTACK is asserted at least once.

In CBLT mode the Read Pointer must be incremented automatically: if the AUTOINC_ENABLE bit is set to 1 in the Bit Set 2 Register (see § 3.27), the Read Pointer is automatically incremented with the readout of the End Of Block word of each board; if the AUTOINC_ENABLE bit is set to 0, the Read Pointer is not automatically incremented and only the Header of the first word is read.

N.B.: Please note that, according to the VME standard, a Chained Block Transfer readout can be performed with 256 read cycles maximum: as a consequence, a readout with a greater number of read cycles may require more CBLT operations.
This limit is not due to the board itself but only to the VME standard: it is actually possible to performed a CBLT readout with more than 256 read cycles if the timeout of the BUS Timer (BTO(x)) is disabled or delayed.
If the latter action is not allowed and the CBLT readout stops before having read all data, the new CBLT cycle will start from where the token was left in the previous cycle: this goes on until the last board is reached and all data read, so that a BERR is generated.

6.6.2. Multicast Commands

Once set the address of the boards as described in § 6.6, the boards can be accessed in Multicast Commands (MCST) mode. The MCST mode allows to write in the registers of several boards at the same time by accessing a dummy Address only once. The latter is composed by the MCST Base Address plus the offset of the relevant register, according to the list shown in Table 3.4. Refer to § 3.1.4 for details on MCST addressing mode.
MCST access can be meaningless (even if possible) for the setting parameters depending on the individual channel characteristics.

N.B.: the MCST/CBLT Address Register must NEVER be accessed in MCST mode since this can affect the CBLT and MCST operations themselves.

7. References

[1] C. Cottini, E. Gatti, V. Svelto, “A new method of analog to digital conversion”, NIM vol. 24 p.241, 1963.

[2] C. Cottini, E. Gatti, V. Svelto, “A sliding scale analog to digital converter for pulse height analisys”, in Proc. Int. Symp. Nuclear, Paris, Nov. 1963.

[3] G. Bianchetti et al., “Specification for VMEbus CRATE Type V430”, CERN-EP, January 1990.

[4] VME64 extensions draft standard, Vita 1.1-199x, draft 1.8, June 13,1997.
VMEBus for Physics Application, Recommendations & Guidelines, Vita23-199x, draft 1.0, 22 May 1997.
Both documents are available from URL: http://www.vita.com