# A 16 channel high resolution (<11 ps RMS) Time-to-Digital Converter in a Field Programmable Gate Array



2012 JINST 7 C02004

(http://iopscience.iop.org/1748-0221/7/02/C02004)

PUBLISHED BY IOP PUBLISHING FOR SISSA

RECEIVED: *October 31, 2011*
REVISED: *December 21, 2011*
ACCEPTED: *January 6, 2012*
PUBLISHED: *February 1, 2012*

TOPICAL WORKSHOP ON ELECTRONICS FOR PARTICLE PHYSICS 2011,
26–30 SEPTEMBER 2011,
VIENNA, AUSTRIA



# A 16 channel high resolution ($<$11 ps RMS) Time-to-Digital Converter in a Field Programmable Gate Array

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ABSTRACT: A 16-channel Time-to-Digital Converter (TDC) was implemented in a general purpose Field-Programmable Gate Array (FPGA). The fine time calculations are achieved by using the dedicated carry-chain lines. The coarse counter defines the coarse time stamp. In order to overcome the negative effects of temperature and power supply dependency bin-by-bin calibration is applied. The time interval measurements are done using 2 channels. The time resolution of channels are calculated for 1 clock cycle and a minimum of 10.3 ps RMS on two channels, yielding 7.3 ps RMS (10.3 ps/$\sqrt{2}$) on a single channel is achieved.

KEYWORDS: Front-end electronics for detector readout; Digital electronic circuits

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doi:10.1088/1748-0221/7/02/C02004

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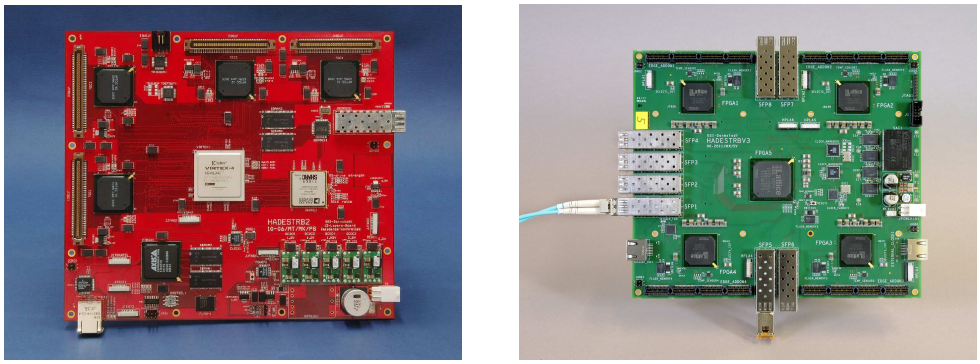
## 1 Introduction

High precision time measurements are essential elements of many applications including physics experiments involving charged particle identification, e.g. Time-of-Flight (ToF). As an example, in the HADES experiment at GSI Helmholtz Centre for Heavy Ion Research Darmstadt, the TDCs measure the ToF of the produced charged particles in several detector systems. The precision of the measurement directly correlates to the ability to discriminate between different types of particles. Additional necessary measurements in physics experiments, such as Time-over-Threshold (ToT) and drift time measurement applications, also require high precision time measurement. With specific Front-End Electronics (FEE) it is also possible to do many other measurements, e.g. charge measurements with Charge-to-Width (Q2W) FEE.

The module for precise time measurement used in HADES experiment, TRB2 [1] (figure 1), uses ASIC TDCs designed at CERN [2]. Although this module has been used successfully not only for HADES, but also for other experiments, e.g. PANDA DIRC, over the past years, there are obstacles to continuing with this module. As indicated in [3], the limited time resolution (40 ps) and limited availability of the HPTDC are a couple of these obstacles. These limitations have directed the research towards TDCs in FPGAs, which have high precision, low cost and short development time.

Various methods, including time stretching, time interpolation, ring oscillator and Vernier methods are used for TDC designs in FPGA and a review of methods is given in [4]. These designs [5–8] had time resolutions between 45 ps and 1.3 ns. Recent developments [9–11] have proved that it is also possible to reach higher time resolutions with the Tapped Delay Line (TDL) method [4]. Time resolutions less than 15 ps were achieved with lab tests using various FPGAs. Based on these experiences it was decided to build a successor of the TRB2 based on TDCs in FPGAs: TRB3 (figure 1b). The development of this board is still ongoing.



**(a)** TRB2 **(b)** TRB3

**Figure 1.** Time-to-Digital Converter Readout Boards: (a) TRB2, with ASIC TDCs, (b) TRB3, with TDCs to be implemented in FPGAs.

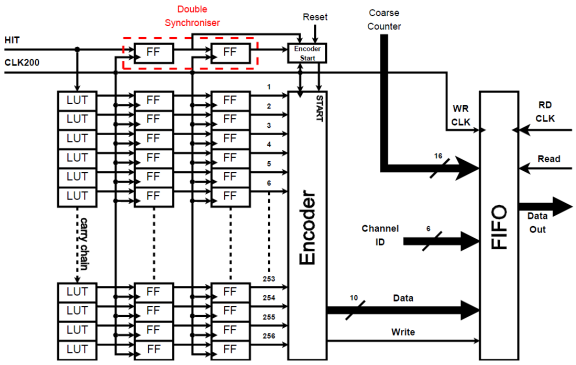



**Figure 2.** Diagram of a channel.

## 2 Architecture of the TDC

The architecture of the designed TDC consists of a fine time measurement block, a coarse counter with granularity of 5 ns, an encoder for the conversion of the result to binary number and a First-In-First-Out (FIFO) memory block for data storage. A block diagram of the designed TDC is shown in figure 2.

In each TDC channel the measurement result of the fine time measurement block is converted to a binary number in the encoder and saved in the FIFO with a coarse time flag. The time interval between different signals measured at different channels can be calculated by simply taking the difference of the relevant measurement results. In figure 3a an example of two signals, their coarse and fine time values and the calculation of the time interval between these signals are shown.

### 2.1 Fine time measurement

For fine time measurements the Tapped Delay Line (TDL) method is used. This method is based on a delay path with delay elements, which have similar propagation delays. With the start signal the propagation along the delay line starts and with the stop signal the output of the each delay



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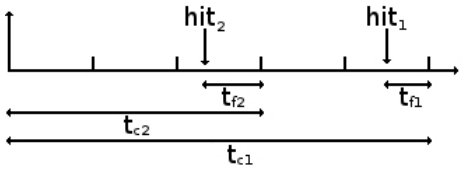
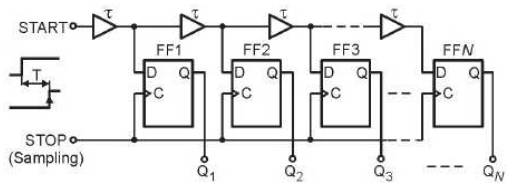



(a)

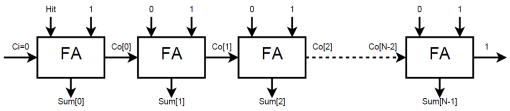
$$\Delta t = t_{hit_1} - t_{hit_2} = (t_{c1} - t_{f1}) - (t_{c2} - t_{f2})$$
$$= (t_{c1} - t_{c2}) - (t_{f1} - t_{f2})$$

(b)

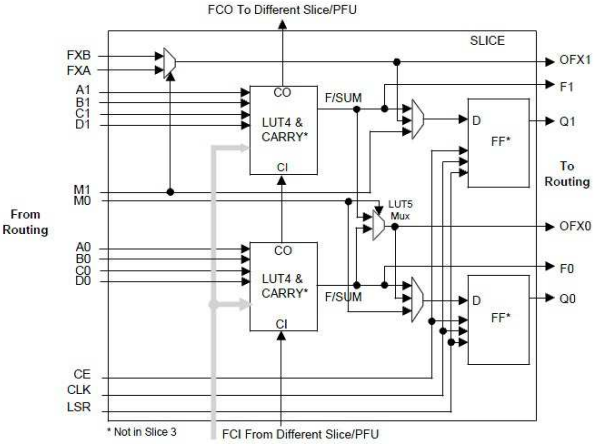
**Figure 3.** (a) Illustration of two time measurements and (b) calculation of the time interval between them.




**(a)** Tapped Delay Line. [4]




**(b)** Tapped Delay Line realised with full adders. [12]




**(c)** Lattice FPGA slice diagram. [13]

**Figure 4.** Look Up Tables programmed as full adders along the carry chain are used as delay elements of Tapped Delay Line and their outputs are registered at the registers located at the same slice.

element is latched (figure 4a). The location of the propagating signal along the delay line defines the fine time measurement between start and stop signals.

The delay line is realised on the dedicated carry chain structure of the Lattice FPGA using the 4-bit Look Up Tables (LUT) and the registers, as delay elements and as latches respectively. In figure 4c the diagram of a slice with 2 LUTs and 2 registers is shown.

In our design each LUT is programmed as a 1-bit full adder and a N delay element chain is created as a N bit adder (figure 4b). All bits of one of the operands are set as '1' and the other operand as '0' except the first bit. The start (hit) signal is assigned to the first bit. As soon as the hit signal arrives to the TDC, starting from the first full adder, the result bits change to '0' and a carry signal is sent to the adjacent full adder. When the stop signal is sent, the outputs of the full adders are latched and the number of zeros defines the location of the propagating carry signal. In our design, the stop signal is defined as the next rising edge of the system clock after the start signal. As the maximum time interval to be measured by the fine time counter is one clock cycle, the total propagation time of the carry signal, along the delay line, has to be longer than a clock period. Manual placement of the delay elements and the corresponding registers are done in order to achieve a uniform delay along the line.

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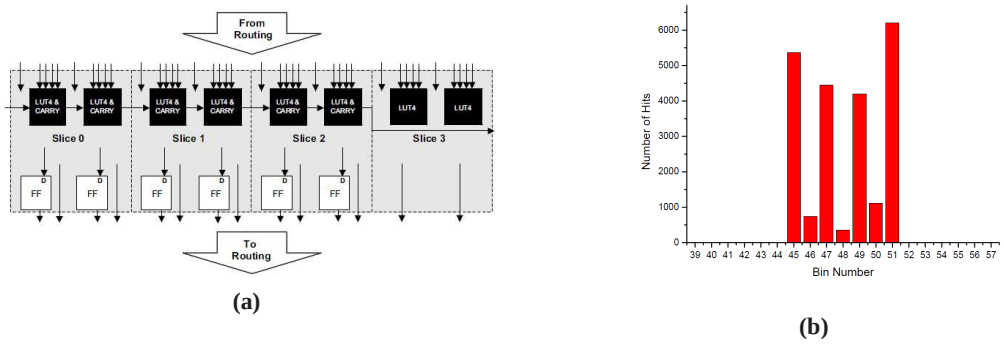


**(a)** **(b)**

**Figure 5.** (a) Programmable Functional Unit of Lattice FPGA. [13] (b) Bin width pattern of a PFU.

### 2.2 Effects of FPGA architecture

As the uniformity of the propagation delays of the elements and the propagation delays from the delay elements to the latches is very important for the precision of the TDC, the architecture of the FPGA used and the placement of the channels in the FPGA have great importance. While some non-uniformity can be handled with careful placement in the FPGA, some related to the FPGA architecture can not be omitted. The main non-negligible non-uniformity is caused by the non-uniform propagation delay between the LUTs. In figure 5 the block diagram of a Programmable Functional Unit (PFU) with 4 slices and the relative bin width of these LUTs are shown. The longer connections between the adjacent slices and the adjacent PFUs cause wider bins - ultra wide bins (UWB) - and lower resolution.

In order to increase the sensitivity of the UWBs and reduce their bin widths the Wave Union Launcher (WUL) [14] is implemented. Using this method makes it possible to have two measurements for the same hit signal using the same carry chain, effectively dividing the UWBs into smaller bins. The result decreases the maximum bin width and the average bin width and therefore decreases the RMS of each channel. Also, as two measurements are used in order to calculate the RMS, the resolution is automatically decreased by a factor of $\sqrt{2}$.

## 3 Test results

A test board [15] with a Lattice ECP2M50E FPGA with 50K LUTs is used in order to test the performance of the designed TDC. 16 TDC channels are implemented in the test FPGA. The tests are done at room temperature. Statistical code density test and statistical test method are used in order to define the bin width distribution and the resolution of the TDC. For mean time measurements precise time intervals created by different cable lengths are measured. The coarse counter operates at 200 MHz frequency having 5 ns granularity. For this period, the active delay elements in the tapped delay line is around 270 for two transitions. As the jitter caused by the clock is high enough to affect the resolution of the TDC, time measurements within 1 clock cycle are the focus of the tests.



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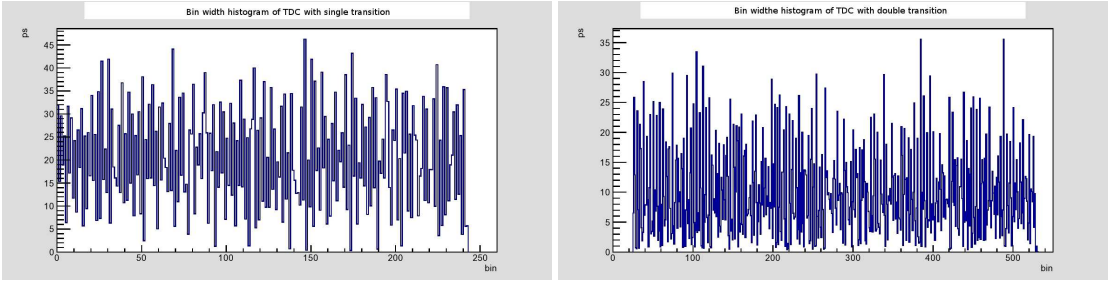


**Figure 6.** Bin width histogram for single and double transitions.

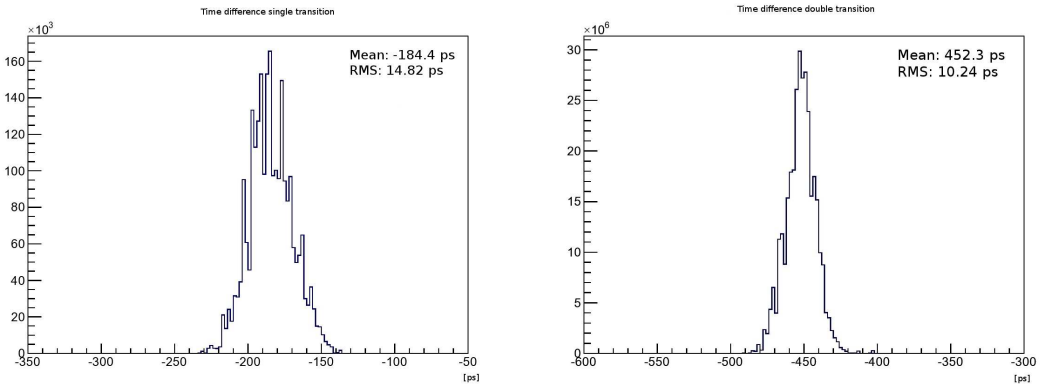


**Figure 7.** Time interval resolution of TDC with single and double transitions.

### 3.1 Statistical error and mean time measurements

A random signal, which is not correlated with the system clock of the TDC, is applied to a channel of the TDC and the histogram of the fine time measurements is created. For each histogram at least 500 000 measurements are made. If the total hits in the histogram ($H_T$) and the period of the system clock ($P$) are known, using the hits in the bin ($H_n$) the bin width of each bin ($BW_n$) can be calculated [14] as: $BW_n = P * H_n/H_T$. The bin widths of the TDC are calculated and histograms are created for 1 transition (without the WUL) and 2 transitions (with the WUL) (figure 6).

The implementation of two transitions divides the UWBs into smaller bins as expected. As it can be seen in figure 6, the implementation of two transitions reduces the average bin width to 10 ps from 20 ps and the maximum bin width to 35 ps from 45 ps. The fluctuation in the bin width is again the result of the non-uniformity of the routing along the carry chain line.

The resolution of the TDC is calculated by measuring a fixed time interval using two channels over 2 000 000 times and calculating the statistical error of the measurements. The resolution calculations are done after calibration. The fixed time interval is created by applying the hit signal to two channels over two cables with different lengths. The RMS of the time interval measurements with 1 transition is calculated as 14.82 ps. The RMS of the time interval measurements reduced approximately by the factor of $\sqrt{2}$ for the TDC with 2 transitions is 10.24 ps. As this is the statistical error of two channels together, the statistical error, resolution, of one TDC channel is 10.24 $ps/\sqrt{2} =$



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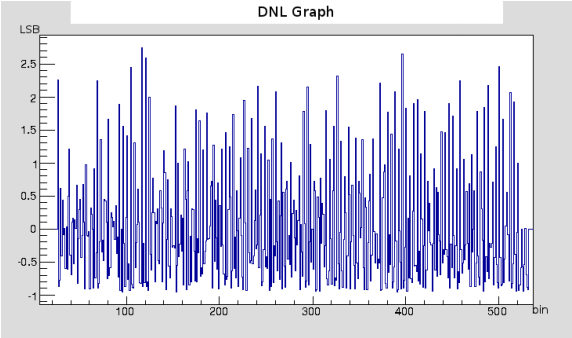


**Figure 8.** The differential non-linearity of the TDC.

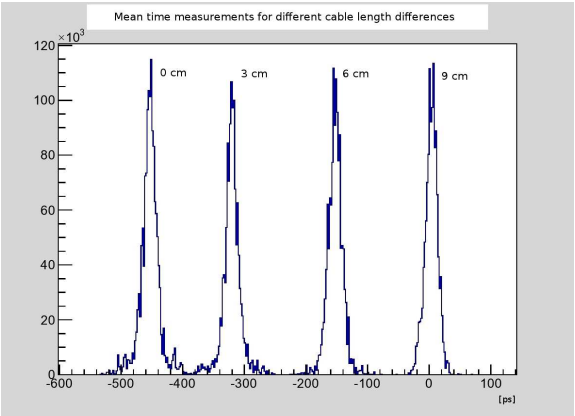


**Figure 9.** The shift of measured mean time with 3 cm cable length increase.

7.2 *ps* RMS. The resolution of the TDC with single and double transitions can be seen in figure 7.

The single shot precision of the designed TDC can be measured by the differential non-linearity (DNL) of the bins (figure 8). The DNL values of the bins are between 2,74 and -0,96 LSB. The high DNL values are caused by the UWBs, which are different than the other TDC implementations. Using multiple transitions in the delay line (multiple measurements) will decrease the effect of the UWBs on the DNL.

For the mean time measurements test different time intervals are measured with the double transition TDC. The time intervals are created by increasing the signal propagation delay to one of the channels using 3 cm longer cable for each measurement. For each 3 cm increase in the cable we observed a shift of 150 ps in the mean time (figure 9). This result is considered to be valid, as we know the propagation delay of a signal over a 1 m twisted pair cable is approximately 5 ns [16].

### 3.2 Stability

In order to test the stability of the resolution of the TDC and the mean time measurement we collected data for over 340 000 000 hit signals. The temperature is kept constant at ambient temperature during the measurements. Over the test time interval the peak-to-peak change in the resolution was 0.15 ps, whereas it was 2.5 ps in the measured mean time.



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## 4 Extra feature — trigger window

Many applications are interested in a time section rather than the whole time axis. Therefore, processing any hit signal and reading out would create suparfloug data. In order to reduce the data load and the junk data produced, a time section selective trigger window is implemented. The window is relative to the readout trigger signal and the window edges can be controlled with a slow control.

## 5 Summary & outlook

A 16 channel TDC is implemented in a Lattice ECP2M50E FPGA using tapped delay line method. The wave union launcher is used to reduce the average bin size and subdivide the large bins. Time resolution tests are done for 1 clock cycle (5 ns) and a maximum time resolution of 7.2 ps RMS is achieved. Average bin width of the TDC is $\sim$10 ps. 20 K LUTs are used in the design. The maximum latency and the dead time of the TDC is 45 ns and 30 ns respectively.

As for further optimisation of the TDC the system clock will be increased to higher frequencies in order to decrease the length of the delay line, thus reducing the resource consumption. The dead time of the TDC will also be reduced to adapt to multi-hit applications. Last but not least, Time-over-Threshold measurement ability will be integrated.

We see the future of the TDCs being implemented in general purpose FPGAs, as they are cost efficient, fast to develop and very flexible, and they can be adapted to many experiments and applications. Therefore, a new TDC module, TRB3, based on TDCs implemented in FPGAs is under development. The aim of this module is to reach a time resolution of less than 14 ps RMS and in total 256 TDC channels using 4 150 K LUT Lattice ECP3 FPGAs. TRB3, first to be used in real applications, will be used in several experiments, e.g. HADES, PANDA DIRC, CBM etc.

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