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TRB3: a 264 channel high precision TDC platform and its applications

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ABSTRACT: The TRB3 features four FPGA-based TDCs with < 20 ps RMS time precision between two channels and $256+4+4$ channels in total. One central FPGA provides flexible trigger functionality and GbE connectivity including powerful slow control. We present recent users' applications of this platform following the COME&KISS principle: successful test beamtimes at CERN (CBM), in Jülich and Mainz with an FPGA-based discriminator board (PaDiWa), a charge-to-width FEE board with high dynamic range, read-out of the n-XYTER ASIC and software for data unpacking and TDC calibration in ROOT. We conclude with an outlook on future developments.

KEYWORDS: Data acquisition circuits; Front-end electronics for detector readout; Digital electronic circuits

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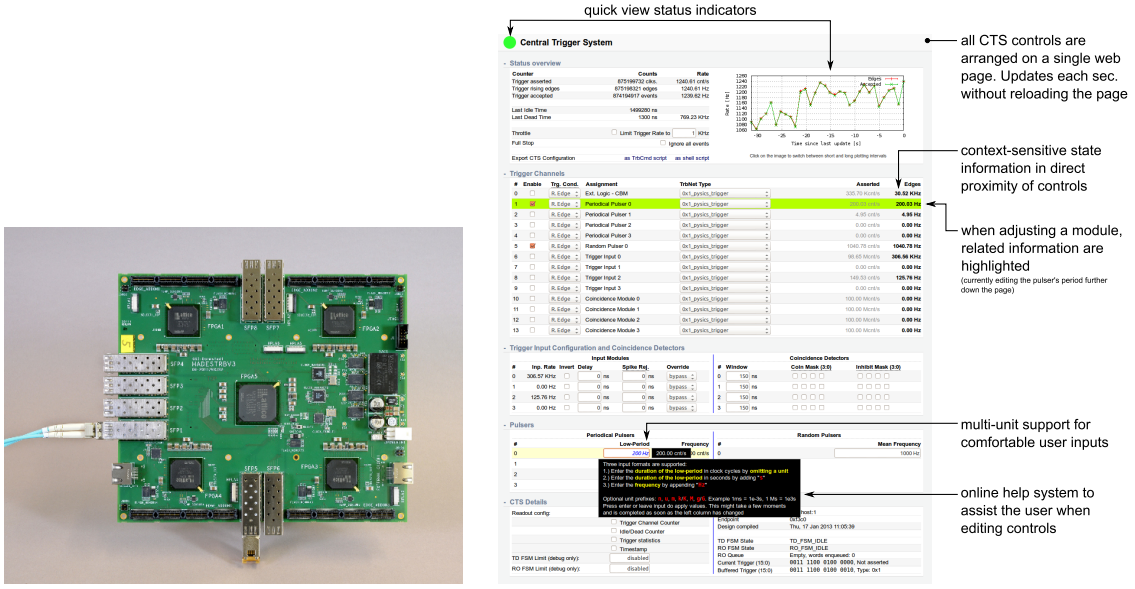
1 Introduction

The $4+1$ FPGA board "TRB3" (figure 1a) can serve various applications in experimental particle physics (and beyond) due to its general-purpose design. It uses Lattice ECP3-150EA FPGAs as complex commercial electronic components while realising the remaining auxiliary parts with simple standard components. Moreover, the board provides flexible connectivity by eight SFP ports and mezzanine extensions for every FPGA including a high pin-out for the peripheral FPGAs. We call this concept COME&KISS: COMplex COMmercial Elements & Keep It Small and Simple. This ensures a wide range of applications in data acquisition scenarios as well as a long-term maintainability of the platform.

Usually, in each of the four peripheral FPGAs a tapped delay line TDC is implemented with < 20 ps RMS time precision between two channels providing 64 channels plus one reference channel, see section 2. The TDCs are typically used for leading edge measurements or — by using the TDC channels in pairs — one can additionally extract the width of the digital pulse. The central FPGA serves as a flexible central trigger system and manages slow control and read-out of the peripheral FPGAs over a single gigabit Ethernet connection. Thus, only 48 V supply voltage and a desktop computer with controlling and event-building software are needed for a complete data acquisition system.

The project provides a comfortable, robust and modular software environment, ranging from low-level register access to the FPGA firmwares on the command line to high-level control via



(a) (b)

Figure 1. (a) The TRB3 without any mezzanine cards. (b) Screen shot showing the Central Trigger System web interface.

web2.0 technologies, see section 3. This is complemented by comprehensive specifications and documentations [1] provided by the large user base including the experiments HADES/CBM and PANDA at GSI in Darmstadt, Germany.

In section 4 existing front-ends and applications are presented. In sections 5 and 6 results of two test beamtimes are summarised in which the TRB3 platform has been successfully deployed.

2 Precise time digitisation in FPGAs

One key component of the TRB3 is the $64+1$ channel time-to-digital converter (TDC) implemented in the peripheral FPGAs of the TRB3 with a time precision down to 7.2 ps on a single channel. It "misuses" the carry chain lines and the logic blocks along the lines as delay elements in order to generate delay lines for fine time measurements. Each channel can save time information for up to 127 hits per trigger and can cope with burst hit rates of up to 66 MHz. Owing to its flexible design, an application-specific trade-off between number of channels, time precision and dead-time can be achieved for each front-end design. Implementation details can be found in [2] and first applications are described in [3].

3 Software environment

3.1 Central Trigger System and slow control

The TRB3 firmwares as part of the HADES experiment use the TrbNet [4] for asynchronous readout and busy-release scheme trigger distribution. Its configuration can be transparently controlled via command line tools including bindings to Perl. Furthermore, a modular Central Trigger System (CTS) was developed [5], which includes an user-friendly interface with web2.0 interactivity.

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It uses mouse-over effects to indicate connected configuration areas of modules. For example, in figure 1b, the pulser's period is currently edited, including a black box describing valid input values. The maximum accepted trigger rate of a TRB3 system is 700 kHz and owing to the modular design of the CTS, external trigger information can be easily integrated. Currently, modules for the experiments CBM [6] and A2@MAMI [7] decoding the trigger event numbers are available.

3.2 TDC delay line calibration and data stream unpacking

Since the length of the total propagation delay on each delay line of the TDC depends highly on the specific placing and routing of the elements inside the FPGA, a proper calibration of this fine-time is necessary. If one assumes that the read-out clock is uncorrelated to the measured signals, a *flat* fine-time histogram of all detected signals is expected. Any deviation must be due to different propagation delays, thus each element can be calibrated appropriately (for details see [2]). However, if the detector signal rate is not sufficient (leading to insufficient statistics in the fine-time histogram), artificial hits stemming from an uncorrelated signal source must be additionally generated and read-out. This technique is already available on the TRB3 and is currently under test.

Any user can profit from several common software developments for this platform concerning data acquisition and analysis. The well established HADES event-builder software [4] can be applied to acquire the data delivered by the front-ends and save them to HLD formatted files. The stored TDC data stream can be subsequently analysed offline by a "standalone" unpacker code [8], solely based on the ROOT software package. This includes well-tested methods for calibration of the delay lines.

The data acquisition and analysis framework DABC [9] and Go4 [10] provide an alternative way to readout and analyse data from the TRB3 [11]. DABC can be used like the standard HADAQ software for acquiring and storing data in HLD files. Additionally, DABC can deliver data at the same time to a running Go4 analysis via a TCP/IP socket connection. The main advantage of such technique is that many detector and electronics tests can be performed without writing files to disk, just showing results immediately on the Go4 display. Moreover, a standard web browser can be used for live monitoring of DABC and Go4.

Depending of experimental needs, a Go4-based analysis provides different methods of TDC channels calibration. Either the calibration is automatically recalculated when a specified number of hits (typically 10^5–10^6) has been accumulated in each channel. Alternatively, one can store calibration functions determined by separate measurements ("static approach") and use such calibration files for any following measurements. This is especially useful in case of low statistics.

4 Front-end electronics

4.1 PaDiWa: COME&KISS leading edge discriminator

The PaDiWa[1] is the first front-end board following the COME&KISS principle (figure 2). It uses the LVDS input buffers of a Lattice MachXO2 FPGA to realise a leading edge discriminator for 16 analogue input signals. Besides that, few standard components like the MMIC BGA2802 (20 dB

[1] Acronym for PANDA, DIRC, WASA.

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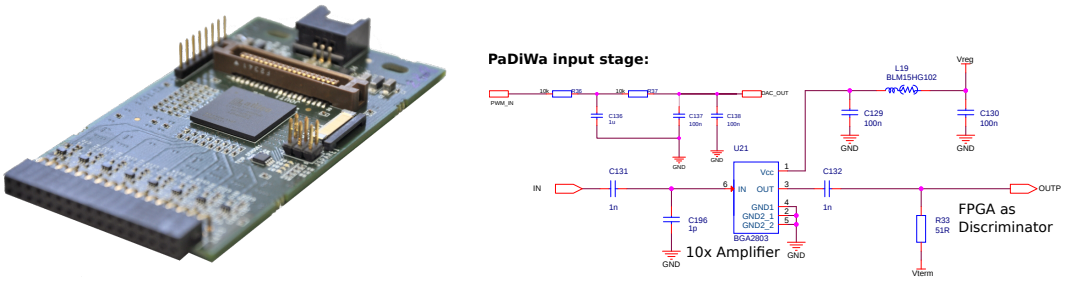
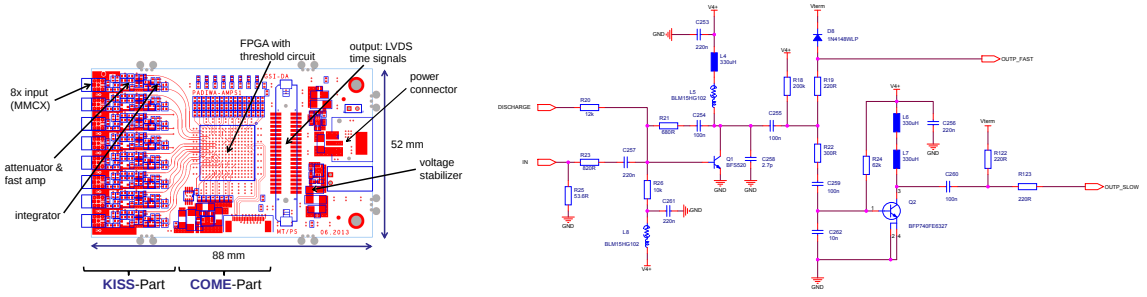


(a) (b)

Figure 2. (a) The PaDiWa leading edge discriminator front-end. Other versions with different analogue connectors are available. (b) The schematic of one channel showing the KISS part (FPGA excluded).



(a) (b)

Figure 3. The Charge-to-Width front-end for HADES ECAL. (a) The layout again illustrating the COME&KISS principle. (b) The corresponding schematic of one channel (excluding the FPGA).

wide-band amplifiers) and RC low-pass filters are used to generate the threshold voltages via pulse-width modulation. Using test pulses with an amplitude of 500 μV and a length of 6 ns, a time precision of the full system including the TRB3 of 23 ps was measured [3]. This front-end has been successfully used in beamtimes, see sections 5 and 6.

4.2 Charge-to-width front-end for HADES ECAL

The charge information of a pulse extracted from the time over threshold measurement is usually not precise enough for calorimeters. Thus, the leading edge measurement can be complemented by a modified Wilkinson ADC circuit, which encodes the charge in the width of the digital pulse delivered to the TDC. A proof-of-concept board was already successfully tested and a version with an improved dynamic range is currently designed for the HADES ECAL detector (figure 3). It is based on the experience with the PaDiWa board and provides 8 input channels (using in total 32 FPGA TDC channels for two leading edges and two trailing edges for each input channel) with a charge precision of 0.2 % and a high dynamic range of 250. The board is currently in assembly.

4.3 n-XYTER ASIC for HADES pion tracker

The TRB3 can also be used as an infrastructure to read out specialised integrated solutions using the peripheral FPGAs, for example to provide a timing reference, transport the acquired data to the event-builder and configuration of the attached ASIC via slow control. This was realised for

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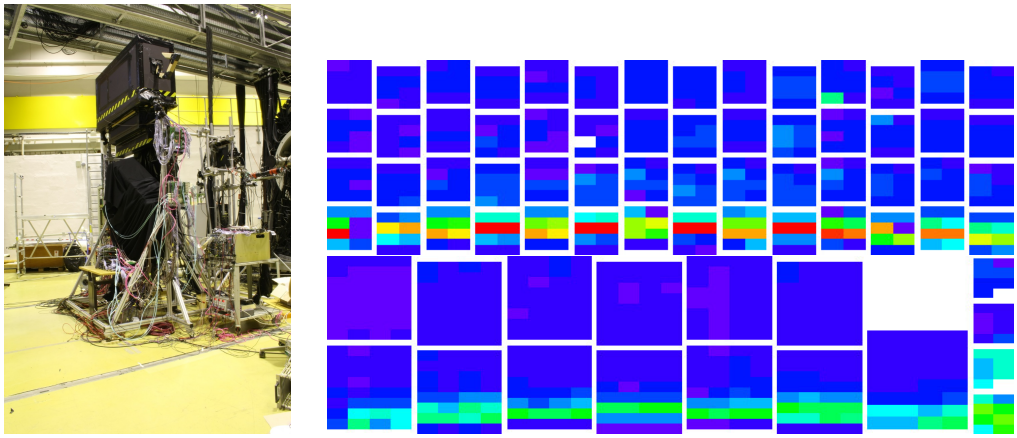

(a) (b)

Figure 4. Results of the test beamtime in Jülich: (a) Picture of the test setup. (b) Hit patterns of the Cherenkov rings.

the n-XYTER ASIC [12, 13], which provides the digital timestamp and the analogue pulse height of self-triggered 128 channels. In this case, the integration of the read-out and slow control (e. g. trigger windows) on the peripheral FPGA was easily achieved due to the well-documented VHDL interfaces of the TRB3 platform. The peripheral FPGA also reads out the ADC for the digitisation of the pulse height information.

5 Jülich test beamtime 2012

In order to prove the concept of a DIRC detector made of acrylic glass and to test and debug the electronics envisaged for the PANDA DIRC detectors under experimental conditions, a prototype setup was placed in Jülich behind the TOF experiment (figure 4) in October 2012. Here, protons with a momentum of 2.95 GeV and a rate of 10^7 Hz were scattered at a target and detected in two different DIRC detectors. Additionally, different multi-anode PMTs were tested. The PaDiWa single photon detection efficiencies for MaPMTs and MCPs equal to those of standard NIM based discriminators and amplifiers used in previous tests. In total, 10 TRB3s with PaDiWa front-ends were used providing 2400 channels, which was the largest system of TRB3s used in a test beamtime so far. This test experiment showed the need of an easy-to-handle and economical DAQ platform such as the TRB3.

6 Mainz test beamtime 2013

This most recent test experiment, for the development of a Barrel DIRC detector for PANDA (figure 5), took place in July 2013 at the MAMI-B microtron in Mainz (electron accelerator) with a beam energy of 855 MeV. A Cherenkov counter prototype using the DIRC principle was placed in the beam line. The prototype comprises a highly-polished fused silica bar with a lens attached, an oil-filled expansion volume and a photon detector matrix of 6 64-channel MCP-PMTs, which were read out by the TRB3 system. In total, 4 TRB3s with TDC implementations were used with

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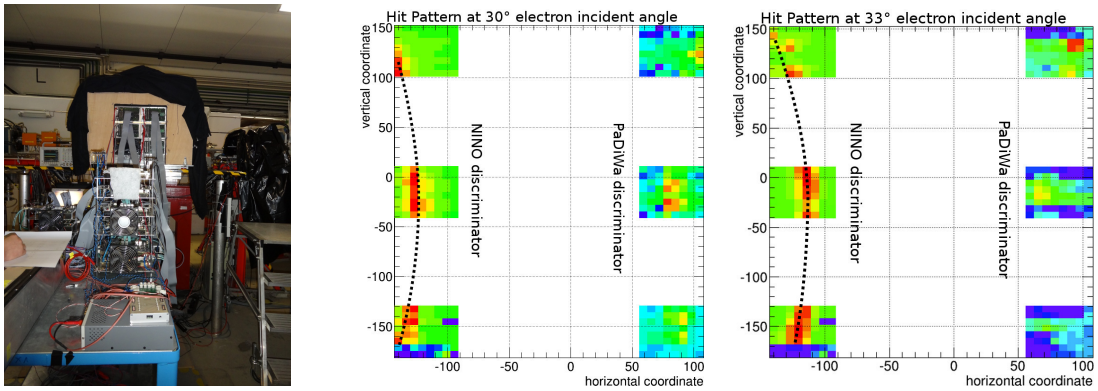

(a) (b)

Figure 5. Results of the test beamtime in Mainz 2013: (a) Picture of the test setup with the tower of 4 TRB3s. (b) Hit patterns at different incident angles and with different discriminator boards. The Cherenkov rings (black dotted lines) are clearly visible for the NINO discriminator and move as expected while changing the incident angle.

two different discriminator front-ends: the PaDiWa and the NINO ASIC. The beam current was set to achieve a trigger rate of approximately 6 kHz. The results show a worse Cherenkov photon detection for PaDiWa with respect to the NINO ASIC, as seen in the hit patterns, which is probably caused by differences in the amplification stage (the gain of the latter is about 10 times larger). However, the TRB3 provided a stable platform for a successful test beamtime.

7 Outlook and future developments

Finally, we present some planned or ongoing extensions of the platform: the detection of leading and trailing edge in a single TDC channel, which doubles the number of channels per board for timestamp and width measurements. This feature is highly desired for the described charge-to-width front-end. The dependency of the precision with the temperature is discussed in [14]. The temperature independency of the PaDiWa thresholds and of the TDC calibration is currently investigated. There are also several further front-end developments: integration of the MuPix ASIC for the PANDA luminosity detector and the SPADIC ASIC for a TPC in Mainz. A ~ 50 channel 10 bit 65 MSPS ADC AddOn (4 can be put in one TRB3) is in the layout phase. For the PANDA Straw Tube Tracker the development of an ADC inside FPGA is followed. Test measurements show that an ADC with 8 bits resolution and > 50 MSPS is possible. Since both ASICs use the CBMnet protocol, an implementation of CBMnet on the TRB3 was started. Furthermore, an extension of TrbNet with defined propagation delays of trigger signals for PANDA is being developed and tested.

Acknowledgments

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