HADES Data Acquisition Upgrade

Outline

- Motivation / Aim
- TRB V2
- List of Projects
  - RICH, MDC, TOF, RPC, Shower, CTU / MU
  - Milestones / Manpower involved / schedule / risk
- Summary

Motivation / Aim

	max. LVL1	max. LVL2	LVL2 Trigger downscaling factor
pulser rate	17kHz	4-5kHz	10-20
in beam	8kHz	1 kHz	10-20

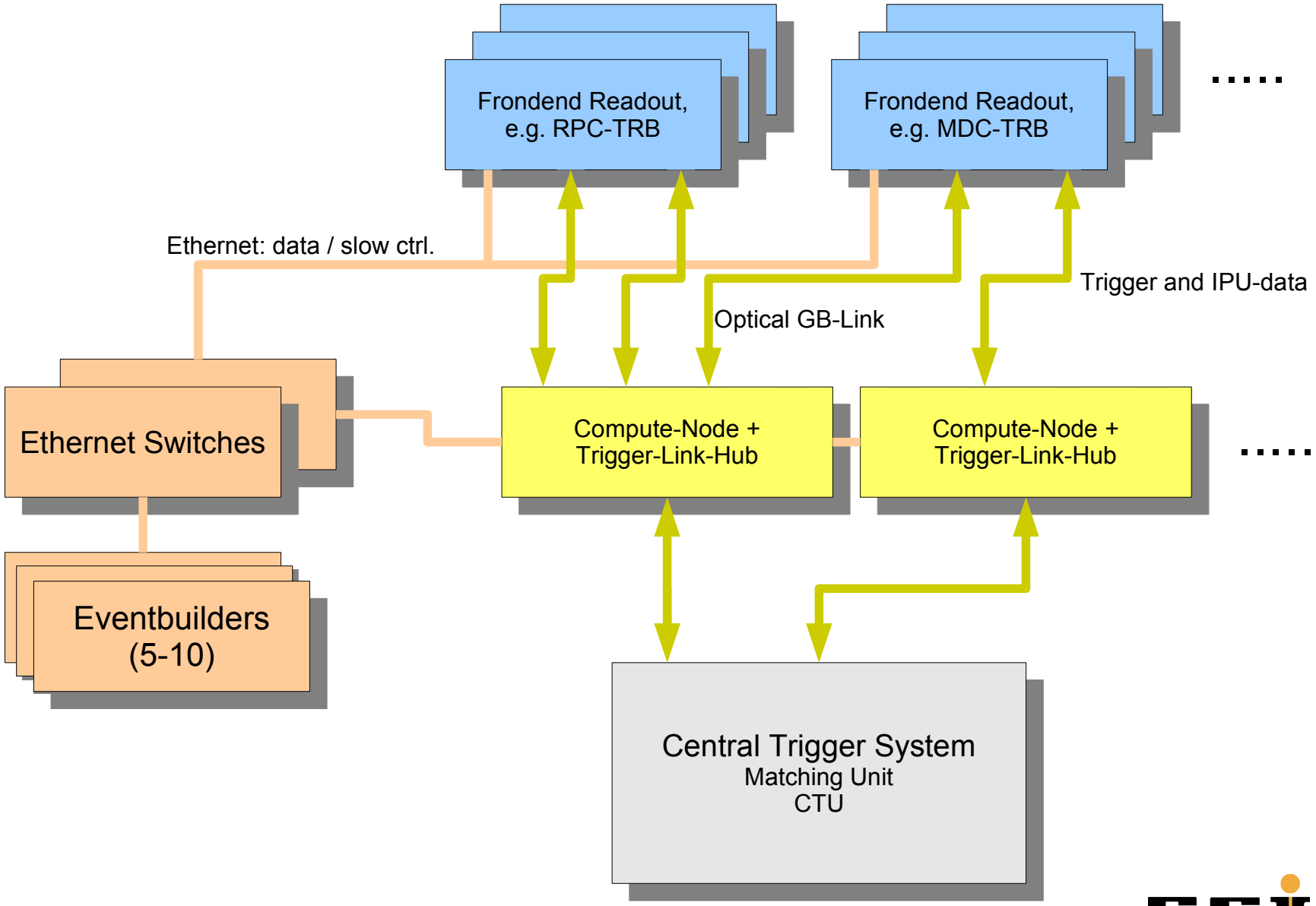
	max. LVL1	max. LVL2	LVL2 Trigger downscaling factor
in beam	3-4kHz	1-2 kHz	around 3

- Main Problem:
  - The limitation of the LVL1/LVL2 rate
- Measures:
  - Increase LVL1/LVL2-rate capability
  - Improve on the LVL2 trigger-algorithm (W. Kuehn)

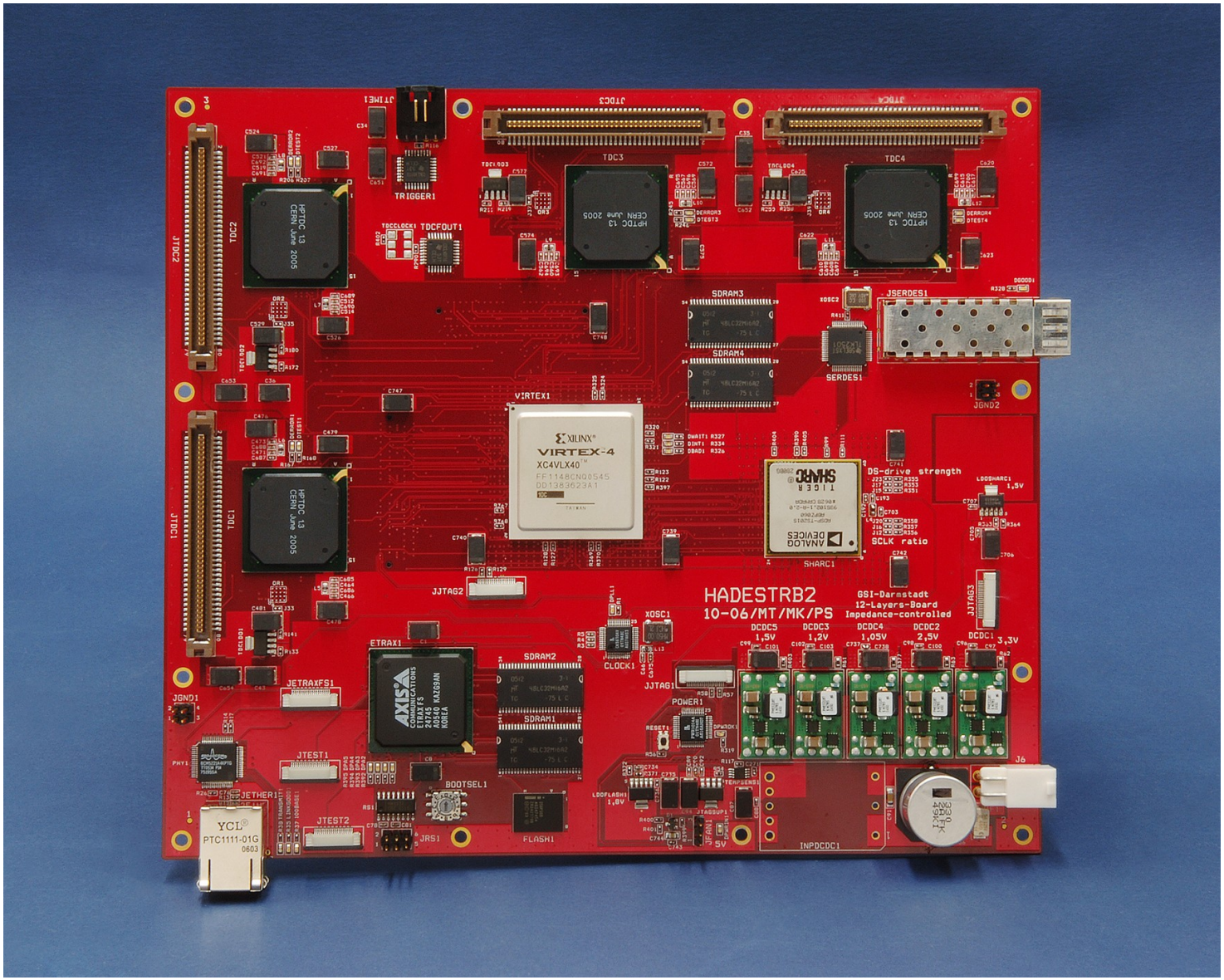
Objective: 20 kHz primary data rate to ensure measuring rare decays in heavy systems

Risk: Not ready till mid. 2008 (6 months comm.)

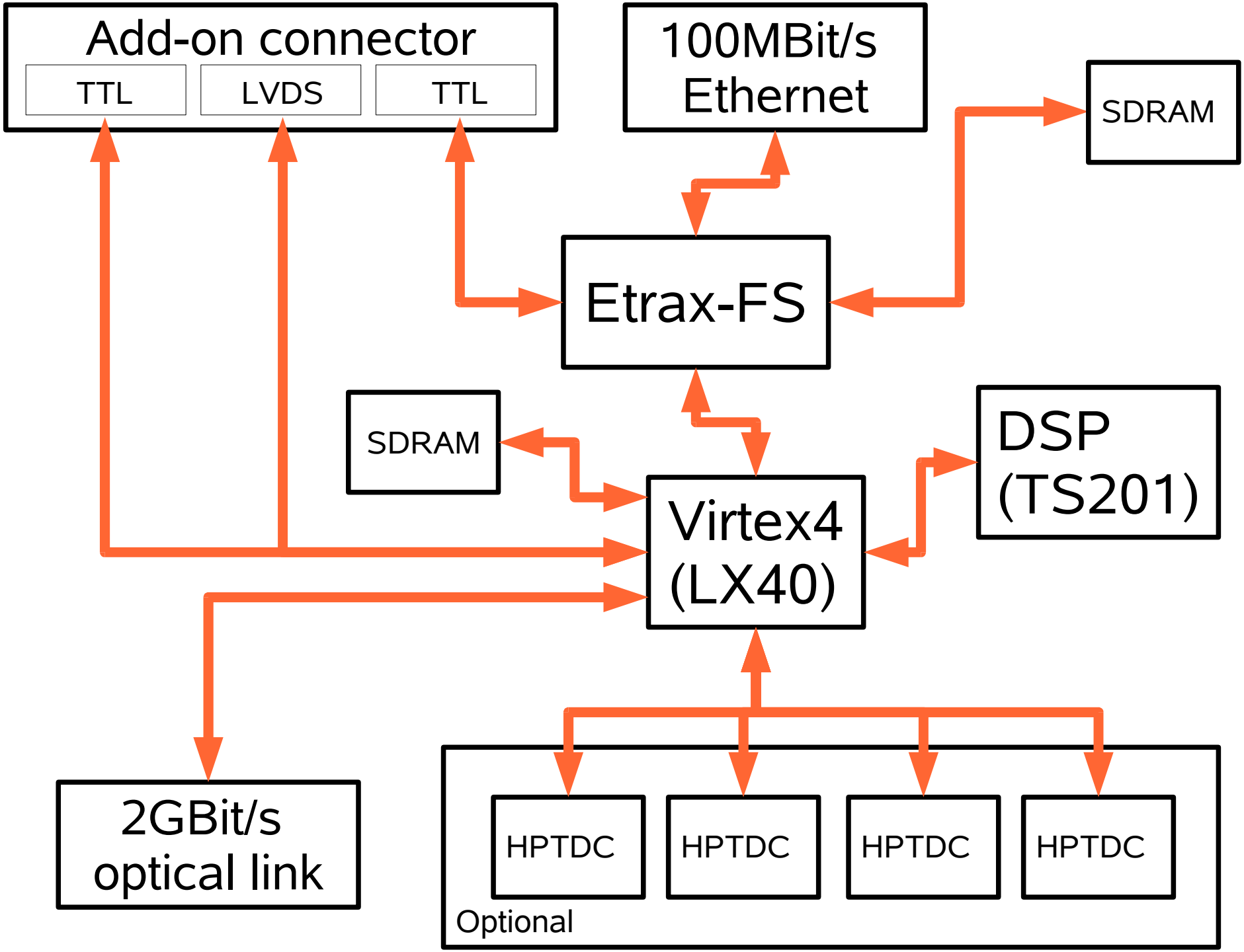
“new” DAQ Architecture



TRBv2



- successor of TRBv1, which is used in the experiment
- larger FPGA
- faster CPU
- Tiger-Sharc DSP
- 2 GBit/s optical link for trigger and data
- TRBv1 functionality given


Add-on connector
TTL
LVDS
TTL
100MBit/s Ethernet
SDRAM
Etrax-FS
SDRAM
DSP (TS201)
Virtex4 (LX40)
2GBit/s optical link
HPTDC
HPTDC
HPTDC
HPTDC
Optional

TRB V2, why? consequences?

Advantages to use TRB V2 as DAQ-FEE-system

- Use one common platform for all subsystems!
  - Concentrate manpower on one main project
    - data transport issues are solved only once => more stable
    - easier to debug, distributed knowledge, less maintenance, lower cost
- Interesting also for other experiments: CBM, Panda, PET-readout

Nothing is for free, general solution needs...

- more time until deployment (more complex)
- new trigger / IPU-bus over optical links (IP-core)
- many people involved, more communication, better documentation needed, ... => **advantage**

TRBv2 connectivity: Add-on Boards

- 15 GBit/s connector + many multipurpose I/Os
- Add-on-boards provide the connectivity to the other detectors / new applications / other experiments

TRB V2 can be our common DAQ-FEE-platform

- RPC, Forward Wall, Beam-detectors, TOF, PET
  - With HPTDC
- MDC, RICH, Shower
  - Without HPTDC

Status / Manpower / Schedule / Risk TRBv2

Status:

- TRBv2 ready to be used for RPC, Forward-Wall, Beam-Detectors, TOF => TRBv1 functionality

=> **low risk!**

Manpower:

- Current main developers:
  - TRBv2: Marek Pałka, Radek Trębacz
  - TRB Net: Ingo Fröhlich, Jan Michel
    - Involved: Marcin Kajetanowicz , Krzysztof Korcyl + others

Missing things / Schedule:

- DSP: Marek: 2 month, DMA: Radek: 2 months
- Run-Control: Radek, Marek, Sergey: 3 months
- TRB-Net: Ingo & Jan Michel, 6 months

Status / Manpower / Schedule / Risk TRB HUB

Purpose:

- distribute LVL1/2 triggers, IPU-Link, slow-control
- TRBv2 add-on: FPGA with 13 optical links

Status:

- Schematics finished, Layout finished on Monday

Schedule:

- PCB: June
- Programming of FPGA:
  - Commissioning: Marcin, Marek: 1 month
  - TRB HUB VHDL-code: Ingo, Jan Michel: 3 months (after TRB-Net itself is finished)

Risk: low

Status / Manpower / Schedule / Risk TOF-detector-FEE

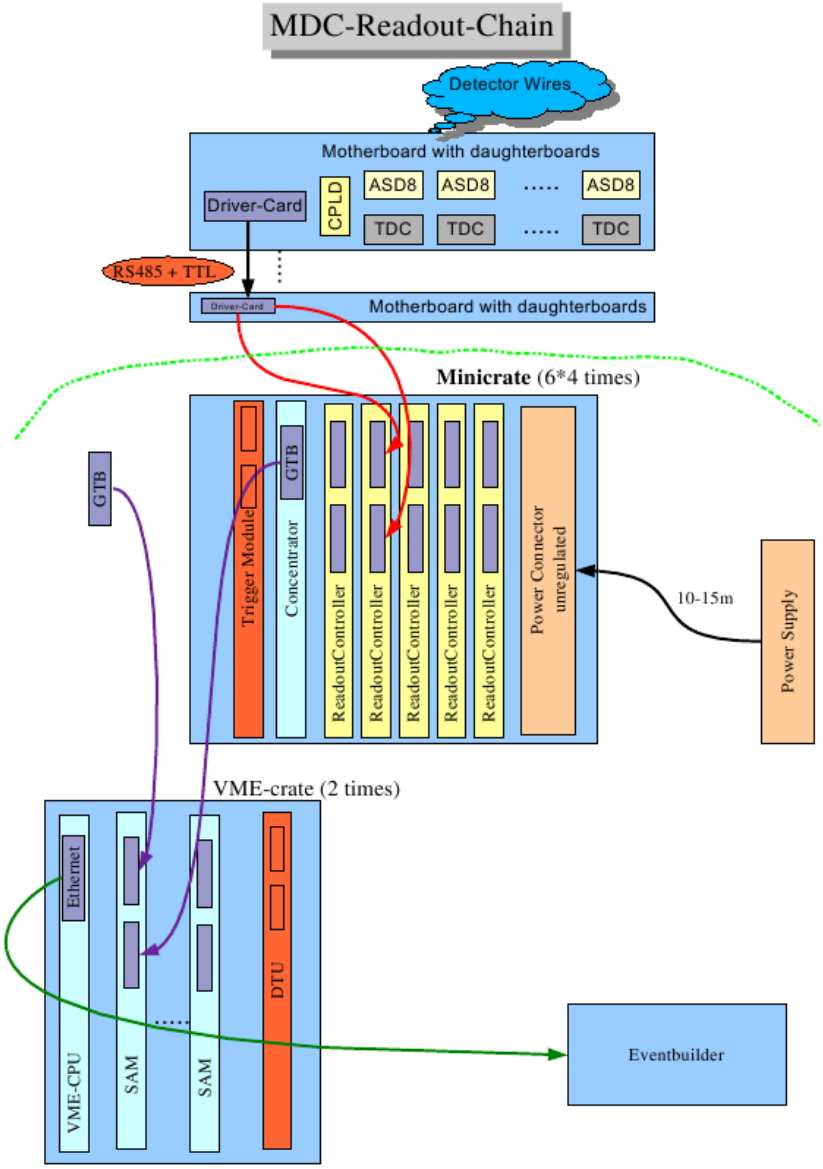
- FEE with Q2W (ToT) logic needed for TRB
  - get rid of CAMAC etc.
  - the rest is identical to RPC
- Evgueni Usenko (INR Moscow, Fedor Guber's group)
  - Analogue expert, one of the designers of the NINO ASIC
- Concept:
  - TRB-add-on with PM-amplifier and Q2W logic for 128 channels, based on NINO

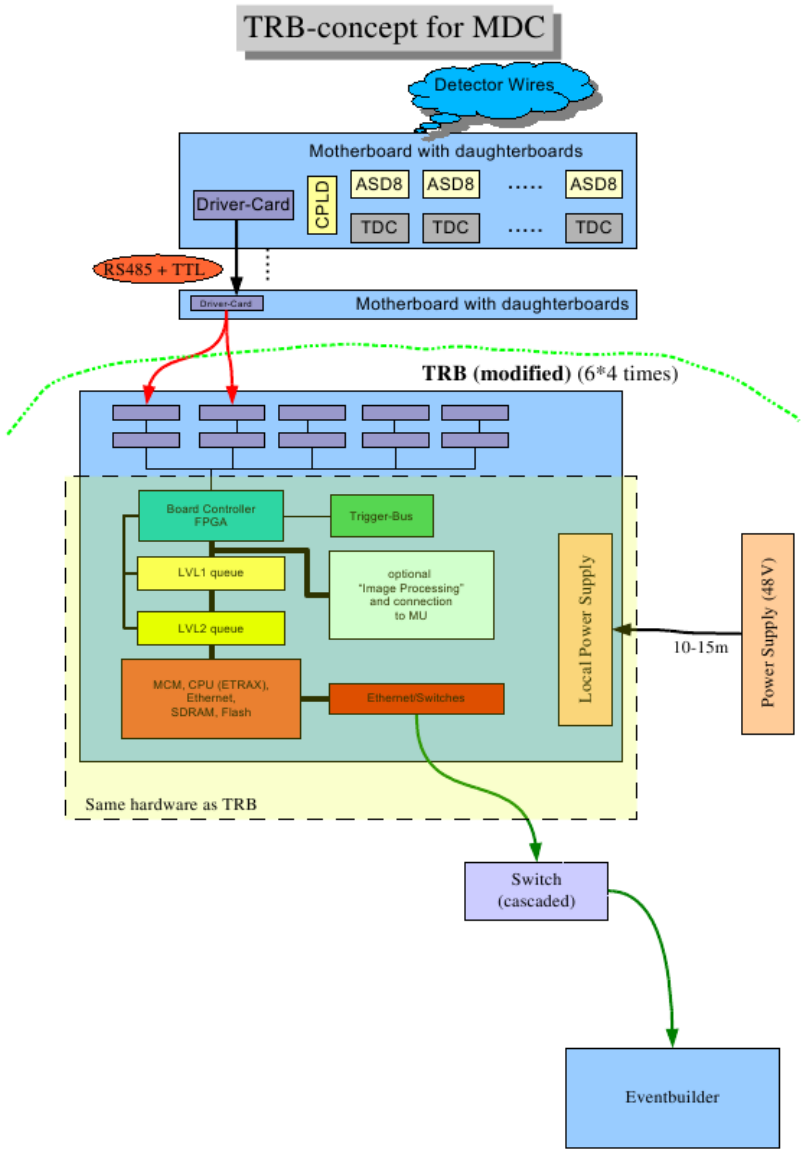
Schedule:

- detailed schedule worked out
  - first PCB: July
  - with second version: decision if solution is fitting our needs: December 2007

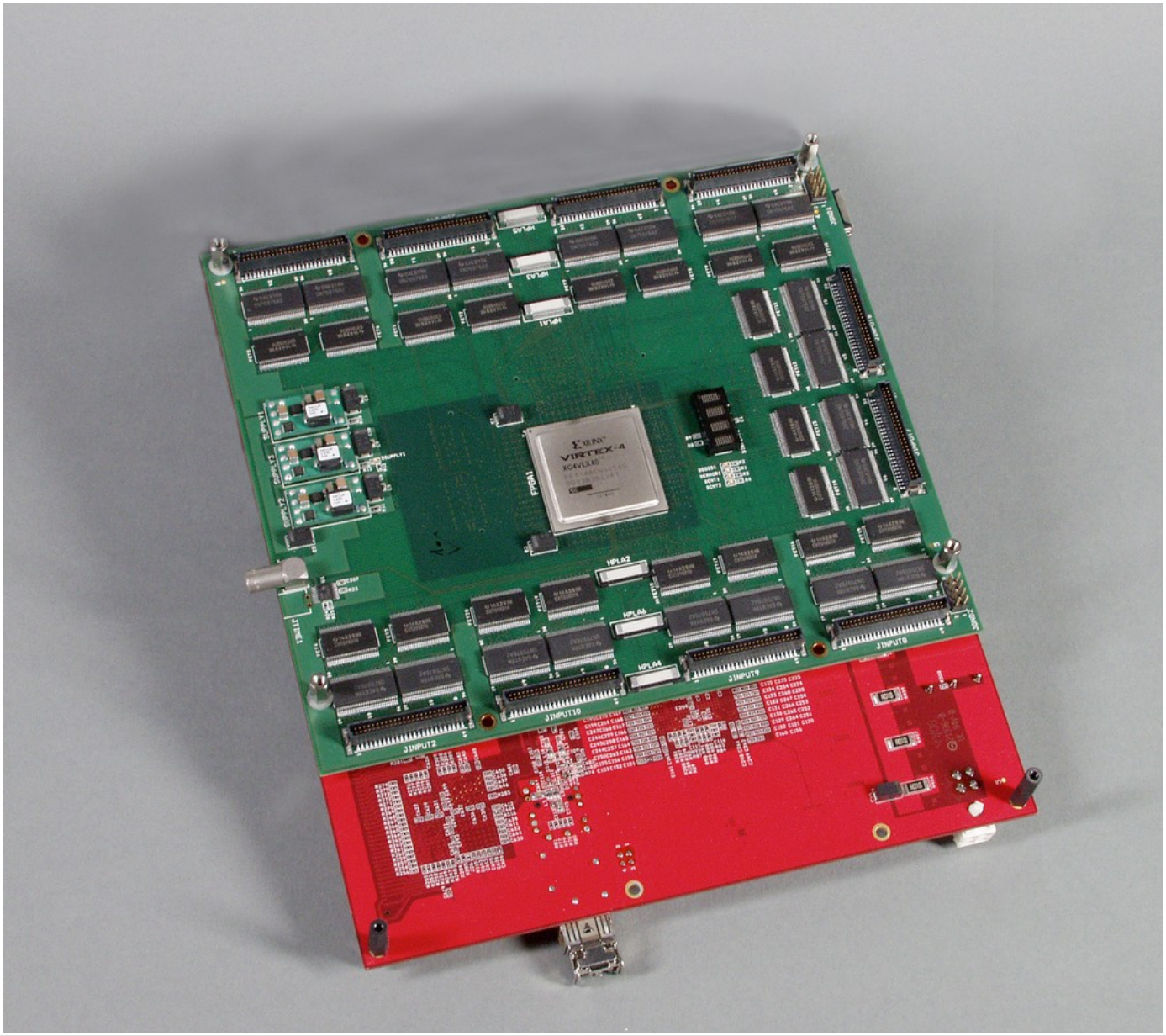
Risk: medium; technically: low (fallback: Forward-Wall electronics)

MDC Setup: current and new (with TRB)





Status / Manpower / Schedule / Risk
TRB-MDC-Add-on



- Readout of MDC-Motherboards
- VHDL code written and simulated
- Token-chain working
- Manpower: Attilio Tarantola
- Readout: same as for HPTDC
- Schedule: 3 months
- Risk: very low

Status / Manpower / Schedule / Risk TRB-MDC-Driver-cards

- Strong demand for new MDC-driver cards:
  - cables! cables! cables!
    - crosstalk and "ringing" of the MDC-FEE due to copper cables squeezed between motherboards
    - heat dissipation
    - missing possibility to re-program the motherboard-CPLD
    - hassle with the chains of motherboards
- Project: **New MDC-driver card**
  - Optical Transmission via Polymere Optical Fibre (POF)
  - FPGA (SERDES) on driver card for data-transmission
  - Option: Time-Signal via optical cable
  - **Result:** pure optical connection with small cables!

Status / Manpower / Schedule / Risk TRB-MDC-Driver-cards II

Status:

- Design idea, schematics done
- components ordered

Schedule:

- PCB finished in June
- **Research Project!**

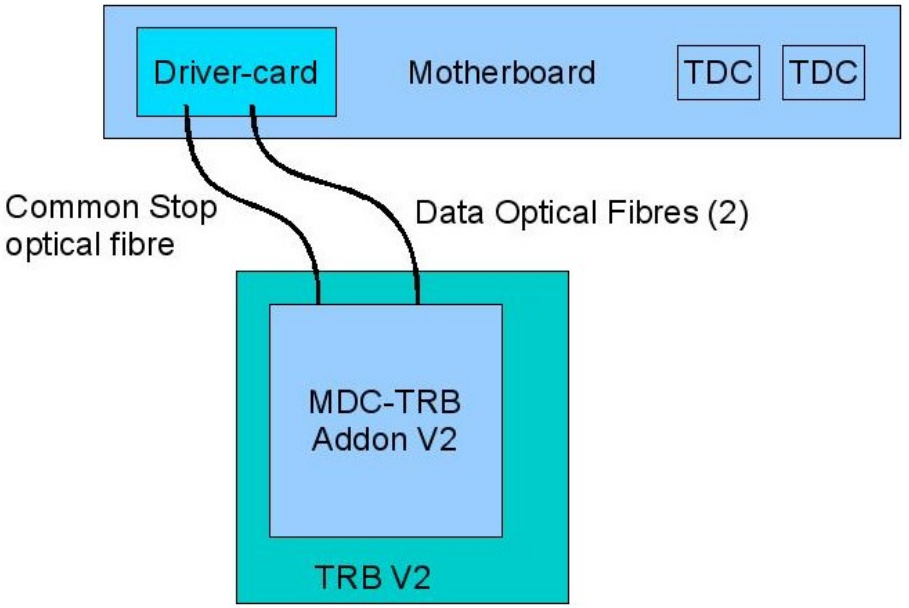
Manpower:

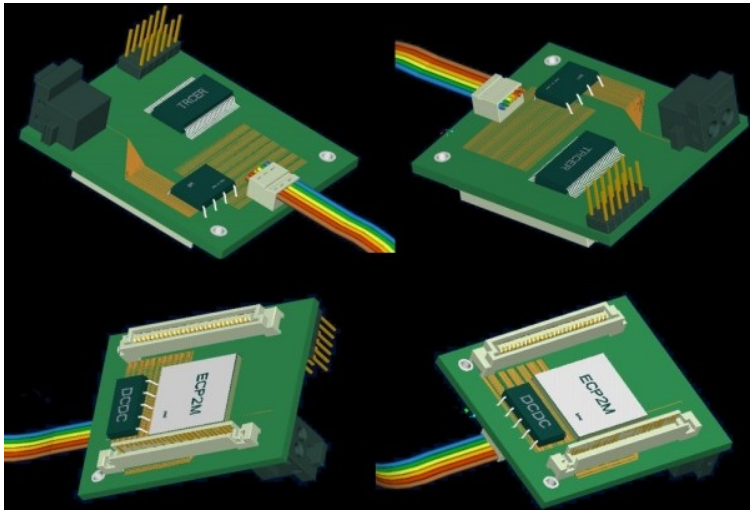
- Yanyu Wang

Risk:

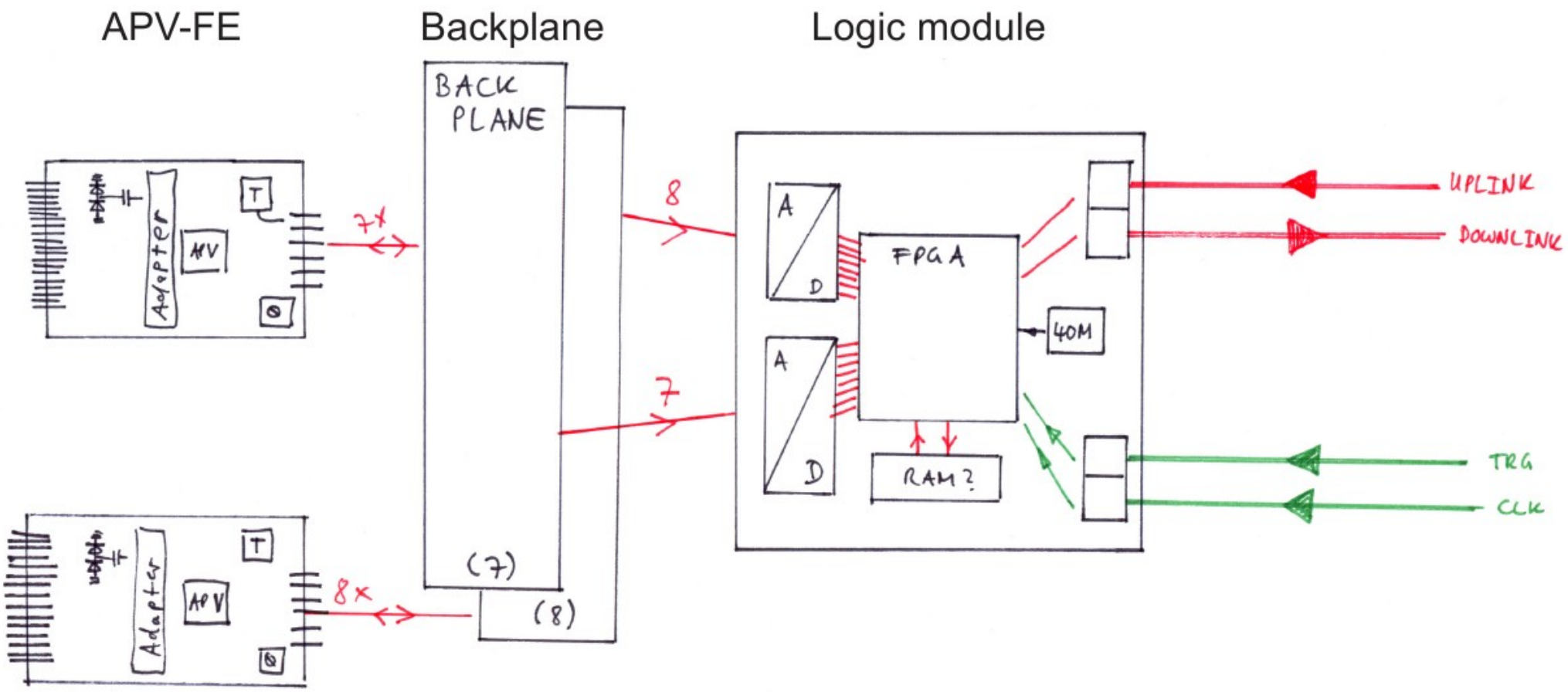
- High, due to lack of manpower at HADES

TRB-add-on can be used for RICH-DAQ!





Modular concept for the RICH readout

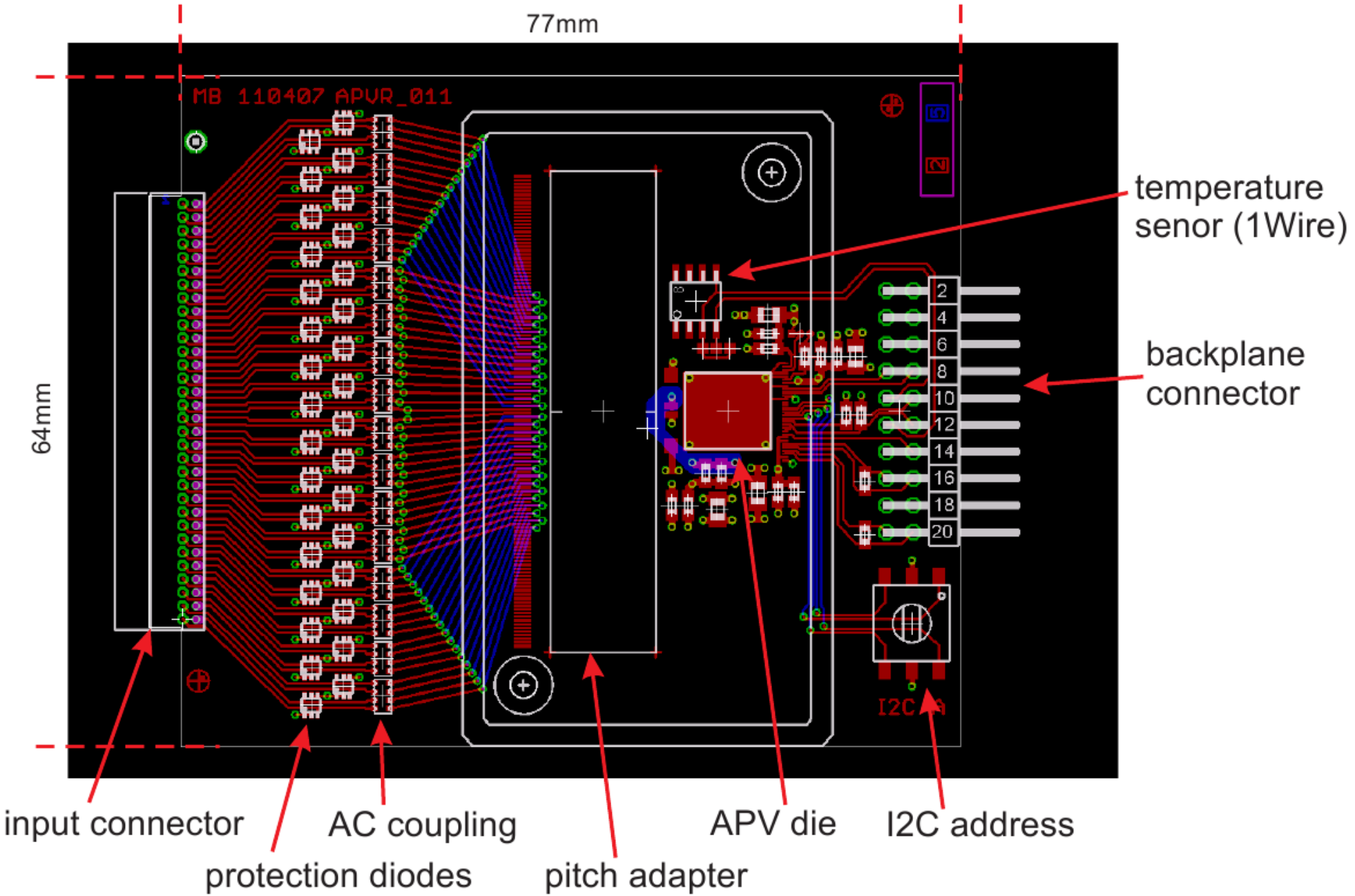


- 64 channels (AC coupled)
- diode input protection
- analogue buffer (30 evts)
- low power (vacuum)
- slow control (I2C)
- temperature sensor (1Wire)

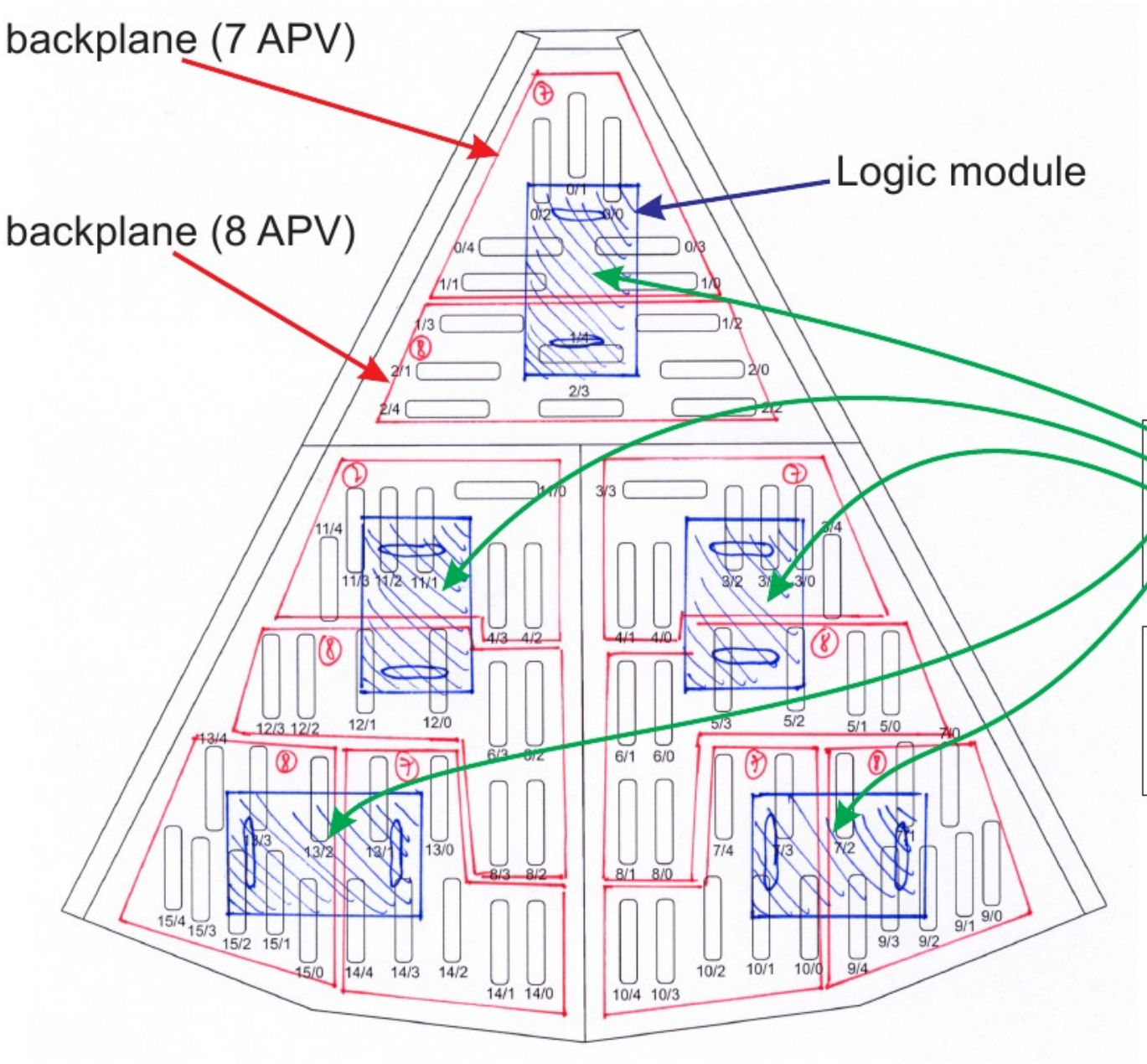
- passive backplane
- low power distribution
- CLK fanout
- TRG fanout
- mechanical stability
- 7/8 APVs
- 10 different PCB shapes

- two ADC (8-fold, 40MHz, 12bit)
- one large FPGA (Lattice SC)
- local 40MHz clock
- CLK / TRG in(optical)
- endpoint of trigger bus
- all signal handling for 15 APVs
- slow control (I2C, 1Wire)

New APV-FE design (second iteration)

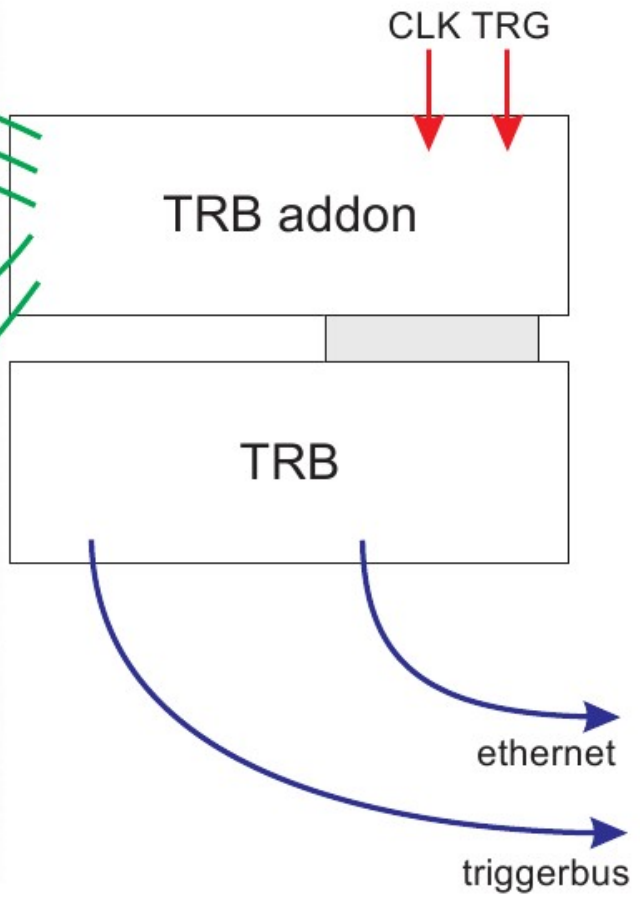


New sector layout



One sector:

- 5x Backplane (8 APV)
- 5x Backplane (7 APV)
- 5x LogicModule
- 75x APV Frontends
- 5x Up/Downlink TRB
- 5x CLK/TRG Uplink



Status / Manpower / Schedule / Risk RICH-DAQ-upgrade

Status:

- Concept, design ideas, APV25 available
- First prototype of APV25 is working for R3B

Schedule:

- reasonable time-schedule discussed: it seems possible but can not be promised from Munich

Manpower:

- Michael Böhmer (+ 2 more persons in the future)

Risk:

High (manpower)

Not so much research but a lot of work...

Status / Manpower / Schedule / Risk Shower-DAQ-upgrade

Concept:

- TRBv2-Add-on replaces „Readout-Boards“ + VME-readout + Fanout-board

Status:

- Concept finished, schematics 80%

Schedule:

- PCB in July, working prototype in October

Manpower:

- Marcin Kajetanowicz

Risk:

Low, fallback: current system (shower is our fastest system!)

More Projects

DAQ-software:

- Parallel Eventbuilding
- Run-Control (control 100 boards instead of 10)
- Sergey Yurevich: full-time

Slow-Control:

- EPICS infrastructure: EE-department (P. Zumbruch)
- Monitoring of states / performance / error-tolerance
- Thresholds and other settings / readings through TRB
  - RPC: Alex Gil
  - Others: not name

Backup-Solution

- If we will not have a LVL2 trigger for Au+Au we can expect (worst case):
  - 150 MBytes/s sustained rate (300 MBytes/s peak)
- This is very inconvenient:
  - 86 TBytes / week
  - expensive (8k€ for tapes/week)
  - Compression can save 30% (tested)
- DAQ and IT-department are able to do this
- Comparison:
  - Phenix is writing since 2004 350MBytes/s sustained to tape (600MBytes/s with compression).

Summary

- Large and demanding project!
- Many people involved
- progress: looks promising
- few parts with high risk
  – fallbacks are possible
- RICH-upgrade: crucial point
  – high risk but no fallback

- „Future-DAQ“ is happening **now** at HADES and really motivates the involved people

DAQ upgrade

Thank you for your attention!

RICH Realtime-Schedule

- Architechture discussion / component availability

  Finished: End of April 2007

- Prototype system: AFE-ADC-BP(1)-LM

  Schematics: 1. July

  PCB-design: 1. August

  Assembled boards: 1. September

  During production time: VHDL-code development

  Function / Performance Tests: 4 Month, til 1. Jan 2008

  During tests: new schematics

New PCB-designs: 1 month, til 1. Feb.

Production: 1 Month: 1. March

- "Final" Test-Setup (1 Sector in Munich) assembled: 1. April
- Final Tests on one sector: 1 month: 1. May
- June: Decision, if new RICH-FEE-DAQ-solution is what we want

If positive:

- Mass production for whole RICH-detector: 3 months: 1. September
- Mechanical replacement at GSI-RICH: 2 month: 1. November
- Commissioning: 3 month: til 1. Feb. 2009

TOF-FEE upgrade

- Architechture discussion / basic investigations Finished: 15.04.07
- Prototype system: Full featured TRBv2 Addon-board
  Schematics: finished <30.04 - 15.05.07>
  PCB-design: <duration 15.05 - 15.06.07, finish-date 15.06.07>
  Assembled boards: <duration PCB prod. 15.06 - 1.07.07, finish-date ass. board 15.07.07>
  During production time: VHDL-code development of the DAQ-group, (no comment)
  Function / Performance Tests: <duration 15.07 - 30.07.07, date>
  During tests: new schematics are prepared

- New PCB-designs: 1 month, < 1.08 - 30.08.07>
  Production: 2 Month: < 1.09 - 30.09.07> note: 1 Month
- "Final" Test-Setup assembled: < 1.10 - 15.10.07>
- Final Tests on one sector: < 15.10 - 15.11.07>

- Decision, if new TOF-FEE-DAQ-solution is what we want

If positive:
- Mass production for whole TOF-detector: 3 months: < 5.01 - 1.03.08>
- Mechanical replacement at HADES-TOF: < from 1.03.08>
  (this has to be done by the TOF-people!)
- Commissioning: 3 month: middle of 2008 year

TRB V2 features (additional to TRB V1)

- Multi Purpose Time to Digital DAQ-System with standard Ethernet data-transport
- 2 GBit/s optical link for online pattern-recognition data transfer and LVL1 and LVL2 trigger
- Large FPGA (Xilinx Virtex4 LX40) for online pattern-recognition, zero suppression, ...
- 3 times faster CPU
- DSP: Tiger-Sharc (600MHz, 128Bit) for TOF-algorithm
- 8 GBit/s bandwidth general purpose IOs for adaption to „any“ application (like digital or ADC readout)
- low cost (around 10€ / TDC channel)

Changes to the DAQ-Upgrade and Impact on FP6-HADES3

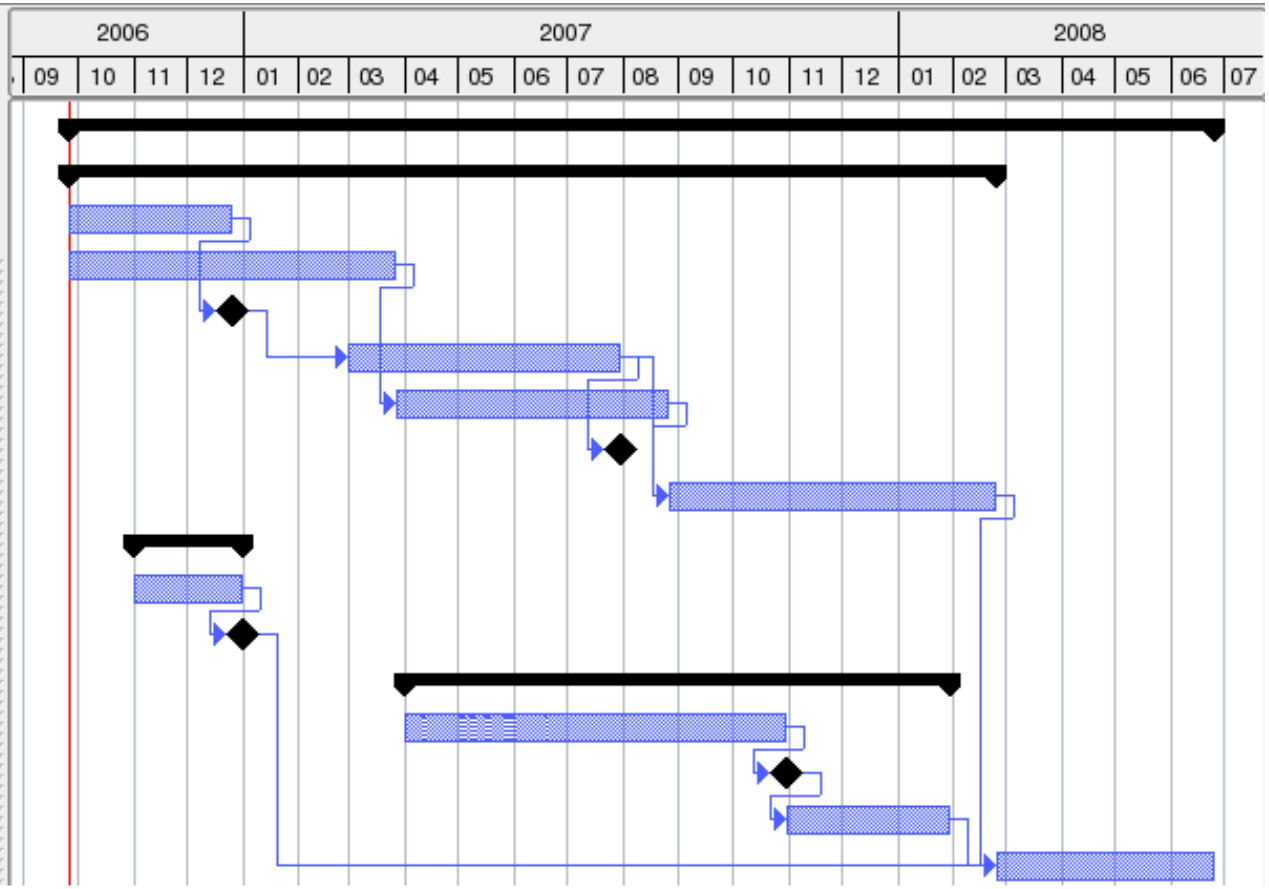
- One platform for DAQ of all subdetectors in upgrade
- results in new Trigger/IPU distribution concept
  – optical links, point to point connection, „hubs“
- possibility to use new VME-CPU (fast) for TOF-readout and IPU functionality (until TOF-FEE is changed to fit to the TRBV2)
- Matching Unit implemented in VME-CPU
- step by step exchange of hardware while ensuring succesfull production beamtimes (next Feb. 2007)

FP6-HADES3 consequences

- TOF and MU projects are delayed

Changes to the Gantt-Chart of the DAQ-Upgrade

Task	Duration
HADES3 Upgrade Project	21
TRB V2 as TOF-Readout	17
Design/Production TRBV2	3
IP-core: Trigger/IPU Links	6
Hardware TRBV2 available	0
Implementing readout functionality	5
TOF/RPC-IPU implementation	5
TRB2 without IPU functionality	0
TOF-readout/IPU integration	6
VME-CPU replacement	2
RICH-CPU replacement	2
RICH VME-CPU replacement finished	0
Matching Unit V2	10
Implementation of Algorithm	7
MU Algorithm implemented	0
MU integration	3
Full System Integration	4



Summary

- Deliverable **D10-1** (almost) fulfilled
- Synergy between RPC-Upgrade project and other upgrade projects (MDC, RICH) allow to use one common system for the DAQ-Upgrade
- New milestones and deliverables defined to reach the goal:
  – 20 kHz LVL1 primary data rate in heavy systems

Original Milestones

ID	Vorgangsname	Duration
1	**HADES 3 (DAQ)**	**540 dys**
2	**CPU upgrade**	**440 dys**
3	VME-CPU replacement	8 mons
4	*HAD-3-M2*	*0 dys*
5	Database interfaces	6 mons
6	Eventbuilder	4 mons
7	*HAD3-M5*	0 dys
8	Integration	4 mons
9	**TOF readout**	**480 dys**
10	Read-out board	9 mons
11	*HAD-3-M3*	0 dys
12	IPU implementation	6 mons
13	*HAD-3-M4*	0 dys
14	Integration	9 mons
15	**Matching unit upgrade**	**440 dys**
16	Implementation BIOS	6 mons
17	*HAD-3-M1*	0 dys
18	Implementation of algorithm	10 mons
19	*HAD-3-M6*	0 dys
20	Integration	6 mons
21	Full system commissioning	3 mons