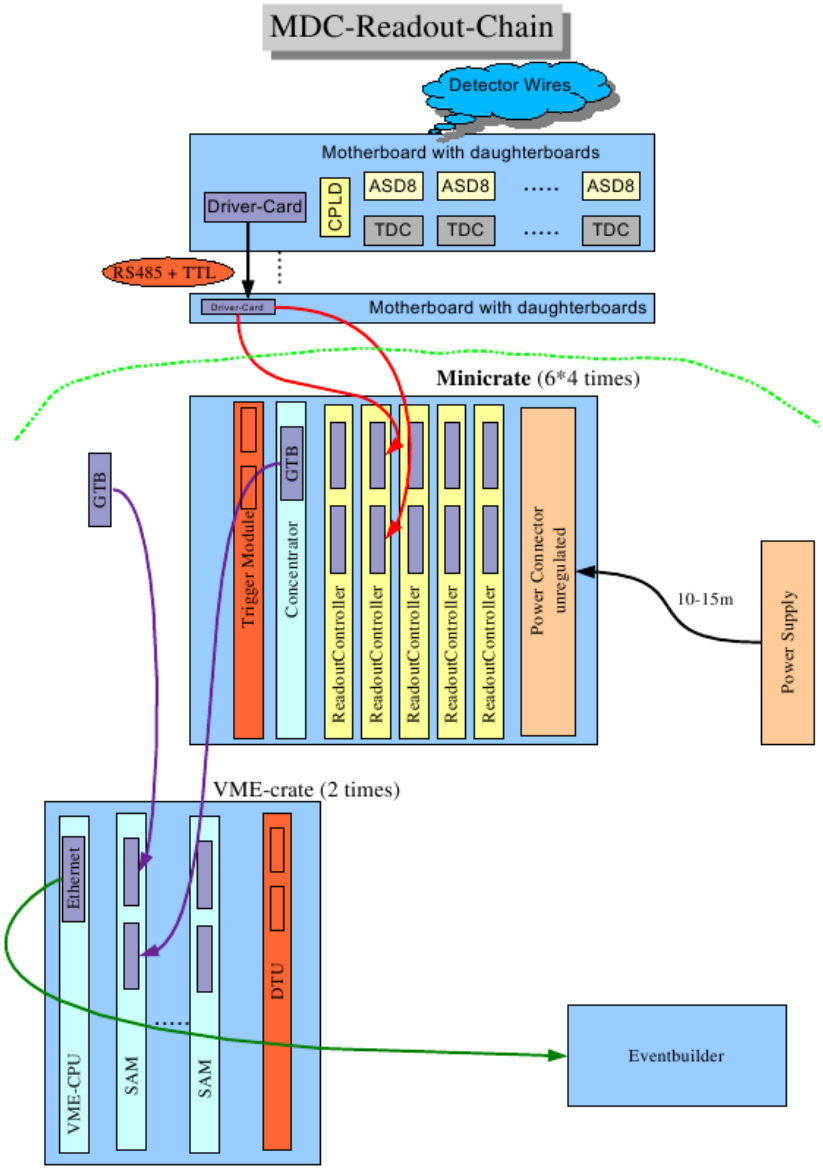
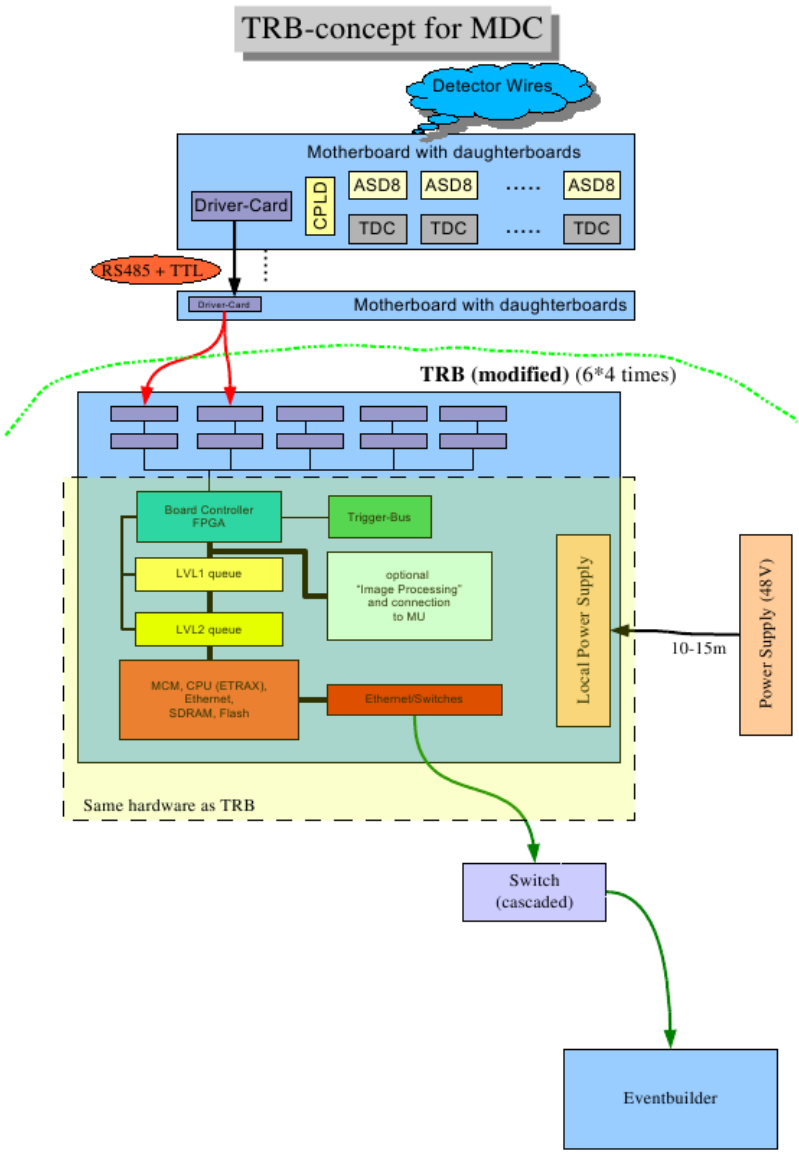
MDC Optical Endpoint

Outline

- Motivation / Aim
  - Hardware Details, Sharing Experiences and no Politics!
- Task
  - Architecture of MDC-System
- Solution
  - Optical Data Transport: MDC-Endpoint
  - Timing Fanout and Power-Supply
- No Summary
- Discussion

Task: HADES MDC Upgrade
Existing and New Setup

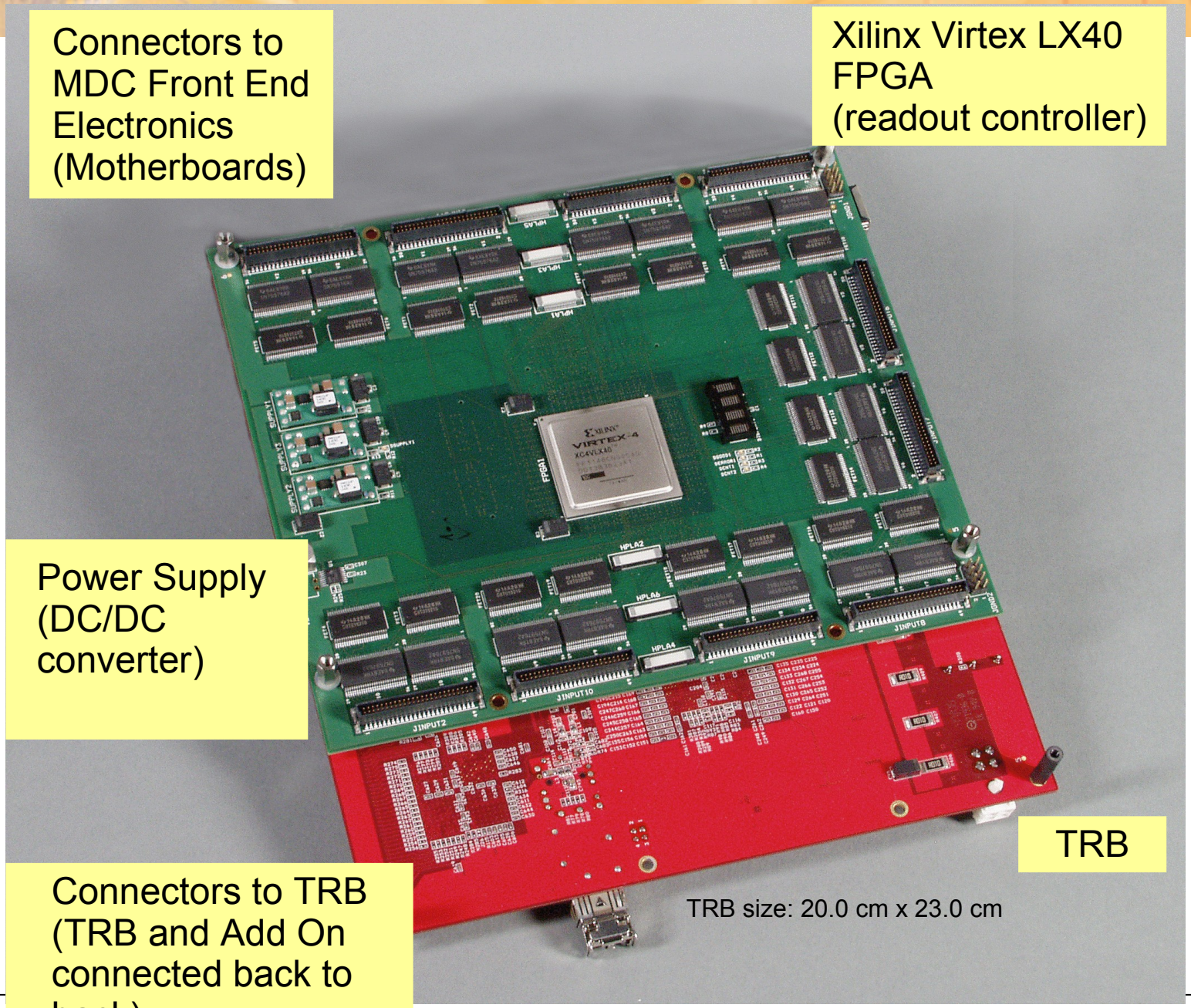




Solution I

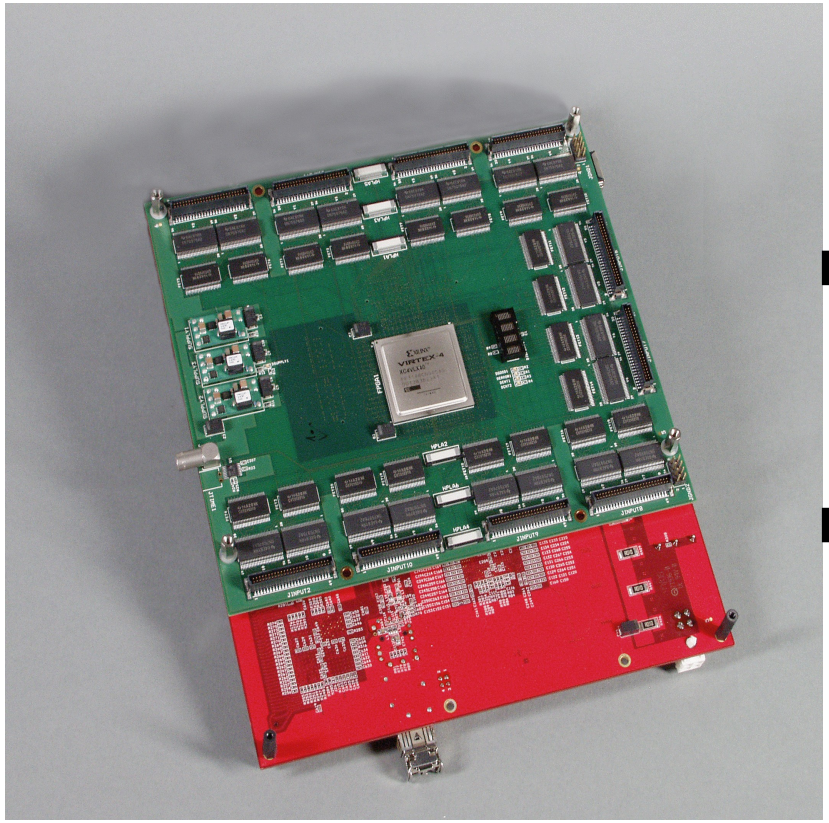
- Asking many people for help! (I)
  - Jan Hoffmann, Attilio Tarantola, Wolfgang Ott, 王彦瑜 (Yanyu Wang), Marek Pałka, Burkhard Kolb, Jörn Wüstenfeld
- Divide problem into smaller parts
  - Readout (II)
  - Data transfer (III)
  - Time Distribution and Power-Supply (IV)
    - Details will be skipped

Solution II: MDC Readout

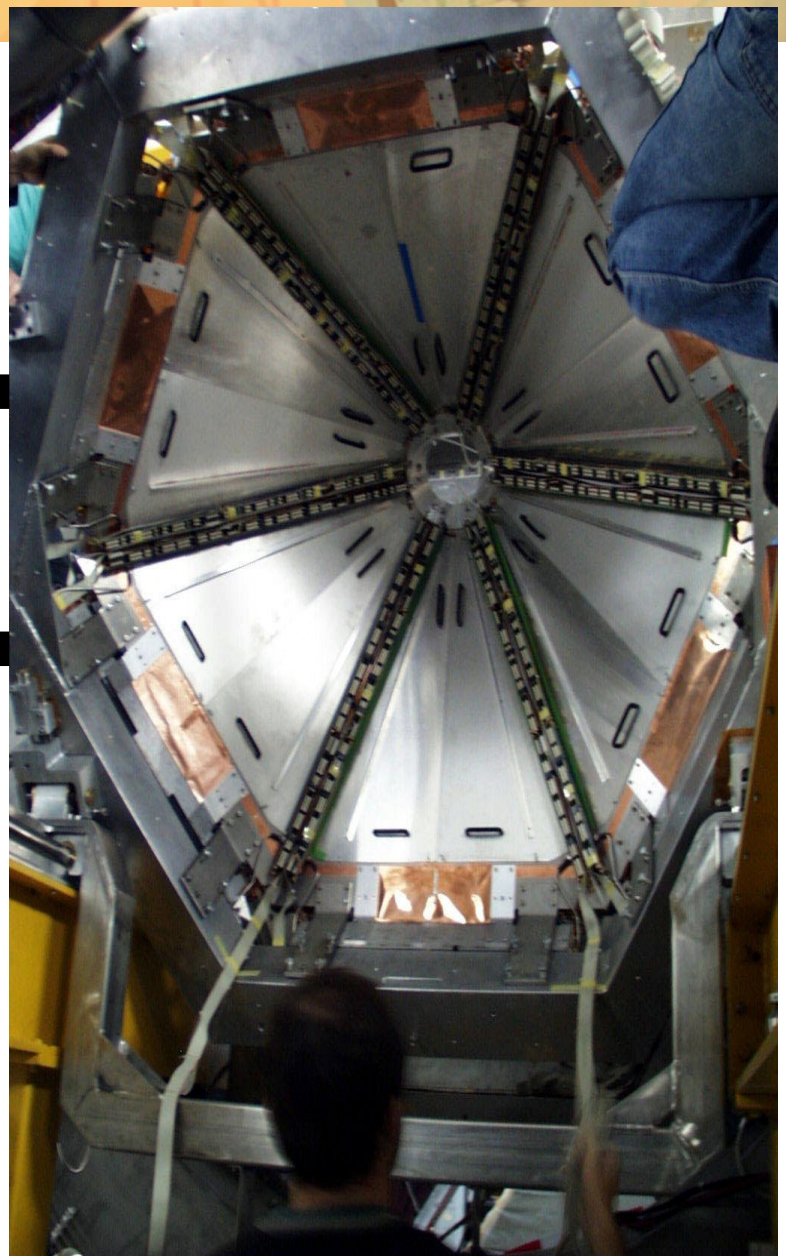


- 24 Boards will read out all HADES MDC chambers (~30.000 TDC channels)
- Parallel readout of ten buses within one FPGA
- Running!
- Possible platform to implement “on line” tracking or RICH ring/MDC segment correlation
- The Processor code is highly reusable: Attilio Tarantola

Solution II: Remaining Problem



10 flat ribbon cables



The Front End Electronics (FEE) is squeezed between MDCs

=> induces readout noise up to oscillations

Solution III: Optical Transmission

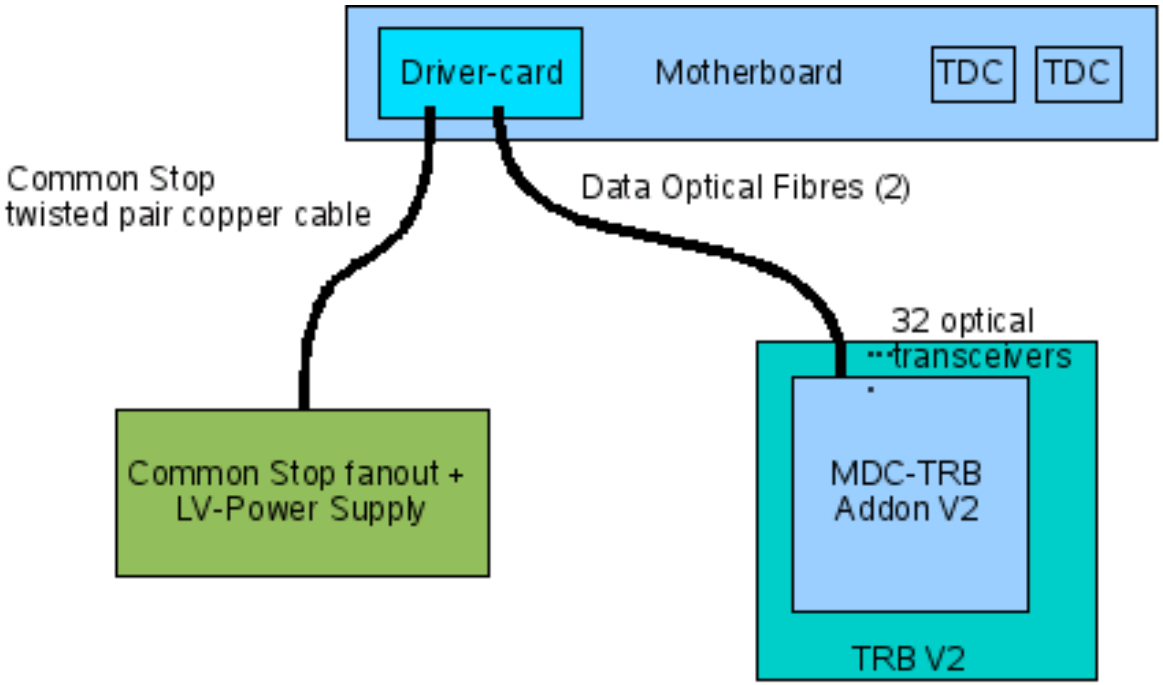
- Optical Transmission solves many problems
  - Has to be affordable (~450 times)
  - Small, low power dissipation
- Fortunate coincidence
  - FPGA SERDES goes down to 250 Mbit/s
  - FOT (Fibre Optical Transceivers) for POF (Plastic Optical Fibre) available for 250 Mbit/s
    - Based on LEDs => cheap

Solution III: POF Transceivers

- Company Firecomms (Ireland) delivers 250 Mbit/s transceivers
- Range: 50 m; no special tools
- Small: 1.6x2.0x1.2 cm^3
- “cheap”: 12 €, (1000 pieces bought)
- Cable: 1.5mm full duplex, 0.60€/m

- Suitable for timing signals?
  - No! Long series of investigations from Firecomms, but no solution found
- Standard FOT
  - Needs AC signal at input to work!
  - LVDS in/output, simple to use, transparent

Solution III: Concept

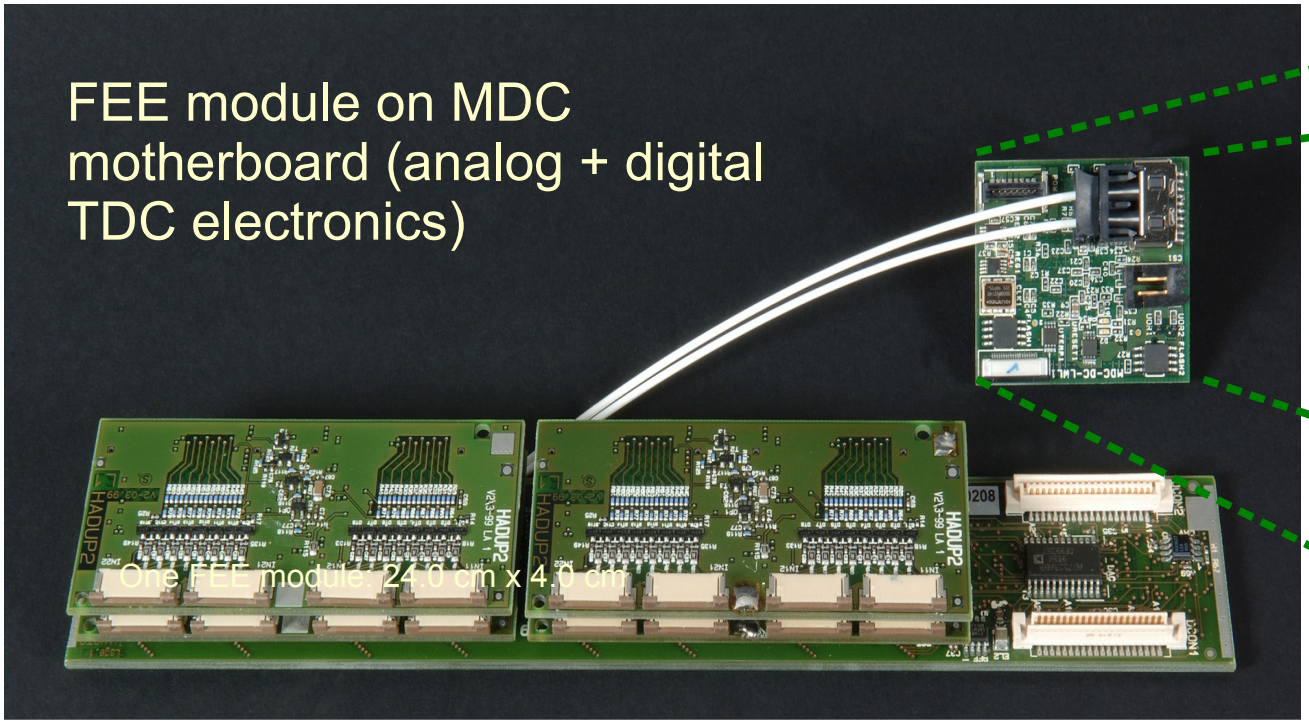


- MDC-Motherboards will be read out by new “Driver Cards”: MDC Endpoint
  - using an FPGA and POF

  Receiver has 32 inputs
  - 12 TRBs for whole MDC system

  Timing:
  - LVDS over copper
    - Two wires twisted pair
- Power:
  - Same board as timing distribution, just LDOs

Solution III: Details about Optical Endpoint



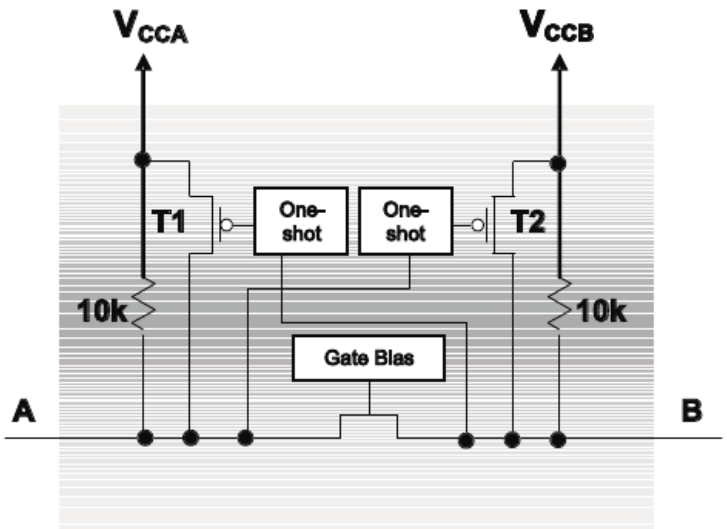
Driver Card size: 4.0 cm x 4.5 cm

- Space limitation: 4.0 cm x 4.5 cm
  - Many tricks in layout (thanks to Jan!)
- Schematics: Yanyu Wang, copied from Jan's GTB-LWL
  - Special SMD-FOT design from Firecomms for us

Solution III: More Details about Optical Endpoint

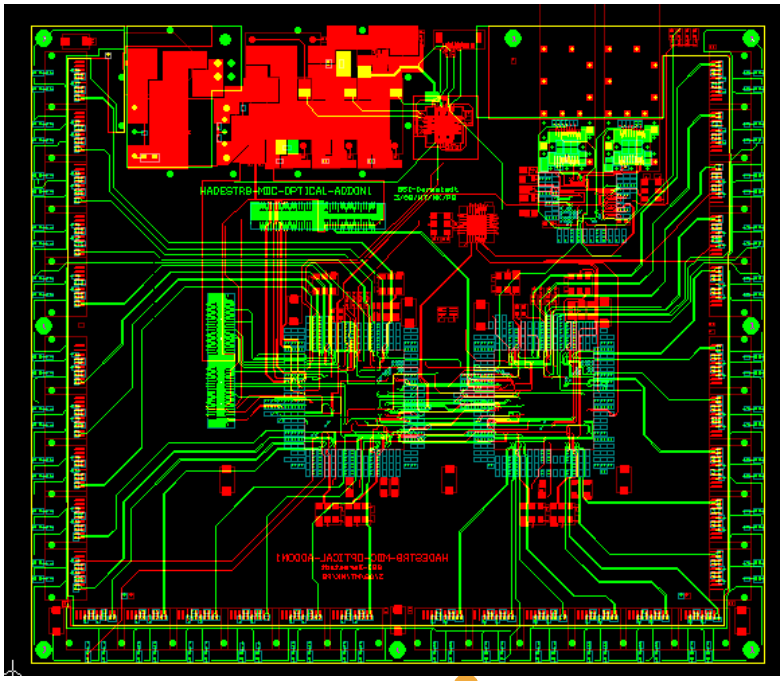
Solution features:

- FPGA: Lattice ECP2M20
  - 1.7x1.7 cm^2, 4 channels SERDES (250Mbit/s - 3Gbit/s)
  - 20k LUTs, 1.2Mbit memory, 20€/piece
- 7 different voltages needed => small LDOs
  - ADP1715 (fixed voltages, 500 mA)
- Double flash architecture (W. Ott)
  - New Flash:
- 5V->3.3V translators: TXS0108E
  - 5.5V -> 1.2V, **without** direction pin, up to 60 Mbit/s
  - Small: 20 pin BGA, 2.5 x 3.0 mm^2
- One wire temperature sensor

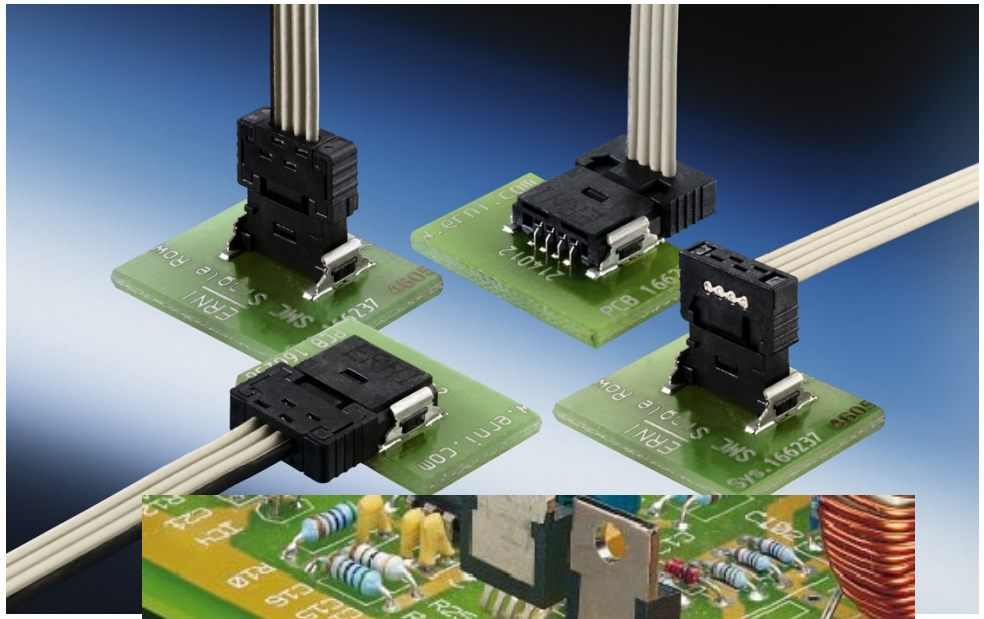


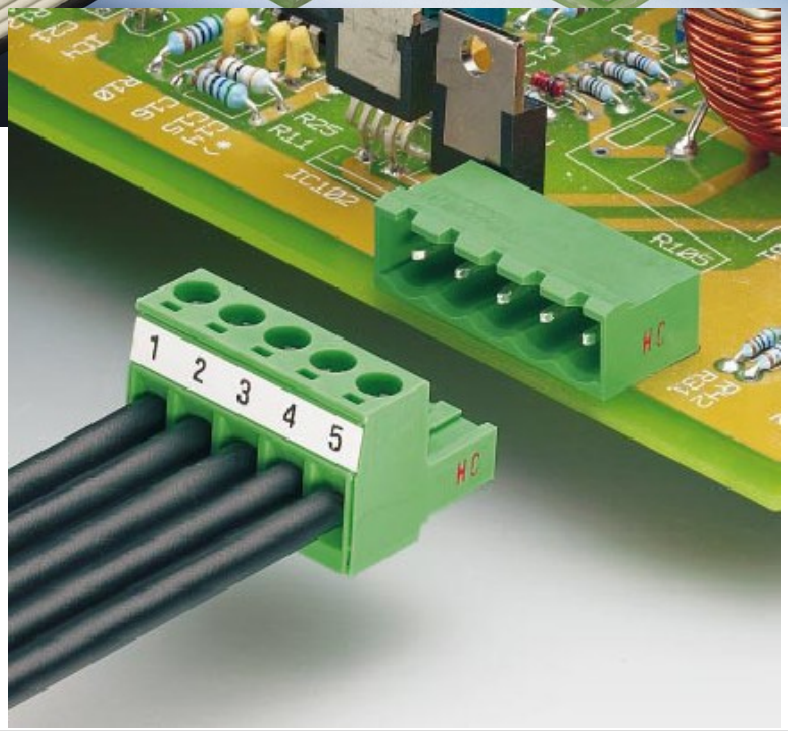
Solution III: TRB-MDC-Optical-AddOn

- 32-channel Receiver Module
- TRB-AddOn
- 2 times Lattice FPGA: ECP2M 100
  - Largest device available: 16 SERDES
  - ~120€
- 1 time Lattice FPGA ECP2M 20
  - SFP PCIe card (Jan) or Ethernet connectivity
  - Produced, waiting for assembly



Solution IV: Power Distribution





- Erni Mini-Bridge was the only usable solution
  - Max. 8 pins, 3 A per pin, **SMD**
  - Expensive: 15€/(5 m cable)
  - First the company refused to sell tools for crimping
- Power Connector:
  - Phoenix contact: High current (16A)
  - Available with **lock**!

Discussion

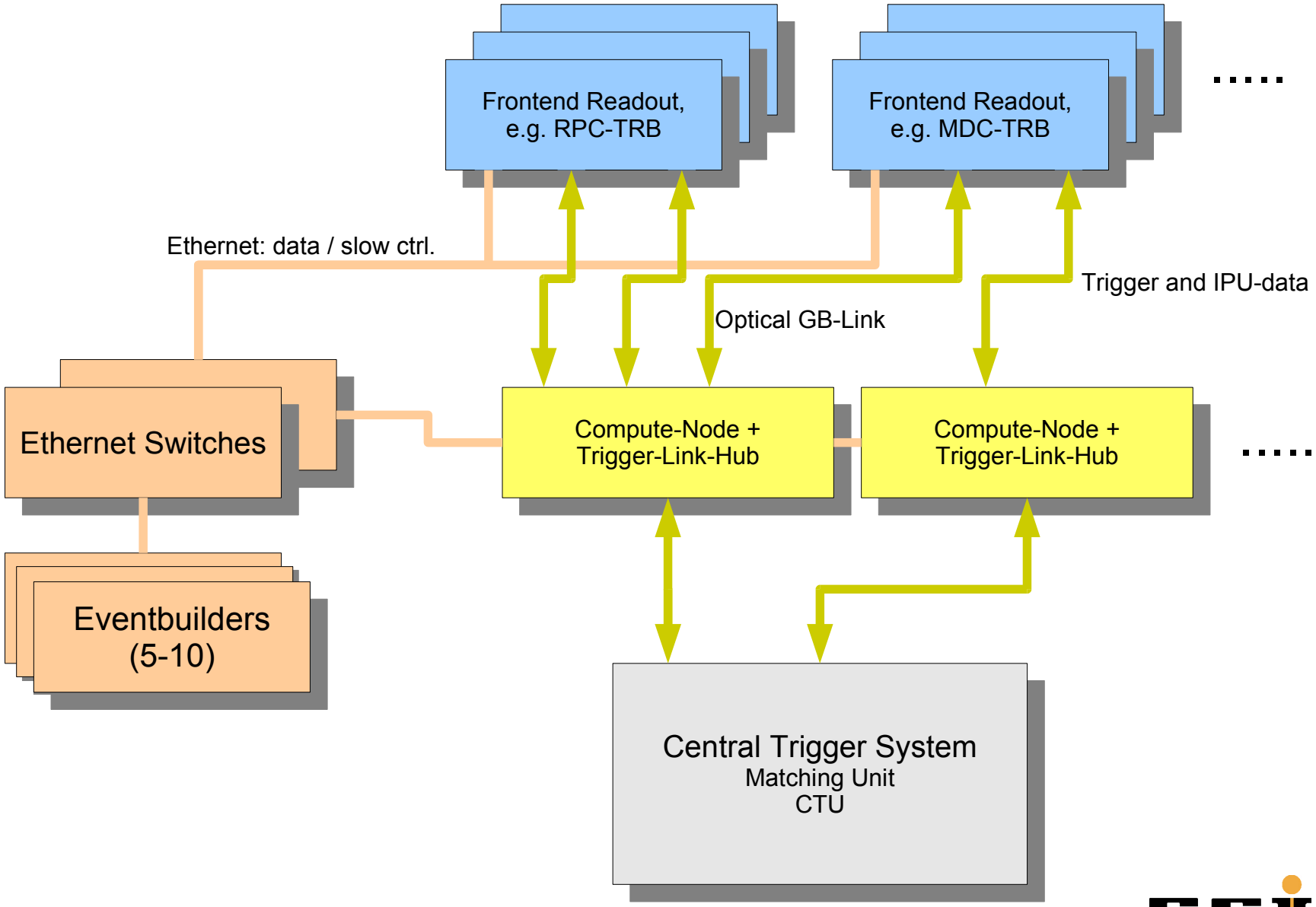
- Different ideas/experiences
-
-

MDC “Optical Endpoint”

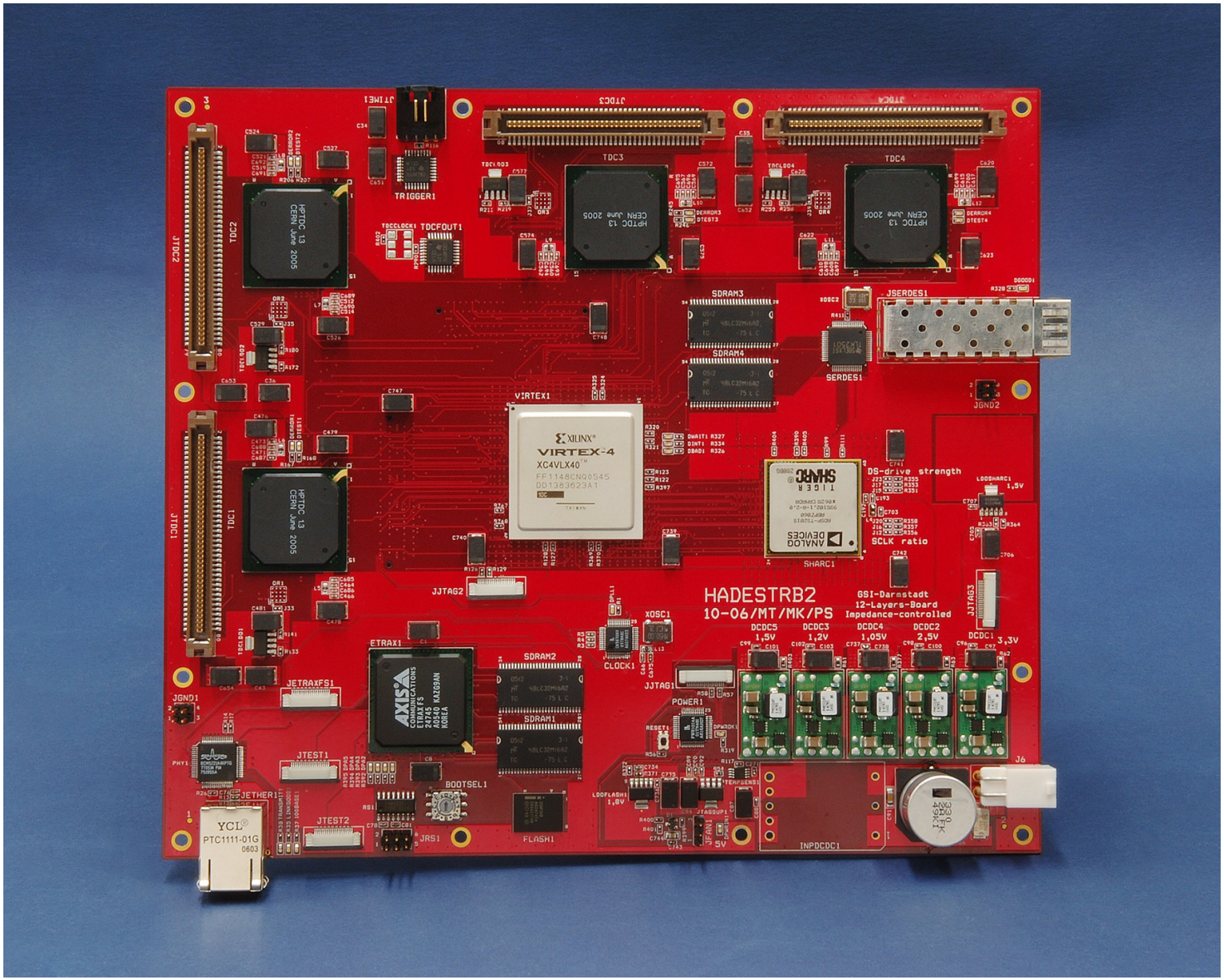
Thank you for your attention!

Backup Slides

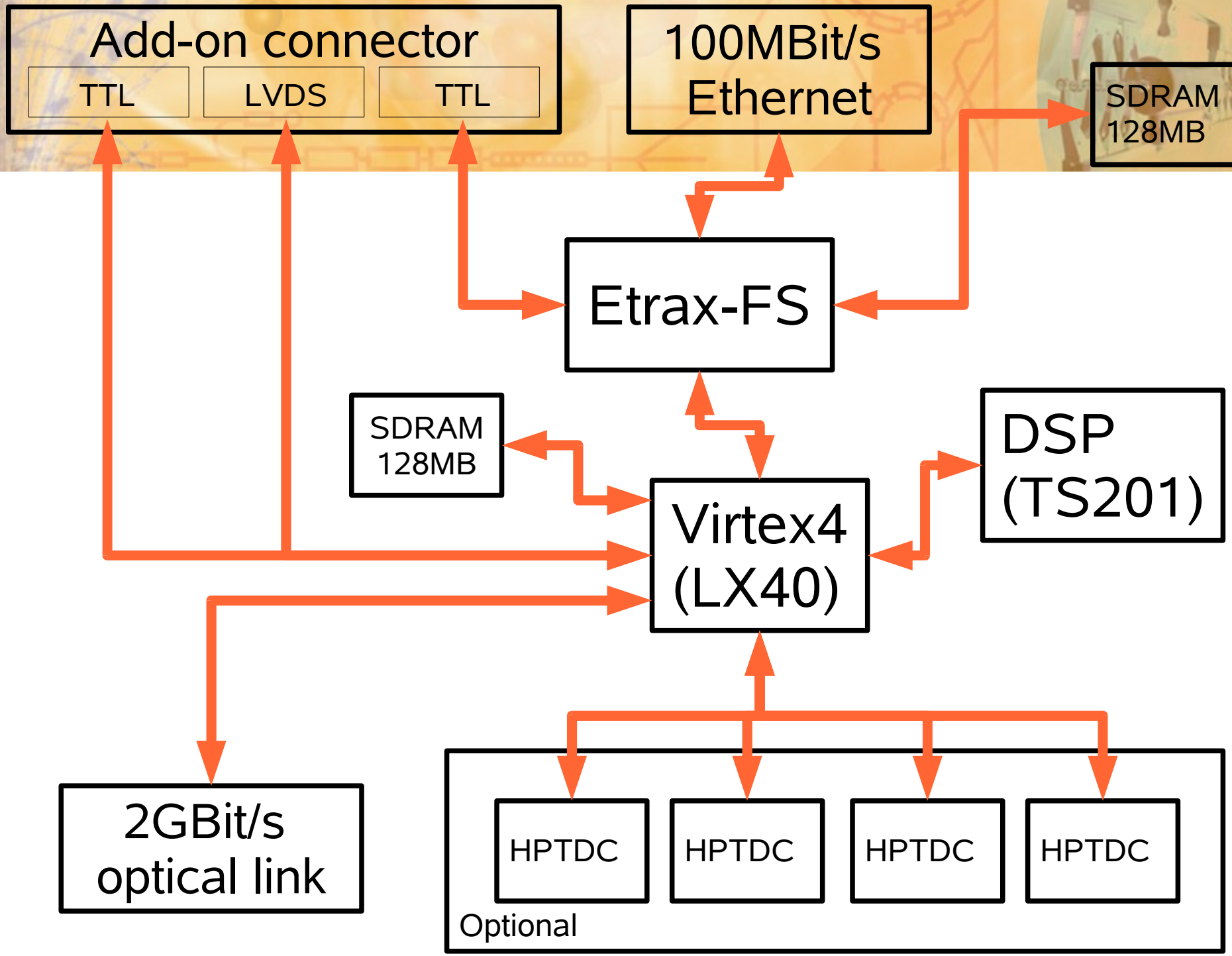
“new” DAQ Architecture



TRBv2



- successor of TRBv1, which is used in the experiment
- larger FPGA
- faster CPU (x3)
- Tiger-Sharc DSP
- 2 GBit/s optical link for trigger and data
- Add-on connector
- TRBv1 functionality given


Add-on connector
TTL
LVDS
TTL
100MBit/s Ethernet
SDRAM 128MB
Etrax-FS
SDRAM 128MB
DSP (TS201)
Virtex4 (LX40)
2GBit/s optical link
HPTDC
HPTDC
HPTDC
HPTDC
Optional

TRB V2, why? consequences?

Advantages to use TRB V2 as DAQ-FEE-system

- Use one common platform for all subsystems!
  - Concentrate manpower on one main project
    - data transport issues are solved only once => more stable
    - easier to debug, distributed knowledge, less maintenance, lower cost
- Interesting also for other experiments: CBM, Panda, PET-readout

Nothing is for free, general solution needs...

- more time until deployment (more complex)
- new trigger / IPU-bus over optical links (IP-core)
- many people involved, more communication, better documentation needed, ... => **advantage**

TRBv2 connectivity: Add-on Boards

- 15 GBit/s connector + many multipurpose I/Os
- Add-on-boards provide the connectivity to the other detectors / new applications / other experiments

TRB V2 can be our common DAQ-FEE-platform

- RPC, Forward Wall, Beam-detectors, TOF, PET
  - With HPTDC
- MDC, RICH, Shower
  - Without HPTDC
- around 100 boards will be used

Status / Manpower / Risk TRBv2

Status:

- TRBv2 ready to be used for RPC, Forward-Wall, Beam-Detectors, TOF => TRBv1 functionality

=> **low risk!**

Manpower:

- Current main developers:
  - TRBv2: Marek Pałka, Radek Trębacz
  - TRB Net: Ingo Fröhlich, Jan Michel
    - Involved: Marcin Kajetanowicz , Krzysztof Korcyl + others

TRBv2 from the point of Electronics

„New“ technologies (high risk)

- LatticeSC FPGA: price, SERDES feature
- ispClock
  - 5 programmable clocks, different standards, rise time
- Power-Sequencer
  - 14 outputs, 10 analog inputs, sequencer, I2C, JTAG
- EtraxFS processor, Axis
  - CPU + 3 CoProcessors
  - Fast, flexible and **complicated**
    - several month of manpower
  - easy to run: standard Linux, development environment
  - Flash: new, not supported, patch solved the problem

Problems, TRBv2

Layout is a major effort

- 8 different voltages
- 13 power „planes“ (different DC/DC converters and LDOs)
- Power filtering, carefully designed pi-filters
- impedance matched differential pairs and length matched differential pairs (500MHz)
  - layout system doesn't support this, Specctra does!
- Plugged-Vias, needed for capacitors (low inductance)
- 4000 „components“, 5200 vias, 8000 connections, 12 layers
- 2 month for Peter Skott
- 150-750€/PCB (10) depending on manufacturer
- 6 month delay due to Q-Print

Problems, TRBv2

- 2GBit/s links did work in the beginning just with short cables
- Eye-pattern open! No sign of problems!
- Tektronix: around 2 MHz „wander“ of time-period from ispClock