The Upgrade of the Multiwire Drift Chamber Readout of the HADES Experiment at GSI

A. Tarantola, I. Fröhlich, B. W. Kolb, J. Michel, C. Müntz, M. Palka, H. Ströbele, J. Stroth, M. Traxler and J. Wüstenfeld

***Abstract*—One of the main goals of the HADES-at-FAIR upgrade project is to achieve sustained trigger rates of 20 kHz in the Au+Au heavy-ion collision system at energies up to 8 GeV/u. In this context, a fast and reliable data acquisition of the 24 Multiwire Drift Chambers (MDCs) is developed. The general concept of the upgrade is based on the Trigger and Readout Board (TRB). This hardware has two digital interface connectors for mounting add-on boards. In the special case of MDC, the add-on board is the interface to the detector Front End Electronic (FEE).**

In the first stage of the upgrade the MDC-AddOn (version 1) has been successfully integrated into the TRB concept thereby replacing the major part of the existing bus-like readout electronics.

In the second stage of the MDC readout electronics upgrade the data transfer between FEE and TRB boards will be changed from a parallel copper bus to several serial optical fiber connections. A Lattice FPGA with SERDES manages data transmission. Dedicated hardware in the FPGA is used to detect Single Event Upsets (SEUs).

For this purpose, an optical add-on board (MDC-OptAddOn) has been designed (with 32 optical data sources) to control the data flow generated by two HADES chambers, respectively. Each add-on board combines the data streams into events and transmits them via high speed optical links to mass storage. Additionally, the large FPGAs open a new possibility to perform first steps for a tracking algorithm.

I. Introduction

HADES (the High Acceptance Di-Electron Spectrometer) is a running experiment installed at the SIS-18 synchrotron (GSI, Darmstadt, Germany). Its experimental program focuses on in-medium properties of light vector mesons and rare hadronic probes obtained in heavy ion collisions. Here, in particular the di-electron decays of vector mesons are of interest as the electrons pass the hadronic medium without interacting strongly. Since the branching ratio for the dilepton decays of vector mesons is in the order of 10^{-4} - 10^{-5}, a fast data acquisition (DAQ) and a fast trigger algorithm is needed to be able to collect reasonable statistics.

The spectrometer uses a level-1 (LVL1) trigger which is based on charged particle multiplicities in the Time Of Flight (TOF) detector array and a level-2 (LVL2) trigger which selects the interesting events by combining the information provided by the detectors. More information about this issue can be obtained from Ref. [1].

HADES will continue its program at its current place at SIS-18, and then move to the upcoming FAIR accelerator complex. Here, HADES will continue its experimental program up to kinetic beam energies per nucleon of 8 GeV.

The large data volumes, expected in experiments with heavy collision systems (Au+Au) already at SIS-18 and with higher energies at the new FAIR facility, require bandwidths which cannot be achieved by the current system.

Therefore, the LVL1 trigger rate has to be above 20 kHz which requires a faster DAQ and on-line event selection. A detailed description of the new DAQ and trigger system is given in [2]. The essential point connection to this contribution is that the overall upgrade project uses the "Trigger and Readout Board" (TRB), already outlined in [3] and described in detail in [4]. The TRB will be the common readout platform for all HADES detectors.

In this context, one of the main goals of the HADES upgrade project is to develop a faster DAQ of the 24 Multiwire Drift Chambers (MDCs) with the aid of the flexible and modular TRB concept which will be roughly sketched in the following.

The TRB is a standalone, ethernet-based hardware which uses an ETRAX-FS processor [5] for DAQ and slow-control functionality. The processor runs a standard Linux kernel and has direct connection to the 100 Mbit/s Ethernet. The TRB supports EPICS (Experimental Physics and Industrial Control System) to allow the integration into the HADES Slow-Control System [6].

Particularly relevant for this contribution is that on the back side the TRB is equipped with two very high data-rate digital interface connectors (42 TTL lines, 32 LVDS lines, 15 Gbit/s), which give the possibility to mount add-on boards.

Two MDC add-on versions have been developed: the MCD-AddOn (version 1) was designed to replace the bus architecture by a star-like system. As the general concept has been successfully tested, a design has been made which contains 32 optical transceivers thus replacing the electrical connection

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A. Tarantola, I. Fröhlich, J. Michel, C. Müntz, H. Ströbele and J. Stroth are with the Institut für Kernphysik, Goethe-Universität, 60486 Frankfurt, Germany.

B. W. Kolb and M. Traxler are with the GSI Helmholtzzentrum für Schwerionenforschung GmbH, 64291 Darmstadt, Germany.

M. Palka is with the Smoluchowski Institut of Physics, Jagiellonian University, 30-059 Krakow, Poland and also with the GSI Helmholtzzentrum für Schwerionenforschung GmbH, 64291 Darmstadt, Germany.

J. Wüstenfeld is with the Institut für Strahlenphysik, Forschungszentrum, 01328 Dresden-Rossendorf, Germany.

A. Tarantola, C. Müntz, H. Ströbele, and J. Stroth are also with GSI Helmholtzzentrum für Schwerionenforschung GmbH, 64291 Darmstadt, Germany.

which turned out to be a source of noise. On the front-end side, the counterpart, we have developed a very small, highly integrated optical end point driver card.

This paper is organized as follows: first, we introduce the original MDC readout, then we explain the concept of the MDC-AddOnv1. In Sec. IV we explain the new optical transmission.

II. The current HADES MDC readout scheme

The readout electronics of the drift chambers are mounted on the drift chambers frames. Analog readout information of the chambers is provided through cables to external readout electronics: 4 or 6 daughterboards equipped with the 8-channel ASD8 (Amplifier Shaper Discriminator) [7] chips are mounted on motherboards. The ASD8 chip amplifies, shapes and discriminates the analog signal produced by the detector. Each channel of the ASD8 chip is connected to one TDC channel which are mounted on motherboards. Short motherboards (equipped with 8 TDCs [8]) with a total number of 64 channels, and long motherboards (equipped with 12 TDCs) with a total number of 96 channels are the basic constituents of the MDC FEE. The TDC determines the start time and width of the signal generated by the ASD8 relative to an external timing signal. Digitized data is transmitted to VME-based Read-Out Controllers (ROC) via standard parallel differential copper cables. Here, signal conversion (to differential signals) is done by so-called Driver Cards (DCs). Each DC is a small board which is plugged on each motherboard and equipped with two transceivers (SN75976A2DL from Texas Instruments). In the ROC data is buffered and transmitted to the VME-based SAM (Steuerungs- und Auslesemodul) module passing trough the Concentrator Module (CM). The CM is the hardware interface between the ROC modules and SAM. The SAM builds chamber's sub-events, using the information provided by the TDCs and sends them to the central event builder of the data acquisition, which builds events with the information provided by all sub-detector systems.

A schematic representation of the readout concept is depicted in Fig. 1.

III. Integration of the MDC FEE into the TRB concept: the MDC AddOn board (version 1)

A first add-on board has been developed to replace the bus architecture depicted in Fig. 1 while keeping the electrical data transmission. This stage allows to implement ROC and SAM readout functionality in one single architecture.

The MDC-AddOn board (version 1) is the interface to the detector motherboard using however the old driver card. A FPGA (Xilinx Virtex4 XC4VLX-10FF1148) is placed in the center of the card. Currently it initializes the HADES chambers FEE and performs a fast parallel data readout.

Together with the TRB, it replaces the major part of existing readout electronics chain: the ROC, the CM and the SAM. Sub-event building is done via the Etrax processor. Each add-on communicates to the chamber's FEE (the old DC) through parallel (differential) bus cables. One MDC-AddOn (version 1) configures and reads out 1088 Time to Digital Converters

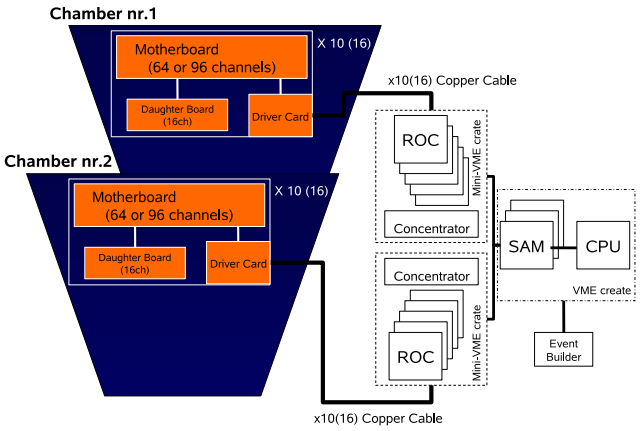

Fig. 1. Current data acquisition scheme of the drift chambers. Analog information is digitized on the daughter/motherboards close to the MDC-chamber, and raw data is transmitted via a pluggable driver card. Then the data is received by the ROCs and forwarded via the concentrators to the SAM and finally to a VME-CPU.

(TDCs) channels in 136 TDC-ASICs which are mounted on the FEE on the chamber's frame. All needed functionality has been implemented and tested on one single chamber [10].

IV. Optical transmission: MDC Optical AddOn and MDC Optical End Point

In the second stage of the upgrade serial optical links replace the parallel copper bus. Optical signals are generated right after the digitization of the analog signals thus reducing noise pickup and increasing the data transport bandwidth (see Fig. 2).

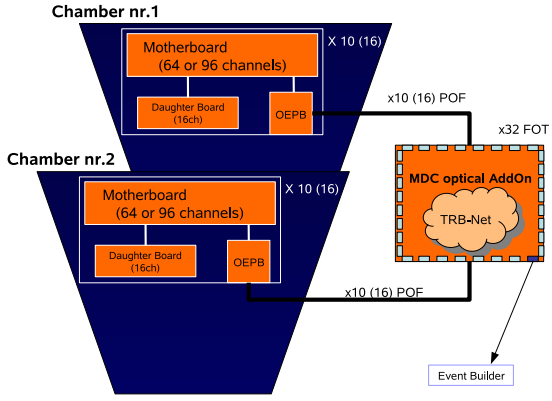

Fig. 2. Optical transmission: new readout scheme. Here, the complete digital readout chain is replaced, including the connection between the FEE and the readout system (realized by replacing the driver card by the Optical End Point Board (OEPB).

This requires three ingredients: A.) the optical add-on board which serves 32 optical connections, B.) a replacement of the FEE driver card (DC) and C.) a protocol which transports the

data. In the following subsections we are going to explain these efforts.

A. The Optical AddOn

Like in the version 1, a dedicated add-on board will be used to read out the chambers.

This new concept will reduce the noise which is induced by the currently used fast signals in the copper bus cables into the very sensitive HADES MDC detector. The data will be received by a MDC-AddOn (version 2 or MDC-OptAddOn), which is equipped with 32 optical transceivers [9] each transporting 250 MBit/s which is sufficient to read out two HADES chambers. The board is equipped with two Lattice FPGAs (ECP2/M100) which receive the data and combine the data stream to events. The large amount of resources in the FPGAs provide the possibility to perform a first fast on-line tracking.

Upon a positive LVL2-trigger, data is consequently transported to mass storage via 2-Gbit optical link which is explained in a separate contribution [2].

B. The Optical End Point Board

On the FEE side, an Optical End Point Board (OEPB) has been developed and will substitute the currently used transceiver FEE card or DC.

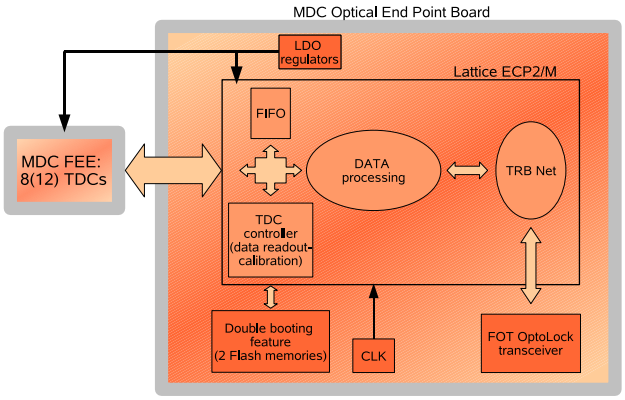

Fig. 3. Block diagram of the Optical End Point Board (OEPB). Its main components are the Lattice FPGA (ECP2/M), containing the data buffer, the end point logic for the TRBNet, and the optical transceiver.

1) Hardware: The OEPB is equipped with a small but powerful Lattice FPGA (ECP2/M) chip, which controls configuration and readout of the chamber's TDCs (see Fig. 3 and Fig. 4).

A Fibre Optical Transceiver (FOT, we use FDL300T from Firecomms) is placed on the board: a resonant cavity (LED at 650 nm) with an encapsulated driver IC couples electrical media signals to light. Its small emission aperture is suitable for Plastic Optical Fibre (POF).

A LVDS input/output is connected directly to the ECP2/M FPGA SERDES, which works down to 250 Mbit/s while the FOT works up to 250 Mbit/s.

The advantage of the OEPB design and the use of optical fibres results in total electromagnetic immunity, amazing simplicity in handling and low power consumption. The employment of a Lattice ECP2/M FPGA with large resources allows for the storage of several events close-to-front-end. However, the challenge of this design was to fulfill the strict space constrains.

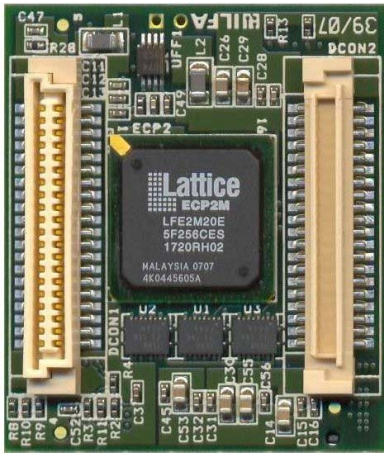

Fig. 4. Picture of the MDC OEPB. On the left and right the connectors for the motherboard are visible. In the middle the Lattice FPGA. The optical driver is on the back side. The space constraints (size: 4.0x4.5cm) were given by the mechanics of the HADES-MDC detector.

2) Configuration Procedure: Due to the large number of FEE boards (nearly 400) and due to difficulties to access these boards when the detector is operational, one of the main issue is the possibility to change the FPGA design remotely. Here, one should notice that the OEPB is equipped with two flash memories (MX25L1605A). This allows for a dual boot feature: generally, a "static" firmware is loaded in the first flash memory (which provides a safe communication but not with all features). A second firmware can be loaded remotely (via optical fiber) in the second flash memory via the "running" FPGA which receives the new firmware, and loads it into the second flash memory via Serial Peripheral Interface (SPI). The flash memories allow operation on a simple 3-wire bus.

Using the "manual reset" pin in the power manager chip on board (TPS3307-25DGNR from Texas Instruments), the FPGA can select the second flash and perform a "soft" reset. When the "manual reset" is deasserted the second flash design is loaded in the FPGA. The dual boot feature accounts for the possibility to change the FPGA firmware very frequently.

C. The Trigger and Readout Network

In the framework of the HADES DAQ upgrade a media independent protocol (TRBNet) has been developed [11] which will be implemented in the MDC readout. The main feature of the TRBNet is the "concurrent" transmission of data/trigger and slow-control data on the same fibre; it guaranties low latency and no data loss due to the back pressure feature. Every board is equipped with a temperature sensor each having a world-wide unique serial number that allows to identify it in the network. Based on this, an individually selectable TRBNet-address is assigned to each board during the start-up phase of

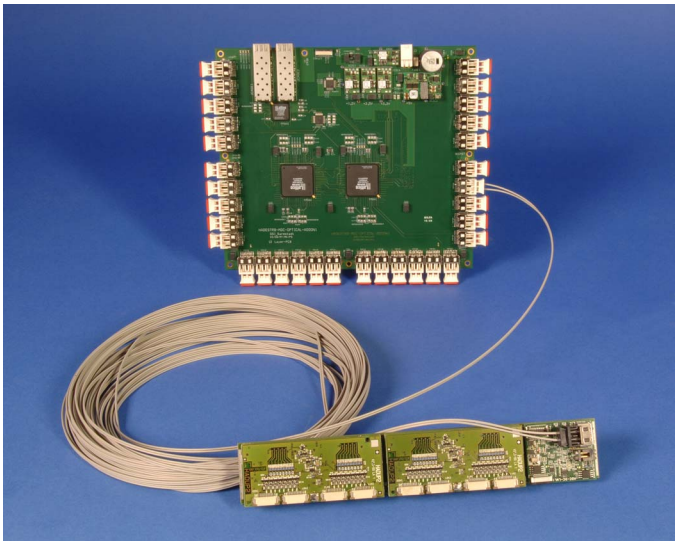

Fig. 5. The MDC-OptAddOn (in back, size: 20.0x23.0cm) among with the FEE (in front): the optical POF is connected to the OEPB (on the right side) which is plugged onto the motherboard. Here, two daughterboards are connected to the motherboard (left part).

the network. This allows for an individual access of all front-ends boards from the central trigger monitoring system over the network and leads to various new possibilities for precise fine-tuning of configuration options.

V. Irradiation and SEUs detection with Lattice FPGA

Given the remarkable success of reprogrammable logic, the interest in their front-end use is here obvious. As shown, such devices have many advantages, but they are susceptible to bit upsets induced by radiation: so called Single Event Upsets (SEUs). The upset's source is the radiation to which the FPGA is often exposed in high energy physics experiments.

A preliminary irradiation test has been performed at GSI, during HADES beam time when a 3.5 GeV proton beam hit a Nb target: an OEPB board was placed for several weeks near the beam at a distance of approximately 12 meters from the target. The particle flux was varied by changing the distance of the FPGA from the beam line. The ECP2/M FPGA die was exposed to different reaction products (protons, neutrons, pions, heavier particles and fragments produced in the mentioned reaction) at very different energies.

Dedicated Lattice ECP2/M Single Even Detection (SED) hardware has been used to detect SEUs and reprogram the FPGA [12], leading to the observation of an average of 2 SEUs per hour at a particle rate of 10^6 particles/s*cm^2.

VI. Summary and outlook

In summary, we are currently replacing the HADES-MDC readout in the framework of the HADES-at-FAIR project. In a first step, we have tested the new system based on the Trigger and Readout Board (TRB) with a dedicated add-on board but with a connection to the FEE based on the old driver card. In a second step, these copper cables will be replaced by POF (Polymer Optical Fibre) which seems to be - due to their easy handling and small drivers - a good candidate for the FEE readout of other FAIR projects as well.

All hardware modules are available. Fig. 5 shows a complete new chain containing the optical hub (MDC-OptAddOn), the cabling and the new driver card plugged onto a MDC-motherboard. We expect that our new developments are sufficient to obtain the new requirements and we are confident to reach the overall goal of having a new MDC data acquisition system with the techniques presented in this contribution.

Acknowledgment

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