

A General Purpose Trigger and Readout Board for HADES and FAIR-Experiments

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Abstract—HADES is a running spectrometer installed at GSI, Germany. PANDA and CBM are planned detector systems for the new FAIR facility at GSI. For these detectors, a general-purpose trigger and readout board with on-board DAQ functionality was developed. The original motivation for this project was the implementation of a 128-channel Time to Digital Converter (TDC) with a time resolution of $\sigma=40$ ps based on the HPTDC chip from CERN into a fully fledged data acquisition system. The application of the board is detector independent, includes a 2 Gbit/s optical link and has the option to employ the TDC chips and/or to integrate versatile add-on boards through 16 Gbit/s connectors. The latter one may interface to the front end electronics of other types of detectors. A large FPGA (Xilinx Virtex 4 LX40) and a TigerSharc DSP can be used as on-board resources for trigger and on-line analysis algorithms. Data transfer to mass storage and slow control is done via an ETRAX processor running Linux and a 100 Mbit/s Ethernet interface.

Index Terms—Triggering, Time measurement, Data acquisition, Modular electronics.

I. INTRODUCTION

MANY modern experiments in the field of hadronic physics are designed to measure with high accuracy rare reaction channels in the presence of large background. To achieve an adequate sensitivity in a limited amount of beam time, data acquisition systems have to operate at high interaction rates, while a powerful trigger must efficiently reject background events to reduce the amount of data written to mass storage.

Such a multi-level trigger system is already used by HADES¹ [1] which is operated at the SIS18 heavy ion synchrotron of GSI, Germany and measures rare e^+e^- decays of (vector) mesons in elementary as well as proton-, pion-, or ion-beam induced reactions off nuclei. As the decays of these particles have a low branching ratio into the di-electron

channel (around 10^{-5}), on-line electron identification, by combining hit information of three different detector systems, is a central element of the HADES trigger system. Real time pattern recognition provides a second level trigger decision before the collected event is transported to mass storage.

At the upcoming FAIR² accelerator complex [2], HADES will continue its experimental programme up to kinetic beam energies per nucleon of 8 GeV. The planned large experiments PANDA³ [3] and CBM⁴ [4] will address questions on the generation of mass, its interplay with the spontaneous breaking of chiral symmetry, the limits of baryonic existence and the creation of de-confined matter at large matter densities. To improve the sensitivity over what can be achieved at existing facilities, the experiments will be operated at high luminosity to provide access to rare decay channels and/or particle production near threshold. The production and detection of states carrying charm quarks, either in hot and dense matter, or in vacuum will be a central issue. Additionally, the measurement and precise spectroscopy of hadronic excitations and their masses, including gluonic degrees of freedom, is very important for the understanding of the strong interaction. Lepton pairs (i.e. e^+e^- or $\mu^+\mu^-$) are also found to be very promising, when used as probes, to unravel the properties of dense matter, because once they are produced in a decay, they do not interact strongly with the surrounding medium. As already mentioned above, the cross sections and branching ratios of the latter processes are low, and the background is orders of magnitude higher in yield. To meet these challenges, the experiments have to operate with interaction rates well above 10 MHz and use sophisticated higher-level data reduction mechanisms (trigger).

In this contribution, we describe a versatile read-out and trigger board, which is currently being developed for the upgrade of the HADES spectrometer. It will also be used by PANDA and for the CBM detector development.

This paper is organized in the following way: first, we explain the presently used HADES readout and trigger system. In Sec. III a description of the new “Trigger and Readout Board” (TRB) is presented. In Sec. IV, we give an overview of the new HADES data acquisition concept where the TRB plays a central role. In Sec. V, we make the connection to the coming experiments at FAIR. Finally, in Sec. VI the paper concludes by summarizing what has been achieved and which issues are still open.

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¹HADES: “High Acceptance Di-Electron Spectrometer”

²FAIR: “International Facility for Antiproton and Ion Research”

³PANDA: “antiProton ANihilation at DArmstadt”

⁴CBM: “Compressed Baryonic Matter”

II. THE HADES TRIGGER AND READOUT SYSTEM

As had been pointed out, HADES measures di-lepton pairs (e^+e^-). The spectrometer runs currently at a primary rate of 10^6 heavy ions per second, and uses a level-1 (LVL1) trigger which is based on the charged particle multiplicity in an array of scintillator detectors. The LVL1 trigger rate in Au+Au collisions, after the upgrade of the DAQ-system, is anticipated to be 20 kHz. A level-2 (LVL2) trigger algorithm selects events by searching for lepton pairs. This serves as a filter to reduce the amount of collected data. Fig. 1 gives an overview of this principle. The trigger signals are produced by a “Central Trigger System” (CTS) which consists of a CTU (“Central Trigger Unit”) and a MU (“Matching Unit”) [5]. The CTU generates digital trigger information, containing the trigger number and the physics source of the trigger, to induce the specific actions of the front-end electronics (FEE) of the individual sub-detectors. The CTU can handle several types of triggers (i.e. different multiplicity classes) and calibration triggers. In the latter case, the digitization is carried out without zero suppression to sample the time-dependent behavior of noise, obtained with 3 to 4 Hz during data taking.

Using this two-level concept, the readout boards send only a fraction of the events to the event builder (EB), which combines the data from the different asynchronous data sources into complete events and finally writes them to mass storage. As the LVL2 trigger decision comes after a latency corresponding to several events (five to ten events are common values), the readout boards must have buffers large enough (LVL1 pipes) to hold the data for this time.

The lepton yield, in the event sample selected by the LVL2 trigger algorithm with an efficiency of 90%, is ten times more than in the unbiased LVL1 events [6]. These numbers were obtained off-line by comparing unbiased and positively LVL2 triggered events. Details of the off-line analysis can be found in [7]. In addition to the LVL2 events, which contain a lepton candidate, some LVL1 events are selected with a preset down-scaling factor. This increases the amount of transported and stored data, but at the same time provides an unbiased event sample for a study of the LVL2 trigger bias (see above). The down-scaling factor ranges from 1:3 to 1:9 depending on the event size. It was tuned to keep the reduction of the accepted LVL1 trigger rate below 10%.

For small collision systems like $^{12}\text{C}+^{12}\text{C}$, the settings described above should typically lead to trigger rates of 17 kHz for LVL1 and 2 kHz for positive LVL2 triggers with a transported data rate of 4 MB/s. For heavier systems, like the reaction argon on potassium chloride ($^{40}\text{Ar}+^{39}\text{K}^{35}\text{Cl}$) typical rates are 7 kHz LVL1 triggers and 1 to 2 kHz positive LVL2 triggers transporting 7 to 14 MB/s.

Under real data taking conditions, we found that the accepted trigger rates are about a factor of 2 smaller than in tests using a pulser with a fixed frequency. This difference is caused by short-time beam intensity fluctuations during spills which cause short periods (10 to 150 μs) without LVL1 triggers and thus no activity of the DAQ-system.

The main reason for upgrading the HADES trigger and readout system is the addition of the new RPC detector

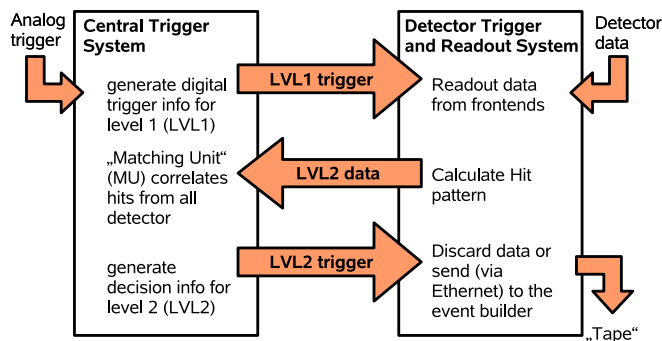


Fig. 1. Basic principle of the HADES two-level trigger system: analog trigger sources are sampled by the central trigger system (CTS). Trigger information is transported to the individual detector trigger systems (DTS) via a LVL1 bus cable. The LVL2 trigger decision by the CTS is based on hit patterns of the detectors, therefore two more connections are used (per DTS). Only data with a positive LVL2 trigger decision are transported to the event builder (EB).

(“Resistive Plate Chamber”) [8], [9]. Since the currently used data acquisition system was designed ten years ago, it was reasonable to reconsider the whole concept and make use of new technologies. Furthermore, the large data volumes, expected in experiments with heavy collision systems (Au+Au) at SIS18 and with higher energies at the new FAIR facility, require bandwidths which cannot be achieved by the current system.

III. THE TRIGGER AND READOUT BOARD (TRB)

The trigger and readout board is a multi-purpose electronic device with on-board DAQ functionality. The original motivation of the TRB project is a new RPC detector (2600 channels) for HADES which upgrades its time-of-flight system requiring a time resolution of less than 100 ps and a signal pulse height measurement for walk-corrections of the detector signals. The TRBv1 version (see below) has already been used for the HADES Forward-Wall and Pion-Hodoscope upgrades (640 channels) [10].

The readout electronics is on board and the data are transported to mass storage via 100 Mbit/s Ethernet and the UDP internet protocol. Two TRB versions have been developed: the TRBv1 [11] was designed to be only a 124-channel Time to Digital Converter (TDC) device based on the HPTDC⁵ [12]. As the concept has been tested successfully during HADES data taking periods, its design has been extended to serve as the new standard readout module for all HADES sub-detectors (TRBv2 [13]).

A. The TRB version 1

The TRBv1 has 4 input connectors (80-pins, high-density), each of which carries 31 LVDS timing input signals and five general purpose LVDS-I/O-signals. The time to digital conversion of the 124 signals is done in four HPTDC chips (as shown in Fig. 2). The 32nd channel of each HPTDC is connected to an external reference timing signal (LVDS, not shown).

⁵HPTDC: “High Performance Time-to-Digital Converter”

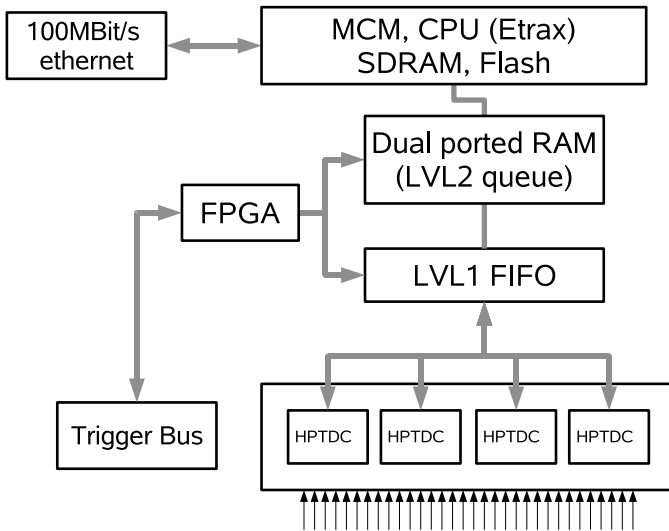


Fig. 2. The TRBv1 block diagram. Discriminated timing signals from the detector (e.g. the RPC) are digitized via 4 HPTDCs. The readout of the HPTDCs is started via a signal on the trigger bus. The data is stored in the LVL1 pipe until the LVL2 trigger decision arrives. Finally, sub event building is done via the ETRAX processor.

The highly configurable HPTDC ASICs [12] allow the user to choose the TDC time range per channel between 780 ps and 25 ps (at 25 ps only a quarter of the channels is available), to detect rising and falling edges of the timing-signal and to define a matching-window. The multi-hit capabilities offer the possibility to measure the Time-over-Threshold (ToT) and thus to obtain pulse height information of the detector signal. An external trigger signal starts the selection of data in the HPTDCs and the board-controller FPGA initiates the readout. The data are then stored in the LVL1-FIFO with a capacity of 128 kB. Where there is a positive LVL2 trigger decision, the data are stored in a dual-ported memory (128 kB) or discarded otherwise (the LVL2 trigger is needed for HADES, but is an option for other experiments). The data are then read out by a single chip computer (ETRAX [14]) running Linux, formatted and transported via UDP over 100 Mbit Ethernet to the event-builder, which collects and orders the individual sub-events from all readout chains. The UDP transport performance of the ETRAX has been measured to be 11 MB/s. Having the DAQ-system with a full featured computer close to the FEE allows the implementation of the slow-control on the TRB (EPICS [15]), e.g. for setting the thresholds of the attached FEE. The TRB uses a 48 V galvanic isolated power-supply which simplifies power-distribution, prevents ground-loops and allows the TRB to be directly mounted on the detector. The time resolution calculated from the time difference between two reference channels (different HPTDCs) resulted (100 ps binning) in $\sigma=40$ ps, as expected from the known HPTDC performance [12]. Great care has been taken for the layout of the PCB to assure impedance matched and decoupled transmission lines of the LVDS-timing signals, which limited the influence of crosstalk to the overall time resolution of 40 ps to less than 20 ps.

The TRBv1 has been fully integrated into the HADES-DAQ system. In November 2005 a full system RPC test, including

the full electronics chain, was performed during a commissioning beam time (^{12}C with 0.8 GeV kinetic energy per nucleon). An important goal of this test was the time resolution measurement of the whole RPC detector-TRB chain. For those particles which traverse two RPC cells, the time differences of the corresponding signals were formed after proper corrections for pulse height and transit time biases. Fig. 3 shows the distribution of these time differences. It has a σ of 110 ps. The resolution of a single RPC detector is thus $\frac{110 \text{ ps}}{\sqrt{2}}=77$ ps.

In the experimental run in April 2007, the TRBv1 was used to read out the Forward Wall and the beam detectors. Stable operation at the expected data rates was achieved. The overall performance of the data acquisition system was still dominated by the original equipment, but measurements of the dead time of the individual sub-systems suggested that the influence of the TRBs on the overall dead time was small.

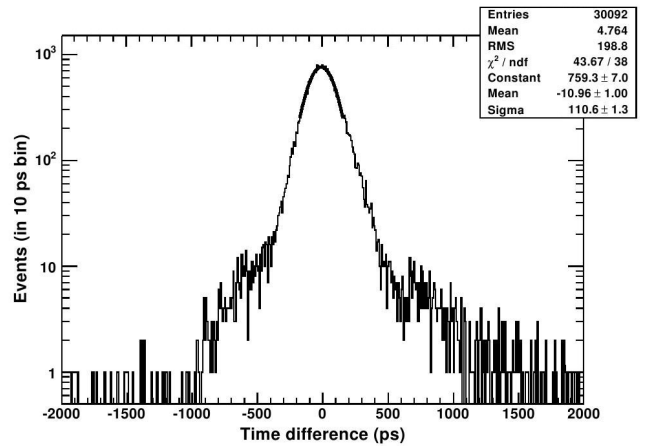


Fig. 3. A histogram of a RPC measurement with beam after the correction with the amplitude information (ToT), the “slewing correction”. The time resolution of the RPC detector using the full electronics chain results to $\frac{110 \text{ ps}}{\sqrt{2}}=77$ ps. The figure has been taken from [16].

With a pulser, we achieved 80 kHz on LVL1 (with large down scaling) and LVL2 rates up to 18 kHz, which corresponds to data rates of 1.8 MB/s (without DMA on the used ETRAX processor).

B. The TRB version 2

The TRBv2 uses an ETRAX-FS processor [14] for DAQ and slow-control functionality. The processor runs a standard Linux 2.6 kernel in the 128 MB of memory and has a direct connection to the 100 Mbit Ethernet. The integrated three IO co-processors (each 200 MHz) provide a high bandwidth data transport without main CPU intervention, avoiding data-rate bottlenecks as seen in the TRBv1. The EPICS support by the TRBv2 will afford a smooth integration into the HADES slow control system [15]. The existing functionality of the TRBv1 has been implemented and tested. Even in the absence of the ETRAX-FS coprocessor and DMA, we were able to reach a rate of 37 kHz for LVL1 and LVL2 without down scaling (only header and trailer). After enabling 50 HPTDC data words in addition (which is the expected mean data volume for the RPC

in Au+Au experiments) we achieved 20 kHz, corresponding to 4 MB/s (LVL1 and LVL2). In a standalone test without data transport via UDP we reached 400 kHz LVL1 rate with the same amount of data words. We have no doubt that we will reach our goal of 40 kHz LVL1 rate and up to 20 kHz LVL2 rate, which would compensate losses due to the spill structure and even allow running the experiment without a LVL2-trigger algorithm at the expense of writing ten times more data to mass storage. Moreover, the DMA transfer is currently under test which will raise the LVL2 data transport bandwidth to the design value of 10 MB/s.

To broaden the spectrum of possible applications, for HADES as well as for future FAIR experiments, we have added a very high data-rate digital interface connector (32 LVDS lines, 15 Gbit/s). Add-on boards can thus be mounted on to the TRBv2 which provide the needed detector-specific interfaces for special connectors/electrical standards, specific FEE (like ADCs) and additional computing resources (FPGAs).

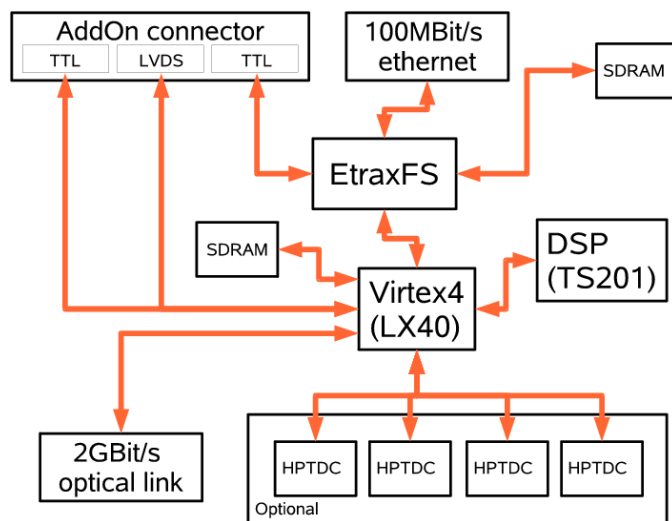


Fig. 4. A block diagram of the TRBv2. It features 4 HPTDCs (128 channels, optional), an ETRAX-FS-Processor [14] with 128 MB memory running Linux, Ethernet-connectivity, an optical link with a throughput of 2 Gbit/s, programmable logic (Virtex 4 LX40) and a TigerSharc DSP (500 MHz, 24 Mbit memory, 4 link ports).

Additionally, the TRBv2 provides an optical link with 2 Gbit/s, (de-)serialized by the TLK2501 from Texas Instruments. This link is used for the following reasons: 1.) It will work as a replacement of the existing HADES trigger bus (which uses RS485 signals), 2.) for additional high speed data transport since the bandwidth of the 100 Mbit/s interface is not enough for the FAIR experiments, and 3.) for the transport of LVL2 trigger-data to the planned LVL2 trigger computing nodes. A FPGA (Xilinx Virtex 4 LX40 + 128 MB RAM) and a TigerSharc DSP (from Analog Devices) can be used as on-board resources for trigger and on-line analysis algorithms. For example, the TigerSharc-DSP will be used for HADES to realize the time of flight algorithm, which is already part of the present LVL2 trigger and implemented on the ADSP-21062 from the same company. Fig. 4 sketches the main components of the hardware. The hardware itself is shown in Fig. 5.

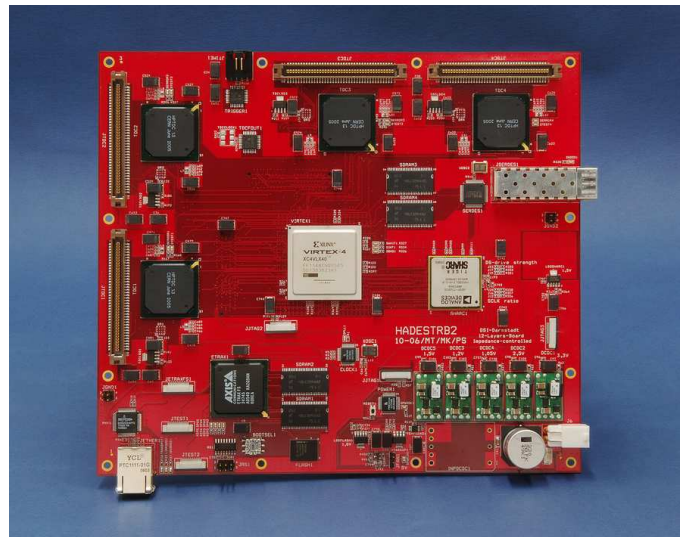


Fig. 5. The TRBv2 module (size: 20x23cm).

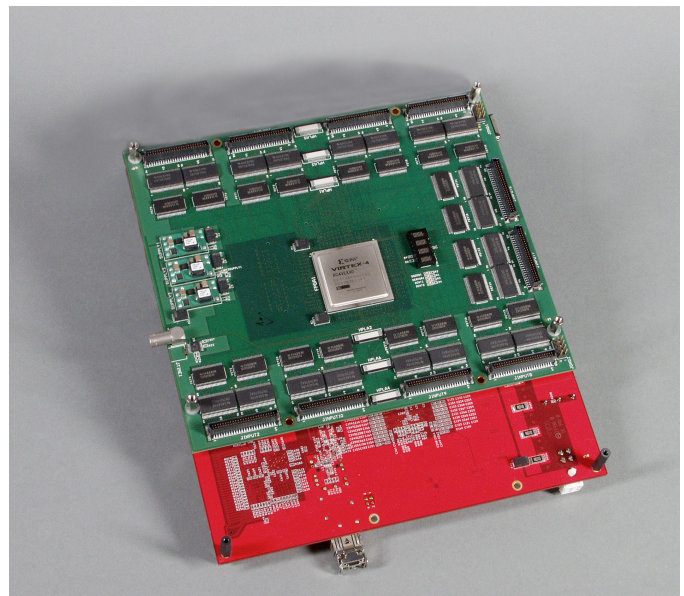


Fig. 6. The MDC-AddOn mounted on the back side of the TRBv2 (which is visible in part only).

The first add-on card built for the TRBv2 has been developed to read out the Multi Wire Drift Chambers (MDC) of HADES. This add-on card receives and collects data from several FEE driver cards and sends them to the TRB via the 32 LVDS high-speed connector. The MDC-AddOn card is equipped with ten connectors, where each has 50 pins and two RS485 transceivers (SN75976A2DL). From each connector, a standard RS485 bus is driven to the FEE driver cards (374 are used in the experiment), which are then placed on the MDC-chamber frame. A FPGA (Xilinx XC4VLX-10FF1148) is placed in the center of the add-on card. The MDC-AddOn card is connected back to the TRBv2 (see Fig. 6) through two connectors (SAMTEC QSE-040-01, 80 pins each). This concept allows the user to read out all 24 MDC-chambers using one single TRB. The MDC-AddOn card is currently

commissioned with one MDC-chamber reading out its ten buses in parallel. The expected data rate for Au+Au at 20 kHz LVL1 is 8 MB/s per TRB, which can be handled via the 100 Mbit/s Ethernet interface. The 128 MB SDRAM of the TRBv2 base module is sufficient to buffer a complete spill.

A “General Purpose” add-on (GP-AddOn) has been additionally designed to provide an interface to the existing HADES trigger bus and a connection to many general purpose signals (like the LVL1 trigger sources). It contains two of the HADES trigger bus connections to allow for the chaining of modules. It has connectors for input and output for RS485, LVDS, LVTTTL and inputs only for arbitrary differential signals (common mode range from -4V to 5V).

The add-ons for the HADES Pre-Shower [17] and for the TOF detector are currently being developed.

IV. THE TRB AND THE HADES READOUT SYSTEM

The TRB is becoming a part of the existing HADES readout and trigger system [5]. The TRBv1 had been integrated using the old LVL1 and LVL2 trigger bus connections. However, as these boards have only readout functions, there are no resources for on-line data processing (e.g. a high performance DSP), desirable for LVL2 trigger applications. Moreover, there is no data path back from the TRBv1 to the CTS.

As the experience during recent HADES data-taking periods has shown, a bus-like trigger distribution system is not easy to monitor and maintain. For example, in the case of a malfunction, all the connectors of the affected bus have to be checked. Furthermore, all hardware modules, besides the CTS, are in a pure slave mode and cannot drive the bus without a trigger. Therefore, we decided for future developments to use only point-to-point connections (with serial links). This approach is also adopted in all modern communication systems, like Gigabit Ethernet and PCI-express.

For the reasons explained above, the trigger distribution system of HADES will be replaced by a star-like distribution system. Most of the connections will be based on the 2 Gbit/s optical links. With 8b/10b encoding, this results in 200 MB/s (raw data rate, without protocol overhead). Fig. 7 shows a sketch of the new trigger concept. It uses a star-like trigger distribution via optical hubs, which could also include intelligent data preprocessing. The CTS will consist of a TRB with the GP-AddOn, providing the connections to the trigger sources and to generate the digital LVL1 trigger information.

The requirements for the protocol, to be used mainly on the optical links, are:

- 1) full back pressure: if one of the readout boards becomes overloaded with detector data, it will generate and assert a trigger “busy” signal which will be forwarded to the CTS to “stop” the generation of the LVL1 triggers. This is done by two mechanisms:
 - a) by locking the CTS after trigger submission until all receivers have released the “busy” signal by sending a termination word.
 - b) on each single point-to-point connection by the employment of a handshake protocol.

- 2) short and guaranteed latency: many front end readout systems in HADES require having the trigger information not later than $1 - 2 \mu\text{s}$ after the timing signal has arrived (a jitter in the order of several 100 ns is allowed). The reason for such short latency is that in order to achieve 40 kHz LVL1 in-spill rate, the read out of the front ends and the release of the “busy” signal has to be carried out in less than $25 \mu\text{s}$.
- 3) data integrity: trigger signals need a protocol without any data loss. Due to possible data loss (e.g. in network switches) the usual implementation is that corrupted buffers are detected by a software protocol on the transport layer. We considered UDP as well as TCP for this purpose, but with UDP the data integrity is not guaranteed and TCP leads to additional delays. The point-to-point handshake, as described above, avoids any data loss.
- 4) the FEE cards (e.g. the MDC driver cards) should be integrated into the network and use the same protocol but on different physical media. This is very convenient for monitoring. Moreover, it makes the use of network bridges obsolete.

First test have been done in this context but as the final design of the network protocol is still ongoing its details will be part of a future publication.

An additional board (HadCom) has been built to test many features of the new trigger system as well as to serve as a communication interface between the new trigger and readout board network with the existing HADES-electronics.

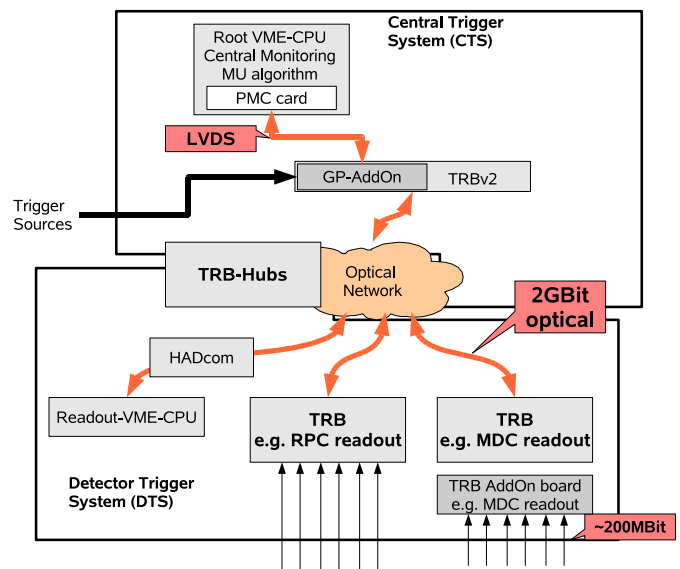


Fig. 7. The TRB in the context of the new HADES trigger system: around 90 TRBs will serve as the new HADES readout boards. Trigger submission from the CTS (which will also consist of one TRB + one VME CPU) is done via the optical cables. The main entities (TRB-Hubs) making the communication are TRBs with a dedicated add-on (16 optical links each).

The integration of the existing VME readout subsystems into the new TRB based data acquisition of HADES will be realized in two ways: for the time of migration, the HadCom module as well as the GP-AddOn can serve as an old-to-

new converter (and vice versa), which means that the optical real time network and the old trigger distribution system can run in parallel. The more elegant way is to use a standard PMC add-on card for the VME-CPU's (e.g. the PMC-DX2004 from Acromag), which has a Virtex-2 and 32 programmable LVDS lines, to be plugged to the corresponding connector of the HadCom or GP-AddOn. In this way, VME-crates can be connected to the HADES trigger system and serve as readout systems (e.g. for general purpose VME scalers and latches). In addition, usage can be made of a VME-CPU in the central trigger system to run monitoring software and pattern recognition algorithms.

One more add-on (Hub-AddOn) has been developed to realize (together with the TRBv2 as a motherboard) the optical TRB-Hub: it is based on the LatticeSCM (LFSCM25) and utilizes its integrated 16 high speed (de-)serializers. This add-on can be re-used for the readout of the RICH [18] detector, as the data coming from the RICH-detector will be transmitted via HUB-AddOn compatible 2 GBit/s optical links. The board is currently being commissioned.

V. THE TRB AND FAIR

The usage of a standardized base readout module, which can be adapted to many applications, would also be very helpful for the large experiments to be installed at the FAIR facility at GSI (PANDA and CBM). Although the FAIR construction itself has not yet begun, the future users of the new facility have already started the research and development for the needed detector subsystems and the readout.

It should be pointed out that the collision rate of these experiments will be much higher than those realized in HADES. Therefore, the employment of a central trigger system and a busy logic is problematic. The approach taken by PANDA and CBM, is to operate the detector systems without a central trigger, following the pioneering work of the COMPASS experiment [20]. Under such conditions, each subsystem generates individual hit information, which is time stamped, and freely streaming to an event builder unit. In particular, the PANDA collaboration favors a very flexible data acquisition system to be able to configure the high-level trigger according to the physics needs [21]. Depending on what is discovered, such a trigger can require the detection of different particle species, particle multiplicities or secondary vertices.

In this context, the TRB can serve as the readout system of PANDA's MDC detector, which should have a time resolution of 2 ns for drift times of 100 to 200 ns. Moreover, the readout system must be able to handle large hit rates up to 1 MHz, and to perform a hit detection (cluster finding). These points are fulfilled by the TRB, which will be connected to a data concentrator via the 2 Gbit/s optical link (or a higher speed version). The trigger-less readout is carried out in the following way: first, the HPTDC data acquisition window is set to be 1 μ s, and second, the TRB is continuously read out with a frequency of 1 MHz. For prototype studies, the HADES optical trigger hub can be used.

The possibility to mount detector specific add-on cards onto the TRBv2 will also help to speed up the development when

evaluating new technologies for the CBM experiment. One of the major challenges of the CBM experiment is the Silicon Tracking System (STS), the central detector of the CBM experiment [22], which is supplemented with a Micro-Vertex Detector (MVD) consisting of two very thin and fine-pitch MAPS ("Monolithic Area Pixel Sensors") [22] pixel detector stations close to the target. The expected raw data rate for a pixel size of 20 μ m, a readout rate of 100 kHz and an ADC resolution of 12 bit, will be in the order of 300 Gbit/s. This clearly calls for additional data reduction mechanisms, which are sketched in [23].

One of the tasks which should be addressed in the near future is how to read out a complete system of these sensors and how the data should be compressed before forwarding. Extended studies are needed here before a prototype can be realized. The TRBv2 can serve as a general purpose readout system with flexible interconnectivity by the optical high speed transmission to allow for efficient data readout studies. Moreover, the built-in DSP makes it possible for the data compression and reduction algorithms to be tested, which later could be run in the CMOS sensor itself. This approach would save time and overhead costs.

VI. CONCLUSION AND OUTLOOK

In summary, we have presented a general-purpose trigger and readout board based on the ETRAX processor and (optionally) the HPTDC for time measurements. The integration of an ETRAX chip with Linux enables slow control and a DAQ with data rates of 10 MB/s per board. Optical links enable fast point-to-point communication where needed and, in addition, replace the currently used trigger-bus by a more flexible trigger transport architecture. The TRB has been developed for the HADES readout system but it can also be used for parts of the new PANDA and CBM detector systems which will be installed at FAIR. Up to now, two versions have been built and tested: the TRBv1 and the TRBv2. The latter one has an optical link and improved IO features (e.g. to mount add-on cards), as well as a TigerSharc DSP. Six different add-on boards are currently under construction or are already commissioned: in this contribution, we have presented the MDC-, the GP- and the Hub-AddOn. Under development are the add-ons for the HADES Pre-Shower and TOF detector. The Hub-AddOn can be re-used for the readout of the RICH detector.

Furthermore, one add-on board is being developed at this time which will serve for the readout of the MAPS sensors, currently being studied for the CBM experiment. The on-board DSP can be used in this context to test different on-line data reduction features. The TRBv2 also fulfills all requirements needed for the PANDA-MDC readout.

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