HADES3 – Data Acquisition and Trigger upgrade, Annual Report: 2006

Outline

- List of Projects
- Description of Work
  - work fulfilled, milestones
- New Synergy
  - TRB V2
  - new Milestones / Gantt-Chart
- Summary

List of Projects for DAQ upgrade

Objective: 20 kHz primary data rate to ensure measuring rare decays in heavy systems

MU	TOF	Common Readout	MDC	RICH	RPC
Matching Unit Concentrator	Replacement TOF readout-board	Replacement of old VME-CPUs	Higher bandwidth digital readout electronics	New digital readout for lowering electronic noise in the RICH detector	TDC-board with readout
Matching Unit Version 2	more powerful TOF-IPU	Parallel working Eventbuilders	Integration of track information to LVL2 trigger	More powerful IPU for lower fake-rate	IPU for RPC

HADES3
HADES1
not FP6 (BMBF)

Description of Work, part 1

Exchange of all VME-CPUs with modern Linux VME-CPUs

- 10 times faster CPUs
- 20 times faster network connection

Necessary tasks:

- Software port to Linux [done]
- Test system [done]
- Step by step exchange [almost done]
  - Hardware changes to existing electronics if required
  - work on old undiscovered bugs, revealed by higher readout speed

Description of Work, part 2

Status:

– **[done]**, for all systems but RICH
  - RICH integration is projected until December 2006

– Impact of upgrade:
  - factor 4 more statistics during Oct. 2005 beamtime!
  - faster startup of DAQ by a factor of 5

Milestones:

– M10-2: VME CPUs replaced (done for the most important ones) [almost reached]

Deliverables:

– D10-1: „x86 based DAQ“ **[almost ready]**

Description of Work, part 3

Faster TOF-Readout and TOF-IPU and faster Matching-Unit (Synergy)

– VME-board with recent digital components (FPGAs, DSPs) to ensure needed performance

More Synergy ?

- Development, progress and success on RPC-DAQ-project „TDC-Readout-Board“ (TRB) revealed new possibility:

TRB V2 can be our common DAQ-FEE-platform

– RPC, Forward Wall, TOF, MDC, RICH

TRB V2, why? consequences?

Advantages to use TRB V2 as DAQ-FEE-system

- Use one common platform for all subsystems!
  - Concentrate manpower on one main project
    - data transport issues are solved only once => more stable
    - easier to debug, distributed knowledge, less maintainance, lower cost
- Interesting also for other experiments

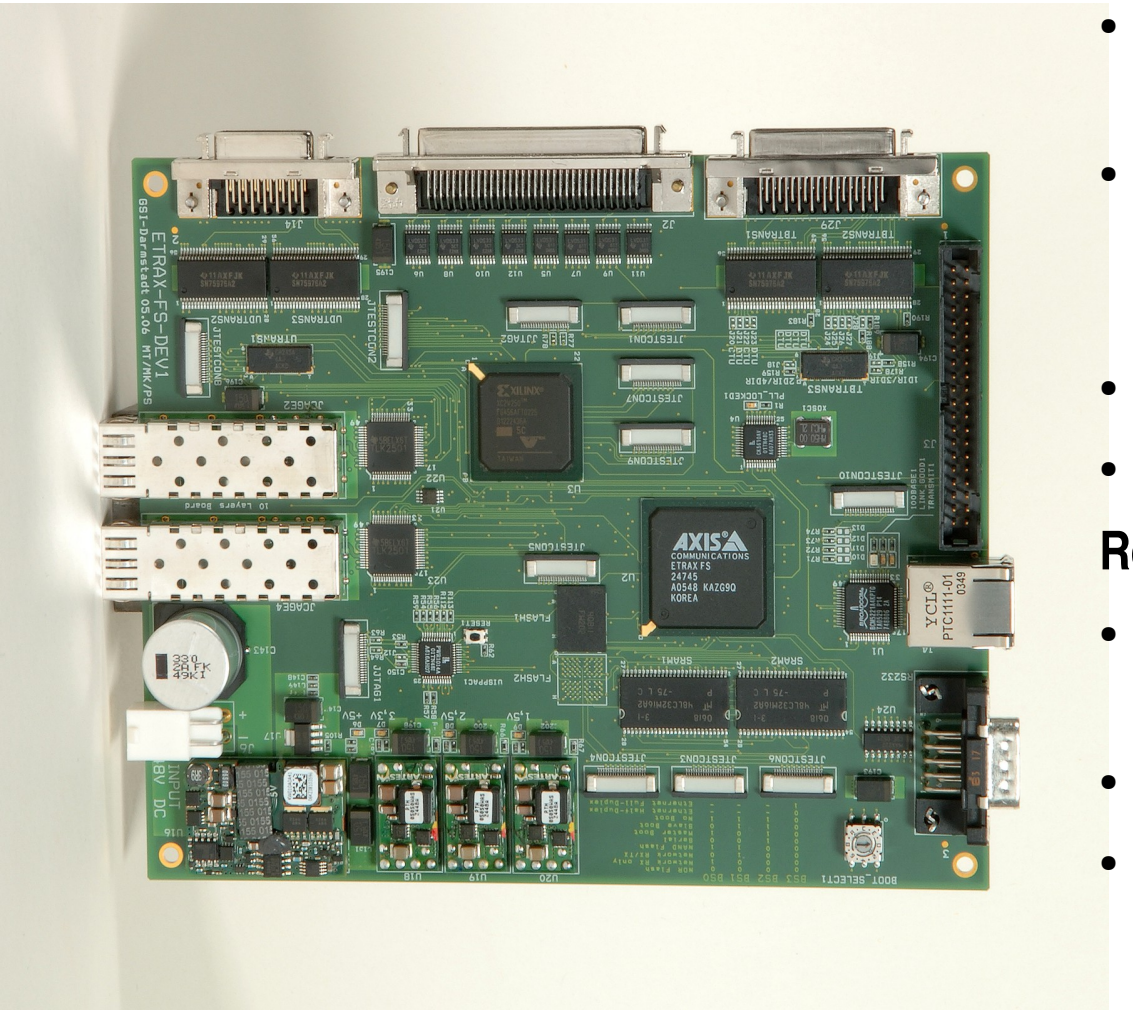
Nothing is for free, general solution needs...

- more time until deployment (more complex)
- new trigger/IPU-bus over optical links (IP-core)
- many people involved, more communication, better documentation needed, ... => **advantage**

TRB V2 features (additional to TRB V1)

- Multi Purpose Time to Digital DAQ-System with standard Ethernet data-transport
- 2 GBit/s optical link for online pattern-recognition data transfer and LVL1 and LVL2 trigger
- Large FPGA (Xilinx Virtex4 LX40) for online pattern-recognition, zero suppression, ...
- 3 times faster CPU
- DSP: Tiger-Sharc (600MHz, 128Bit) for TOF-algorithm
- 8 GBit/s bandwidth general purpose IOs for adaption to „any“ application (like digital or ADC readout)
- low cost (around 10€ / TDC channel)

On the Way to an Universal Readout-Module, TRB Test Board



TRB development board:

- Intermediate step to TRB V2 to test new technologies
- 3 times faster single chip computer with Ethernet and 128 Mbytes of Memory
- FPGA chip (Virtex 2)
- Two 2 Gbit optical links

Results:

- Optical Links run without errors at 2.0GBit/s
- New CPU is performing as expected
- Connection of VME-CPUs (TOF, MU) to HADES-Trigger-Distribution-System

=> **Ready to go for TRB V2.0**

TRB V2 status

- Design finished with lessons learned from „TRB Test Board“
- PCB is in layout
- TRB V2 will be produced in late November
- TRB V1.0 functionality implemented:
  - July-August 2007
- TRB V2.0 with IPU functionality:
  - Beginning of 2008

Changes to the DAQ-Upgrade and Impact on FP6-HADES3

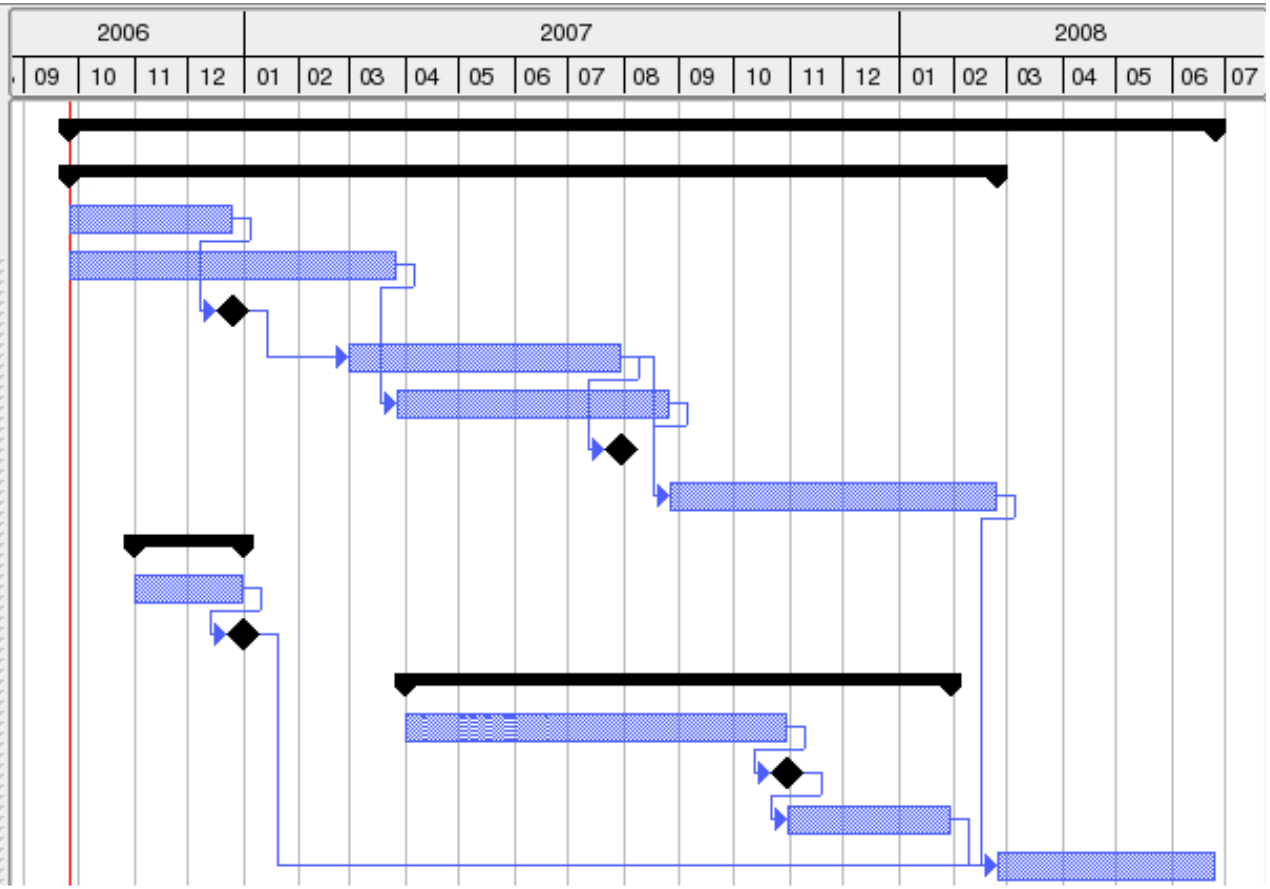
- One platform for DAQ of all subdetectors in upgrade
- results in new Trigger/IPU distribution concept
  – optical links, point to point connection, „hubs“
- possibility to use new VME-CPU (fast) for TOF-readout and IPU functionality (until TOF-FEE is changed to fit to the TRBV2)
- Matching Unit implemented in VME-CPU
- step by step exchange of hardware while ensuring succesfull production beamtimes (next Feb. 2007)

FP6-HADES3 consequences

- TOF and MU projects are delayed

Changes to the Gantt-Chart of the DAQ-Upgrade

Task	Duration
HADES3 Upgrade Project	21
TRB V2 as TOF-Readout	17
Design/Production TRBV2	3
IP-core: Trigger/IPU Links	6
Hardware TRBV2 available	0
Implementing readout functionality	5
TOF/RPC-IPU implementation	5
TRB2 without IPU functionality	0
TOF-readout/IPU integration	6
VME-CPU replacement	2
RICH-CPU replacement	2
RICH VME-CPU replacement finished	0
Matching Unit V2	10
Implementation of Algorithm	7
MU Algorithm implemented	0
MU integration	3
Full System Integration	4



Summary

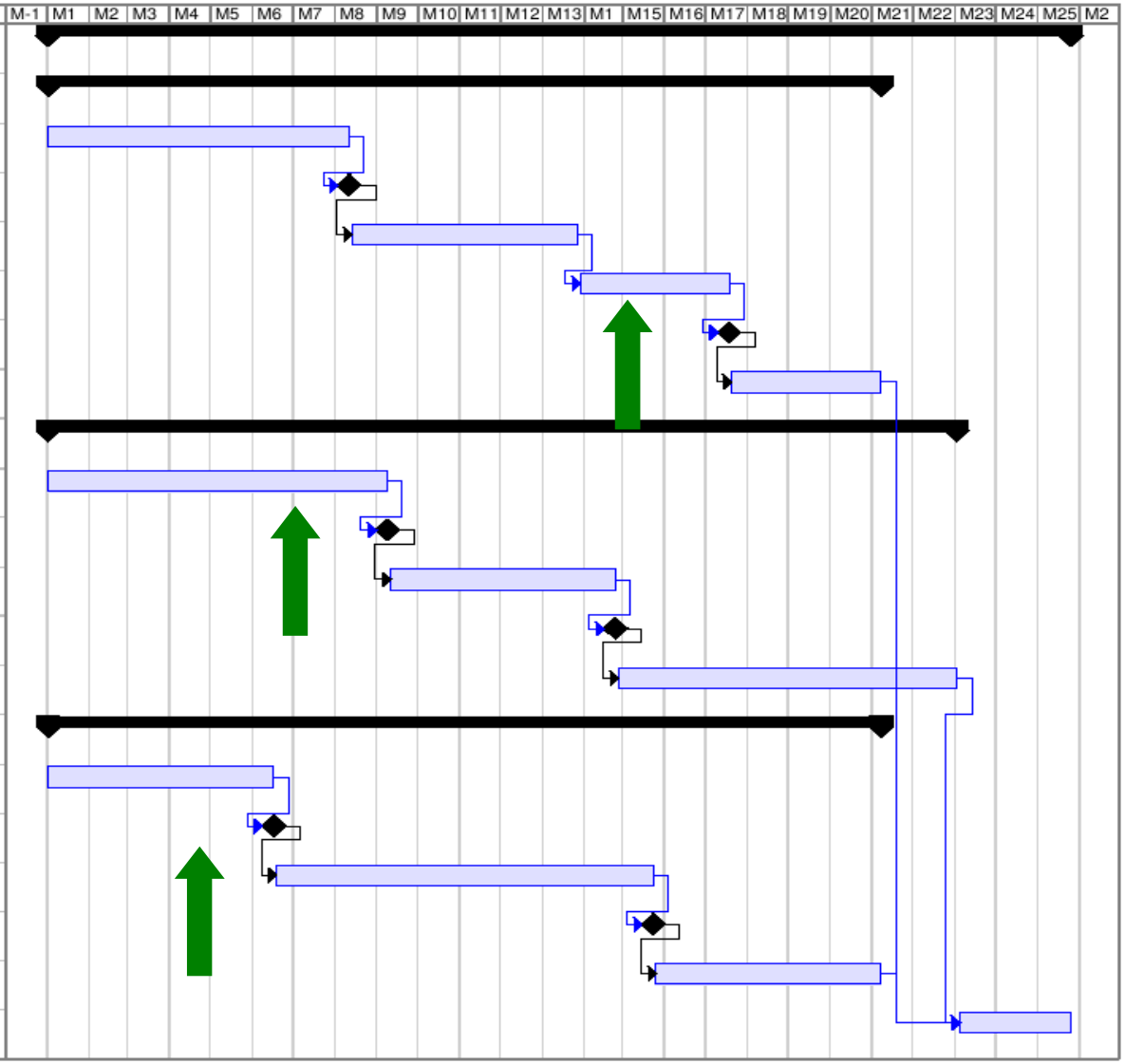
- Deliverable **D10-1** (almost) fulfilled
- Synergy between RPC-Upgrade project and other upgrade projects (MDC, RICH) allow to use one common system for the DAQ-Upgrade
- New milestones and deliverables defined to reach the goal:
  – 20 kHz LVL1 primary data rate in heavy systems

DAQ/Trigger upgrade

Thank you for your attention!

Original Milestones

ID	Vorgangsname	Duration
1	**HADES 3 (DAQ)**	**540 dys**
2	**CPU upgrade**	**440 dys**
3	VME-CPU replacement	8 mons
4	*HAD-3-M2*	*0 dys*
5	Database interfaces	6 mons
6	Eventbuilder	4 mons
7	*HAD3-M5*	0 dys
8	Integration	4 mons
9	**TOF readout**	**480 dys**
10	Read-out board	9 mons
11	*HAD-3-M3*	0 dys
12	IPU implementation	6 mons
13	*HAD-3-M4*	0 dys
14	Integration	9 mons
15	**Matching unit upgrade**	**440 dys**
16	Implementation BIOS	6 mons
17	*HAD-3-M1*	0 dys
18	Implementation of algorithm	10 mons
19	*HAD-3-M6*	0 dys
20	Integration	6 mons
21	Full system commissioning	3 mons



Why do we need an upgrade?

- Parts of the electronics is obsolete / deteriorates / not fast enough for large systems
- Micro-Spill-Structure of beam costs about factor of 2 in DAQ-rate
- Charged particles from upstream sources
- Photon-efficiency of RICH detector, noise

→ RICH-patterns are essential for performance of LVL2 trigger

- Low LVL2 suppression for systems larger than Ca+Ca → lower statistics

Hades DAQ and Trigger- Overview

HADES DAQ and LVL2 Trigger

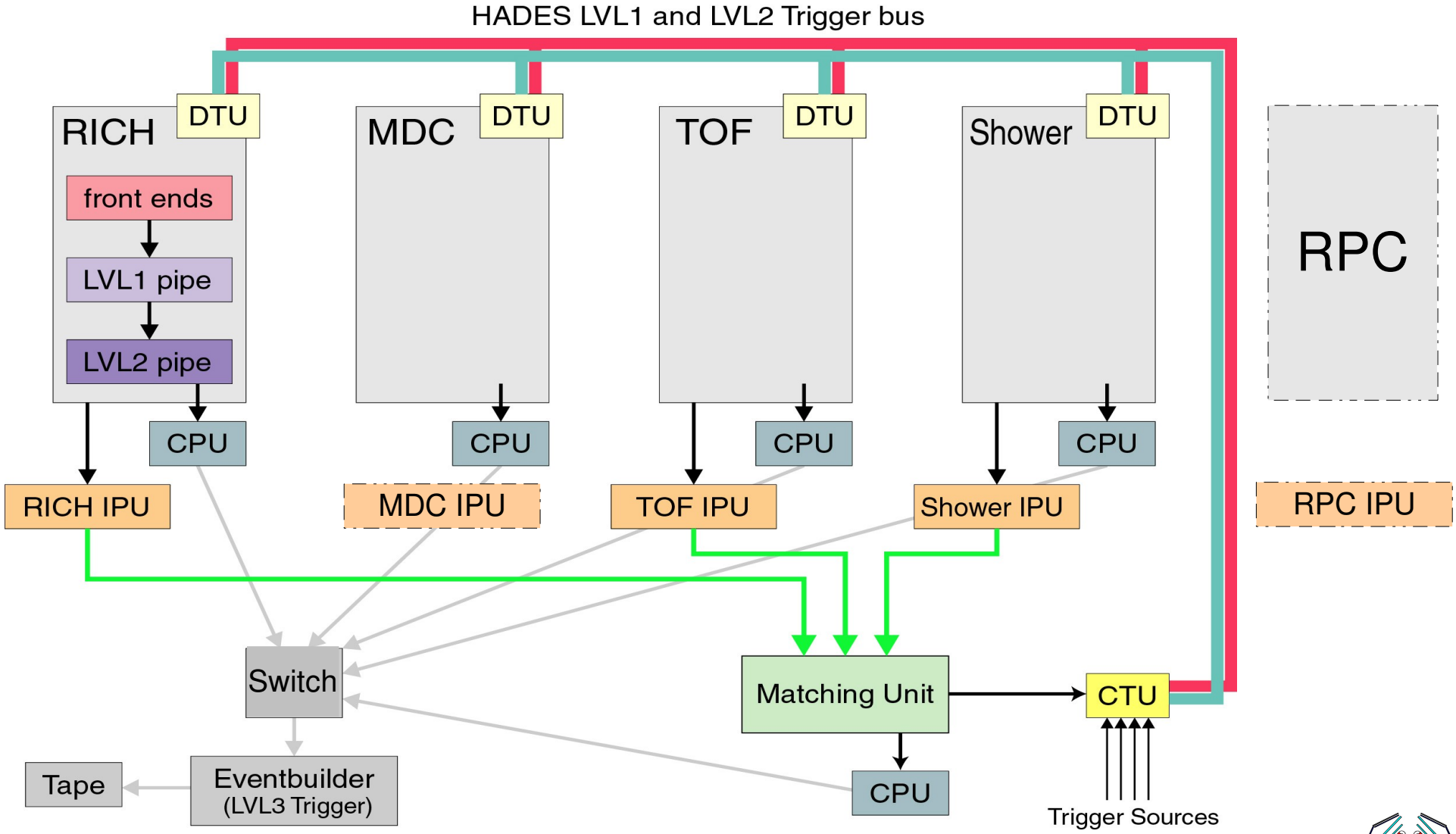
- Consists of approx.
  - 120 VME-modules
    - 70 custom-built
  - several hundred of digital/mixed-signal FEE boards with DAQ and trigger functionality
- Raw data rate 3 GByte/s
- Demands efficient LVL2 trigger, done by online feature extraction / pattern recognition

Why do we need an upgrade?

Consequences / Strategy:

- More bandwidth to mass-storage needed
  - New commercial VME-CPUs
- Rebuild necessary custom electronics with available new technology
- More powerful and more selective LVL2 trigger is needed
  - Improve on algorithms
  - Faster IPU-hardware
  - Add new subsystems to LVL2 trigger

Hades DAQ and Trigger- Overview



Investment Summary

Item	costs[k€]
TOF-IPU board production	35
MU board production	10
x86 VME processors	55

Task

- Each Taskleader will give a short presentation regarding the status of the technical work fulfilled, milestones and deliverables reached and information about delays in the workplan of his task.