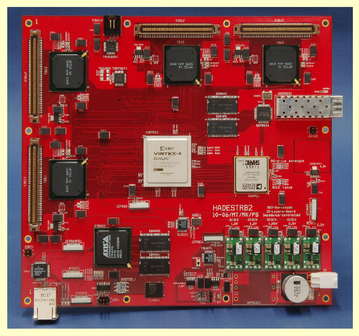
Implementation of a High Resolution Time-to-Digital Converter on a Field Programmable Gate Array

Cahit Uğur[1], Eugen Bayer[2], Nikolaus Kurz[3], Michael Traxler[3]

[1] Helmholtz-Institut Mainz, Johannes Gutenberg-Universität, Mainz, Germany; [2] Department for Digital Electronics, University Kassel, Kassel, Germany;
[3] GSI Helmholtz Centre for Heavy Ion Research, Darmstadt, Germany;

Motivation

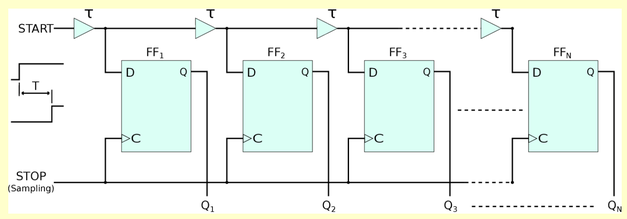
- to have high channel density, high resolution, low power, lower costs;
- to replace ASIC based TDCs (HPTDC) on the previous board, thus remove dependencies on availability of the ASIC-TDCs;
- to provide more flexibility in the design and provide solutions for different requirements;
- to provide different measurement capabilities with different addon boards, e.g. ToF, ToT, Q2W, etc.;
- to use in different experiments, e.g. HADES, PANDA, CBM, etc.



TDC Readout Board (TRBv2)
Photo by Gaby Otto, GSI Darmstadt, 22.12.2006.

Method Used

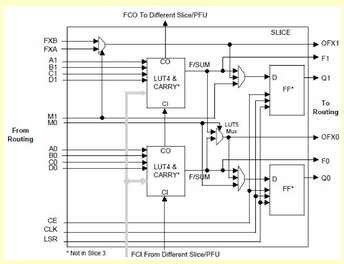
- A delay line composed of ***N* delay elements** is used
- Each delay element has a **propagation delay of *τ***
- Required delay elements: ***N = Measurement Range / τ***
- The propagation starts at the rising edge of the ***START*** signal
- The situation of the delay line is **sampled** with the ***STOP*** signal
- Measurement result: ***T = n * τ***
- Very short conversion time



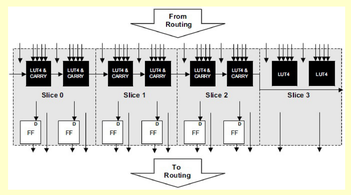
Tapped Delay Line Method
J. Kalisz, Review of methods for time interval measurements with picosecond resolution, Metrologia, 2004.

Implementation

- Smallest programmable elements of an FPGA, Look Up Table (LUT), are used as delay elements
- LUTs and the dedicated carry chain line in the FPGA form the delay line
- System clock is used as the *STOP* signal and state of the delay line is sampled in the registers
- @200 *MHz*, 5 *ns* measurement range, minimum ~245 delay elements needed



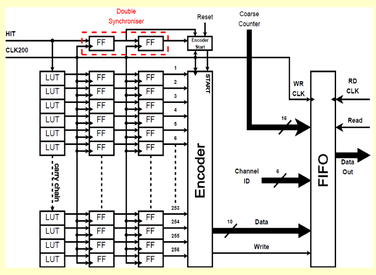
Slice diagram of Lattice FPGA
LatticeECP2/M Family Handbook, HB1003, Version 04.3, March 2009.



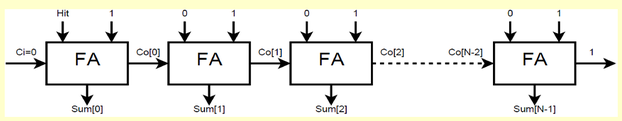
Programmable Functional Unit of Lattice FPGA
LatticeECP2/M Family Handbook, HB1003, Version 04.3, March 2009.

Architecture of TDC

- LUTs are programmed as Full Adders
- Hit signal starts the propagation along the delay line
- System clock samples the state of the delay line
- Encoder is used to convert the result to binary number
- Results are saved in memory (FIFO) with a time stamp from coarse counter with 5 ns granularity



Architecture of a TDC channel

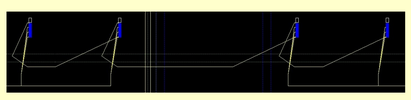


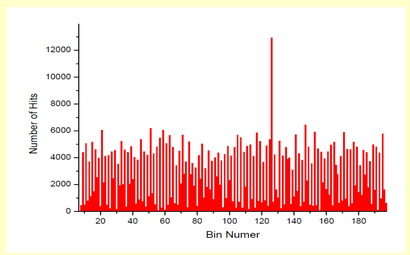
Delay line created by a chain of Full Adders
J. Song et al., A high-resolution time-to-digital converter implemented in field-programmable-gate-arrays, IEEE TRANSACTIONS ON NUCLEAR SCIENCE, 2006.

Effects of FPGA Architecture

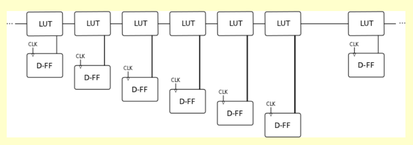
The resolution of the TDC highly depends on the uniformity of the propagation delay between the delay elements → **GREAT** care with placement is necessary!

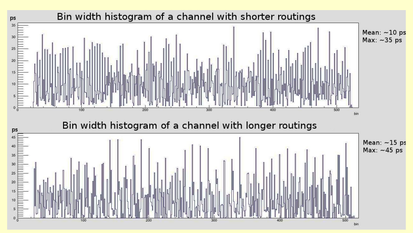
Large propagation delays between the PFUs cause ultra wide bins (UWB)



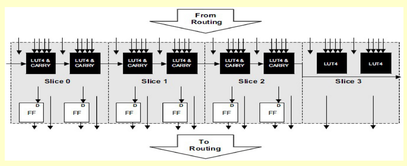


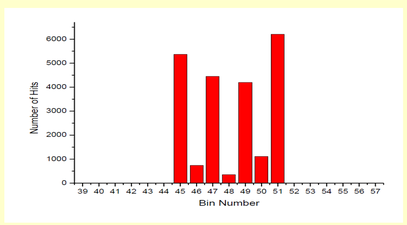
Non-uniform routing between some LUTs cause some wider and empty bins





Routing architecture causes non-uniform bin pattern, which cannot be avoided

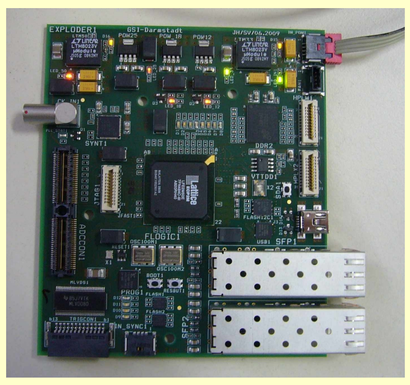




Test Results

Test Setup

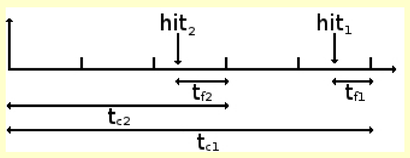
- Lattice ECP2M50E FPGA with 50K LUT is used for tests
- 16 channels are implemented in the FPGA
- System runs at 200 *MHz*
- Measurement results for 1 clock cycle (5 *ns*) are presented



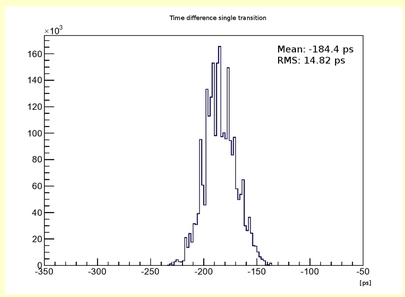
Test board - EXPLODERv1

- Fixed time interval created by using different cable length
- Time difference between 2 channels is calculated as:

$$\Delta t = (t_{coarse1} - t_{coarse2}) - (t_{fine1} - t_{fine2})$$



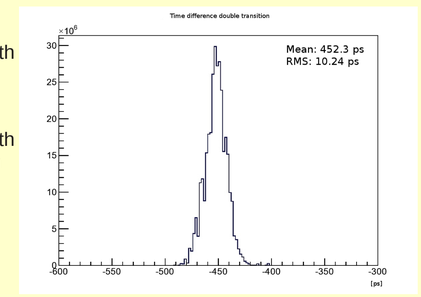
Time Interval Measurements



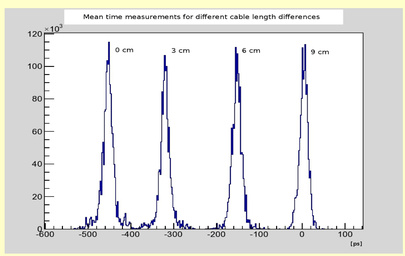
Time resolution with single transition 14,82 *ps* RMS

Time resolution with double transition 10,24 *ps* RMS

Factor of √2 improvement



Mean Time Measurements



Shift of mean for different time intervals

Important Parameters

16 Channels

Average bin width ~10 *ps*

Max bin width 30 *ns*

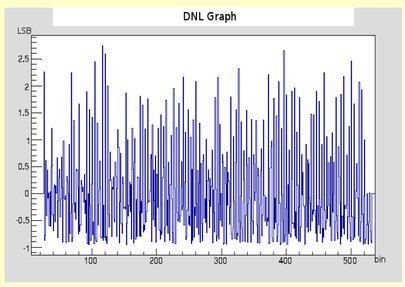
Max conversion time 45 *ns*

Time resolution ~11 *ps* RMS

Resource consumption 20 000 LUTs

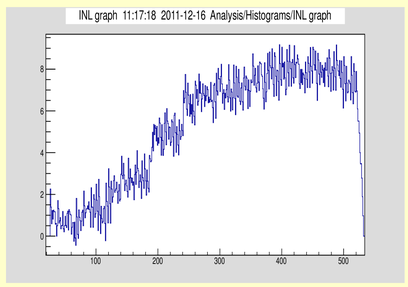
Dead time 30 *ns*

Non-Linearity Measurements



DNL
-0,96 – 2,74 LSB

INL
-0,5 – 9 LSB

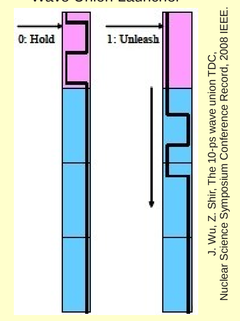


Wave Union Launcher

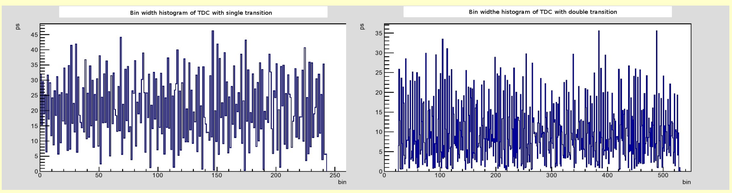
- Ultra wide bins cause lower resolution
- With the wave union launcher two measurements are done for the same hit signal, thus increasing the sensitivity
- A wave is unleashed with an incoming hit signal
- The location of the edges are calculated
- The change in the bin widths with the method:

max. bin width: 45 *ps* → 35 *ps*
avg. bin width: 20 *ps* → 10 *ps*

Wave Union Launcher



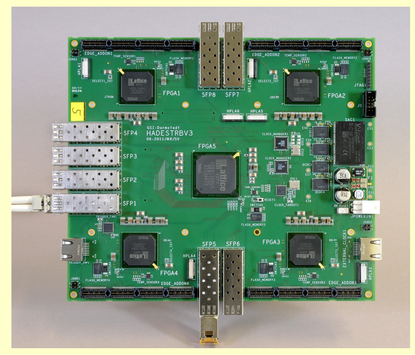
J. Wu, Z. Shi, The 10-ps wave union TDC, Nuclear Science Symposium Conference Record, 2008 IEEE.



New Development

TRBv3

- 256 channels on board (planned)
- ~11 *ps* RMS time resolution
- Different front end electronics possible with addon boards
- Readout on board
- Will be used for Hades, PANDA, CBM, etc.
- Compared to TRBv2 with ASIC-HPTDC from CERN, 3 times higher resolution for 1/3 of the cost per channel



TDC Readout Board (TRBv3)
Photo by Gaby Otto, GSI Darmstadt, 29.09.2011.

50. International Winter Meeting on Nuclear Physics, Bormio (Italy)
23-27 January 2012

Contact

Cahit Ugur

Helmholtz-Institut Mainz
Johannes Gutenberg-Universität

D-55099 Mainz / Germany