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INTERNATIONAL PHD PROJECTS IN APPLIED NUCLEAR PHYSICS AND INNOVATIVE TECHNOLOGIES

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Gigabit Ethernet status and data transport on TRBv3

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Outline

1. Gigabit Ethernet in HADES

- 2. TrbNet
- 3. TRBv3
- 4. TrbNet-Over-GbE
- 5. Bi-Directional Ethernet
- 6. Summary

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Gigabit Ethernet in HADES



- UDP over GbE used to send collected data to Event Builders
- Implemented on concentrator boards (HUBv2) and detector specific (Shower, MDC)



Gigabit Ethernet in HADES

Layered structure

- GbE Buffer HADES specific interface and data buffer
- Packet, Frame Constructors UDP packets construction
- Frame Transmitter, IPCores Gigabit Ethernet, media access

Implemented on Lattice ECP2M FPGAs

- Uses 2 IPCores: Tri-Speed MAC and SGMII/GBE PCS
- Platform independent upper layer
- Ressource utilization for full entity:
 - 6k LUTs (6% for ECP2M100)
 - ~150kB RAM (26% for ECP2M100) (without GbE Buffer ~80kB)

Performance

- Full entity maximum throughput 50MBps
- UDP construction only throughput 98MBps
- For full entity, the speed can be augmented in trade of RAM consumption
- No packet/frame loss or rejection due to corrupted construction





Gigabit Ethernet in HADES

HADES specific interface (GbE Buffer)

- Construction of Hades Transport Unit Queue
 - Queue consists of several subevents
 - Subevent can contain data from several endpoints
 - Uneven subevent size requires buffering
 - Drop in performance
- Event builder selection mechanism

UDP construction

- Packet sizes up to 64kB
- Packet fragmentation into Ethernet frames of up to 9kB (Jumbo frames)
- Checksum calculation
- No need for ARP in HADES case (only uplink)
- All parameters are register-configurable

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Media access

- Realized by IPCores
- Autonegotiation
- Link state control
- Conversion to 8b/10b









TrbNet

- 3 logical channels (priority):
 - LVL1 trigger
 - Data transport
 - Slow control
- Endpoint addressing scheme
 - Broadcasts
 - Unicasts
- Media independent
 - Optical links
 - LVDS lines
- Packet retransmisson
- Performance:
 - 75% of network bandwidth
 - for 2Gbps using 8b/10b encoding data rate of 1.2 Gbps

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TRBv3

- Key features:
 - 5x Lattice ECP3 150
 - 4x for TDC or other purpouse
 - 1x main control
 - > 8x 3.2 Gbps SFP
 - Multiple protocols
 - 4x 208 pin connectors
 - Input lines for TDC-in-FPGA
 - Connectors and power supply to small Addon Boards
 - 1x regular Addon connector

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No ETRAX!



TRBv3 with small AddOns to cope with many applications.



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TrbNet Over GbE

- Main idea:
 - No ETRAX on board
 - TrbNet endpoint on each FPGA

Control the board via Ethernet using TrbNet



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Bi-Directional Ethernet



- Reuse old components: packet/frame construction and transmission, TrbNet interface
- New elements: frame receiver, flow controllers, response constructor(s)
- Still pure VHDL logic (except media access)
- Without GbE Buffer Full featured, full-speed, multiprotocol Ethernet endpoint

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Bi-Directional Ethernet

Address assignment

- Empty registers after reboot no access from outside
- Temperature sensor with unique ID on each board (not MAC address)
- TRB DHCP
 - By default no address filtering on endpoints
 - Address mapping table on server
 - 1. Board sends request with its unique ID
 - 2. Server responds with broadcast message containing matching addresses
 - 3. One board accepts
 - 1. Saves the addresses
 - 2. Sets up filtering
 - 4. Others drop the message
- ARP needed for larger systems

Bi-Directional Ethernet

Status



Done:

- Test setup: injection of received frames into output stream
- Most of the connection handling in two directions

Still to develop:

- Addressing mechanism
- Higher level protocols implementations

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Summary

- UDP and Gigabit Ethernet implementation successfully used in HADES
- TRBv3 new possibilities and new challenges
- TrbNet-Over-GbE forces the development of Bi-Directional Ethernet implementation
- Project in development first results are present

