DAQ Status and Upgrades

Outline

- **Status**
  - Preparations for Beamtime May 2006
  - Things to do
- **Upgrades**
  - Why?
  - EU-Contract
  - TRB, Readout and IPU-boards
  - Trigger Distribution

Status DAQ / Trigger

- No known **new** problems since Sep05
- Changes / Improvements
  - new VME-CPUs in all subsystems but RICH
    - 3-4 times faster readout
    - no big effect for light systems expected (more downscaled data)
  - TRB readout of Hodoscope in beam-transfer-line integrated into DAQ
    - stably running at:
      LVL1: 30 kHz
      LVL2: 10 kHz (with data!)

Status DAQ / Trigger II

- Expected rates for beamtime:

	max LVL1	max LVL2	LVL2 trigger downscaling factor
pulser rate	17 kHz	4-5 kHz	10-20
in beam rate	8-6 kHz	1-3 kHz	10-20

- Stability issues:
  - Last experiment with light system: aug04
    - higher LVL1 rates
    - TOF ?
    - RICH -> IPU -> MU link ?
  - no signs of new problems while testing with pulser
    - not 100% realistic, thresholds, data-fluctuations

Status DAQ / Trigger, Things to do!

- Full System integration
  - MDC, new chamber
- DAQ-Runcontrol, DAQ-Monitoring, Online Monitoring (P. Zumbruch): Saturday 9^{00}
- Detector-data still ok?
  - RICH thresholds, Shower Thresholds
  - ....
- Cosmic Rays Run: scheduled 24^{th} to 28^{th} of April
  - With all detectors set to running condition
- Data has to be checked carefully by sub-detector responsibles as early as possible to have time to react when problems occur.

Upgrades / Why?

- DAQ/Trigger does not perform for heavy systems
  - Statistics of our experiments is not good enough
- Rates during last beamtime sep05 Ar+KCl

	max LVL1	max LVL2	LVL2 trigger downscaling factor
beam rate	3-4 kHz	1-2 kHz	around 3

- **Reasons I:**
  - Micro-Spill-Structure of beam costs about factor of 2
  - The limitation of the LVL1 rate in hardware
  - bad LVL2-Trigger reduction value (saturates LVL2)
    - Charged particles from upstream sources in RICH
    - Photon-efficiency of RICH detector, noise
      - RICH-patterns are essential for performance of LVL2 trigger

Upgrades / Why? II

Reasons II:

- **Maintainability**, operating:
- Aim (quoting Herbert): „3 people have to be able to run a HADES shift!“
  - needs much more stable DAQ-system
  - thresholds of detectors have to be more stable
- We need a scalable system for future extensions

Upgrades / Measures

Consequences / Strategy:

- More bandwidth to mass-storage needed
  - New commercial VME-CPUs (W. Kühn)
- Rebuild custom electronics with available new technology, make it a **scalable** system
  - (many small and „cheap“ boards)
- More powerful and more selective LVL2 trigger is needed
  - Improve on algorithms
    - ideas: Ring fitting instead of ring-matrix?
  - Faster IPU-hardware for more complex algorithms
  - Add new subsystems to LVL2 trigger
    - MDC tracks

List of Projects in DAQ

MU	TOF	Common Readout	MDC	RICH	RPC
Matching Unit Concentrator	Replacement TOF readout-board	Replacement of old VME-CPUs	Higher bandwidth digital readout electronics	New digital readout for lowering electronic noise in the RICH detector	TDC-board with readout
Matching Unit Version 2	more powerful TOF-IPU	Parallel working Eventbuilders	Integration of track information to LVL2 trigger	More powerful IPU for lower fake-rate	IPU for RPC

FP6 DAQ project

Aim: accept 20 kHz primary data rate to ensure measuring rare decays in heavy systems

Who is paying for these projects?

Upgrades / EU

EU-FP6 Construction Contract

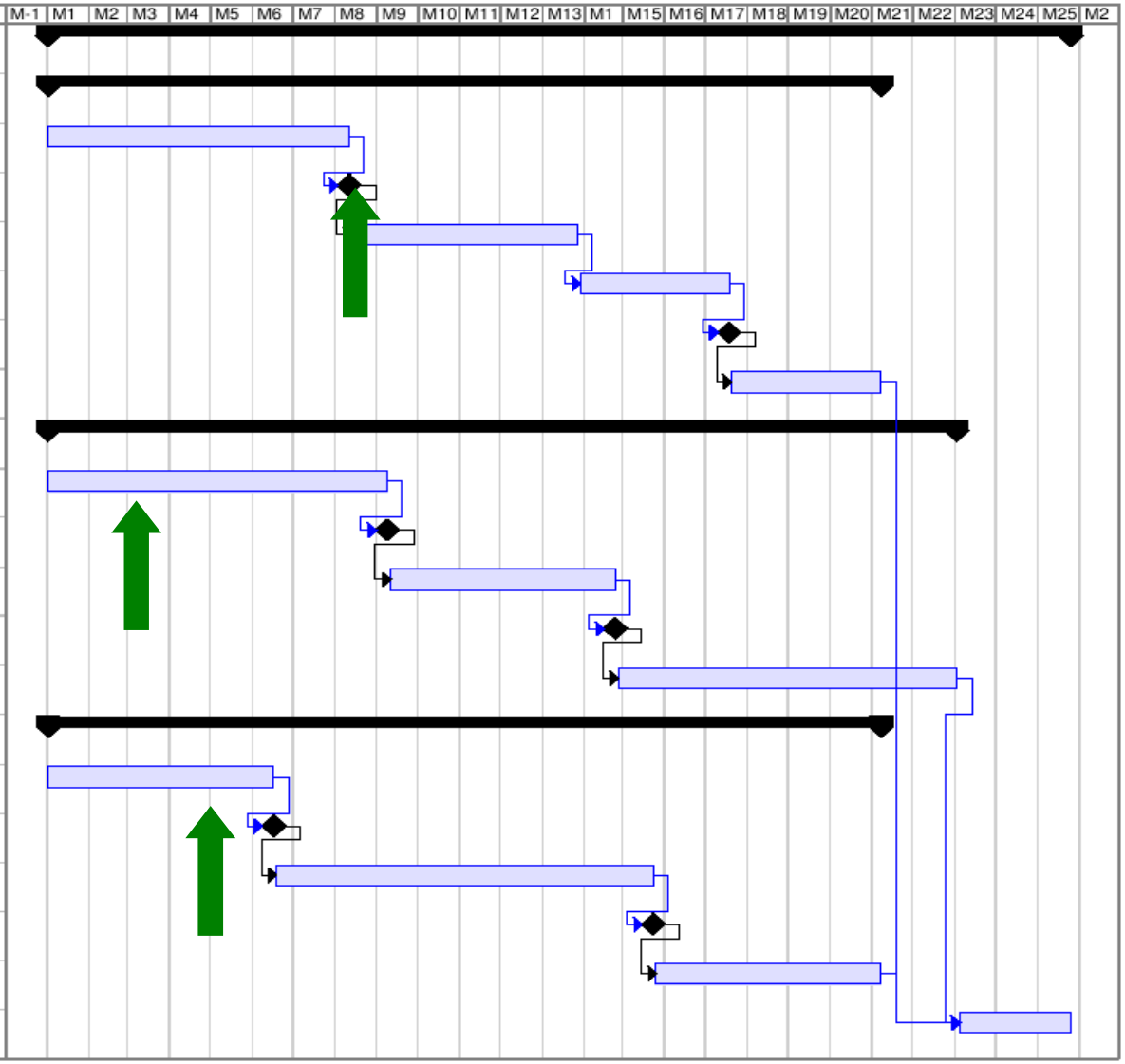
- Resistive Plate Chamber / **RPC**
  - Timing (Time of Flight)
  - correction with amplitude (walk correction)
- Forward Wall
- DAQ-Upgrade
- Pion Hodoscopes

BMBF (Bundesministerium für Bildung und Forschung)

- MDC Readout / Trigger (Frankfurt)
- RICH Readout / Trigger (München)
- LVL2 Compute Node, Trigger Board (Gießen)

Milestones EU-FP6 contract

ID	Vorgangsname	Duration
1	**HADES 3 (DAQ)**	**540 dys**
2	**CPU upgrade**	**440 dys**
3	VME-CPU replacement	8 mons
4	*HAD-3-M2*	*0 dys*
5	Database interfaces	6 mons
6	Eventbuilder	4 mons
7	*HAD3-M5*	0 dys
8	Integration	4 mons
9	**TOF readout**	**480 dys**
10	Read-out board	9 mons
11	*HAD-3-M3*	0 dys
12	IPU implementation	6 mons
13	*HAD-3-M4*	0 dys
14	Integration	9 mons
15	**Matching unit upgrade**	**440 dys**
16	Implementation BIOS	6 mons
17	*HAD-3-M1*	0 dys
18	Implementation of algorithm	10 mons
19	*HAD-3-M6*	0 dys
20	Integration	6 mons
21	Full system commissioning	3 mons



DAQ-Upgrade / Synergy

Synergy

- One common platform for readout of detector data
- One common way of distributing IPU data downstream to the Matching Unit
- New digital-trigger distribution for scalability

Advantages of this approach

- Saves development **time** (manpower) and **money**
- Easier/**possible** to maintain, debug
  – distributed knowledge

- *Shows that we can learn from experience* :-) *!*

DAQ-Upgrade / Synergy II

Is it possible to use one platform?

- Very similar FEE and DAQ/Trigger tasks
  - RPC
  - Forward-Wall
  - Pion-Hodoscope
  - TOF (needs new FEE!)
- Readout/Trigger can be unified
  - MDC (TDCs stay)
  - RICH (FEE stays, will be exchanged later)
  - Shower(?)

Answer: yes!

But what platform? What do we have already?

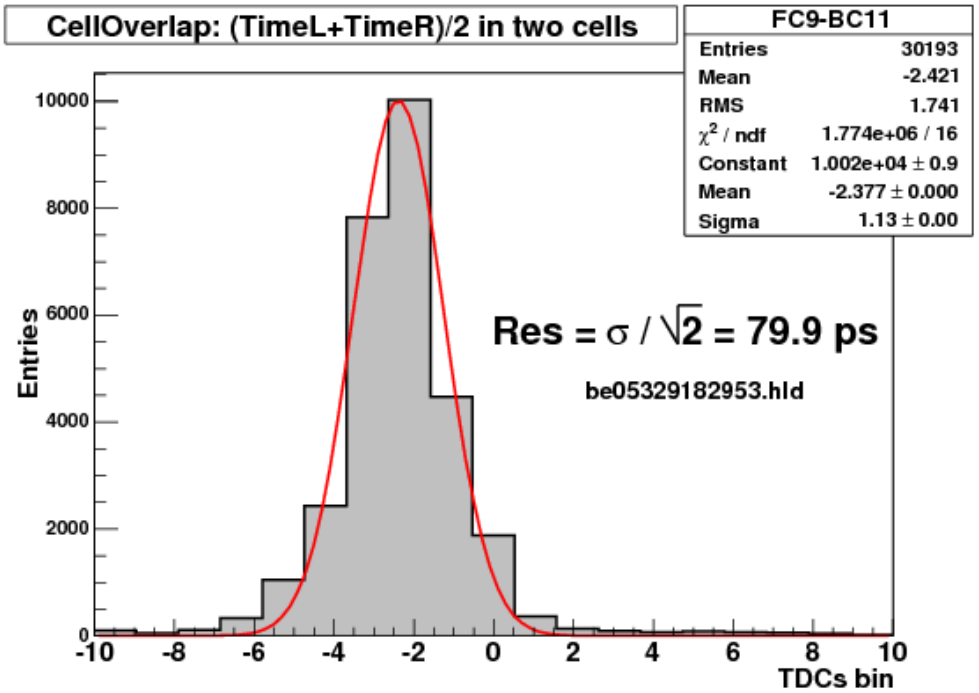
Requirements/Features for RPC

- Time resolution below 60ps
- Purely digital, ADC information is encoded in Time-over-Threshold
  - No delays required, no ADCs needed, HPTDC-ASIC from CERN
- At the detector, short signal cables
- LVL1 and LVL2 pipes at the FEE
- Readout and data transport on one board, **no VME**
- Avoid „*Low Voltage Power-Supply Nightmare*©“ (high currents over long cables: Ohm's Law, Inductive-effects)
  - 48V DC/DC, telecom standard
- Data Reduction/Feature extraction on the same board

➡ One fits for many!

TDC/Triggered Readout Board, TRB, Results I [1]

- Project of a larger team, very complex, time-consuming
- Concept is accepted and working: RPC Test Nov 05



[1] M. Traxler , D. Gil, M. Kajetanowicz, K. Korcyl, M. Palka, P. Salabura, P. Skott, R. Trebacz: GSI Report 2006

TRB, Results II

TDC-Resolution

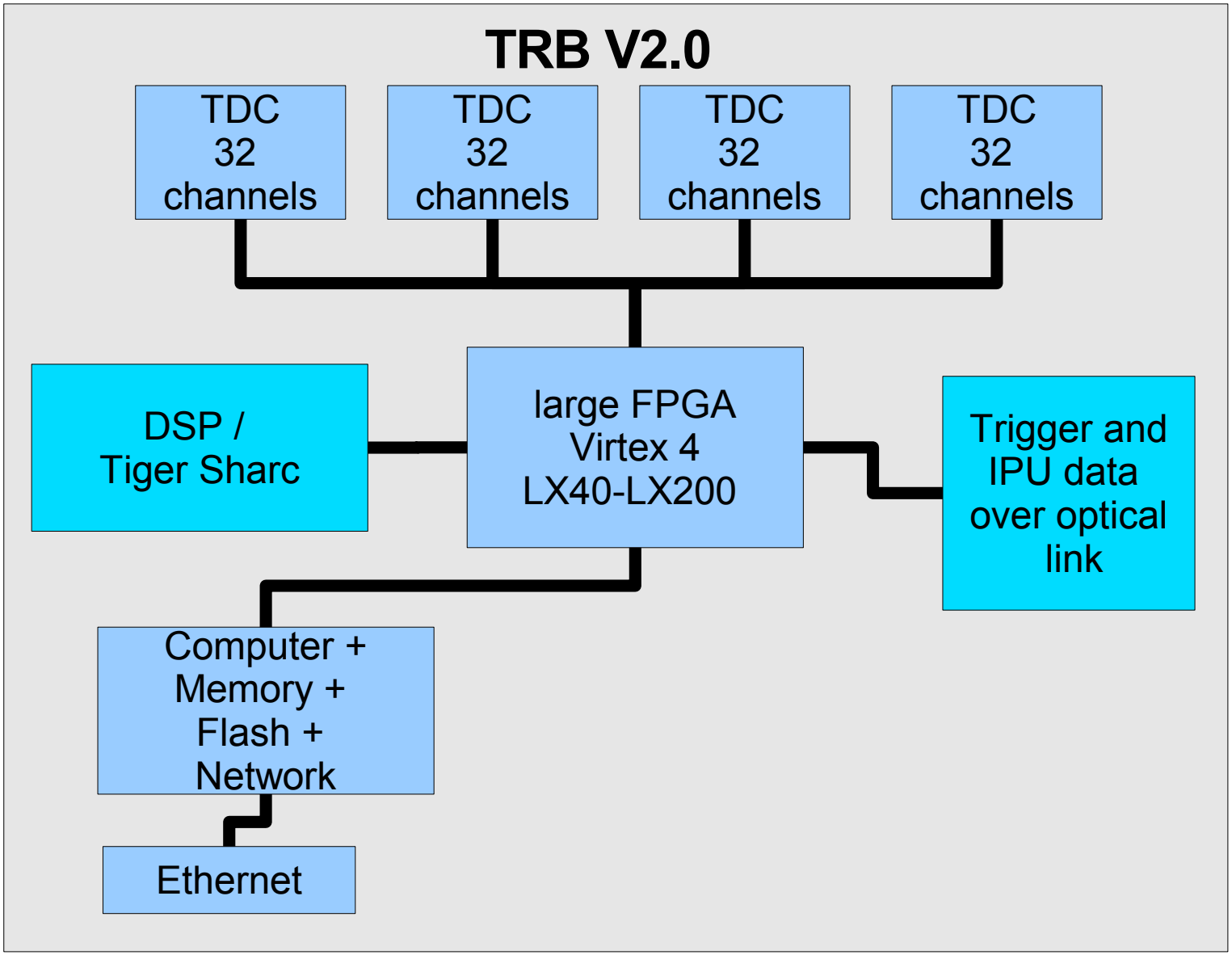
- sigma between 2 channels (4 TDCs): 38ps
- no signs of crosstalk on TRB (has to be verified with more careful measurement)

Performance:

- LVL1 readout of 60 TDC-words/event: 35kHz
- LVL2 readout of 60 words/event: 5-6kHz
- LVL2 readout of empty events: 18-19kHz
- all without DMA, no optimization in FPGA

- Missing: Matching Unit Connectivity

Future/Upgrade: TRB V2



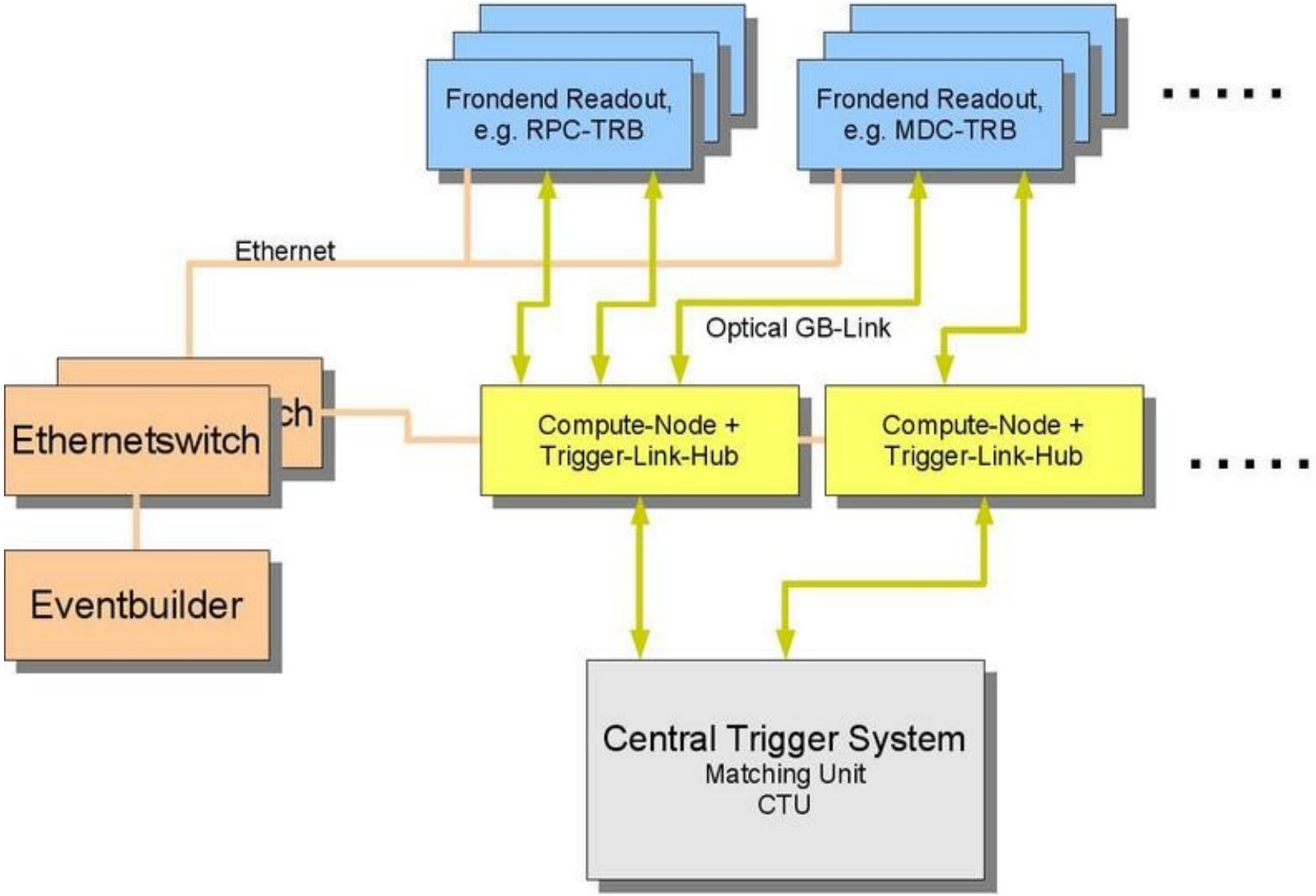
Future/Upgrade: TRB V2

- Additional Features:
  - 2 Gbit optical link for online pattern-recognition data transfer **and** LVL1 and LVL2 trigger information (not timing)
  - 3 times faster CPU (21€/piece)
  - Large FPGA for online pattern-recognition, zero suppression, IPU functionality ....
  - DSP: Tiger-Sharc (TOF-algorithm), optional
  - option: remove TDCs, connectors for readout of:
    - MDC, RICH

➡ One fits for all!

Implications?

DAQ/Trigger-Distribution Architecture



Trigger Distribution

- Tree-Structure (point to point) instead of star (bus)
- IPU data and Trigger-Distribution over one optical 2 GBit/s link
  - low delay needed for trigger-decisions and busy
- Protocol worked out and simulated by Ingo Fröhlich
  - DAQ-Wikipage
- List of advantages over traditional bus architecture:
  - Point-to-point links
  - scalable
  - galvanic decoupling, works over long distances!
  - higher speed (RICH raw data to new RICH IPU?)
  - at the end cheaper than copper

Summary

Beamtime

- Beamtime may06 still needs preparation
  – support needed from detector experts

Upgrade

- EU-FP6 construction contract „DAQ/Trigger Upgrade“ is progressing ahead of schedule
- The other systems (not EU-Upgrade) can/should benefit from the TRB-development
- MDC and RICH DAQ-upgrades as well as Compute-Node for IPUs are planned: application to BMBF
- TOF? TRB or with new VME-CPU-Readout?

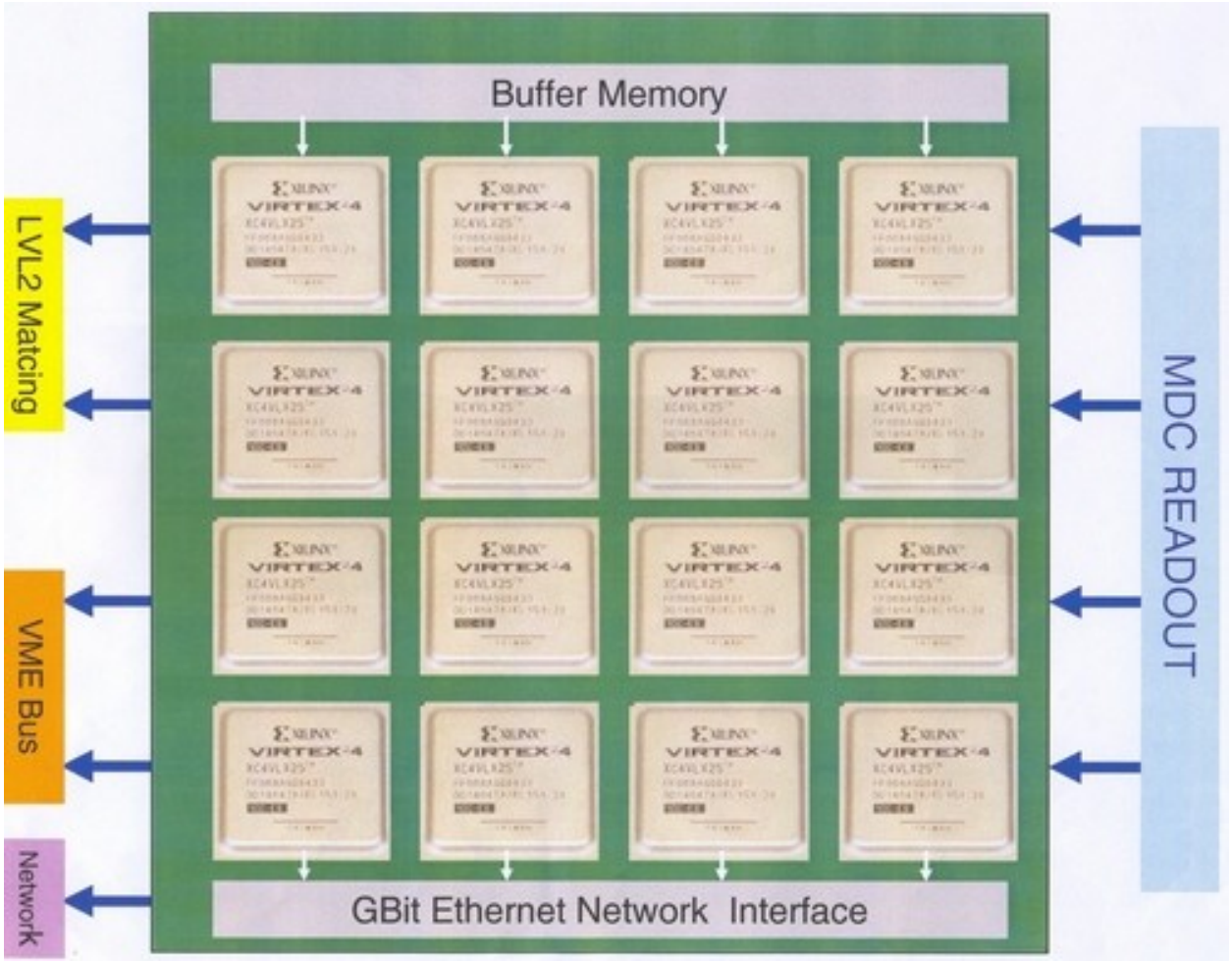
Q&A

- Thank you for your attention!

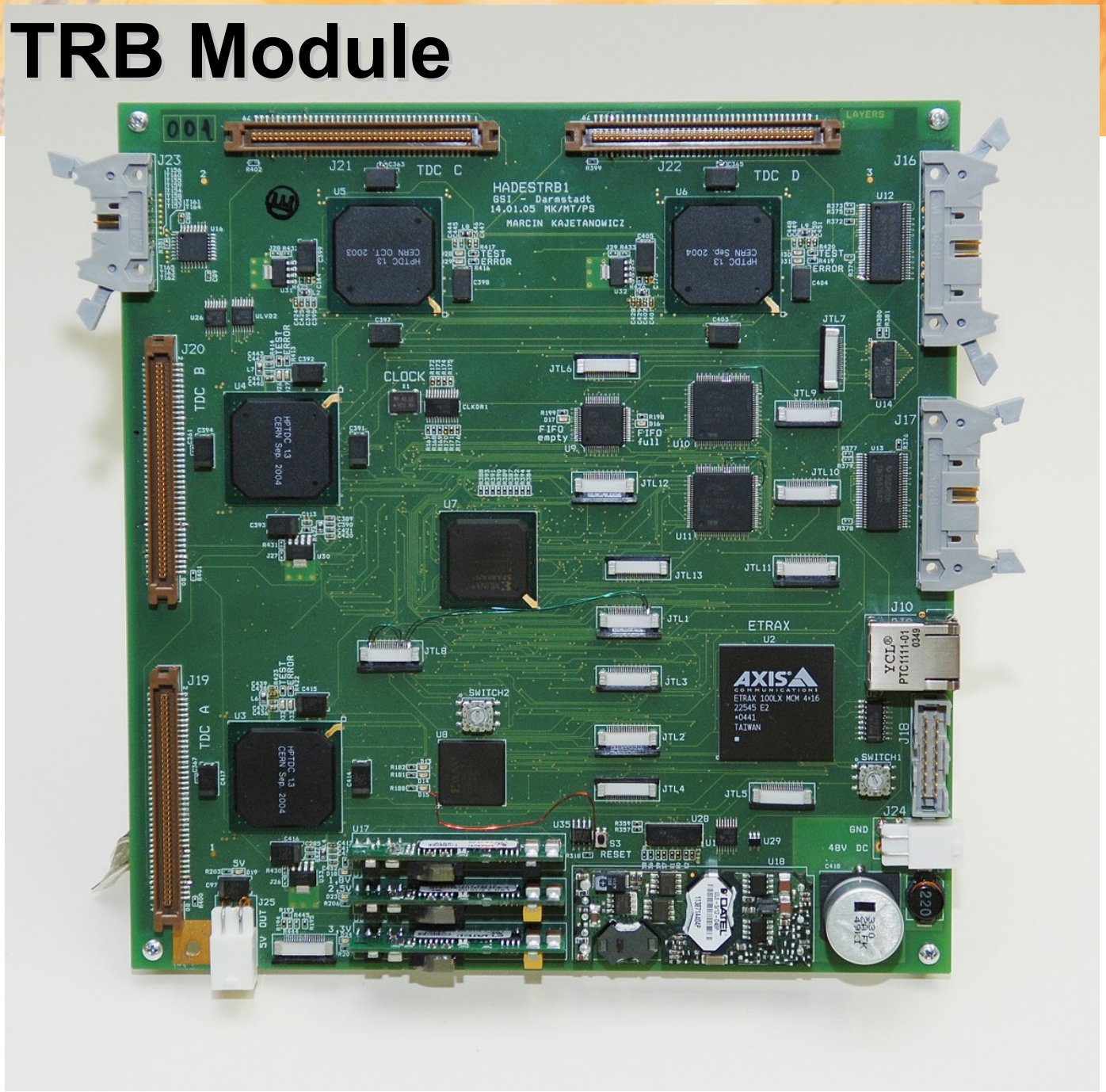
- Q&A

Compute Node, example given

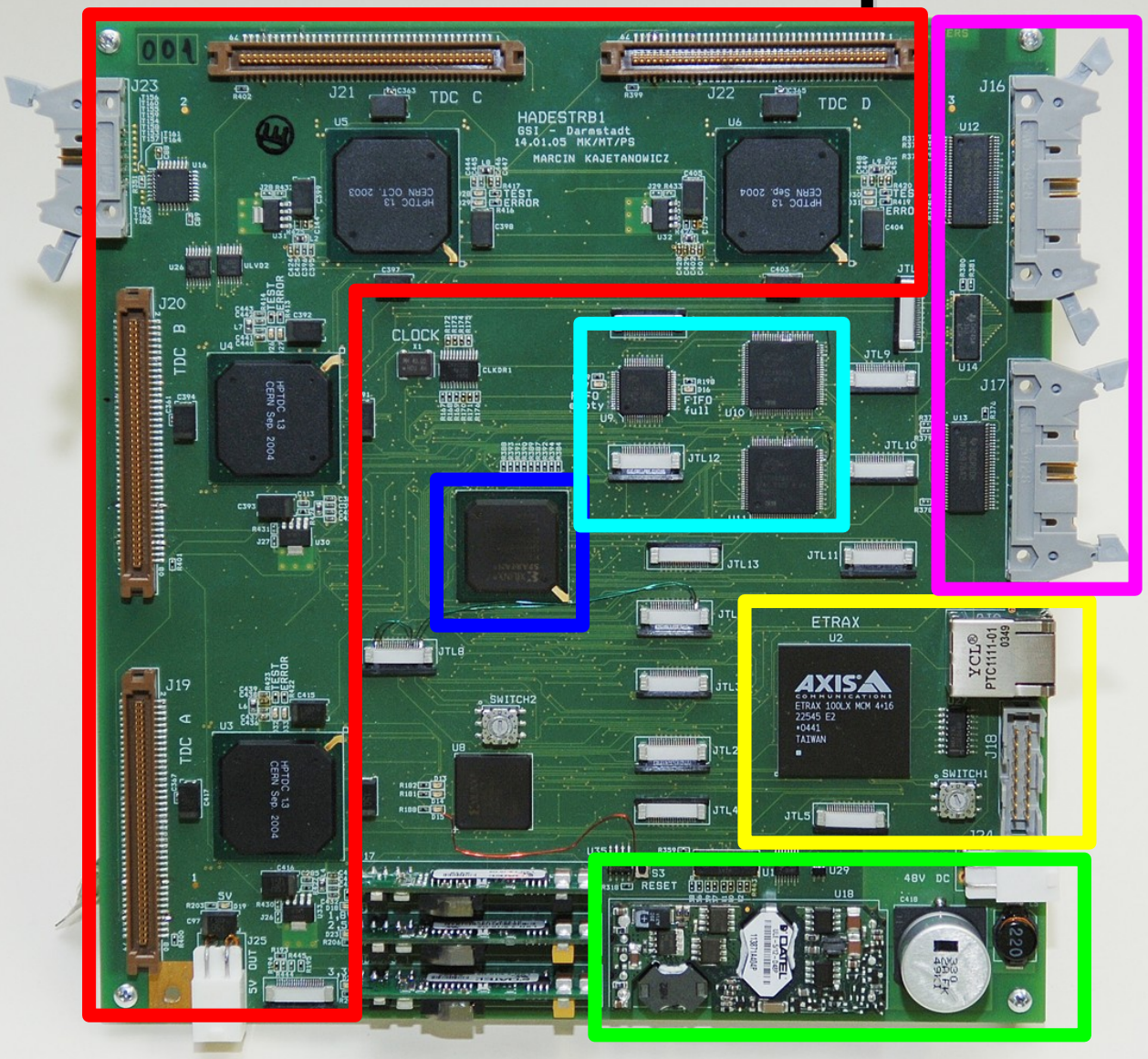
- Compute Node planned by Giessen group



TRB Module


HADESTRB1
GSI - Darmstadt
14.01.05 MK/MT/PS
MARCIN KAJETANOWICZ
J21
TDC C
J22
TDC D
J23
J16
J17
J20
TDC B
J19
TDC A
J10
J18
J24
J25
CLOCK
FIFO empty
FIFO full
ETRAX
AXIS
ETRAX 100LX MCM 4+16
22545 E2
0441
TAIWAN
SWITCH1
SWITCH2
RESET
GND
48V DC
5V OUT
HPTDC 13
CERN Sep. 2004
TEST ERROR

TRB Module and components



- 4*32 channels TDC, HPTDC
- 80 pin twisted pair cable, KEL connector
- Single Chip Computer with Ethernet
- FPGA
- DC/DC 48V, isolated
- Memory

Architecture