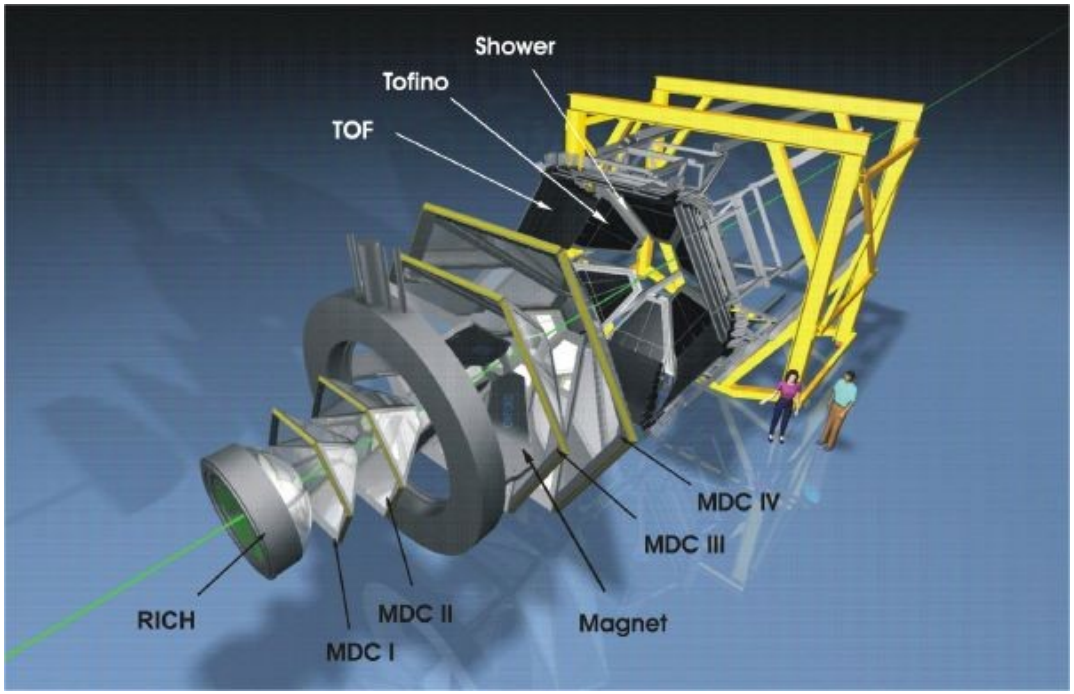
The New Data Acquisition System for The HADES Experiment

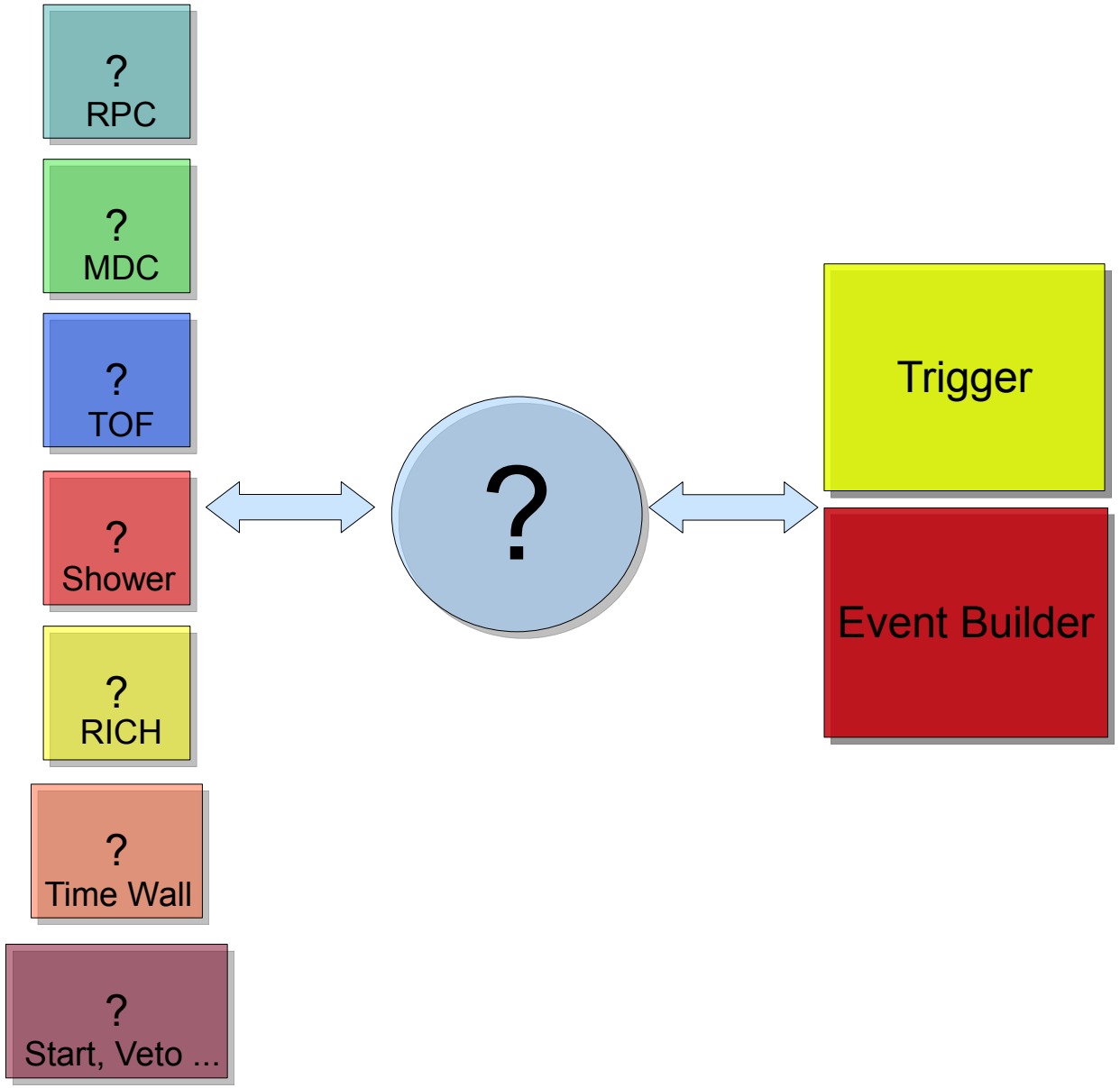


- HADES (High Acceptance Di-Electron Spectrometer) consists of several detectors
- In total 80k front-end electronic channels
- HADES data acquisition system is fully operational
- Successful data taking in medium sized ion systems at 1-2GeV/u, 8kHz primary rate, 3-4kHz readout rate

HADES at FAIR

- Proton and a heavy ion beams (~ up to 200 tracks per event)
- Amount of data: in peak 400 MB/s (150 MB/s mean)
- Primary data acquisition rate of 20 kHz
- This upgrade is ongoing
- Timescale: to be finished at the end of the 2009 year
- Available technology is used
- Limited funding - cheap boards
- Reasonable for the other projects
- DAQ upgrade includes front ends

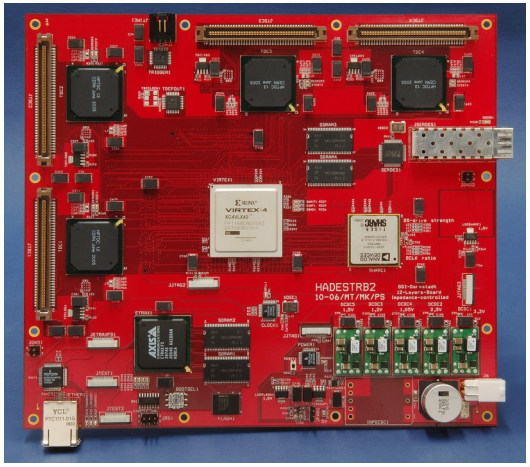
The DAQ System



- New readout electronics for each detector
- New media and protocols for the data transfer and the trigger distribution
- New event builder and a central trigger system(CTS)

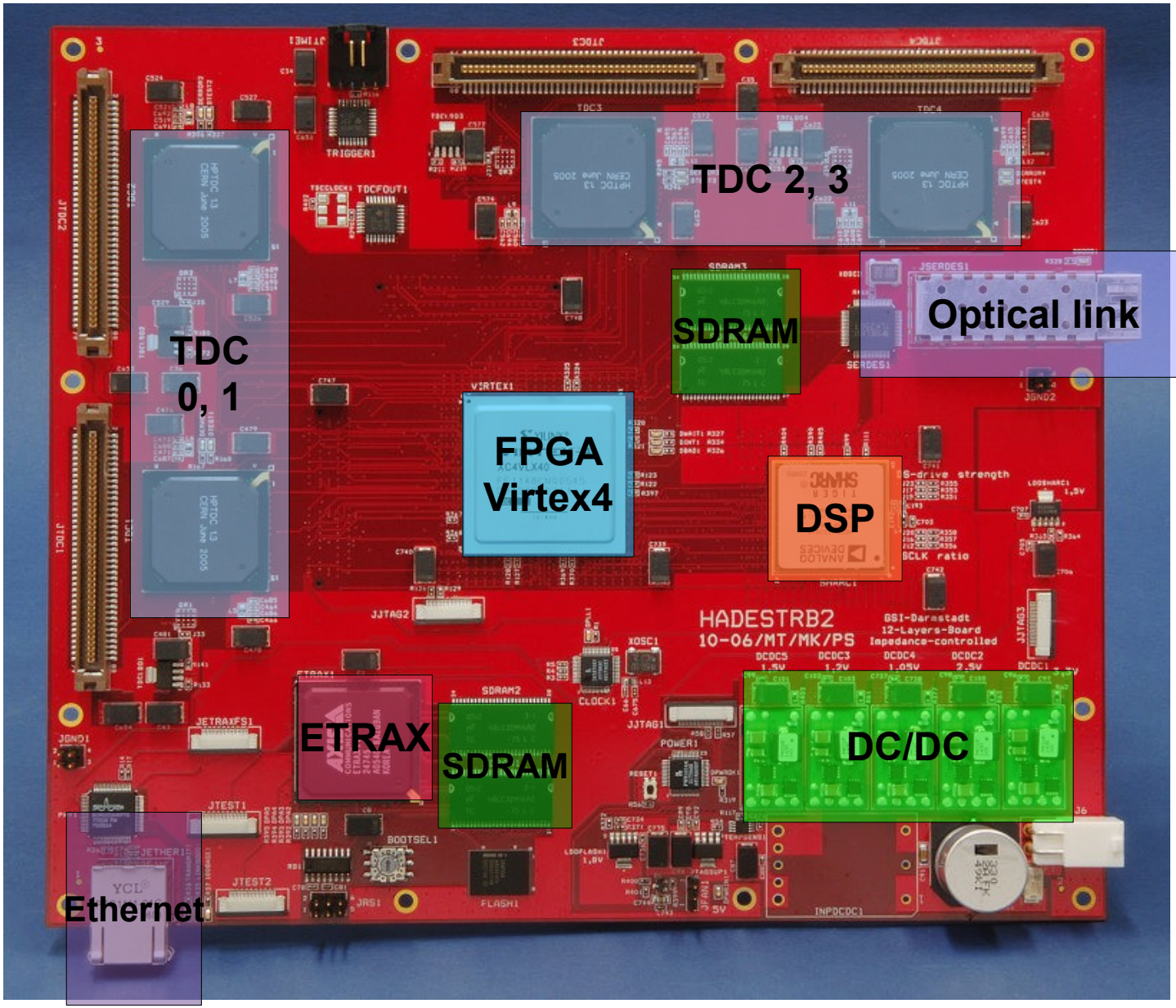
New Concept of The HADES DAQ

- One platform concept
- Stand alone boards (TRBs)
- Pluggable AddOns to TRB
- Tree like structure
- High granularity (~100 TRBs)
- A special network protocol (TRBnet)
- A modular design to increase the scope of applications
- Reduced development effort/time and simplified debugging



The TRBv2 – Trigger and Readout Board

The TRBv2



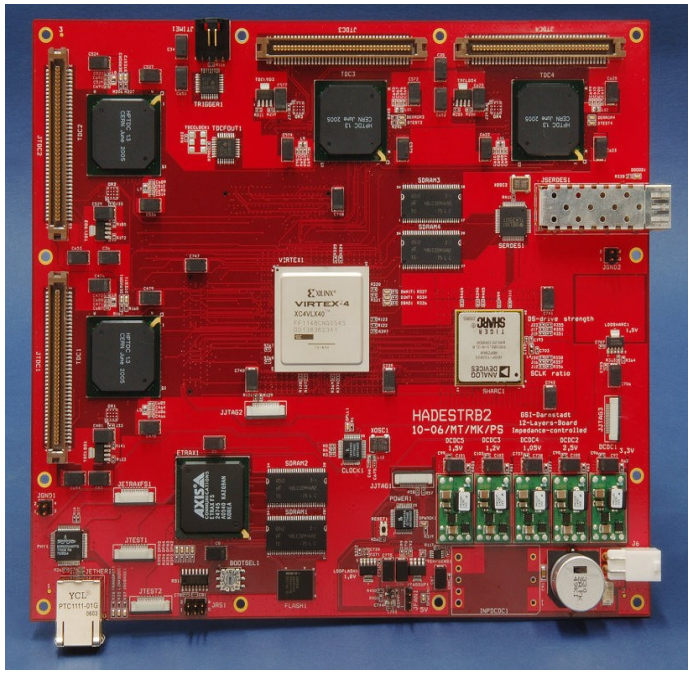
- 4 TDC – 128 channels (~40ps RMS resolution)
- 4x512Mb SDRAM
- FPGA – Virtex4LX40
- ETRAX FS – 4 processors, Linux core
- 100Mb/s,TCP/IP
- 2,5 Gb/s optical link
- DSP TigerSharc
- DC/DC converters
- AddOn connector

The DAQ Hardware

?
RPC

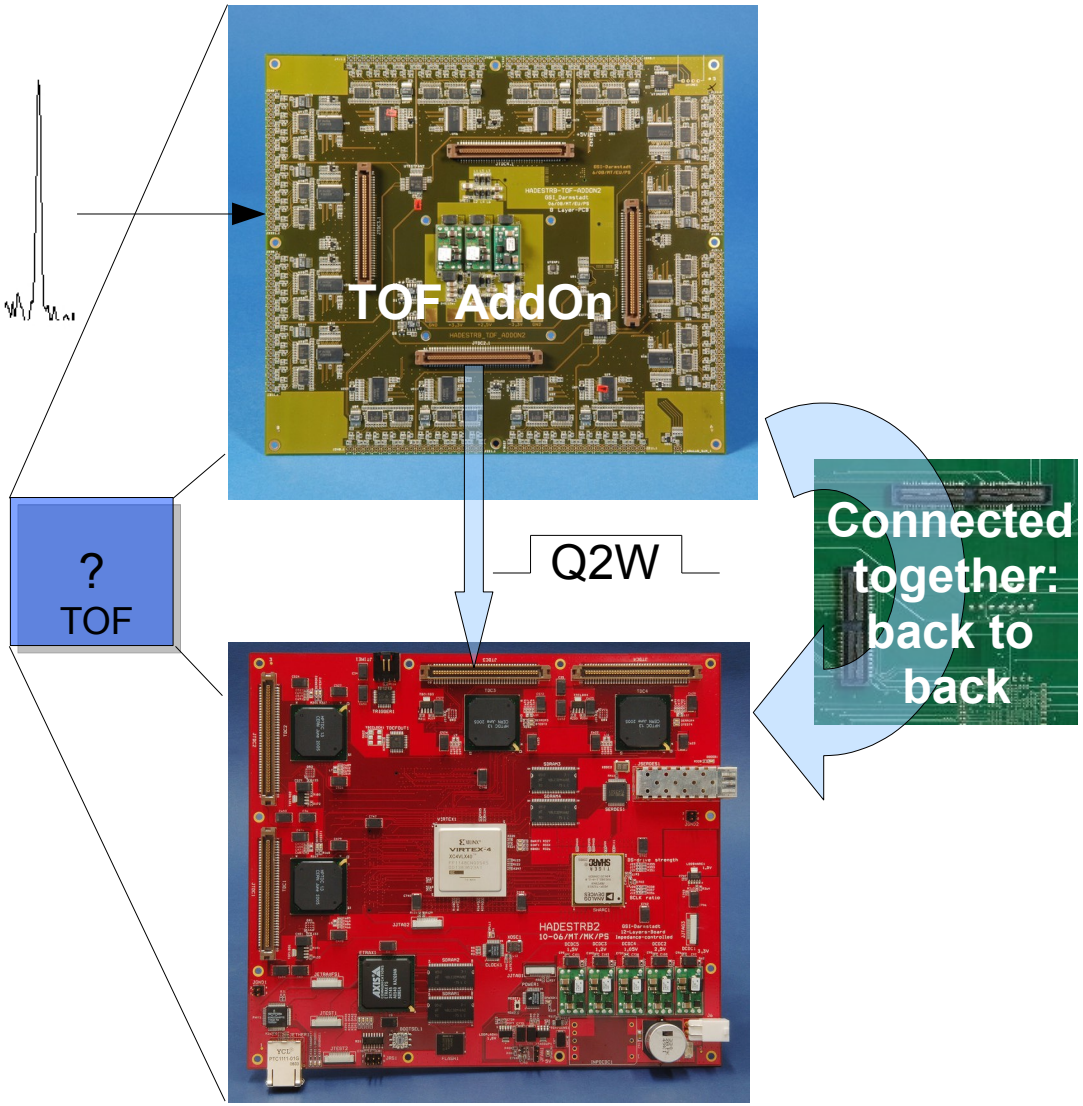
?
Time Wall

?
Start, Veto ...



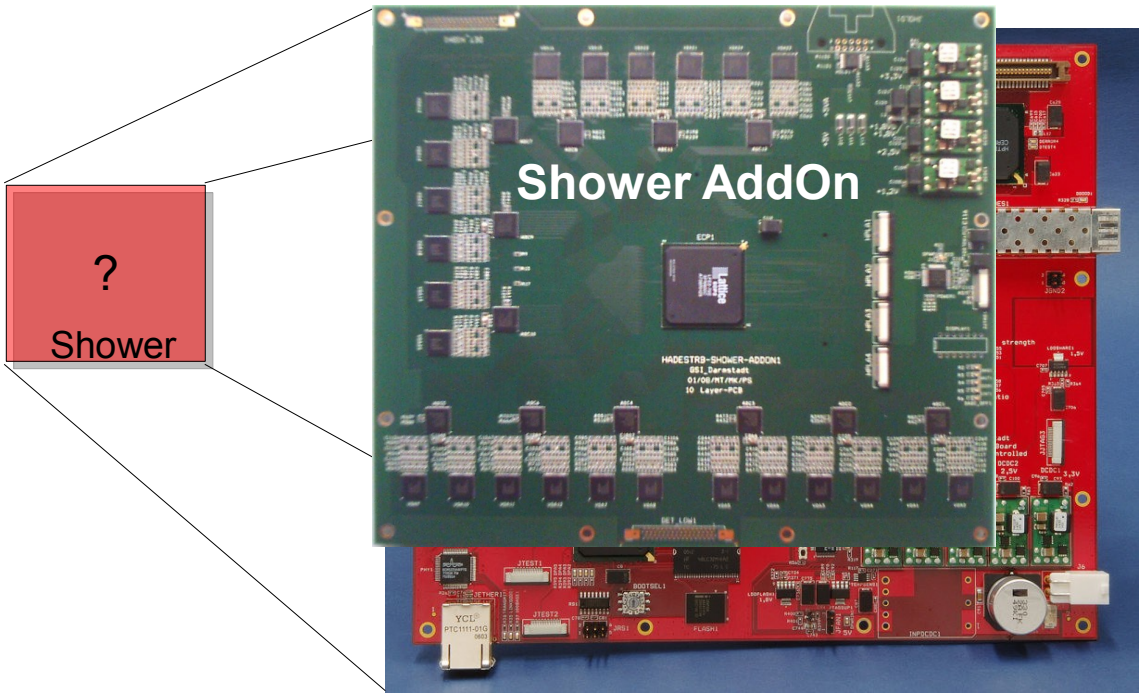
- The TRB reads out the RPC, Time of Flight Wall and beam detectors
- The TRB was successfully used in 3 production beam times

The DAQ Hardware



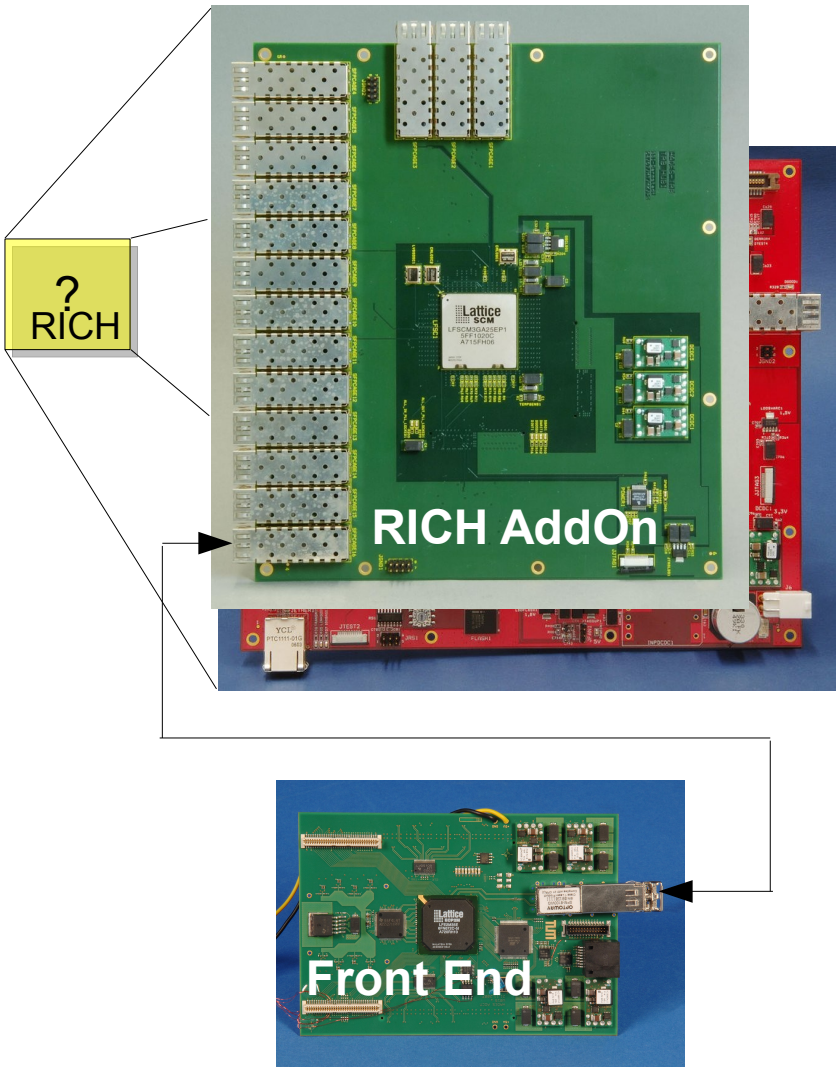
- The TRB gives a power supply and a slow control
- 128 Q2W channels

The DAQ Hardware



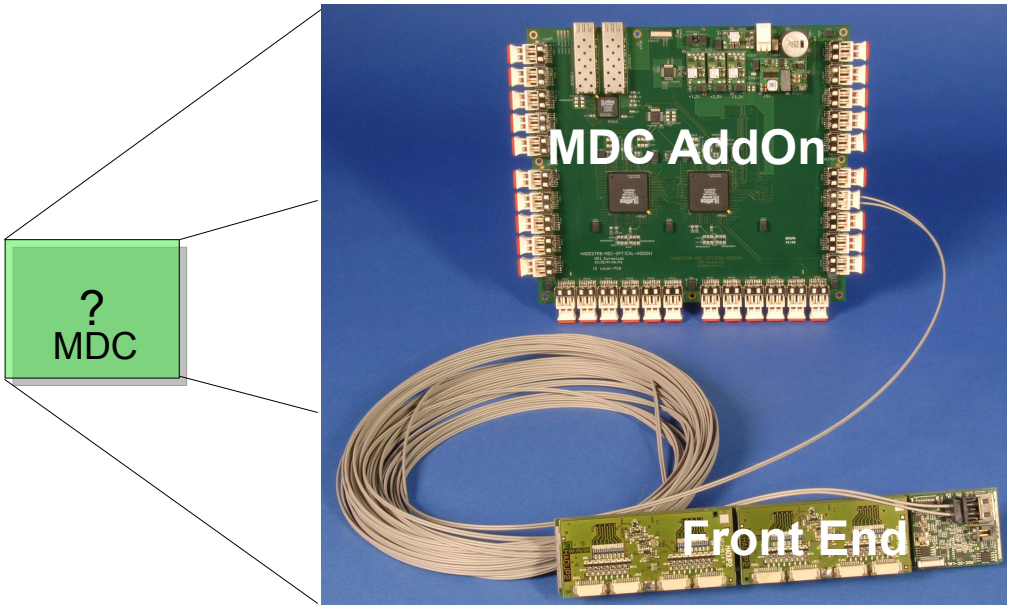
- 96 channels 10-bit ADCs
- 40/60 MSPS
- ADC type: AD9212 from Analog Devices
- FPGA: Lattice LFE2-70E-5F900C

The DAQ Hardware



- FPGA (Lattice SCM 25) with 16 SERDES
- 16 SFPs (Small Form-factor Pluggable transceivers) optical connectors
- receive/transmit 16 * 2Gb/s (4 * 1Gb Ethernet)
- 30k channels
- Front end ADCs comparable with Shower ADCs

The DAQ Hardware



Cheap technology - POF
(Polymer Optical Fiber)

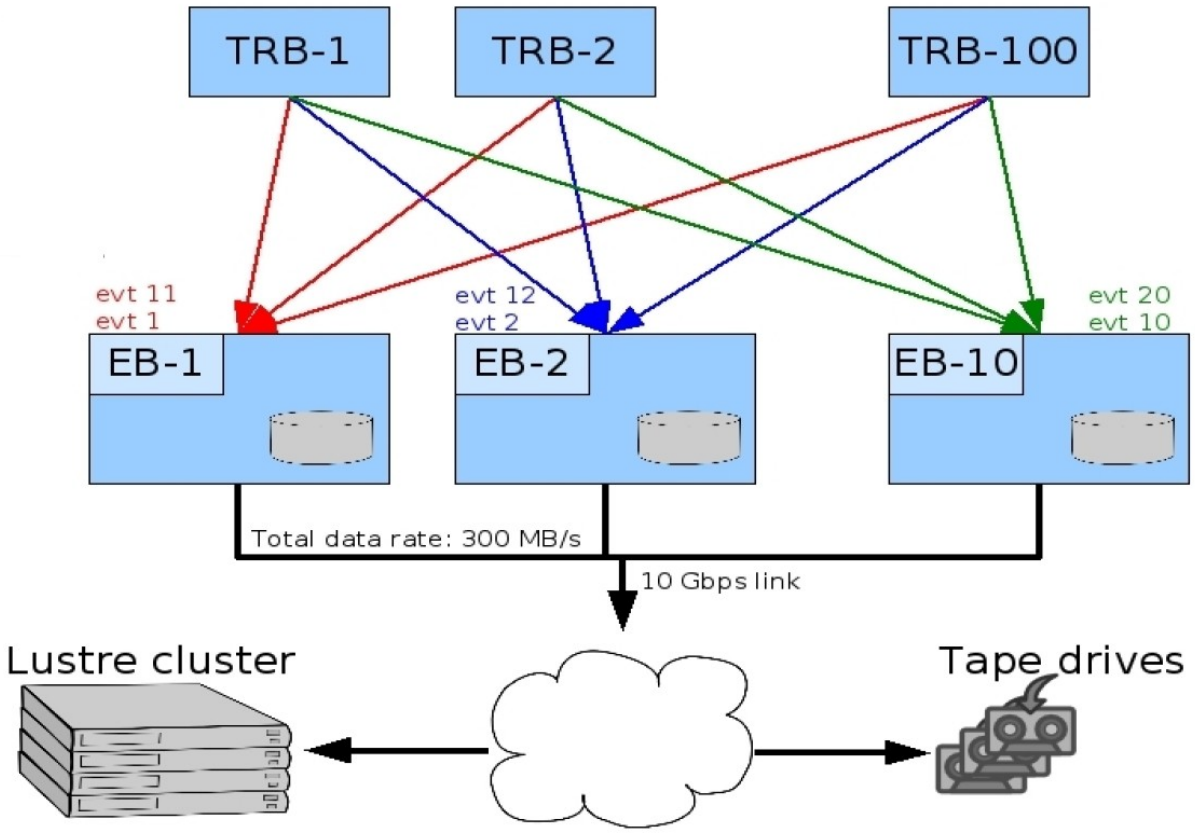
- Reduced induced noise
- Faster connection
- Smaller volume
- Easy handling

A. Tarantola, NSS Poster Session II :
"The Upgrade of the Multiwire Drift Chamber Readout of the HADES Experiment at GSI"

TRBnet - One Protocol for All Connections

- Main features :
  - Low latency 2us
  - Virtual independent data channels (data, slow control, trigger...)
  - Media independent
  - Used everywhere, one protocol for all connections
  - No data loss (back pressure)

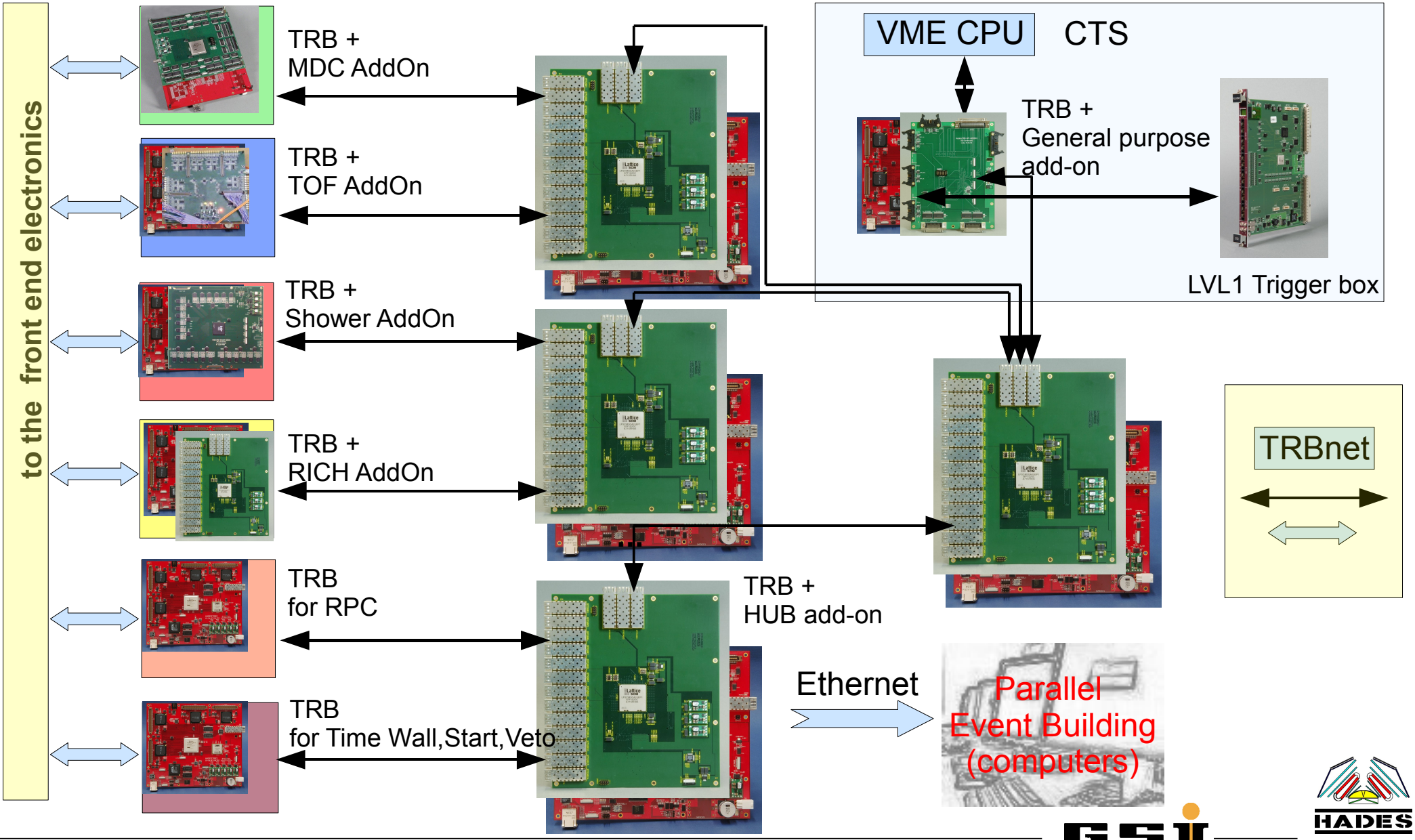
The Event Builder



Parallel Event Building software written

- Tested with 90 data sources (software emulation)
- Slow Control interface for monitoring implemented
- 10GBit/s connection to computer center

The HADES DAQ



Summary

- The Hardware is existing for all detectors
- We successfully used some configurations of this hardware for production and test beams
- The TRBv2 is used not only by HADES:
  PANDA - DIRK detector
  PANDA - MDC readout
  CBM - detector development
  PET- scanner prototype in Coimbra
  KVI - development of FPGA algorithms
  HPLUS - in China, Lanzhou Institute
- The idea of one flexible module as a platform for all detectors has proven to be very useful

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