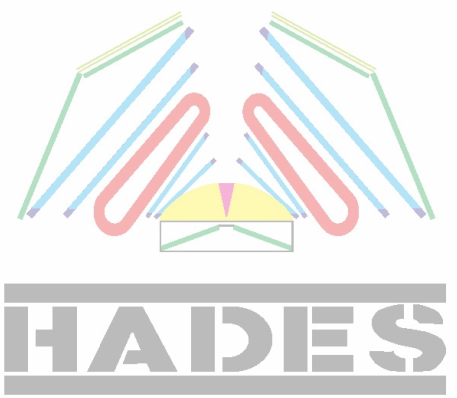


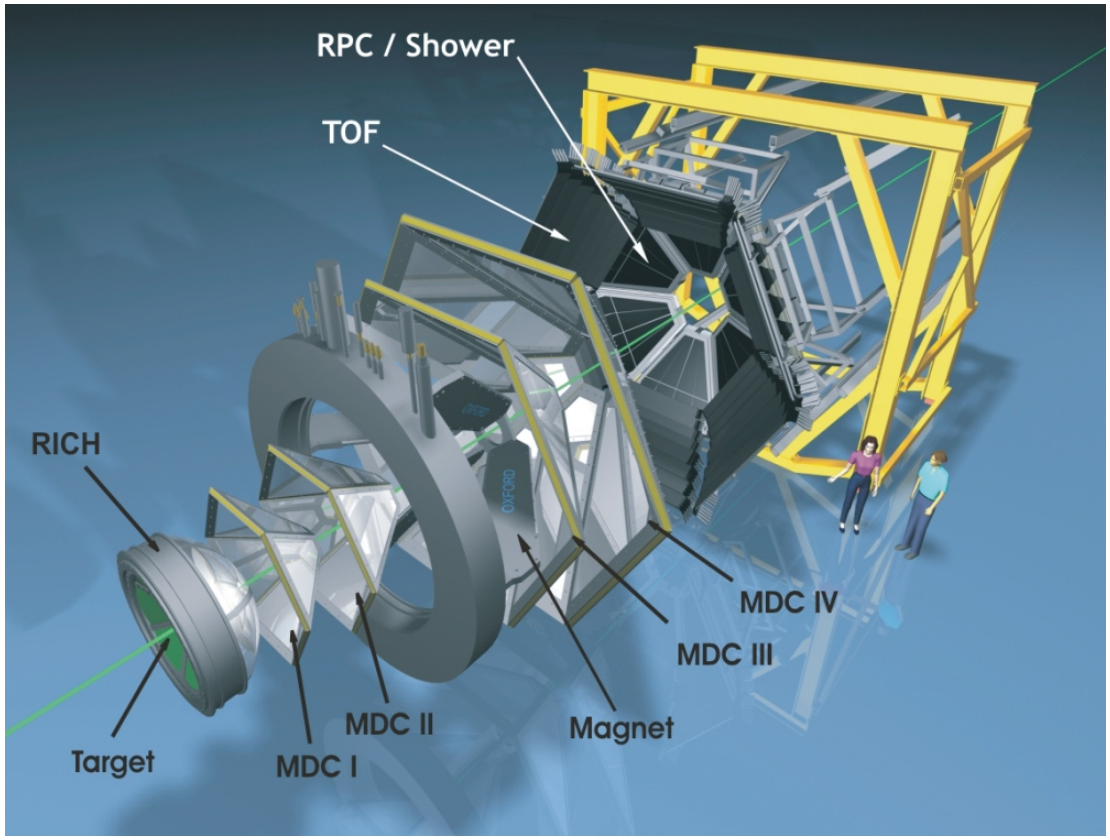
The New Trigger and Data Acquisition System of HADES | 19.03.2012

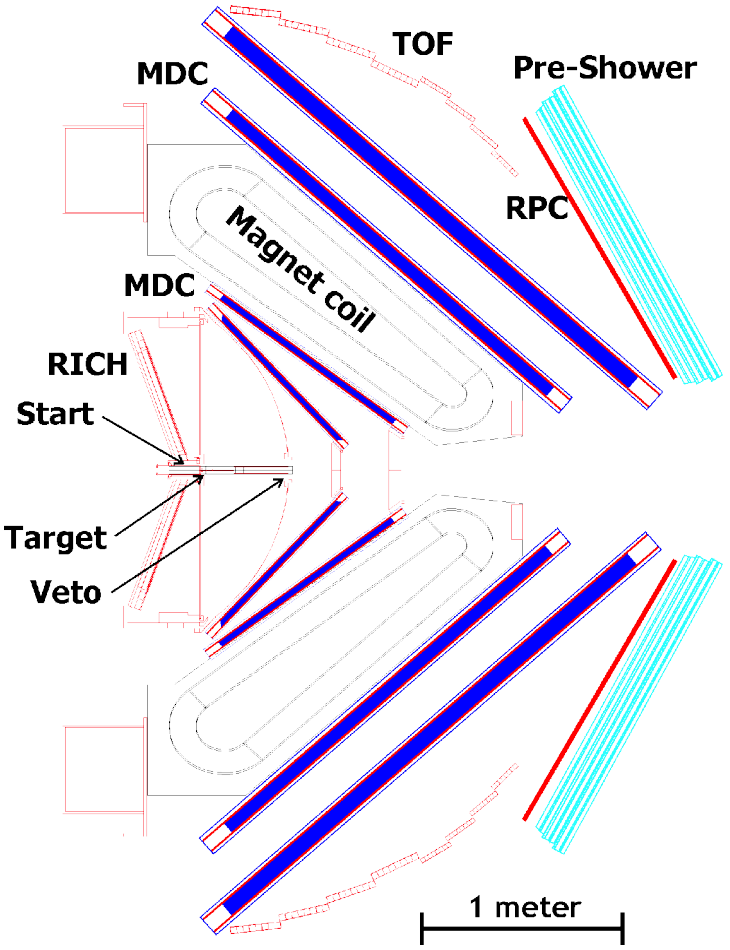
The HADES Experiment
Reasons for an Upgrade: Au+Au
The New Electronics & DAQ Network
A Few Details & Features
Synergies with Other Experiments

Jan Michel for the HADES collaboration

Goethe-University Frankfurt, Institute for Nuclear Physics

The HADES Detector





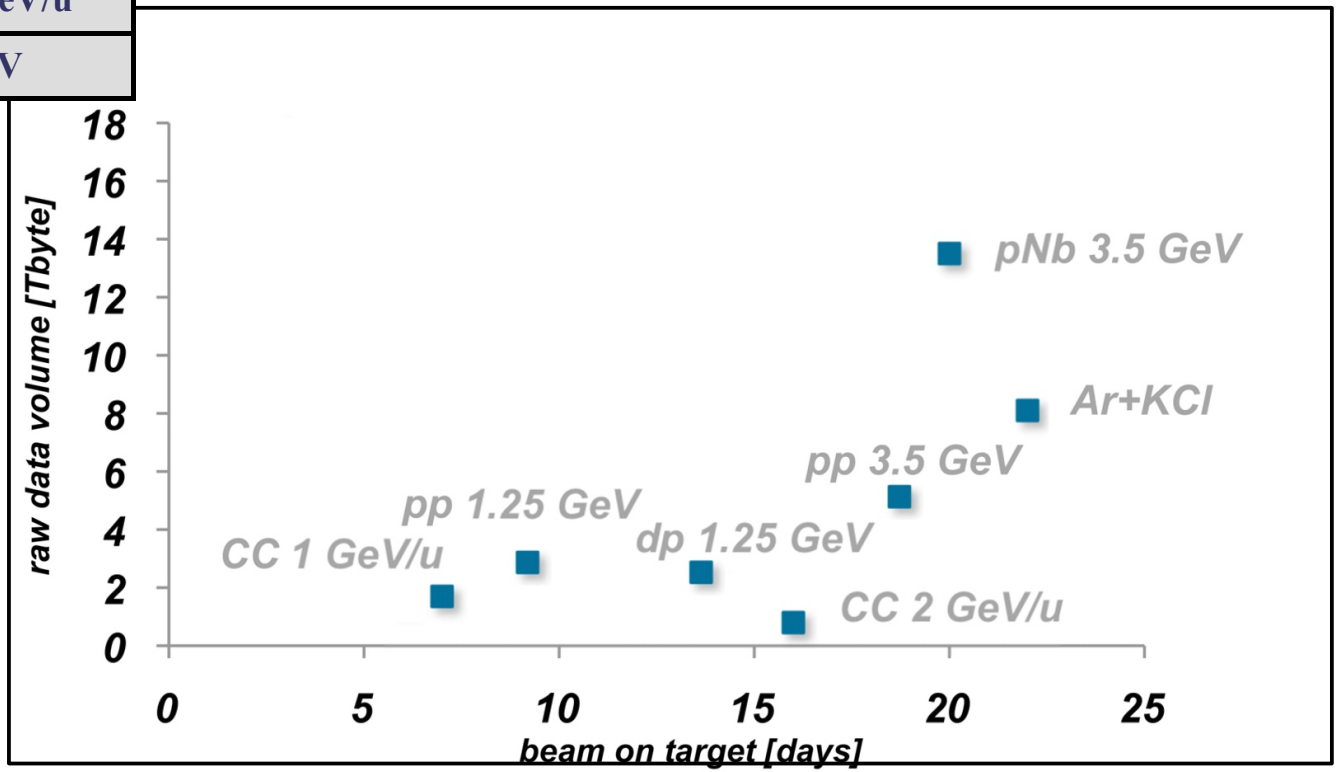
High **A**cceptance **DiE**lectron **S**pectrometer

30,000 TDC channels
50,000 ADC channels
Operational since 2001

Experiments & Datarates

2002	C + C	2 GeV/u
2004	C + C	1 GeV/u
2004	p + p	2.2 GeV
2005	Ar + KCl	1.75 GeV/u
2006	p + p	1.25 GeV
2007	p + p d + p	3.5 GeV 1.25 GeV/u
2008	p + Nb	3.5 GeV

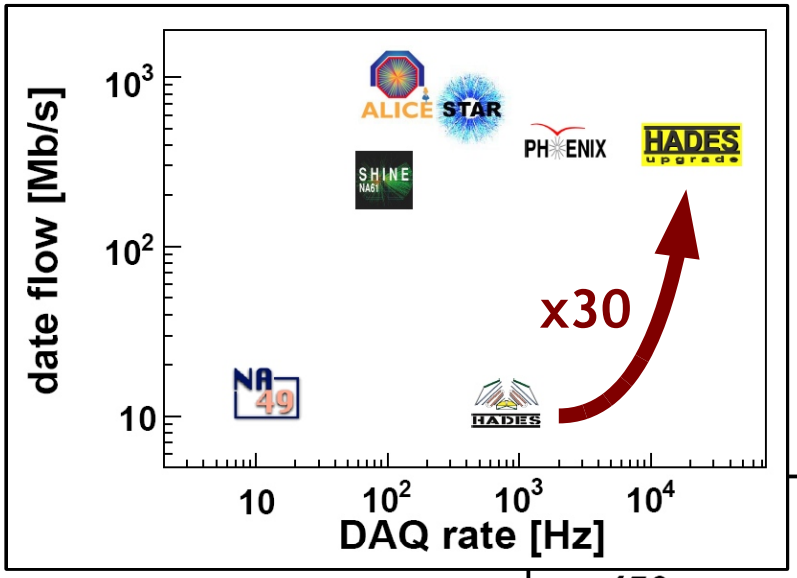
- The HADES electronics was already 10 years old
- Data for Ar+KCl was taken at 3 kHz event rate
  - For Au+Au 0.7 kHz were to be expected (limited by data rate)



HK 7.2, 16.1, 16.2, 16.3, 21.9 ...

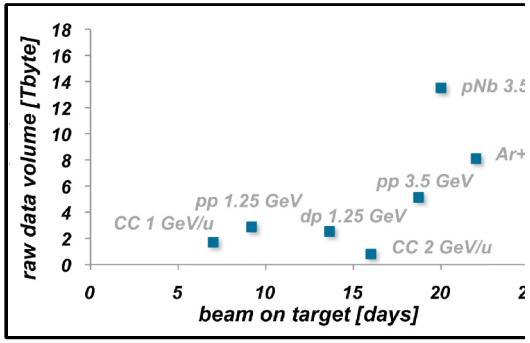
K. Gill (HK 46.3)

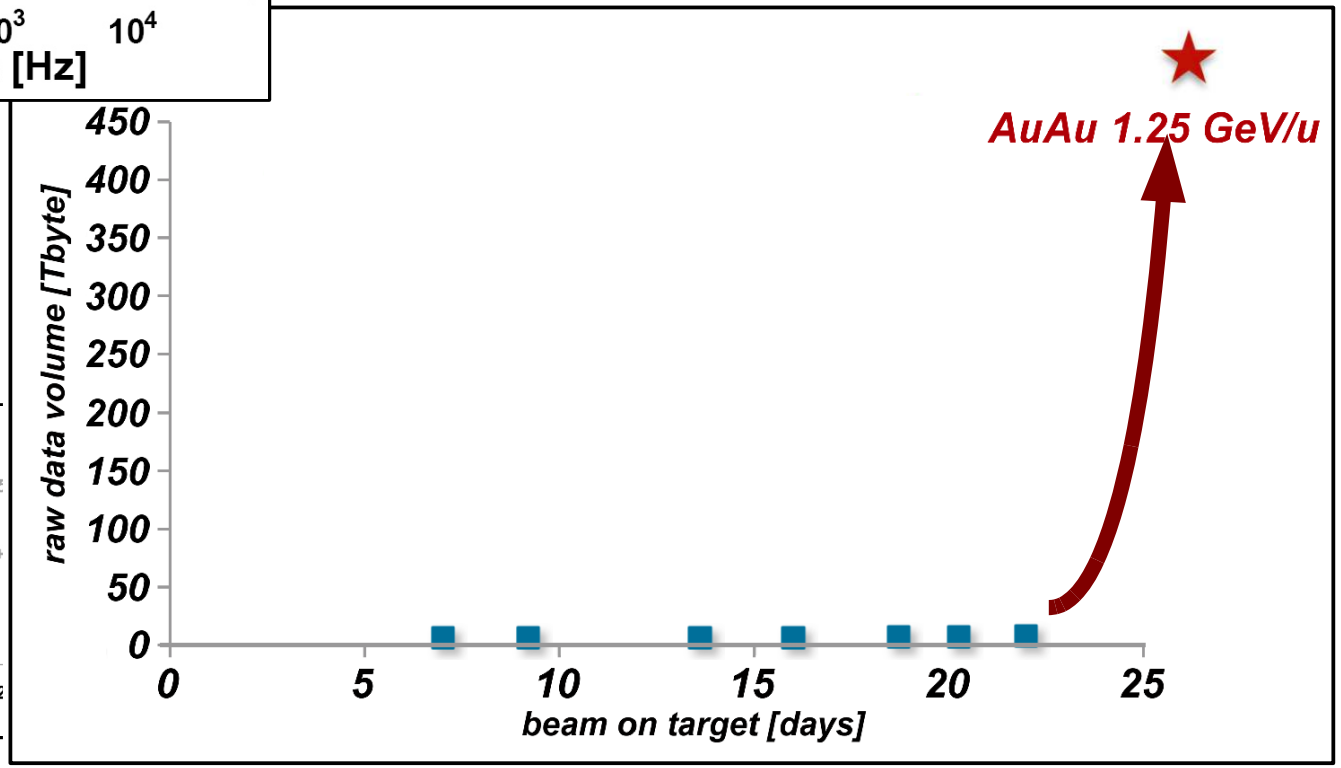
Experiments & Datarates



M. Lorenz

- Goal: Heavier Systems, Higher Statistics, Higher Granularity
  - Event rate up to 50 kHz (pp), 20 kHz (AuAu)
  - Data rate up to 500 Mbyte/s (peak), 300 Mbyte/s (avg)
  - Replacement of most read-out electronics

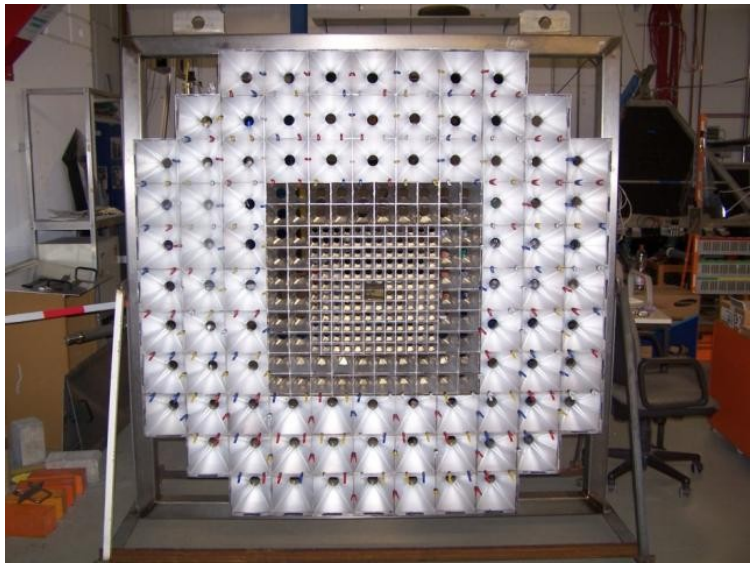




Detector Upgrade

New plane of drift chambers

Resistive Plate Chambers (tRPC) for higher granularity time-of-flight in forward direction

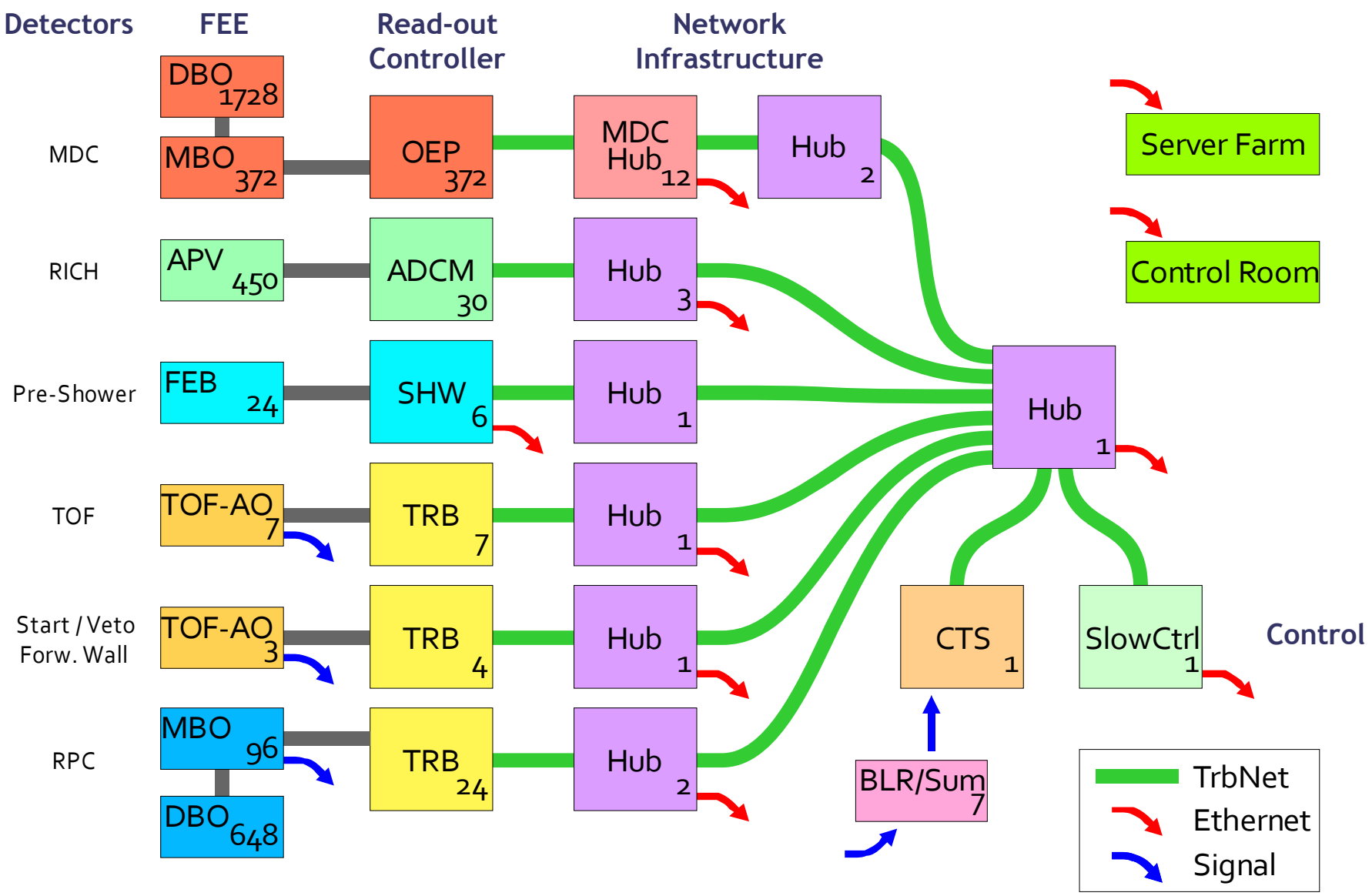


Forward Hodoscope – fragment & reaction plane measurement

The DAQ Upgrade

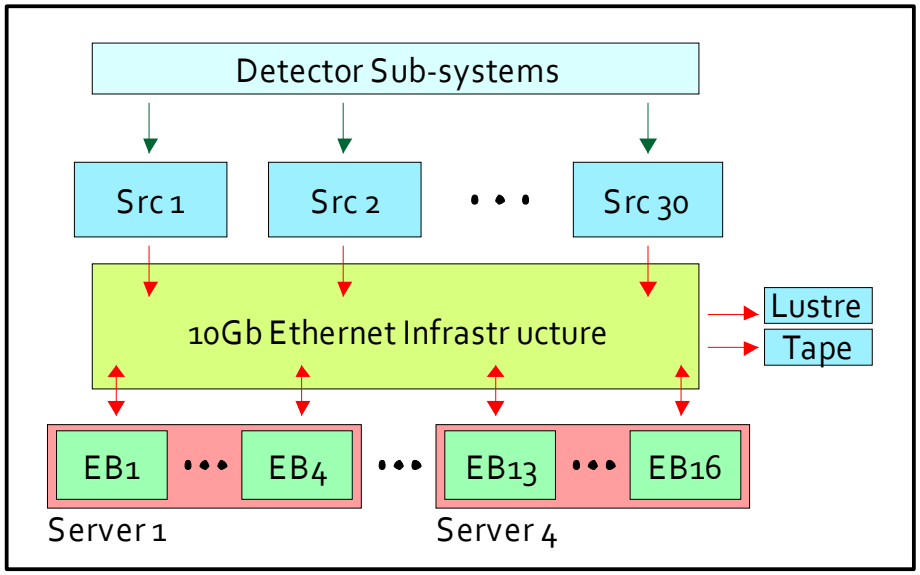
- **High Data Volume**
  - > 300 MByte/s
- **High trigger rate**
  - > 50 kHz
  - Keep trigger-busy-release architecture
    - Low latency required
- **Simple Maintenance**
  - Common implementation of all sub-systems
  - Using the same functional blocks in all devices
- **Hardware**
  - FPGA, optical links
  - Custom network protocol within the detector
  - Off-the-shelf components for other parts

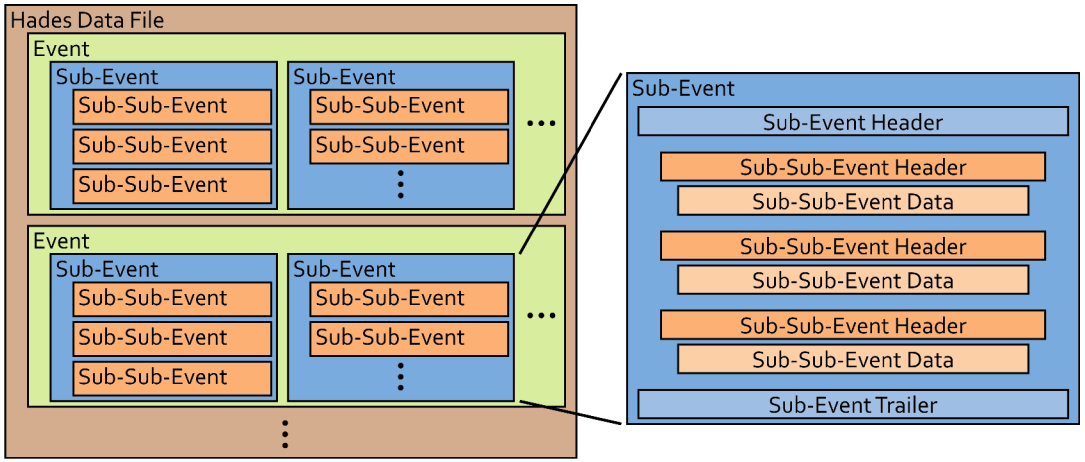
Read-out System



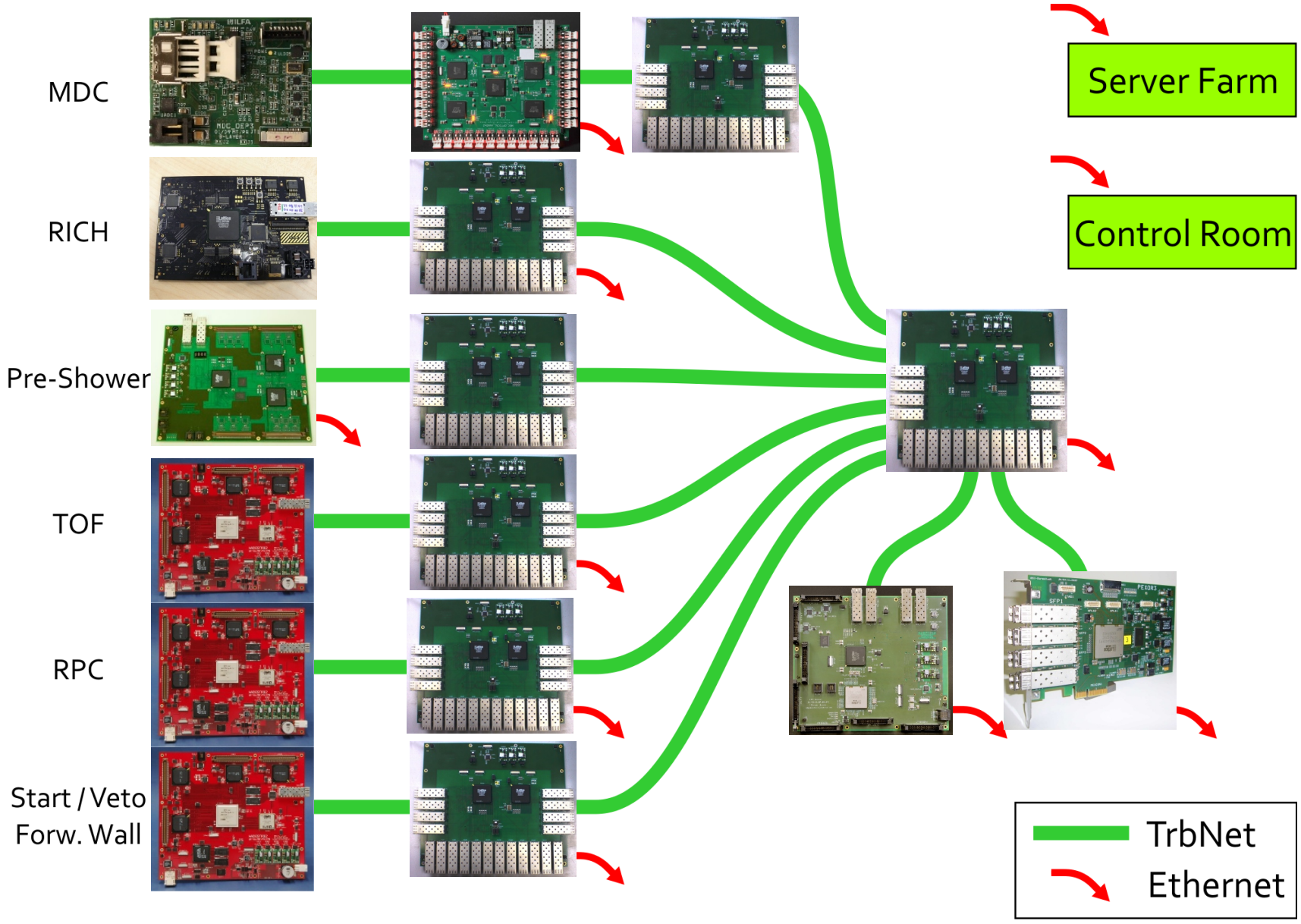
Data Transport & Event Building

- Data from front-ends is collected in 30 data mergers & forwarded via GbE
- Standard GbE-Infrastructure does the routing to 4 servers / 16 event building processes
- Servers:
  - 12 - 32 cores
  - 64 - 128 GB RAM
  - 24 HDD
- Storage:
  - Short term on 180 TB local disks
  - Long term on Lustre / Tape

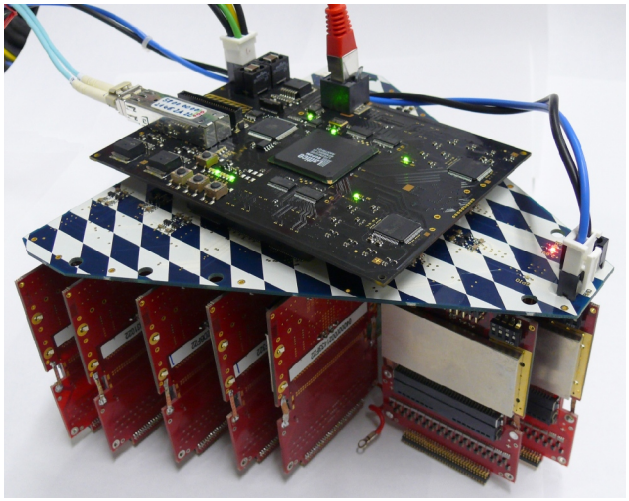




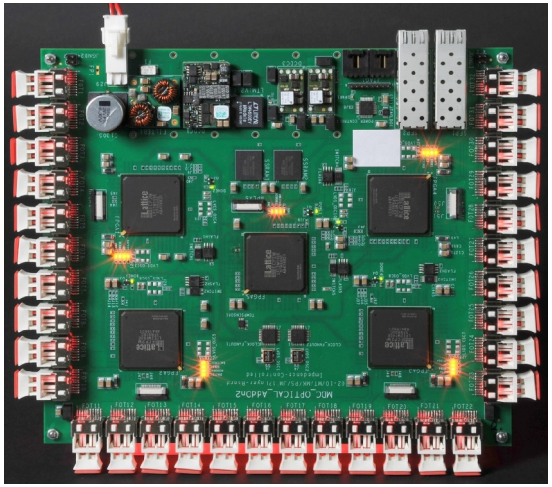
DAQ Network


MDC
RICH
Pre-Shower
TOF
RPC
Start / Veto
Forw. Wall
Server Farm
Control Room
TrbNet
Ethernet

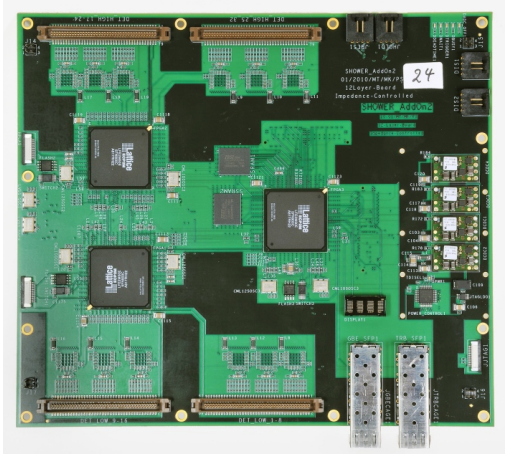
Hardware (excerpt)



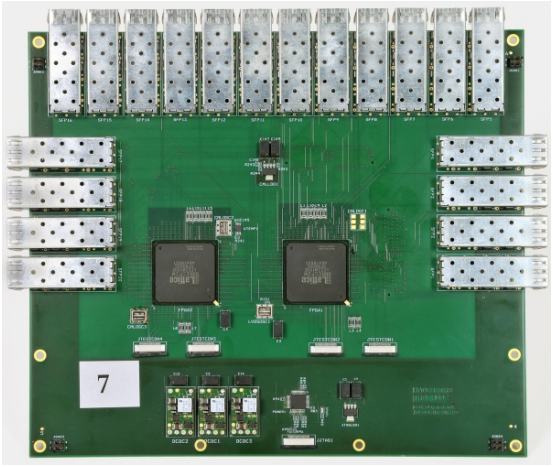
RICH ADCM
ECP2/M-100
16 ch. 12 Bit 40MSPS ADC
(w/ FEE)



MDC-Hub
5x ECP2/M-100
32x FOT (250MBit)



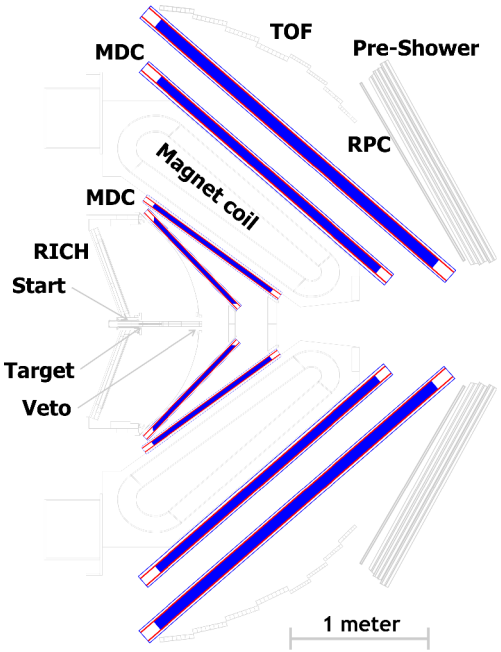
Shower-AddOn:
3x ECP2/M-50
96 ch. 10 Bit 20 MSPS ADC

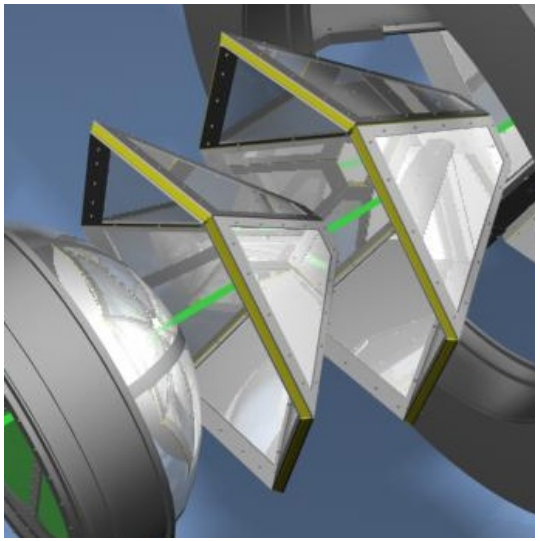


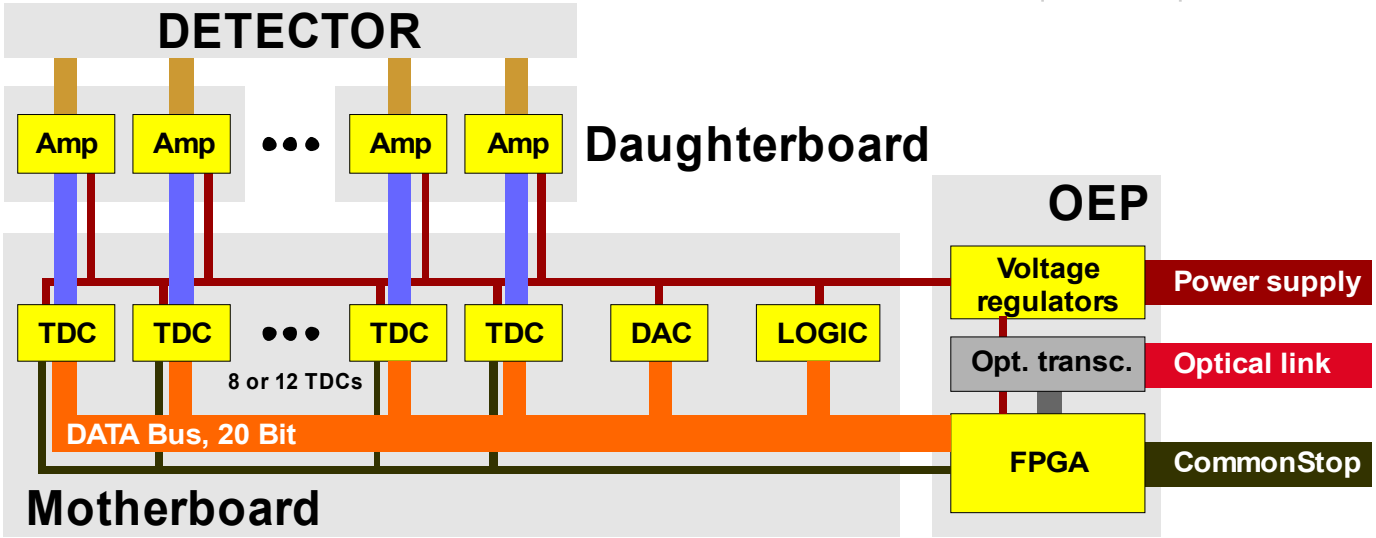
Hub
2x ECP2/M-100
20x SFP (3.1GBit)

MDC Electronics

- 30,000 sensor wires
- 500 ps TDC time resolution
- 200 MByte/s
- constraint space for electronics

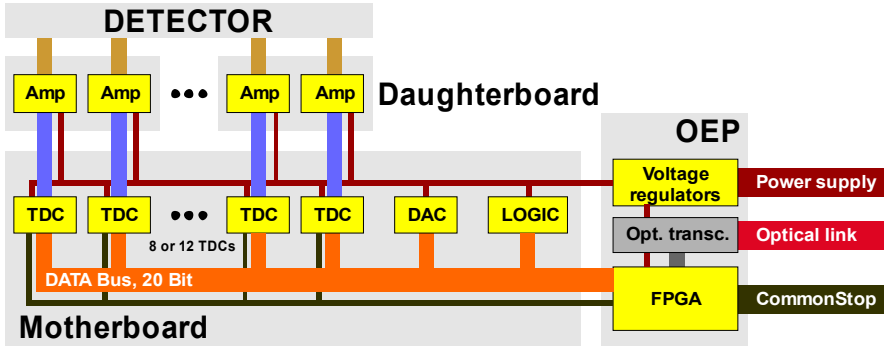




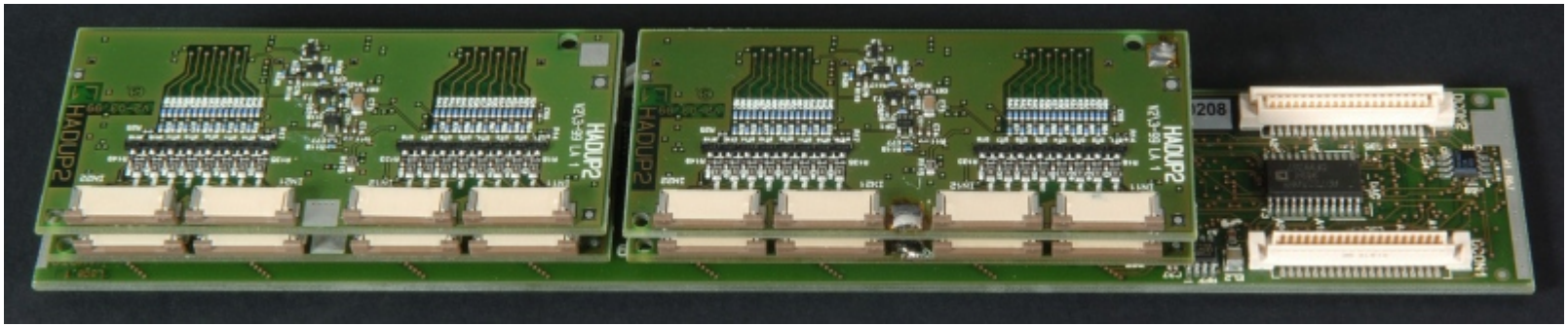


MDC Readout

- Old read-out
  - RS-485 based
  - daisy-chaining of 2 Motherboards
  - big flat-cables

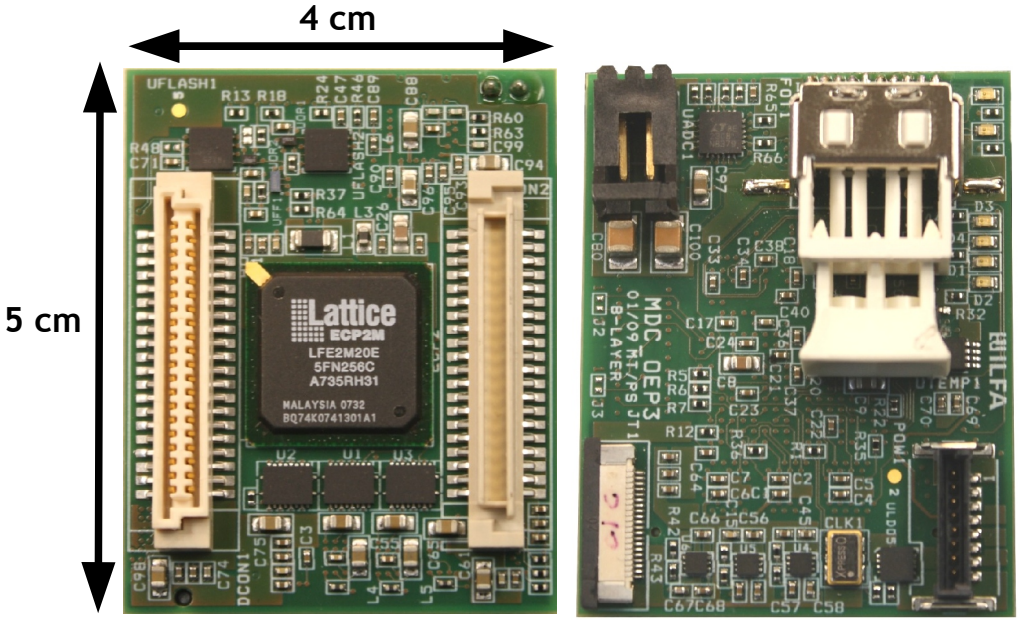


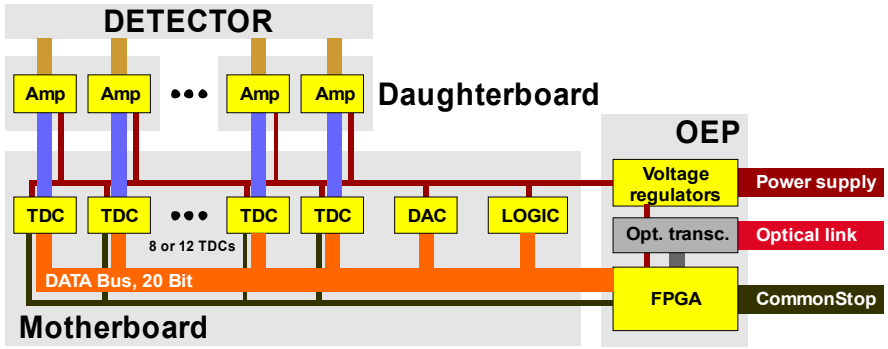
372 boards for all
24 MDC chambers



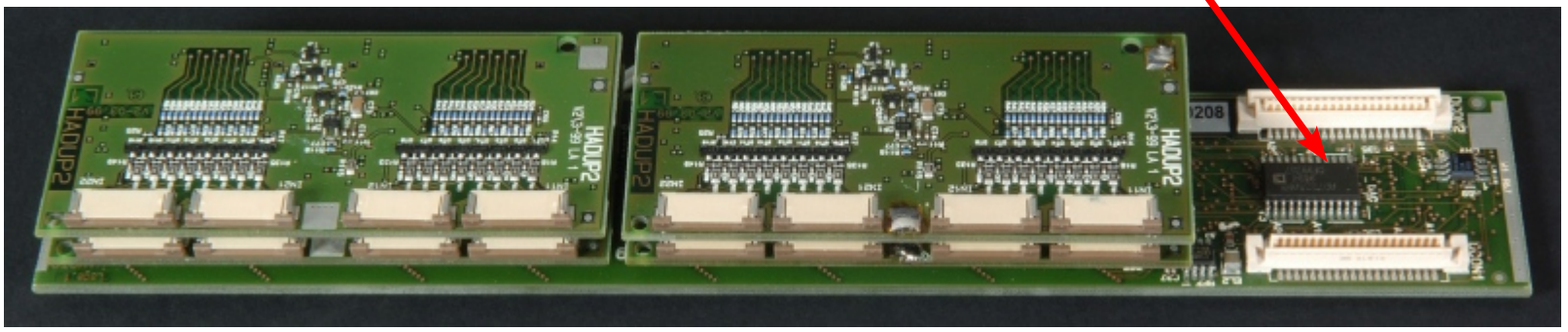
MDC Readout

- Lattice ECP2M-20 configures, controls and read data from FEE boards
- Regulators for all supply voltages
- All voltages are monitored
- 2 ROMs for different FPGA designs
- Temperature sensor
- 250 Mbit/s optical transceiver



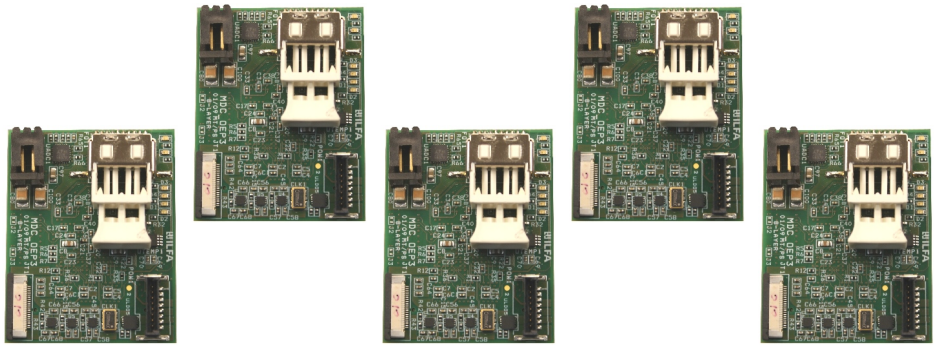


372 boards for all MDC chambers

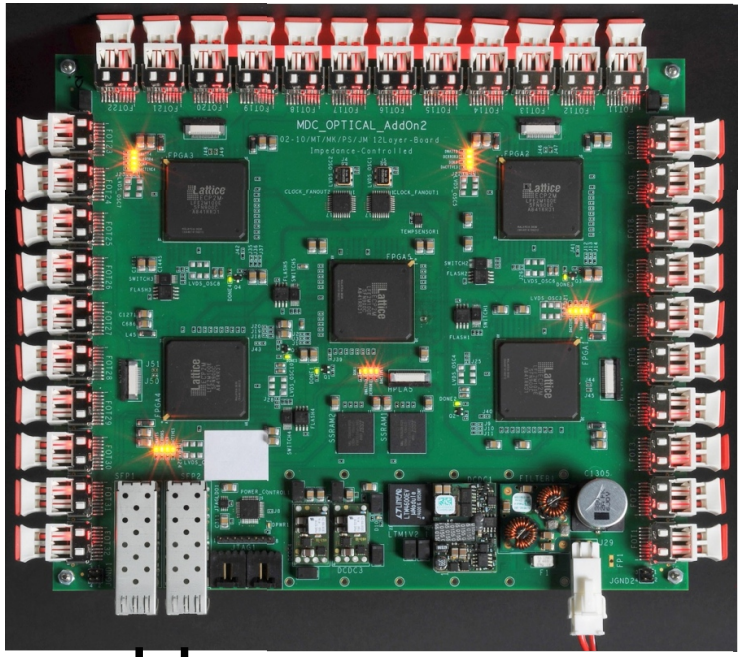


MDC Readout

372x



12x



TrbNet (Trigger, Control)

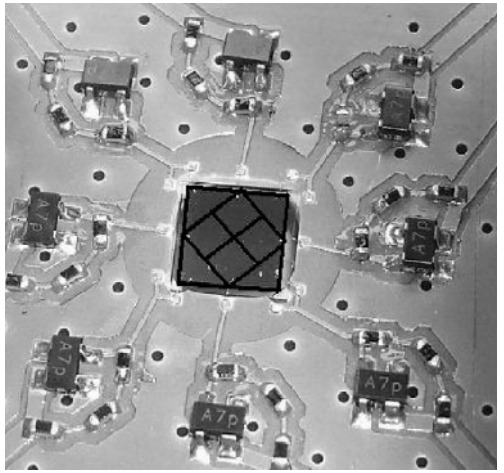
Ethernet (server farm)

MDC Data Concentrator

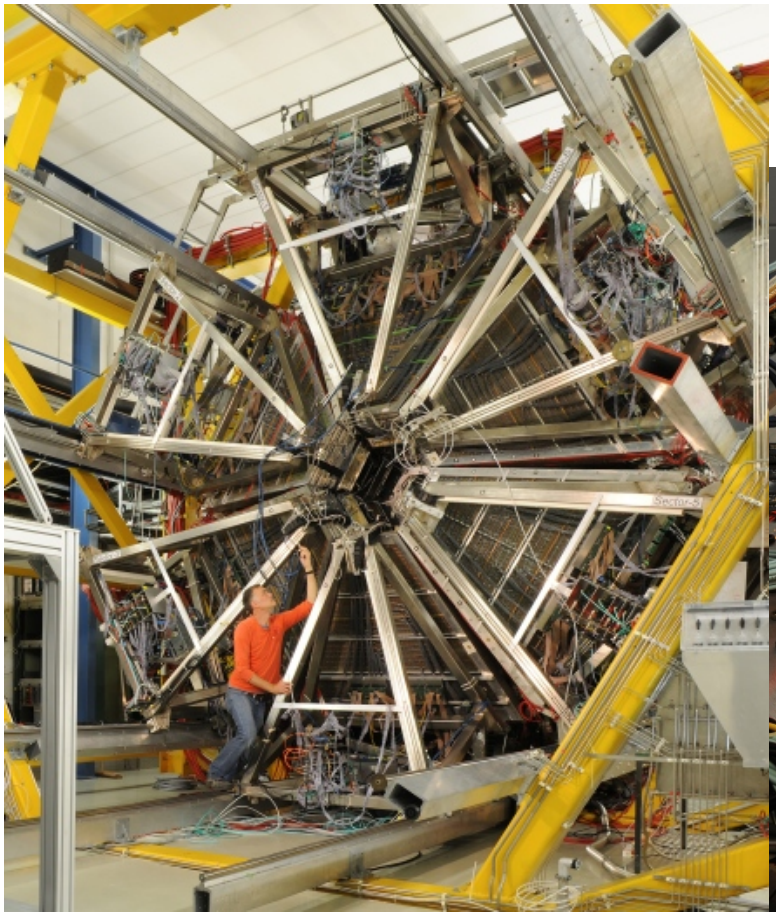
- Data from 2 chambers is combined and sent to servers
- 32x 250 Mbit/s
- 1x 2 Gbit/s TrbNet
- 1x Gigabit Ethernet
- 5x Lattice ECP2M100

Fully Assembled

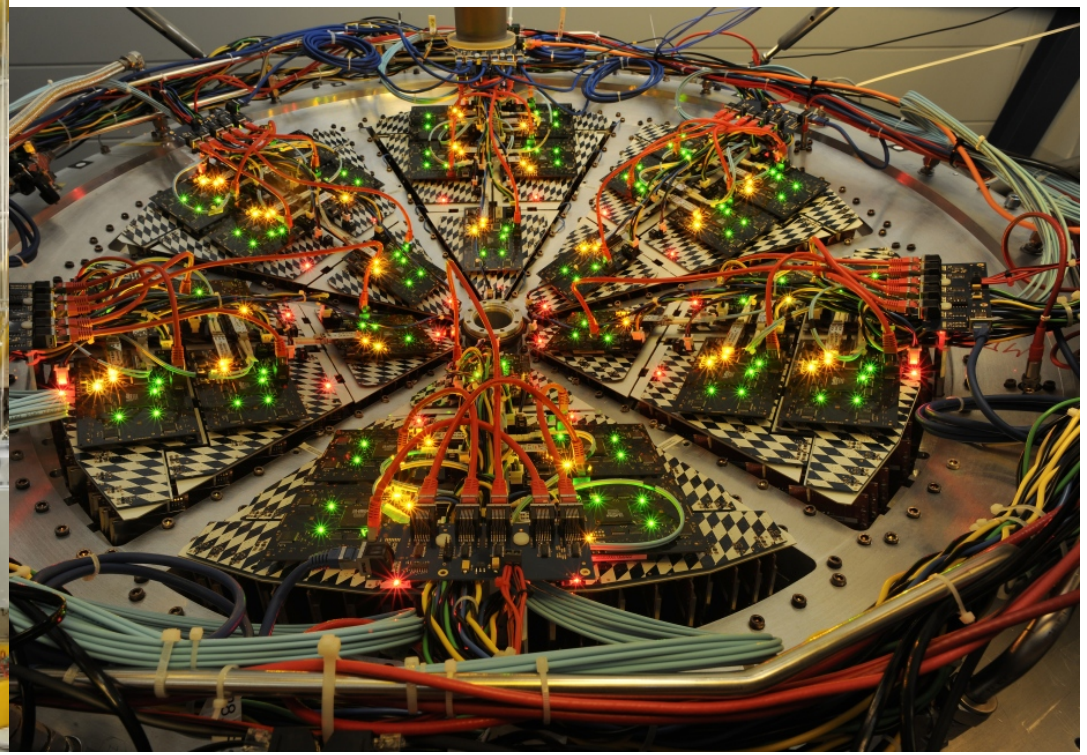
"Start" diamond detector
with pre-amps
(J. Pietraszko, HK 27.7)



Backside of the Detector



RICH detector eletronics



Pictures: Gaby Otto, GSI

DAQ in numbers

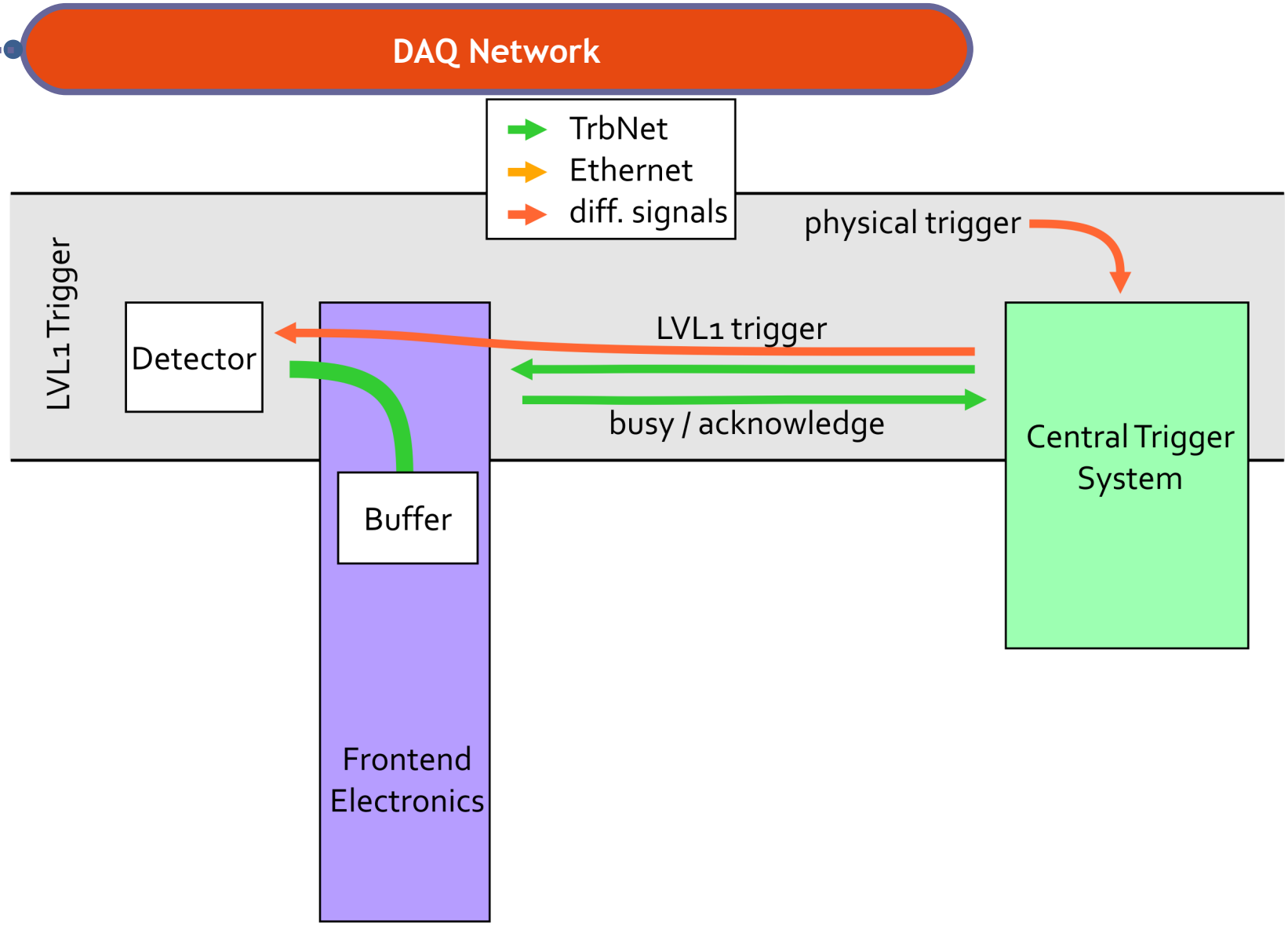
Electronics
- 520 digital PCB with FPGA
- 4,500 PCB in total
- 1,500 ADC channels
  (multiplexed from 50,000 signals)
- 30,000 TDC channels
- 100 kHz trigger rate
- 250 MByte/s (avg.), 400 MByte/s (peak) written to disk

Data transport
- 550 FPGAs
- 1050 optical transceivers (SFP & FOT)
- 7,000 m optical fibre (glass-fibre & POF)
- 800 m 1-wire & CAN bus
- 32 Ethernet switches
- 15 Gbit/s uplink to Eventbuilders
- 10 Gbit/s uplink to storage (Lustre / Tape)

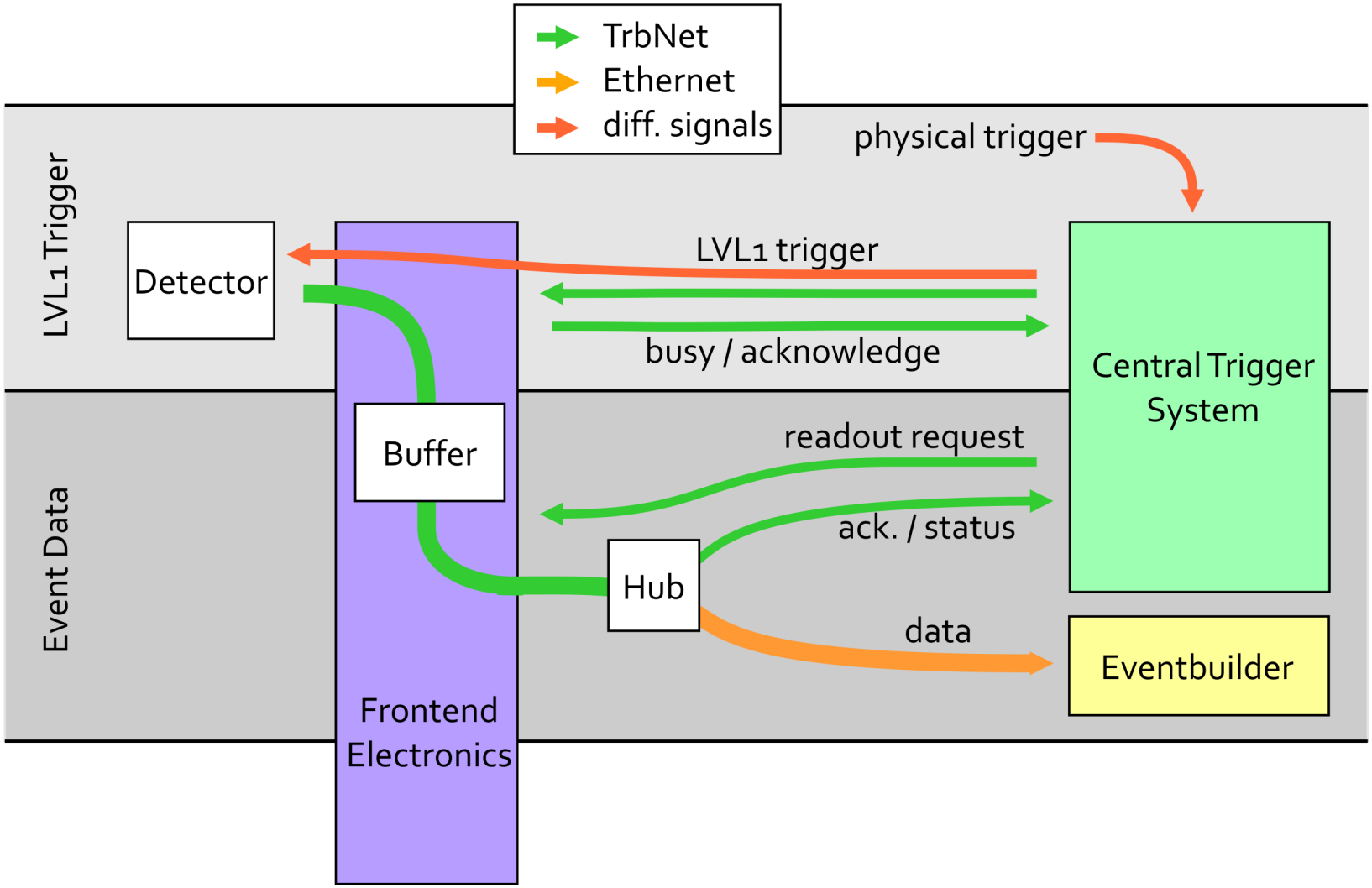
DAQ Power Supply
- > 4,000 voltage regulators
- 9 power supplies
- 5.5 kW total power (FEE only)

Server farm
- 160 TB hard disks
- 44 CPU cores
- 100 TB storage / week

The DAQ Network

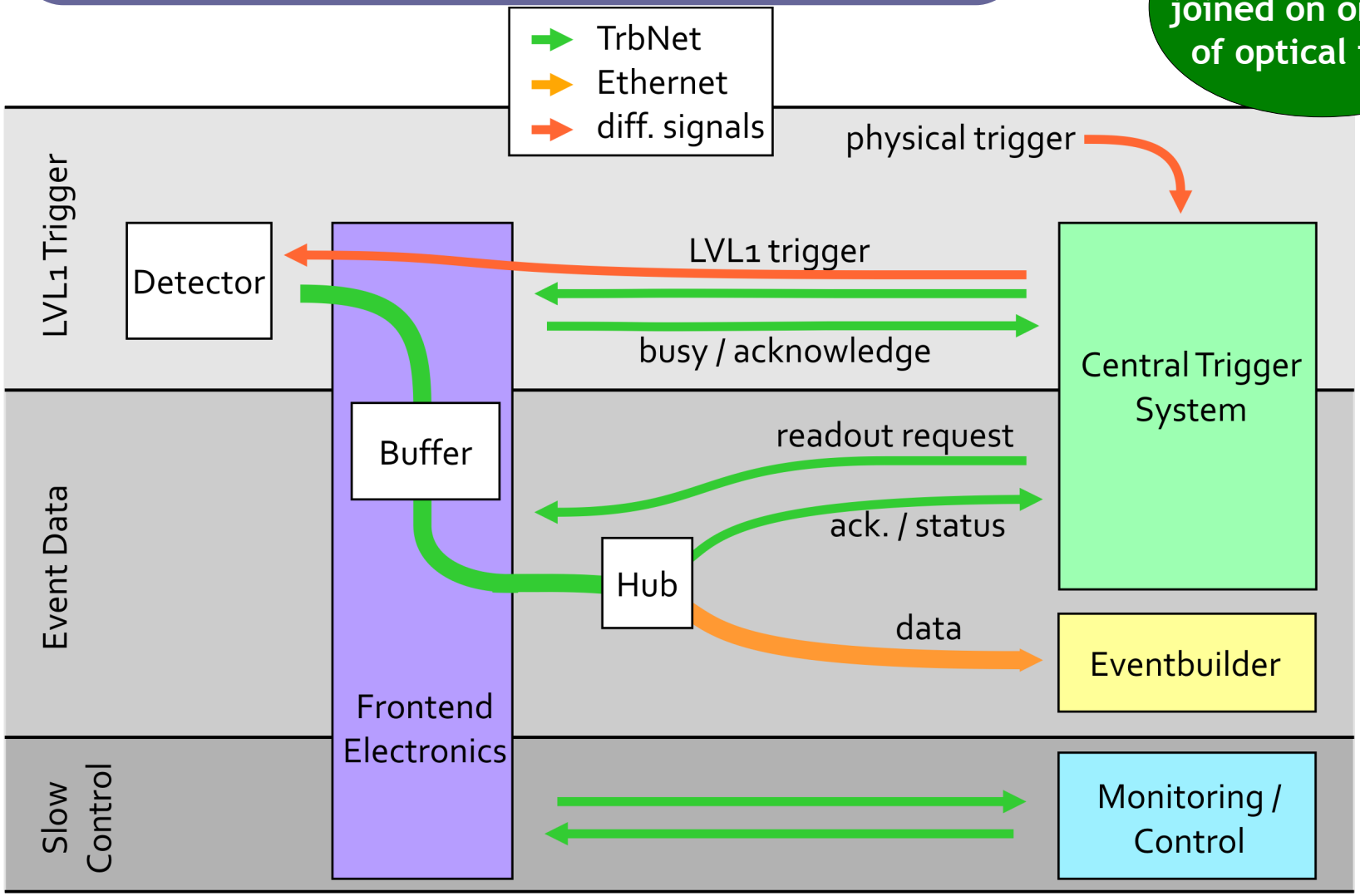

DAQ Network
TrbNet
Ethernet
diff. signals
LVL1 Trigger
physical trigger
Detector
LVL1 trigger
busy / acknowledge
Central Trigger System
Buffer
Frontend Electronics

DAQ Network


TrbNet
Ethernet
diff. signals
LVL1 Trigger
Event Data
Detector
Buffer
Frontend Electronics
physical trigger
LVL1 trigger
busy / acknowledge
readout request
ack. / status
data
Hub
Central Trigger System
Eventbuilder

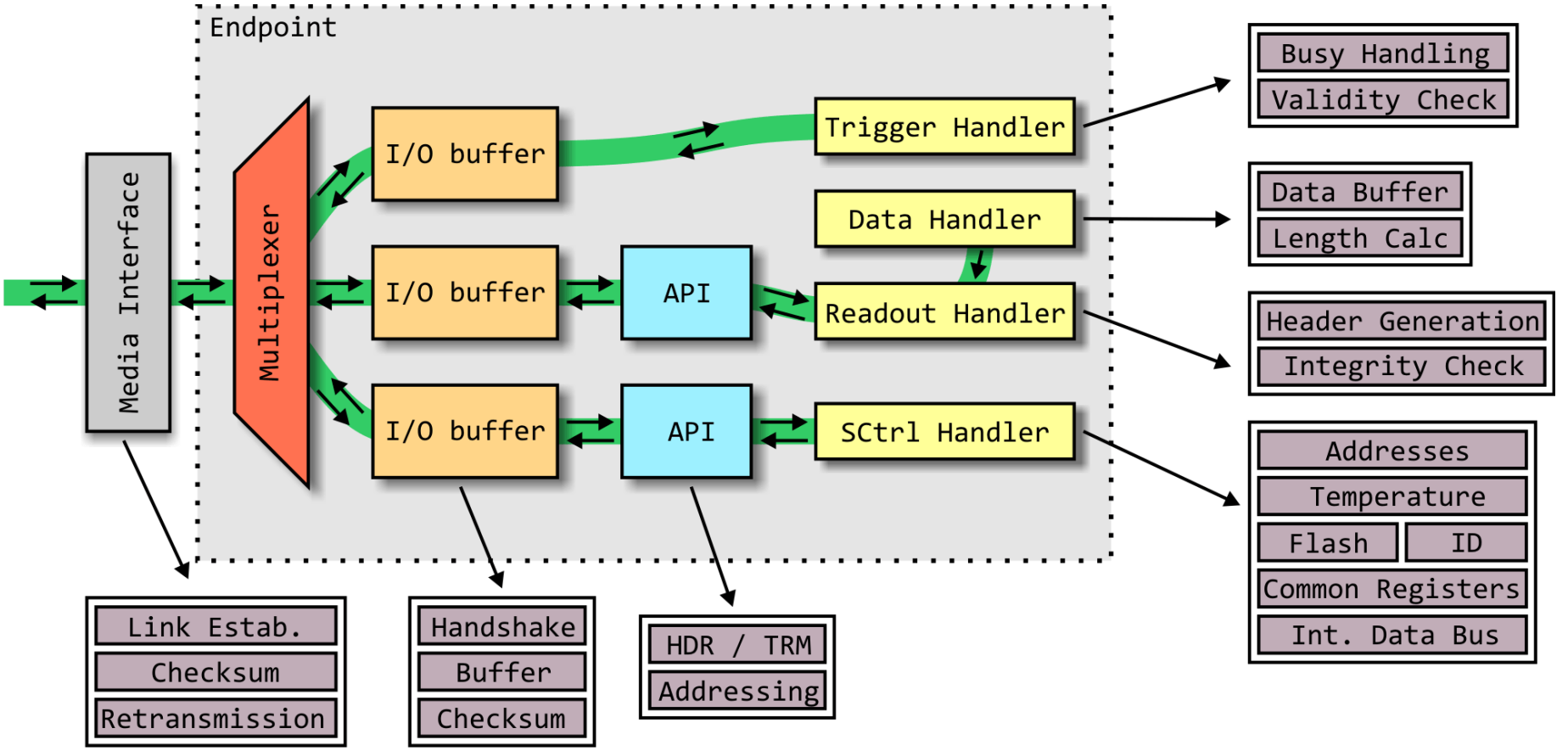
DAQ Network

All functions are joined on one pair of optical fibers



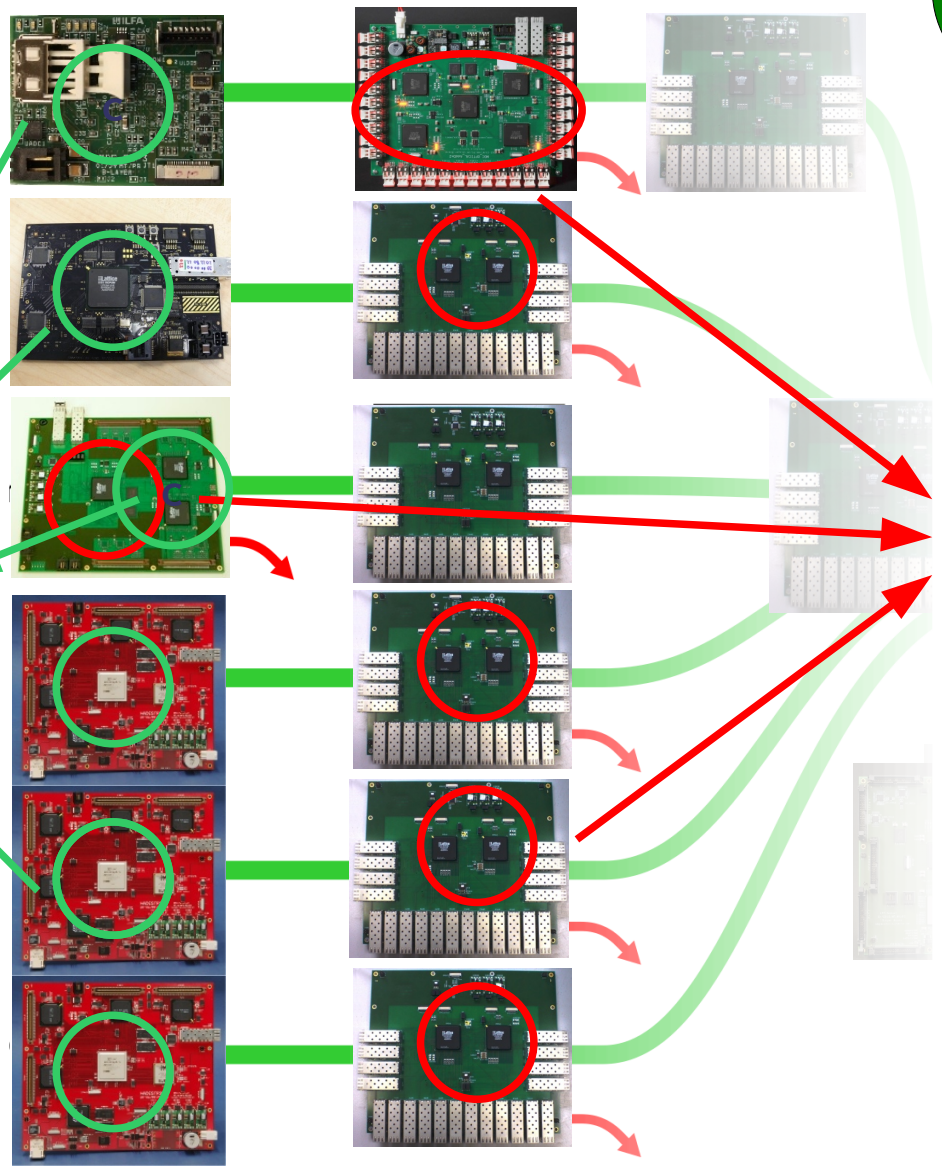
The Network Endpoint

All main functions encapsulated in a reusable block



DAQ Network

Diverse Systems but high reus-ability factor for code



All Front-end boards use identical code - only the control logic for FEE differs

>95% identical code due to same hardware building-blocks

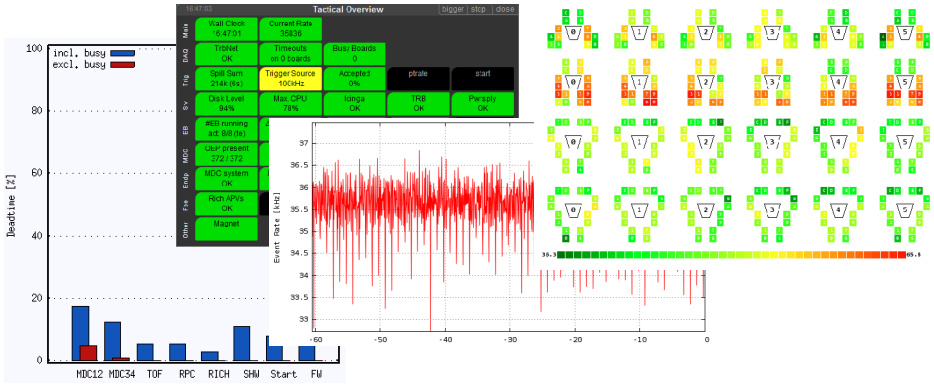
System Monitoring

- **Detailed Information about Front-end Status is vital**
  - Huge set of registers available in each FPGA

- **e.g. for each of the 372 MDC FEE boards**
  - All information is available, but nobody can read it...

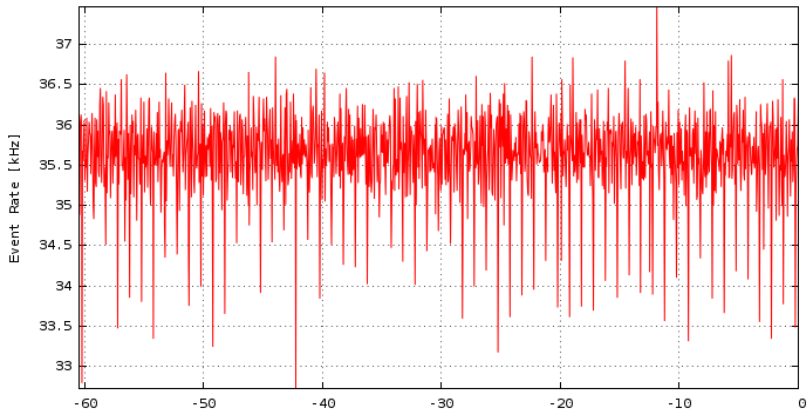
```
0x00000004  0x00000000  0x00000000  0x00000c00
0x00000100  0x00000000  0x00140020  0x0010de0b
0x00000000  0x00000000  0x00000000  0x00000000
0x00000000  0x00000000  0x00000000  0x00000000
0x0005a860  0x00000000  0x00819518  0x000009a4
0x003bcdfc  0x00408356  0x00000000  0x00000000
0x00000000  0x004d7132  0x00000000  0x03479216
0x00000000  0x00000000  0x00000002  0x00000000
0x8b2bae66  0x0000198f  0x003f4304  0x07ce9695
0x0039b414  0x0000951a  0x00000000  0x00000000
0x00000000  0x00000000  0x00000000  0x00000000
0x00000000  0x00000000  0x00000000  0x00000000
```

- **Data needs interpretation & processing**
  - Approach: small core library + independent scripts
  - No special tools, just plain Perl
    - No experts needed, 'everybody' can make changes
  - Browser based
    - Accessible from any PC



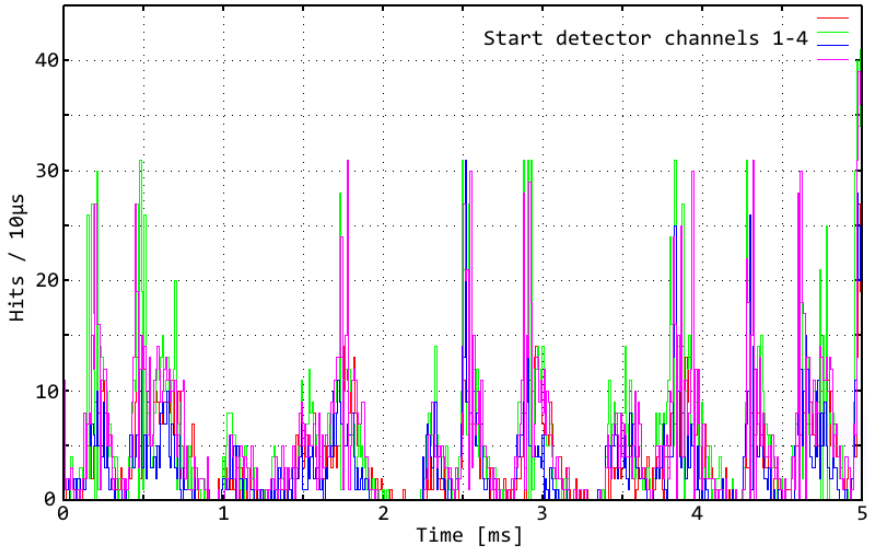
Versatile On-line Monitoring Features

Event Rate (20ms binning)

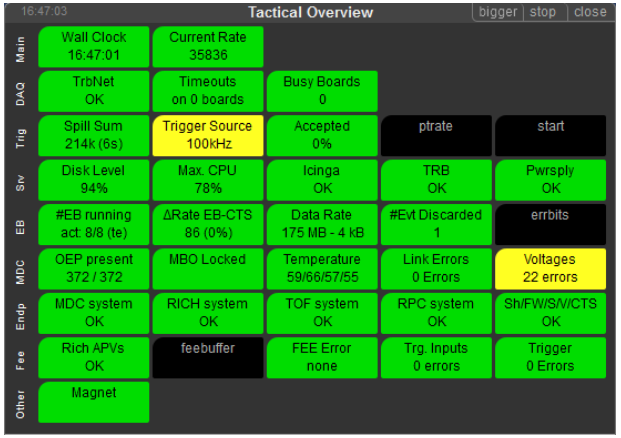


Temperature Monitoring

Accelerator Spill Structure (10 µs binning)



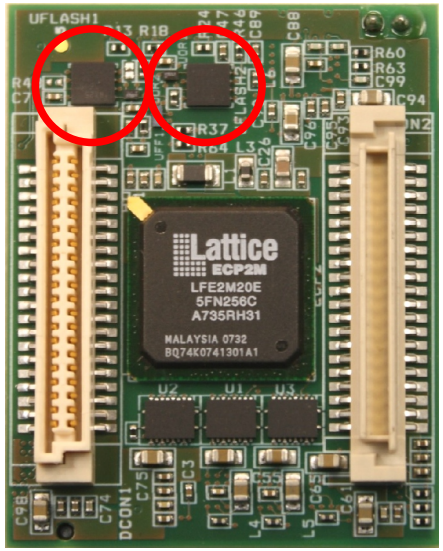
Automatic Checks for Vital Parameters



One-click documentation / guide for operator

“Slow”-control: Features

- **How to upgrade firmware in ~400 FPGA distributed all over the detector?**
  - Connect flash ROMs to logic in FPGA
  - One command in software framework
  - 30s to programm + 60s to verify (full system, ~500 MByte !)
- **Failsafe?**
  - Dual-boot with “golden image”




```
> trbflash program 0xfffd bit/mdcoep_20120307a.bit
Found 372 Endpoint(s) of group MDC_OEP_V3
NAME: mdcoep_20120307a.bit
DATE: Wed Mar  7 22:30:59 2012

Start programming ImageFile
'bit/mdcoep_20120307a.bit'
Programming Endpoint(s) @ Address 0xfffd
Symbols:
  E: Erasing
  P: Programming
  @: Success
  .: Skipped

Block: 0 1 2 3 4 5 6 7 8 9 A B C D E F
0      @ @ @ @ @ @ @ @ @ @ @ @ . . . .
1      . . . . . . . . . . . . . . . @

Success

Verifying Endpoint(s) @ Address 0xfffd
Symbols:
  V: Verifying
  X: Failed (see logfile 'trbflash.log' for details)
  @: Success
  .: Skipped

Block: 0 1 2 3 4 5 6 7 8 9 A B C D E F
0      @ @ @ @ @ @ @ @ @ @ @ @ . . . .
1      . . . . . . . . . . . . . . . @

Success
```

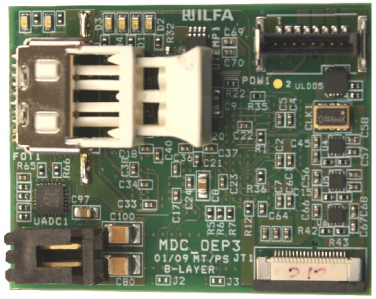
The Real Challenge

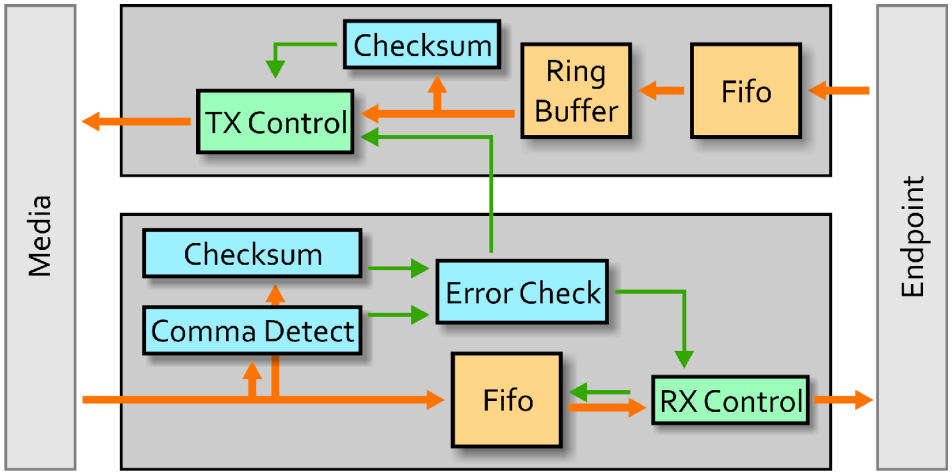
"The first step is to get a system working. The real challenge is to keep it running."

- **Optical links are immune to noise...**
  - … but transceivers are not
  - Especially when operated 10 cm away from field wires (1.8 kV) and PMTs (1.4 kV)
- **Dramatic increase in bit error rate from < 10^{-15} (lab) to > 10^{-11} (experiment)**
  - 200 transmission errors (single bit errors) per minute

- **Data check on link-level (80 bit packets, 8 bit CRC + control char.)**
  - Automatic retransmission within < 2 µs
- **Very succesful**

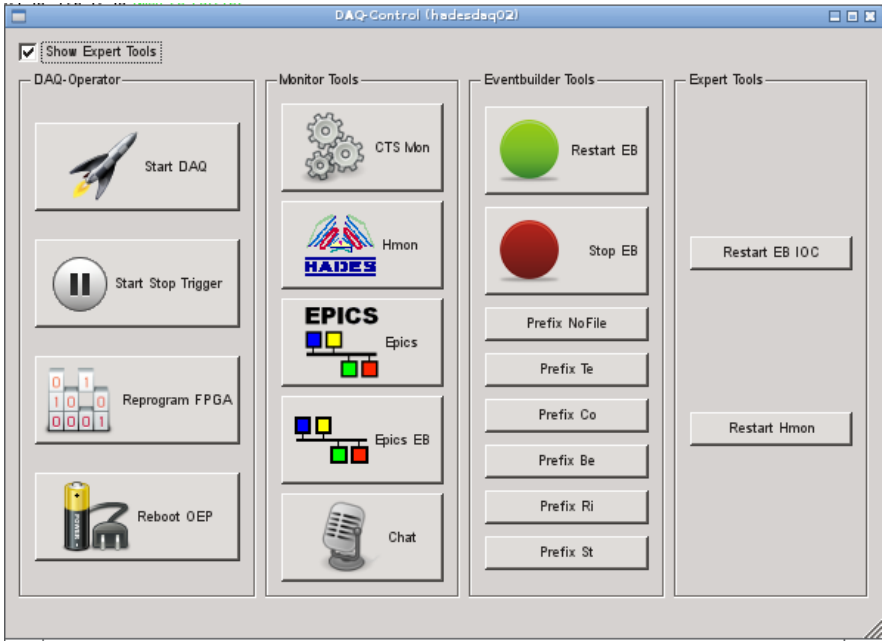
  (can even be used to track down problematic HV parts on TOF wall)

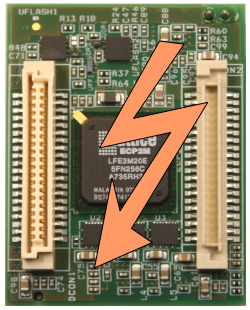


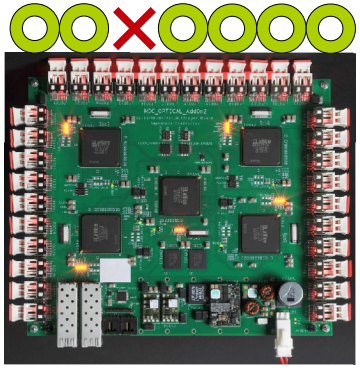


More Challenges?

- **FPGAs tend to fail under harsh conditions**
  - Radiation effects (e.g. SEU)
  - Voltage drops caused by FEE
- **A single failing board should not stop DAQ**
  - Automatic exclusion from DAQ system
  - FPGA design reloaded, reconfiguration of front-end
  - Short DAQ stop to re-synchronize all modules again

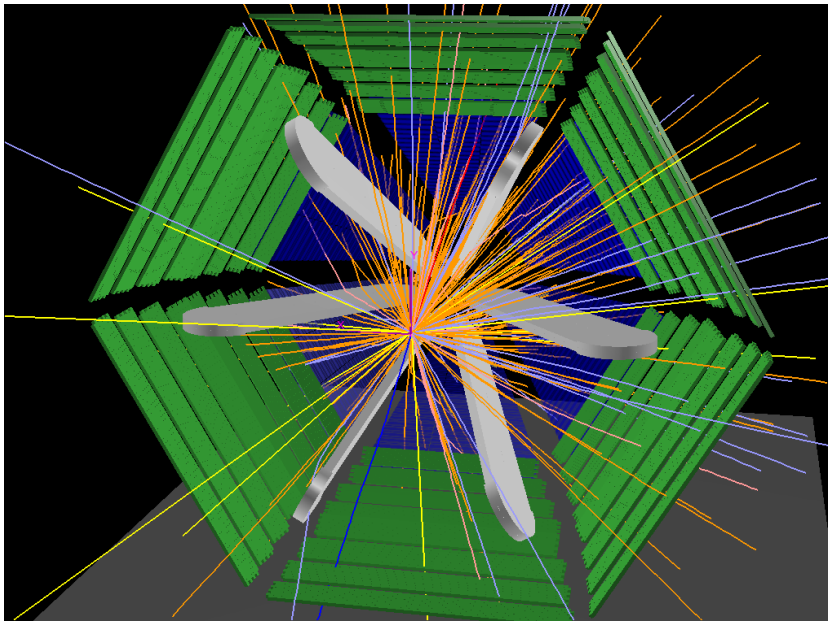






Experiments

- **Several short beam-times in 2010 / 2011**
  - Commissioning of DAQ & Detectors
  - Test of analysis software
- **E.g. August 2011:**
  - 4 days
  - 10^9 events recorded, 18 TB data

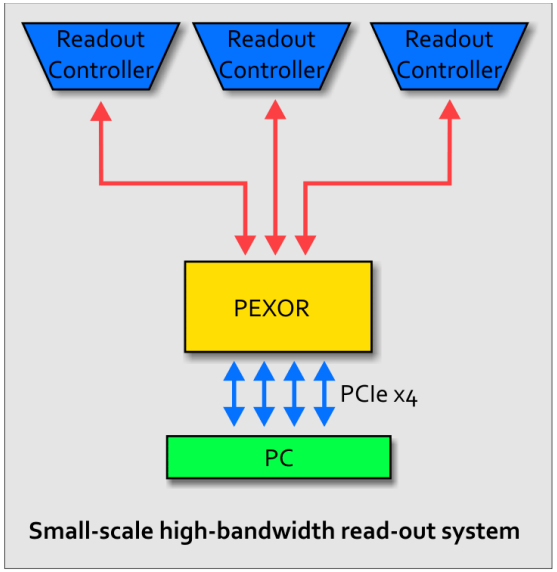


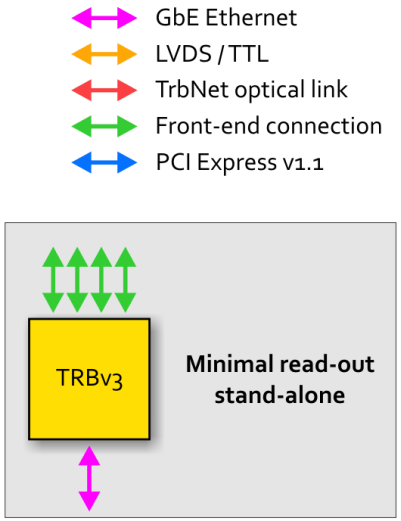
Target	15-fold segmented gold foils 1% interaction rate
Beam energy	1.25 AGeV
Beam intensity	2x10 ions/second
Event rate	10 kHz central events + 3 kHz peripheral
Data rate	200 MByte/s mean 350 MByte/s peak

An universal platform – also in use for other experiments

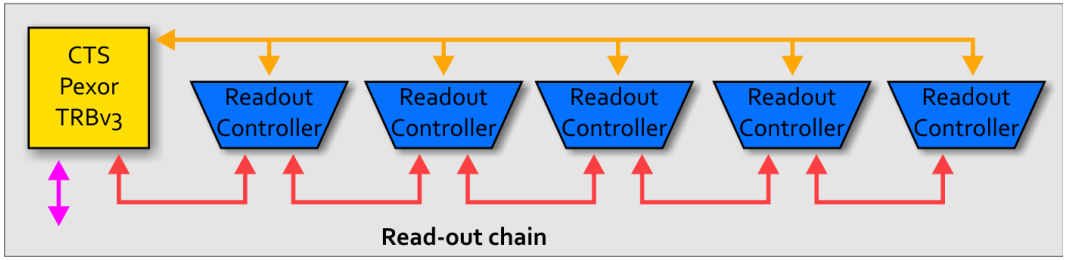
Application in Other Systems

- **Many set-up possibilities using TrbNet-DAQ**
  - Read-out chains
  - Stand-alone set-ups
  - PC-based DAQ





GbE Ethernet
LVDS / TTL
TrbNet optical link
Front-end connection
PCI Express v1.1

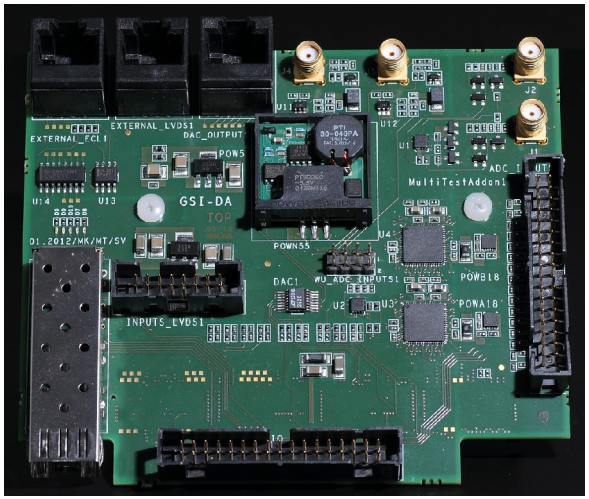


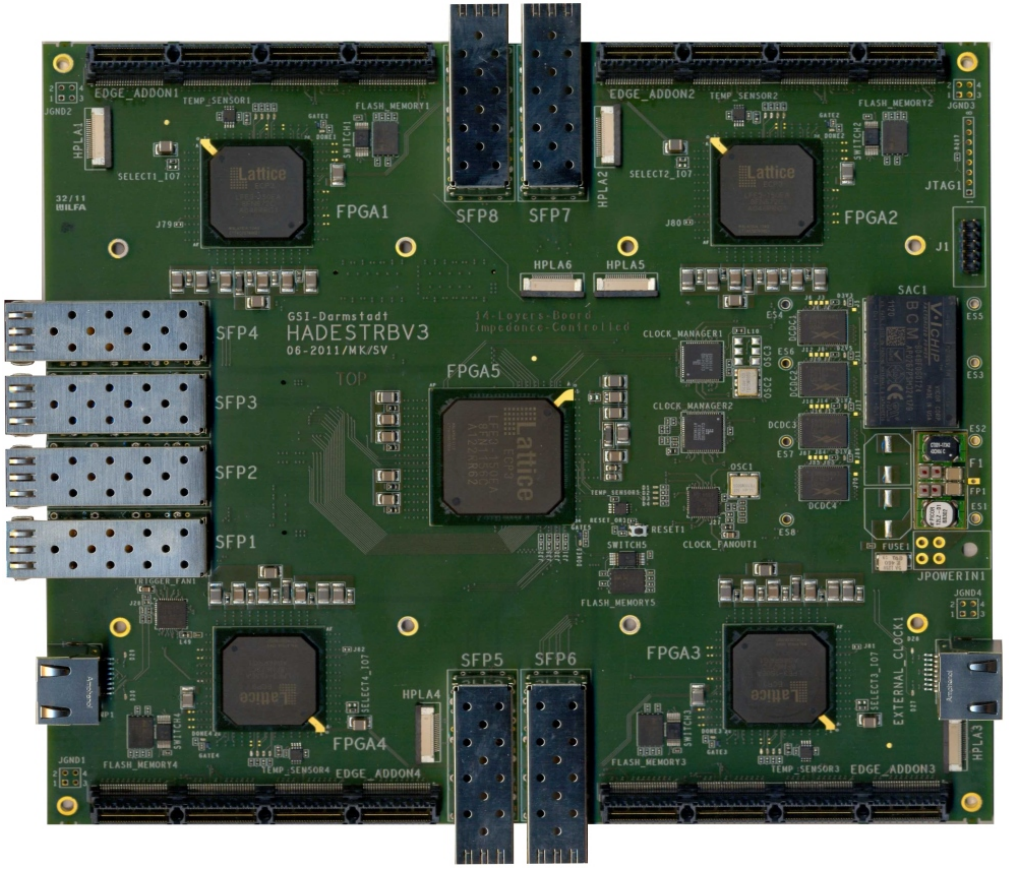
- RPC-PET (Univ. Coimbra)
- CBM-MVD (Univ. Frankfurt)
- … and many more

New Developments

- **TRB3**
  - Multi-purpose FPGA platform
  - Extension via AddOn-Boards
  - 200 I/O per FPGA
  - Up to 32 x 3.2 GBit/s
  - Stand-alone operation possible*
  - Full control via GbE

- In cooperation with
  - PANDA-DIRC (GSI / Univ. Mainz)
  - PANDA-STT (Univ. Krakow)
  - And others

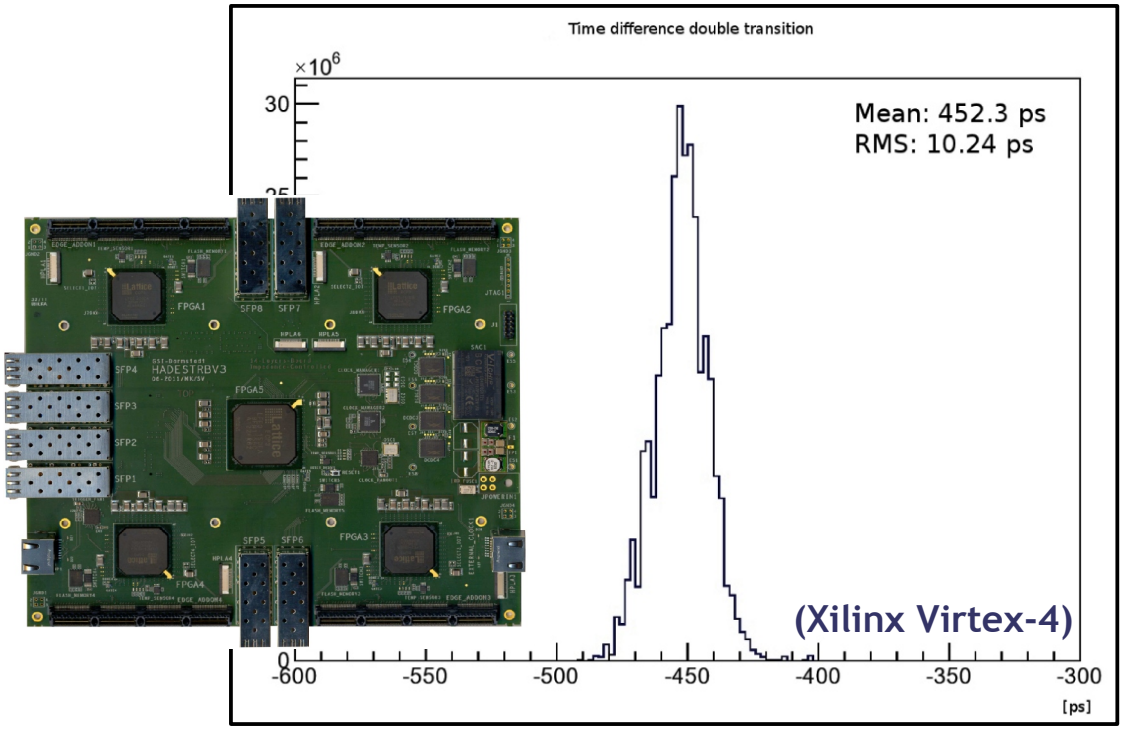


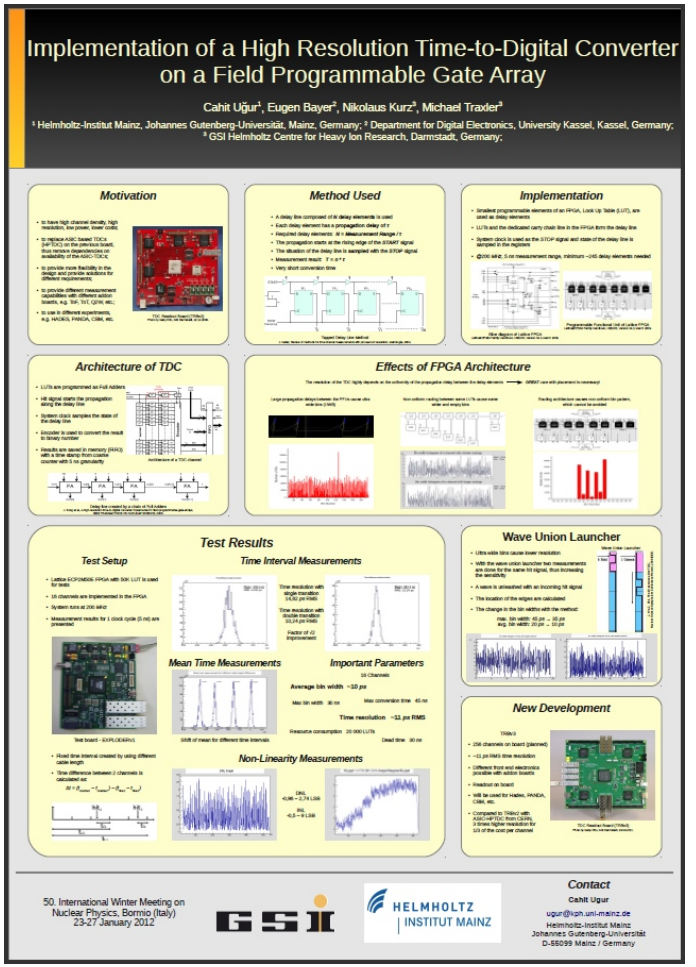


* under development

Main New Application: TDC

- **TDC designed inside FPGAs**
  - Using carry chain delays for time measurement
  - Resolution **< 15 ps**
  - **256 channel / board**



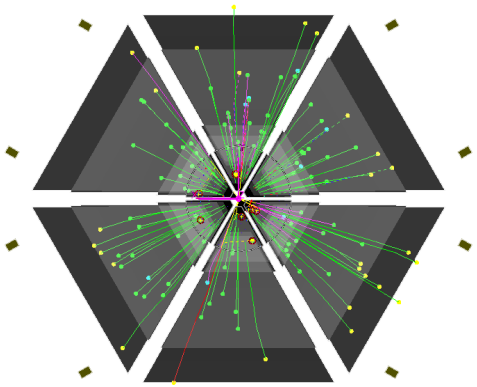


→ See poster C. Ugur - HK 53.10

Summary

- New detectors were added to the HADES set-up
- The Data Acquisition System was completely rebuilt
- Commissioning Beamtimes were conducted in 2010/11
- Successful data taking at 20 kHz event rate and 400 Mbyte/s data rate for Au-Au @ 1.1 AGeV

- The TrbNet concept is a versatile read-out system
- Electronics & Network System in use by several other experiments



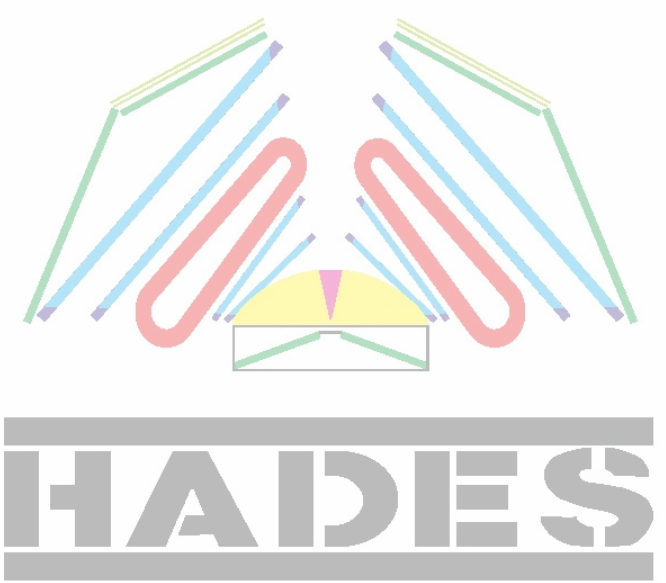
The new HADES DAQ was commissioned, design goals have been reached.

Several other experiments profit from our developments.

We are looking forward to a production beam-time starting next week...

The New Trigger and Data Acquisition System of HADES

J. Michel for the HADES Collaboration
Institut für Kernphysik, Goethe-Universität, Frankfurt
j.michel@gsi.de



GOETHE UNIVERSITÄT FRANKFURT AM MAIN

HIC for FAIR
Helmholtz International Center

GSI

This work is supported by BMBF (06FY9100I), EU FP6, GSI, EMMI and HIC for FAIR

The HADES Collaboration

The answer to life, the universe, and everything else...

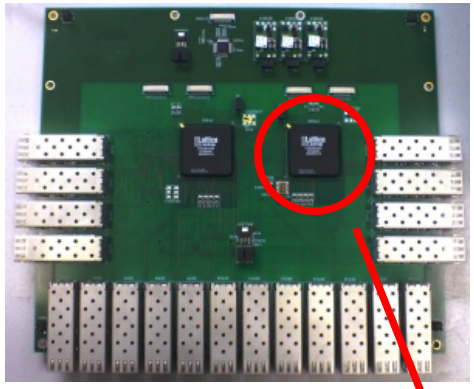
… is not part of these slides. Anyways, here is the backup stuff

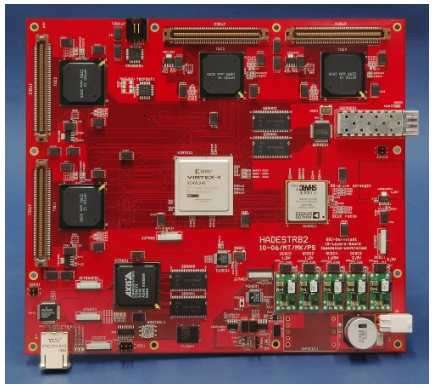
Electronics: Overview

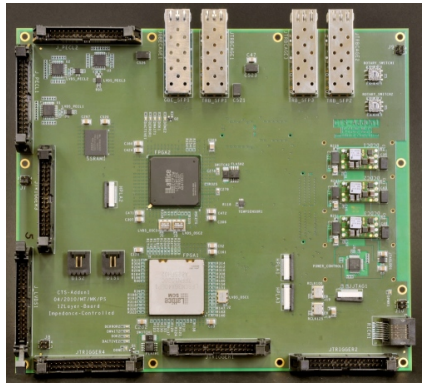
- All boards are based on common building blocks
  - FPGA, optical link
- Only difference: front-end dependent, analog part

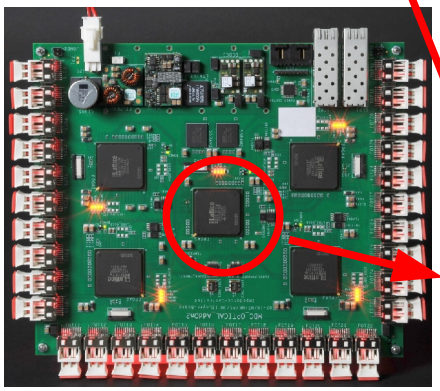
Network Infrastructure

Front-end Boards

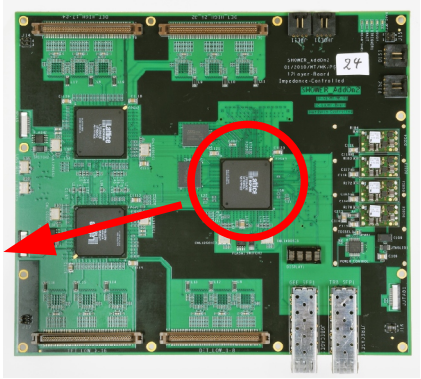






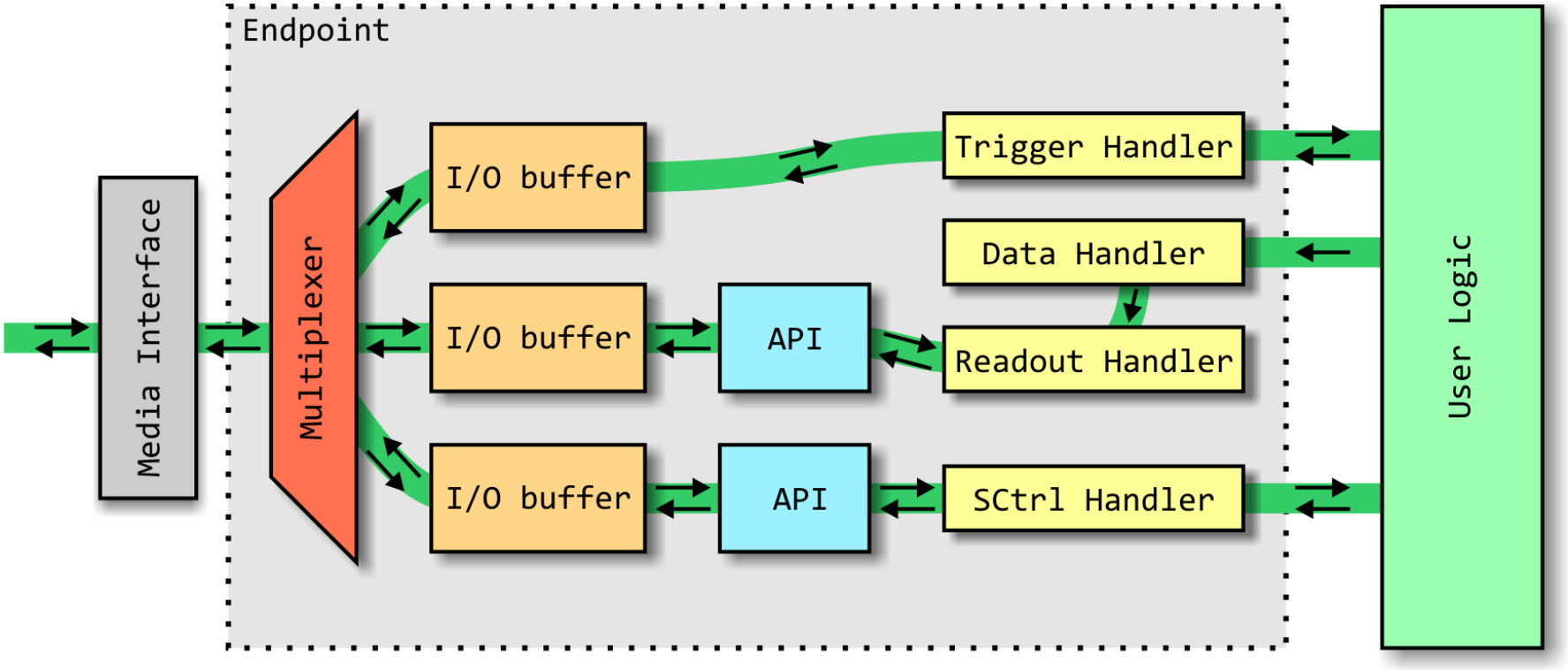


>95% identical code



Network Infrastructure

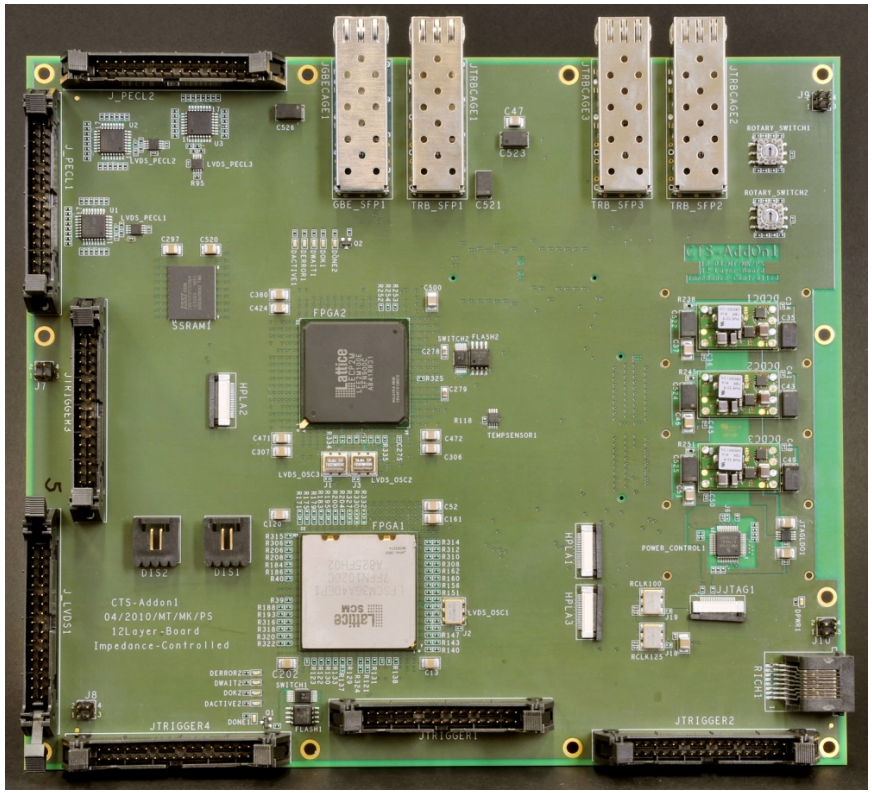
- **Very different types of data are transported on one data link**
  - Low latency (< 5 us), small sized trigger information
  - Long event data streams (up to 40 kByte / event / frontend)
  - Low priority slow control (>1 MB/s)
- **Switching between channels within 100 ns (2GBit/s) / 500 ns (250 MBit/s)**



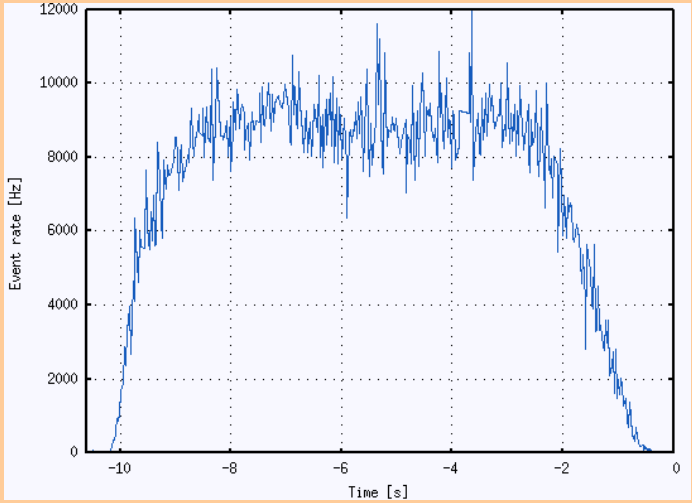
Central Trigger System

- Controls the complete read-out
- Generates trigger information

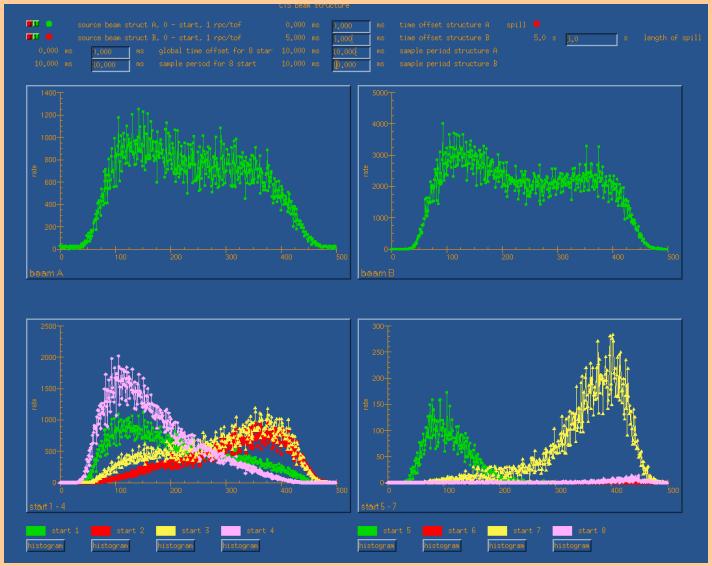
- 4 Optical links (TrbNet, Gigabit Ethernet)
- 2 FPGA
  - Lattice ECP2M for read-out control
  - High-speed Lattice SCM for trigger generation
- 64 inputs sampled with > 800 Mhz
- Complex trigger conditions
  - e.g. “hit in inner start detector but not in veto detector and at least 30 particles in time-of-flight wall”
- LVDS / PECL trigger outputs



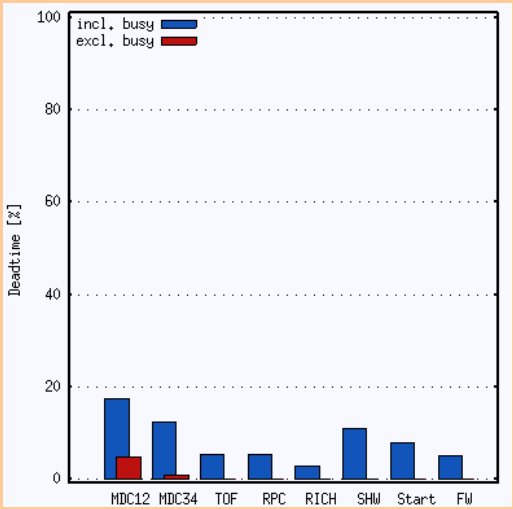
Event Rate Histogram



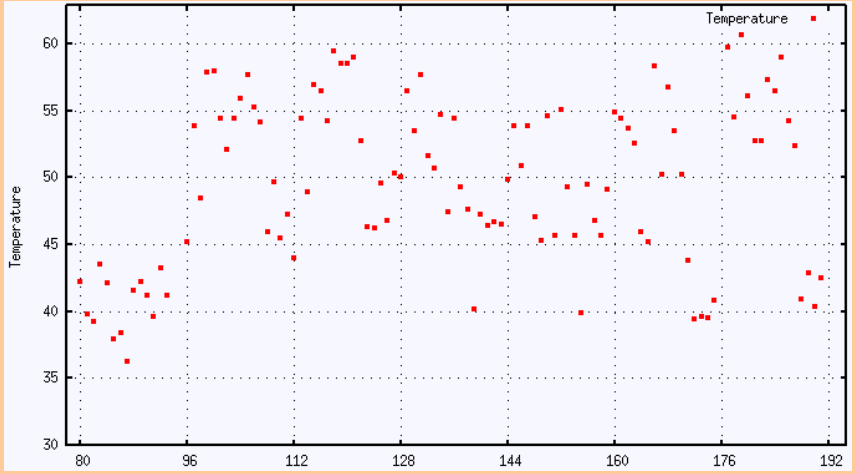
Beam Quality Monitor



Detector Deadtime



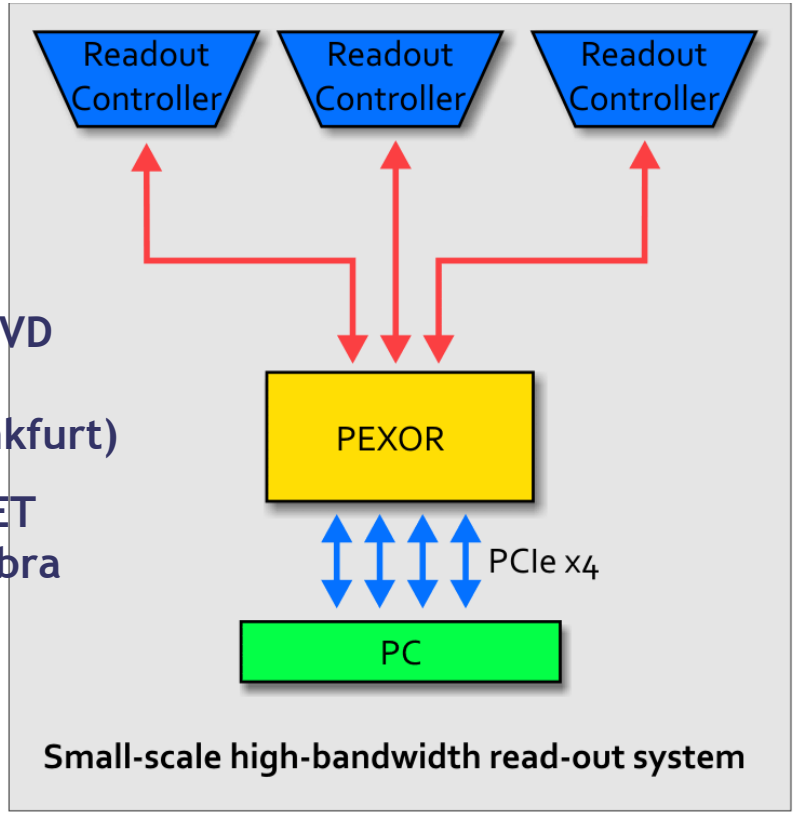
Temperature Monitoring

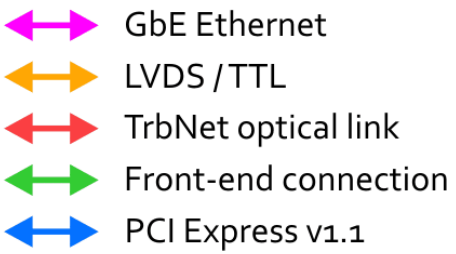


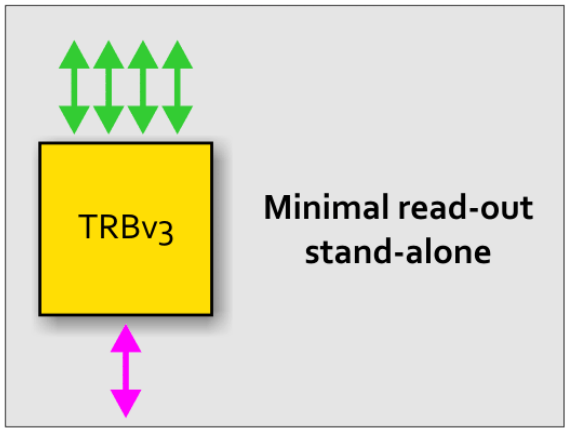
Possible Network Setups

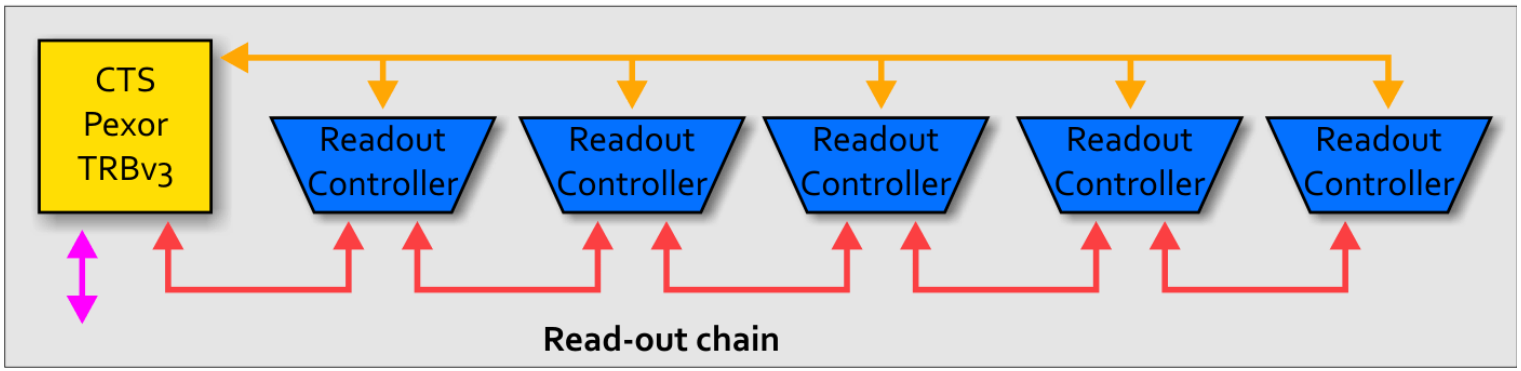
e.g. CBM-MVD prototype (Univ. Frankfurt)

e.g. RPC-PET Univ. Coimbra









Slow Control

- **Addresses are assigned (DHCP-like)**
  - Boards are identified by unique-ID chip
- **Standardized status & control registers**
  - One command to set all boards in the same state
  - Easy to get overview of network situation
- **Internal Data bus**
  - 32 bit data / 16 bit addresses
  - Single register access
  - block transfer
  - Can be split in an arbitrary number of sub-spaces
- **I/O modules like SPI, I2C, 1-wire**
  - Voltage monitoring
  - Temperature
  - Flash ROM programming
- **C-Library gives access from any PC**