A 32-Channel High Resolution Time-to-Digital Converter (TDC) in a Lattice ECP2M Field-Programmable-Gate-Array (FPGA)*†

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The development of the TDC on Xilinx Virtex-4 FPGA [1] has been continued. The dead-time could be decreased to 15 ns by pipelining. In order to test the design in experiments it was moved to the VULOM-4 boards and adapted to triggered systems. Since the differential timing signals were converted to single ended signals on the VULOM-4 board before being fed into the FPGA, a slight decrease in resolution (14 ps RMS) was observed in laboratory measurements between some channels. For this reason a new version of the VULOM-4 board is prepared with shorter single ended signal lines.

First detector measurement data were collected with the CBM setup by using 32 channels on two VULOM-4 boards. The analysis of the collected data is still ongoing. In order to explore the consequences of using a different FPGA architecture and thus increasing the knowledge of TDC designs in FPGAs the existing TDC design was adapted to the Lattice ECP2M FPGA.

A 32-channel TDC was implemented on a Lattice ECP2M. The fine time interval calculations were achieved by Tapped-Delay-Line method using dedicated carry-chain lines. A Multi-bit adder structure was used in order to form the delay line. Each channel has an individual fine counter, an encoder and a First-In-First-Out memory block (FIFO). A common coarse counter generates time flags for the time information of each conversion. The time-to-digital conversion and the data read-out were undertaken at 200 MHz and 100 MHz clock frequency respectively.

The time interval between the rising edge of a trigger signal and the rising edge of the next system clock was measured at the fine counter. The result generated by the fine counter in thermometer code [2] was converted to a binary code in the encoder and stored in the FIFO with a time stamp generated by the common coarse counter as well as a channel number. The data was calibrated offline by using the bin-by-bin calibration method [3].

In our measurements we used two channels in order to measure the time difference between two triggers. The triggers were generated by Tektronix Data Timing Generator DTG5078. Sets of measurements with different time differences were done in order to test the stability and the consistency of the TDC.

The time difference was increased logarithmically starting from zero up to one microsecond in order to observe the effects on the measured mean value and RMS. Figure 1 shows the change of the mean value with the increasing time difference in logarithmic scale. The RMS calculated for the time differences for up to two clock periods (10 ns) was 15 ps. As one transition was used in order to determine the time measurements, the time resolution was also 15 ps.

With rising time differences the resolution of the TDC decreased and reached 35 ps for 1 us time difference. This deviation is induced by the PLL used as time reference and it will be removed from the future design. Figure 2 shows the measurement results obtained within one system clock cycle with 100 ps increase.

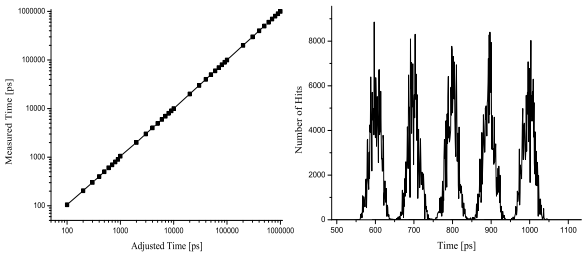

Figure 1: (a) The change of mean value over logarithmically increasing time difference (After channel offsets were cancelled), (b) Five time differences with 100 ps difference.

In order to observe the temperature dependency of the TDC, a series of measurements between 48°C and 80°C were done. The increasing temperature caused malformation of the calibration look-up-table. In parallel RMS value got worse. However, updating the calibration look-up-table overcame this problem.

Some of the important parameters of the designed TDC are as follows: Maximum bin width 48 ps, average bin width 20 ps, highest time resolution 15 ps, maximum conversion time 45 ns, dead time 30 ns, delay chain length 288.

The current results suggest that the designed TDC works very well in different FPGA architectures, e.g. Lattice ECP2M FPGA and Xilinx Virtex-4. Further tests will be done on the EXPLODER board [4].

References

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