



TRB - TestReadoutBoard

HADES Collaboration

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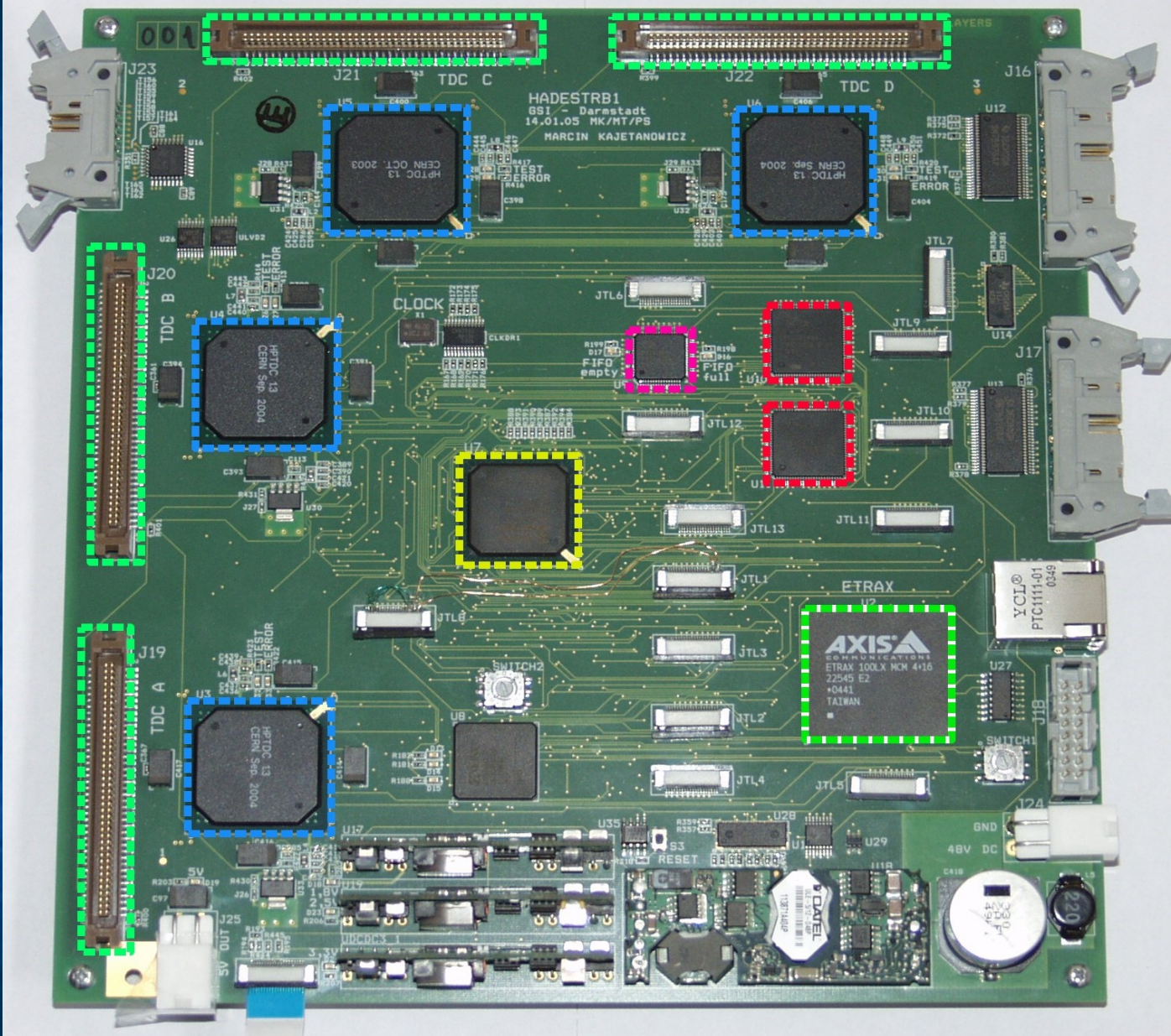
Krzysztof Korcyl

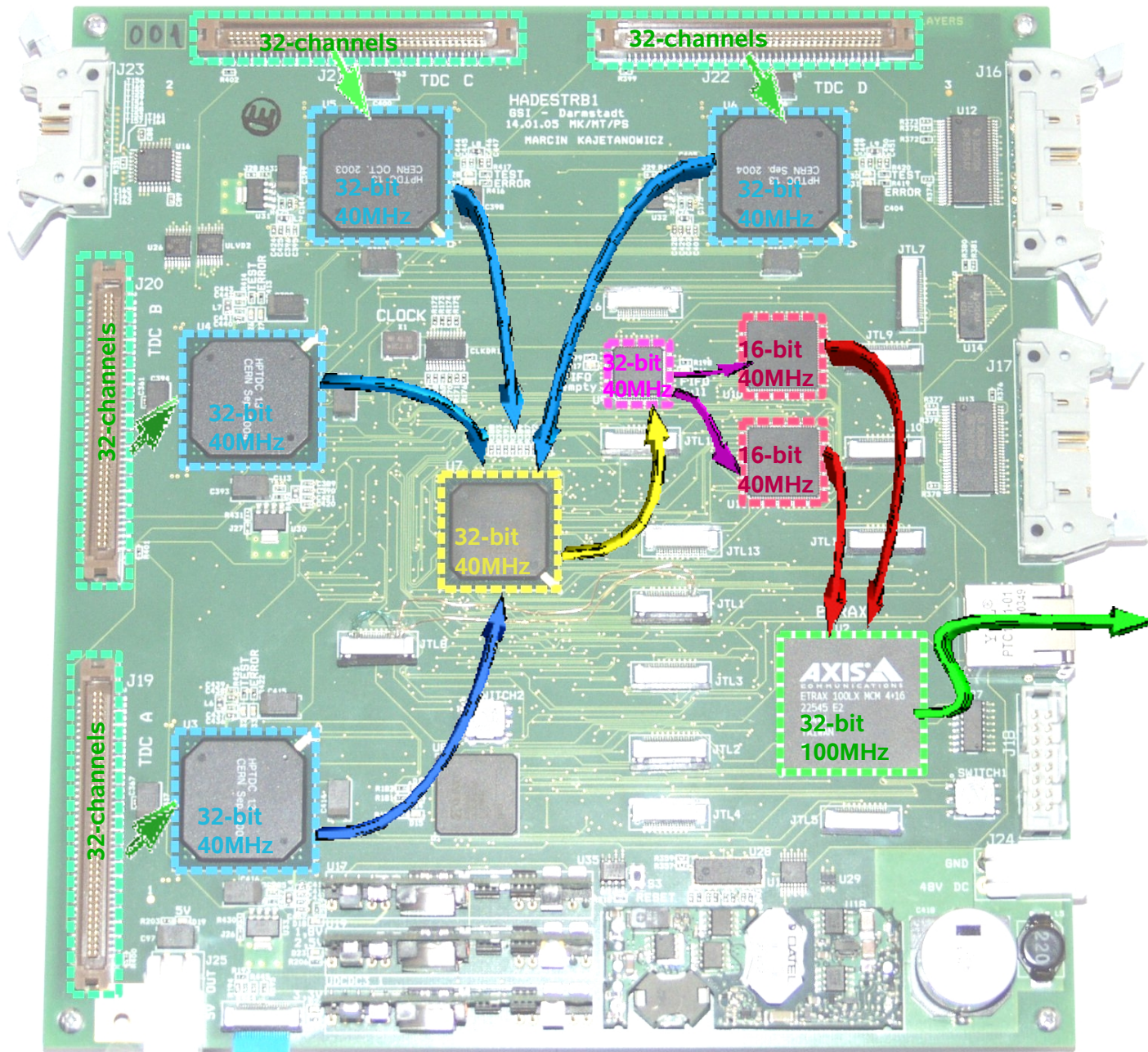
Marek Palka

Piotr Salabura

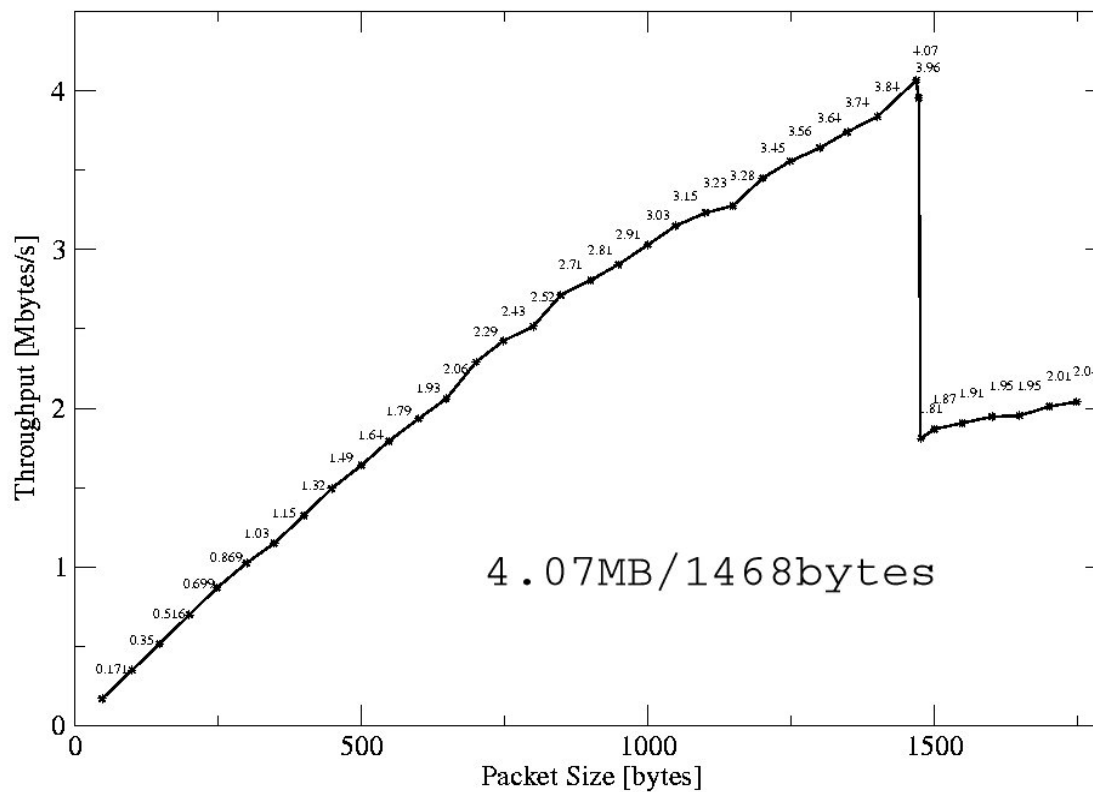
Michael Traxler

Radoslaw Trebacz



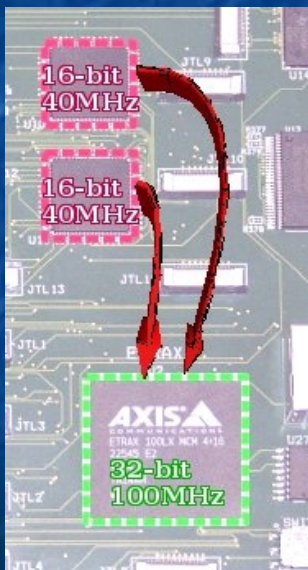
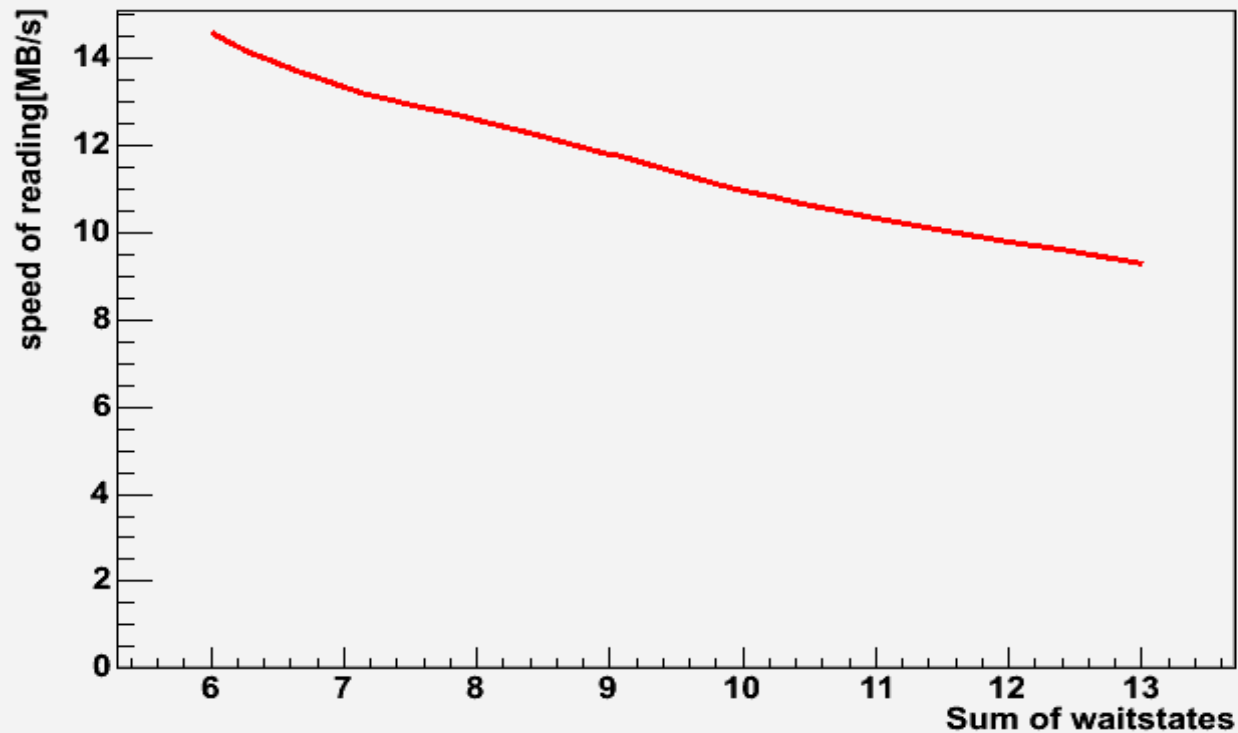


Performance of Axis Etrax Chip in UDP transfer



A wait state is a delay experienced by a processor when accessing external memory

Speed of reading vs. sum of the waitstates



Performance in the HADAQ chain

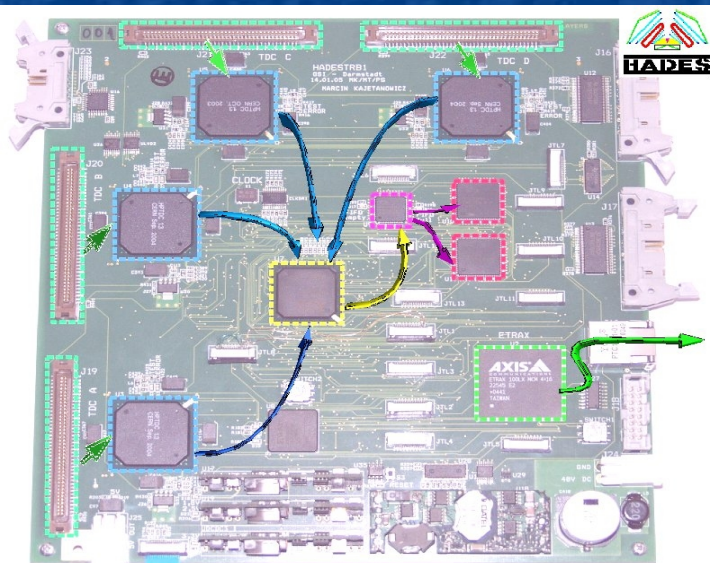
with no data, only headers and trailers: 19kHz

with 60 hits per event: 5 kHz

= 1MB/s

Main limitations:

checking the consistency of data
slow processor
no DMA

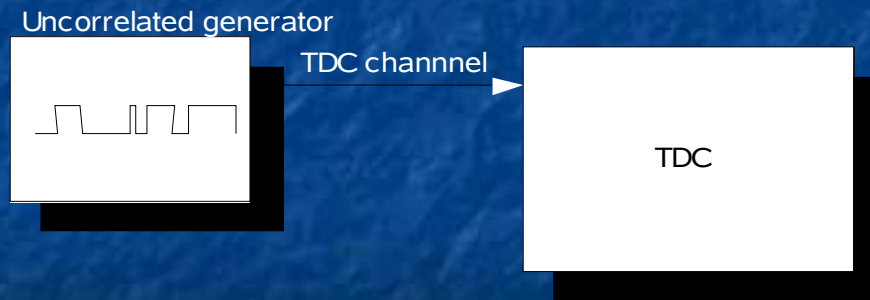




TDC readout prototype

- Differential non linearity: set up
 - Code density test:

Deliver to the TDC a large number of hits about 5M - to get significant statistics from some uncorrelated source. If we then histogram recorded times (8 LSB bits) we should see equal contents - it would be for an ideal TDC.

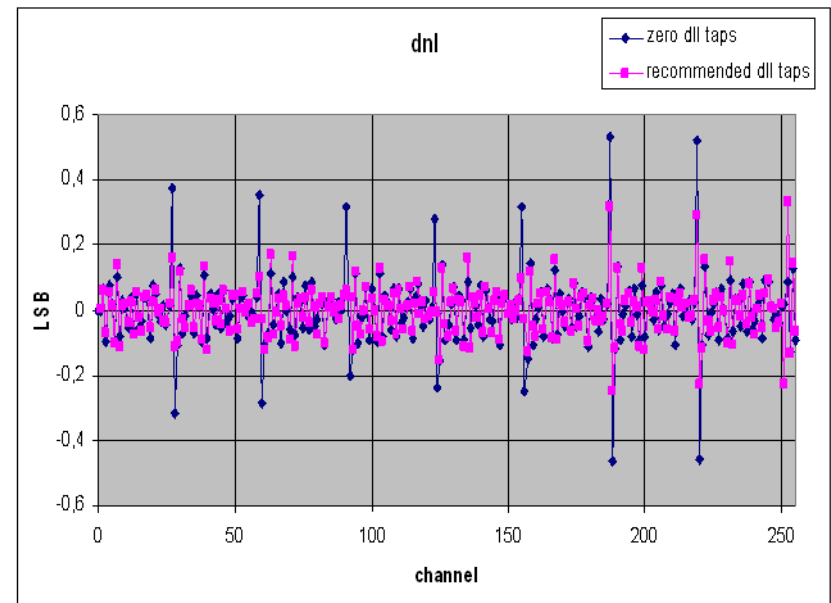
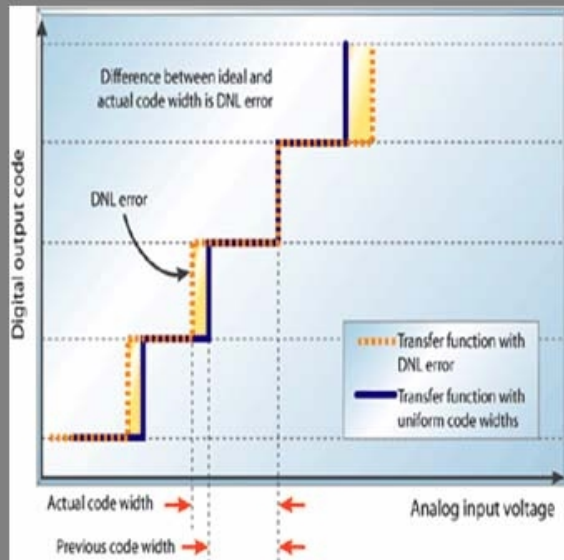




TDC readout prototype

- Differential non linearity:
 - The differential non linearity represents difference between the actual histogram bin contents of the two adjacent bins. This difference is normalized to the expected contents of a bin (to express non linearity as a fraction of the LSB).

Analog-to-Digital nonlinearities – DNL

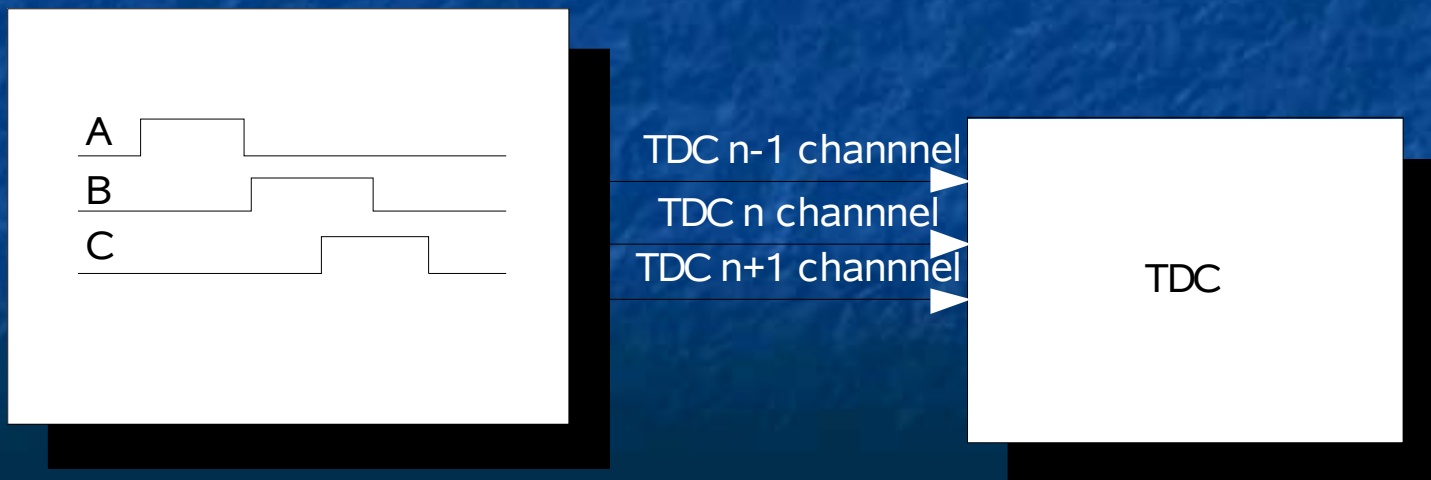




TDC readout prototype

➤ Crosstalk: setup

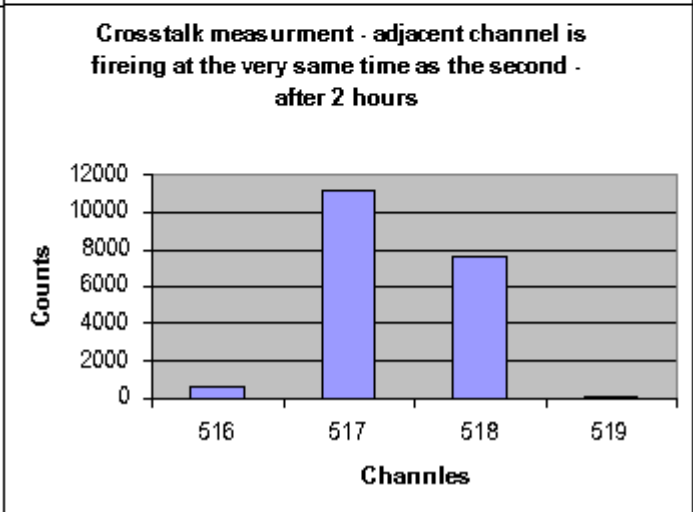
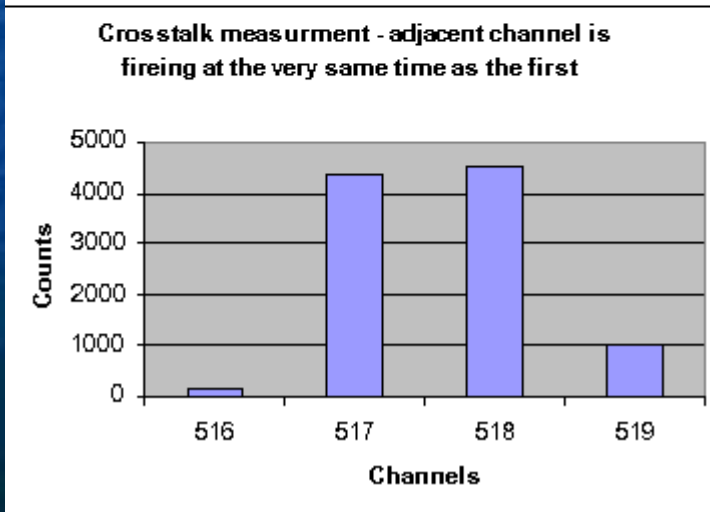
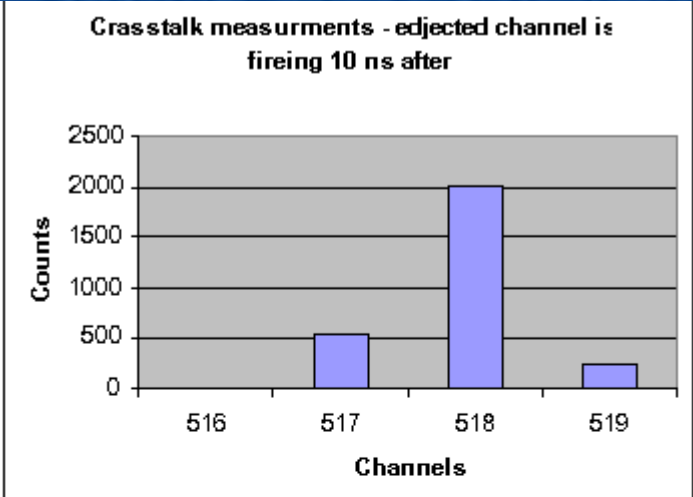
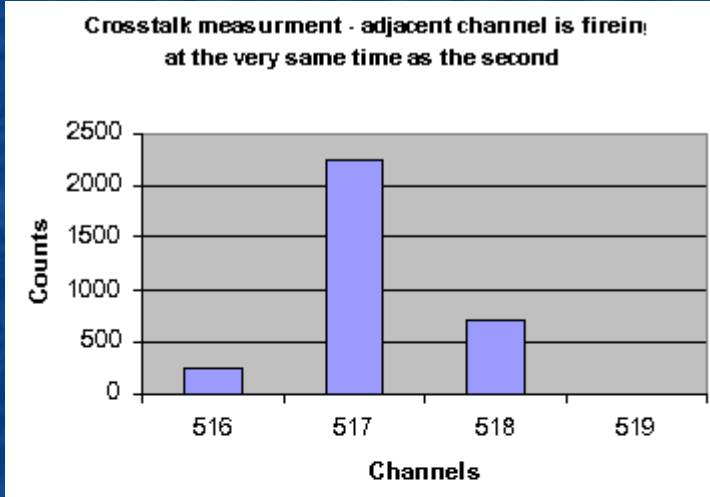
- The crosstalk is then if unwanted interference from another adjacent communications channel appears. In our case this communication channels are involved with time channels -precisely time difference between two channels.





TDC readout prototype

➤ Crosstalk

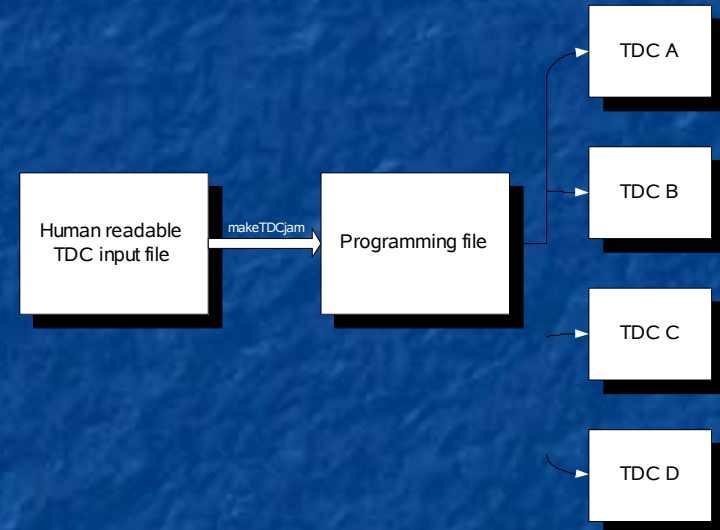




TDC readout prototype

➤ Programming TDC:

- Three steps:
 - Fill input file (human readable) with correct values,
 - Make file understood for TDC interface (`./makeTDCjam - parameters`),
 - Program TDCs (`./resetTDCdata.sh`).





TDC readout prototype

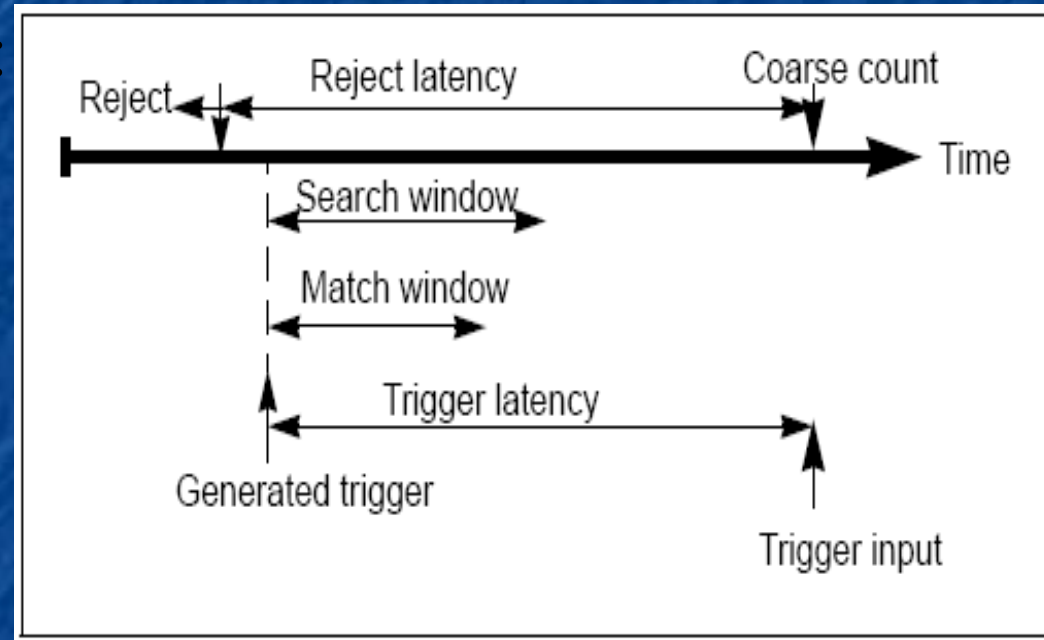
➤ What we can program:

➤ Setup register (646 bits):

- Time resolution,
- Time windows,
- HPTDC mode,
- HPTDC number...

➤ Control register (39 bits):

- Enable/disable channels,
- Using during start TDC.



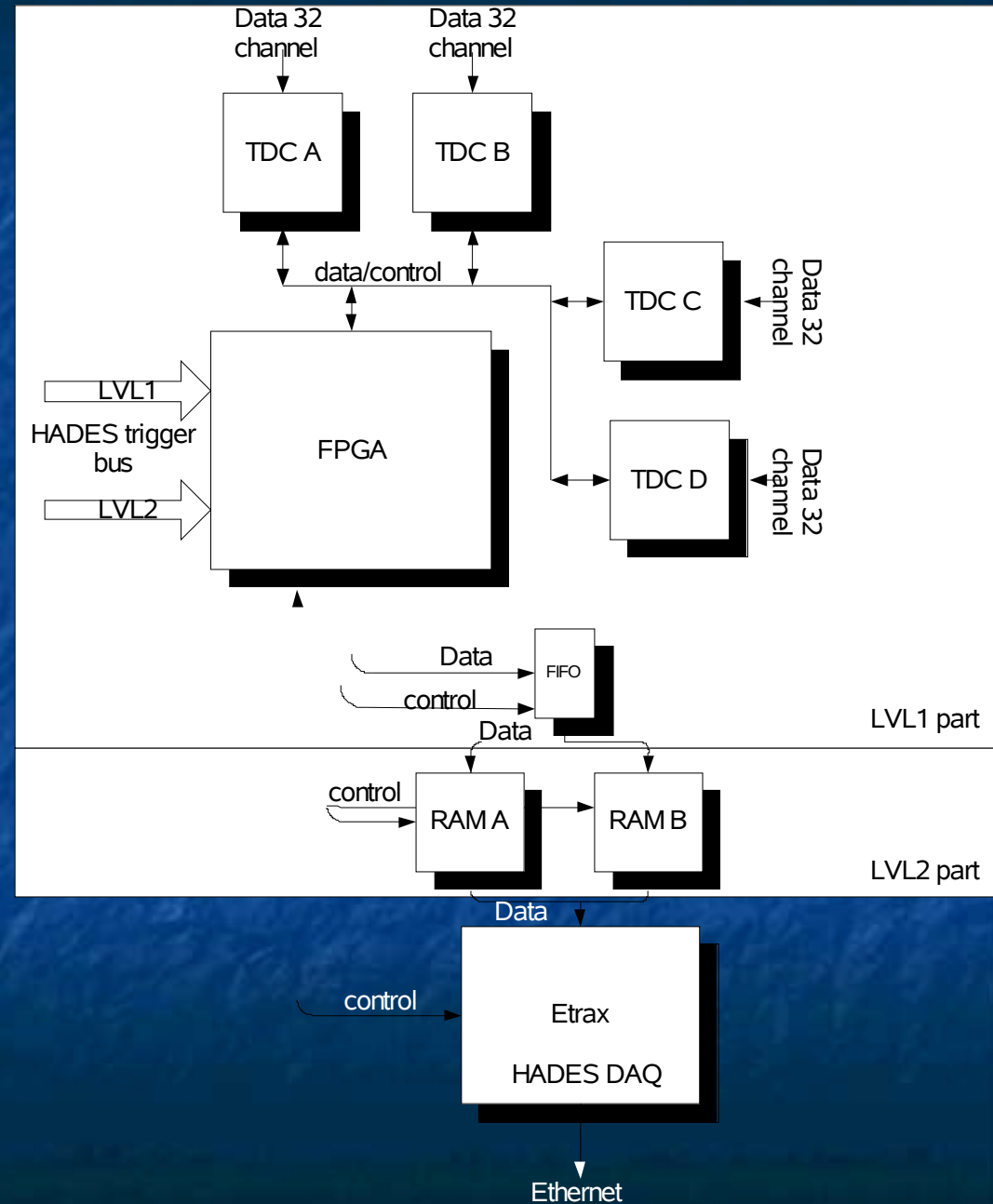


TDC readout prototype

➤ FPGA on TRB board

Cooperation with:

- HADES bus interface,
- Etrax,
- TDC,
- RAMs and FIFO.





TDC readout prototype

➤ Summary

1. System is during tests and improvements,
2. In November there was RPC detector test with beam. It was with full electronic chain (detector, FEE, TRB),
3. TRB was fully integrated into the HADES-DAQ,
4. Crosstalk should be measured in more detail,
5. New four boards has been built – we have some problems with them.

