A compact system for high precision time measurements (< 14 ps RMS) and integrated data acquisition for a large number of channels

2011 JINST 6 C12004

(http://iopscience.iop.org/1748-0221/6/12/C12004)

PUBLISHED BY IOP PUBLISHING FOR SISSA
RECEIVED: *October 15, 2011*
ACCEPTED: *November 11, 2011*
PUBLISHED: *December 2, 2011*

WORKSHOP ON FAST CHERENKOV DETECTORS - PHOTON DETECTION, DIRC DESIGN AND DAQ
APRIL 4–6, 2011, GIESSEN, GERMANY

A compact system for high precision time measurements (<14 ps RMS) and integrated data acquisition for a large number of channels

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ABSTRACT: A high precision (<14 ps RMS time resolution) and high channel density (∼256 channels) Time to Digital Converter (TDC) module (realized in FPGAs) with integrated DAQ is presented. The data is transported over up to 8 Gigabit-Ethernet or optical links with up to 3 Gb/s. Slow-Control information is transported over the same links. It can be attached directly to the detector, which allows the elimination of long cables and crate systems. The full 256 channel TDCs are expected to use approximately 30 W electrical power. The module size is 20 cm by 23 cm. Power is provided by a galvanically isolated 48 V low noise power supply. AddOn-boards adapt to the special needs of the detector to be read out, e.g. containing Charge to Width (Q2W) FEE for PMT readout.

KEYWORDS: Electronic detector readout concepts (gas, liquid); Data acquisition circuits; Electronic detector readout concepts (solid-state); Front-end electronics for detector readout

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doi:10.1088/1748-0221/6/12/C12004

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1 Introduction and motivation

Time measurements are needed in nearly all detector-system setups for experiments involving charged particle identification. Here, mainly time-of-flight applications and drift time measurements in gas detectors are of special interest. For these kinds of applications a TDC is needed in the front-end electronics. The requirements of the experiments on TDCs are constantly rising concerning the time resolution, the input signals (e.g. input rate, multi-hit capability and minimum accepted pulse width), the power consumption per channel, the channel density and finally the price per channel.

A few years ago, the only available TDCs with high time resolution ($<$ 100 ps RMS) were based on ASICs. As an example, a very powerful and versatile solution is the HPTDC developed at CERN [1]. Its multi-hit capability allows applications to encode time and charge information as a digital pulse on one channel. This removes the need for separate ADCs if the charge resolution requirements are moderate and, therefore, reduces the size, power consumption and price of the front-ends. Based on HPTDCs, a module, the TRB2 [2], was developed and is now used very successfully in several experiments and experimental setups. It has 128 TDC channels with on-board DAQ and slow control via an ETRAX-processor running Linux. Data can be transported via a 2 GB/s optical link.

With the lessons learned from the deployment of this board a new version of a TDC platform has been envisaged. Major obstacles for further applications of the TRB2 are the limitations of the HPTDC, these include the limited time resolution of around 40 ps RMS, the limited long term availability of the ASIC, the minimum pulse width of 10 ns and the limited sustained rate capability of hits. Furthermore, the ASIC is not compatible to lead-free soldering processes which makes the production of new boards more complicated.

Recent developments in designing TDCs inside standard FPGAs have been proven to be very successful [4–6] and enables the realization of a very flexible and cost effective solution for our new development of a TDC-module, the TRB3. First of all, it makes it possible to reach a time resolution of $<$ 10 ps for high-end applications. Furthermore, the FPGA-TDC-implementation has the advantage of being flexible to adapt to different needs, e.g. to reach a compromise between resource usage and time-resolution. The specific features can be adjusted by mere reconfiguration of the FPGAs compared to a full re-design cycle in the case of ASIC-based TDCs. Another important point is the pulse width limitation of traditional TDC designs. In the FPGA-TDC the input

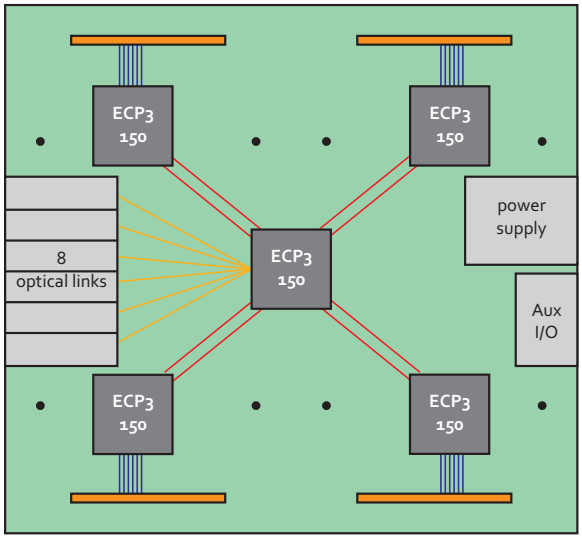

Figure 1. Block diagram of the TRB3. 4 FPGAs take over the TDC functionality. The central FPGA combines the data and sends it to the event builder PC.

signal can be split and fed to two or more TDC-channels in order to remove the pulse width limit completely.

Apart from the < 10 ps time resolution the performance of the TDC designs in FPGAs were tested in detail. The temperature dependence of the mean value of the measured distribution was determined to be 8 ps/K. The RMS increased by 1 ps/K. Additionally, the TDC was tested while changing the supply voltage. The mean changed by 0.4 ps/mV and the RMS decreased by 0.02 ps/mV. At the same time each measurement of the TDC is fed into the calibration table. Using this sliding calibration table, the measured mean and RMS values remained stable, while varying the operating conditions (30 °C - 85 °C and $\pm$50 mV supply voltage).

We were not able to measure crosstalk effects inside the FPGA-TDC (< 2 ps), which is only valid for carefully routed PCBs and signals fed by twisted pair cables.

2 Architecture and features of the TRB3

The TRB3 contains only the main FPGA infrastructure, keeping in mind to be flexible and easily adaptable to different detectors. All functions required are implemented in the FPGAs, making the Linux-CPU and DSP, which can be found on the TRB2, obsolete. A block diagram of the TRB3 is shown in (figure 1) and the assembled module is shown in (figure 2).

The new TDC module is based on large (150k LUTs) but cost effective FPGAs (ECP3 family from Lattice Semiconductor). Multichannel FPGA-TDC designs have been developed already on different boards and the results suggest that up to 64 high-rate multi-hit TDC channels can be integrated in one ECP3-150 FPGA. Hence, the TRB3 board containing four FPGAs will have 256 TDC channels with a time resolution of around 14 ps RMS.

Each of the TDC-FPGAs is equipped with a 208-pin connector (QMS-series from Samtec). This high-density and high-speed connector does not only transport the timing signals but can also be used to transport application specific data.

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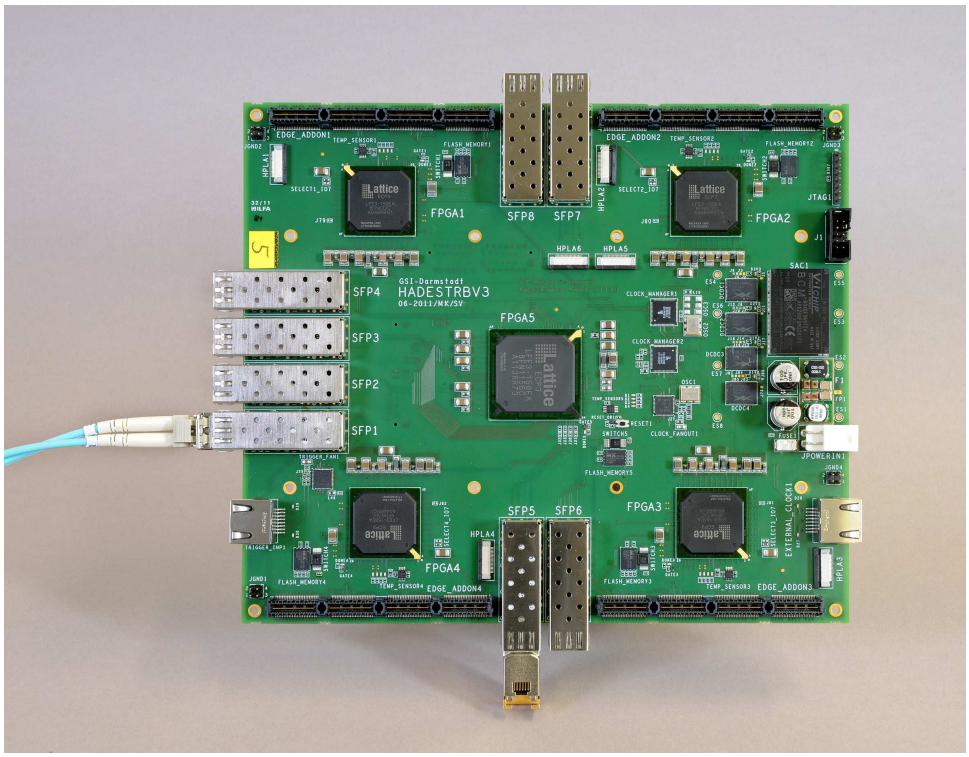

Figure 2. The assembled TRB3 module. The size is 20 cm by 23 cm.

Small AddOn-PCBs plugged onto the TRB3 provide the necessary connectors and additional components. Here, additional FEE for the detector signals to be digitized such as ADCs can be placed. Serial data links with up to 3.2 GBit/s are foreseen as well as interfaces for fast, source-synchronous data interfaces with up to 800 MBit/s per like DDR memories.

The fifth and central FPGA collects and combines all data and sends it to data servers via 8 SFP transceivers. These connections can be configured as GbE-links to be connected directly to off-the-shelf Ethernet switches or as optical links running the TrbNet protocol [3] running at 2 Gbit/s or more. The TrbNet protocol provides a low latency transport for trigger, data and slow-control information, multiplexed on one optical fiber.

The versatility of the TRB3 is further improved by two high speed connectors (160 pins + power) on the back side that are connected to the central FPGA . Here, another AddOn can be connected, for example to adapt to different kinds of interfaces for data transport and/or controls.

The on-board features include a board-wide distribution of high-precision trigger and clock signals. The clock can be provided either by an on-board oscillator or can be supplied externally, e.g. to build a synchronous system with several front-ends. The power to all components is provided by a 48 V galvanically separated DC/DC converter included on the PCB.

A bi-directional bridge between the Gigabit Ethernet and TrbNet links allows the transport of detector data to remote servers and the receival of control messages. Hence, the setup for small applications can be kept small, as only a TRB3, a 48 V power supply and a standard PC is needed to run the TRB3 TDC and DAQ system.

One of the applications for the TRB3 is the read-out of photo-multiplier tubes (PMTs) and

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micro-channel plate detectors (MCPs). For these detectors front-end electronics has been developed. Here, the detector signal is converted into a fast, high resolution LVDS signal. The timing is encoded as the rising edge of the pulse while the integrated charge is encoded as the length of the pulse.

3 Conclusion

A very versatile digital read-out board with high channel density has been developed providing high precision TDC channels as the main functionality. High bandwidth (several hundred MByte/s) DAQ functionality is included as well to form a stand-alone module which can be mounted on the detector. The AddOn-board concept allows the connection to many different kinds of detectors, e.g. the FEE for standard PMTs, fast RPC signals and fast diamond signals have been developed and are proven to work within the HADES experiment. Many new applications are planned (PANDA: Barrel DIRC, Straw Tubes, etc.) to be realized soon.

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