

A General Purpose Trigger and Readout Board (TRB) for HADES and FAIR-Experiments *

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A general-purpose trigger and readout board (TRBv2) with on-board DAQ functionality is currently being developed as a replacement of the existing HADES electronics (DAQ and parts of the FEE) as well as for the PANDA Mini Drift Chamber (MDC) readout [1]. The first version has been successfully integrated into the data acquisition of the HADES detector (TRBv1 [2]). While the main application of the TRBv1 was to be a 128-channel Time to Digital Converter (TDC) electronics based on the HPTDC [3] (we achieve $\sigma = 40$ ps resolution) to read out the HADES-RPC-detector, the TRBv2 has been designed in a way to be detector independent and thus may serve for any high-speed data acquisition by using a flexible add-on board concept.

To broaden the spectrum of possible applications in future DAQ-systems, we added a very high data-rate digital interface connector (15 Gbit/s). It gives the possibility to mount add-on boards to the TRBv2 which then provide the detector-specific interfaces (special connectors) or FEE (like ADCs) and additional computing resources (FPGAs).

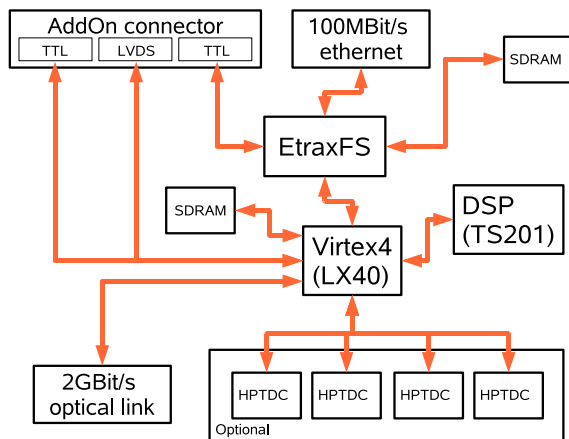


Figure 1: The TRBv2. It features 4 HPTDCs (128 channels, optional), an Etrax-FS-Processor [4] with 128 MBytes memory, Ethernet-connectivity, an optical link with 2 Gbit/s, programmable logic (Virtex 4 LX40) and a Tiger-Sharc DSP (500 MHz, 24 MBit memory, 4 linkports).

In addition, the TRBv2 provides an optical link (2 Gbit/s) as a replacement of the HADES trigger bus

and for high speed data transport (as required for example by PANDA), a large FPGA (Xilinx Virtex 4 LX40 + 128 MBytes RAM) and a TigerSharc DSP can be used as on-board resources for trigger and on-line analysis algorithms.

The TRBv2 uses an Etrax-FS processor [4] for DAQ and slow-control functionality. The processor runs a standard linux 2.6 kernel in the 128 MBytes of memory and is directly connected to the 100 Mbit/s Ethernet. The integrated three co-processors (each 200 MHz) allow a high IO bandwidth without main CPU intervention. The TRB will support EPICS to allow the integration into the HADES Slow-Control System (common project with the EE-department).

An additional board has been built (HadCom), which is used to test many features of the Etrax-FS-Processor [4] as well as the communication interface between the new trigger and readout board network (TrbNet) with the existing HADES-electronics. The TrbNet will be mainly based on the 2 Gbit/s optical links but also allows the integration of VME-CPU's, the add-on boards and the front end electronics in a standardized way.

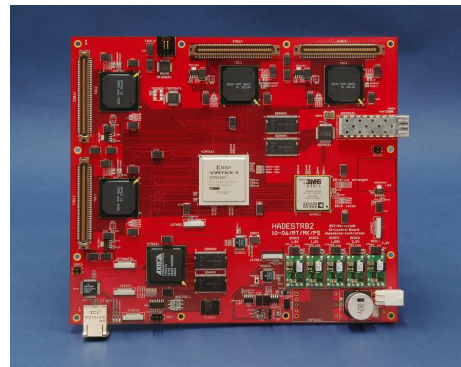


Figure 2: The prototype TRBv2 module.

References

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- [2] M. Traxler, 128 channel high resolution TDC with integrated DAQ-system, GSI Scientific Report (2005) 281
- [3] HPTDC, J. Christiansen, Digital Microelec. Group, CERN
- [4] ETRAX, AXIS Communications, Sweden

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