A 16 Channel High Resolution (<11 ps) Time-to-Digital Converter in a Field Programmable Gate Array

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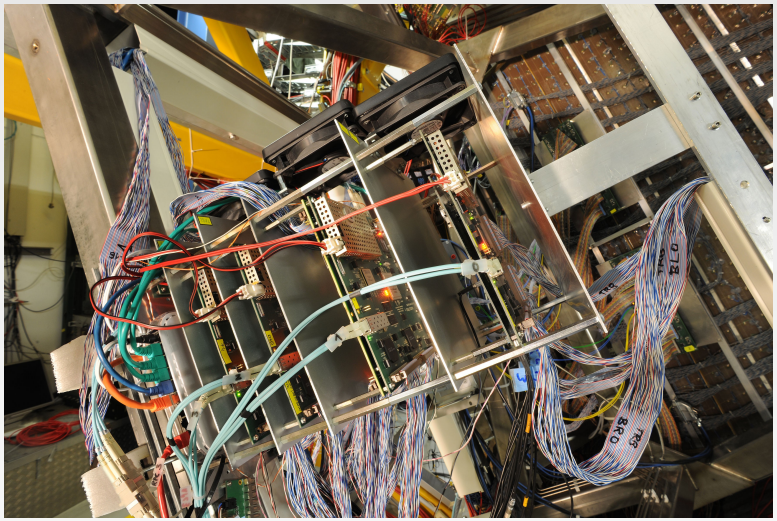
Outline

- Introduction - Motivation
- Background
  - Architectural methods
  - Time interval averaging method
- Implementation of Tapped-Delay Line
  - Architecture of Time-to-Digital Converter
  - Architectural effects of FPGA
  - Wave union launcher
- Measurements
  - Static error & resolution
  - Resource consumption & important parameters
- Conclusion & Outlook

Introduction - Motivation

- Motivation
- Area of application; HADES, PANDA, Daisy, CERN etc.
- Purpose of the project



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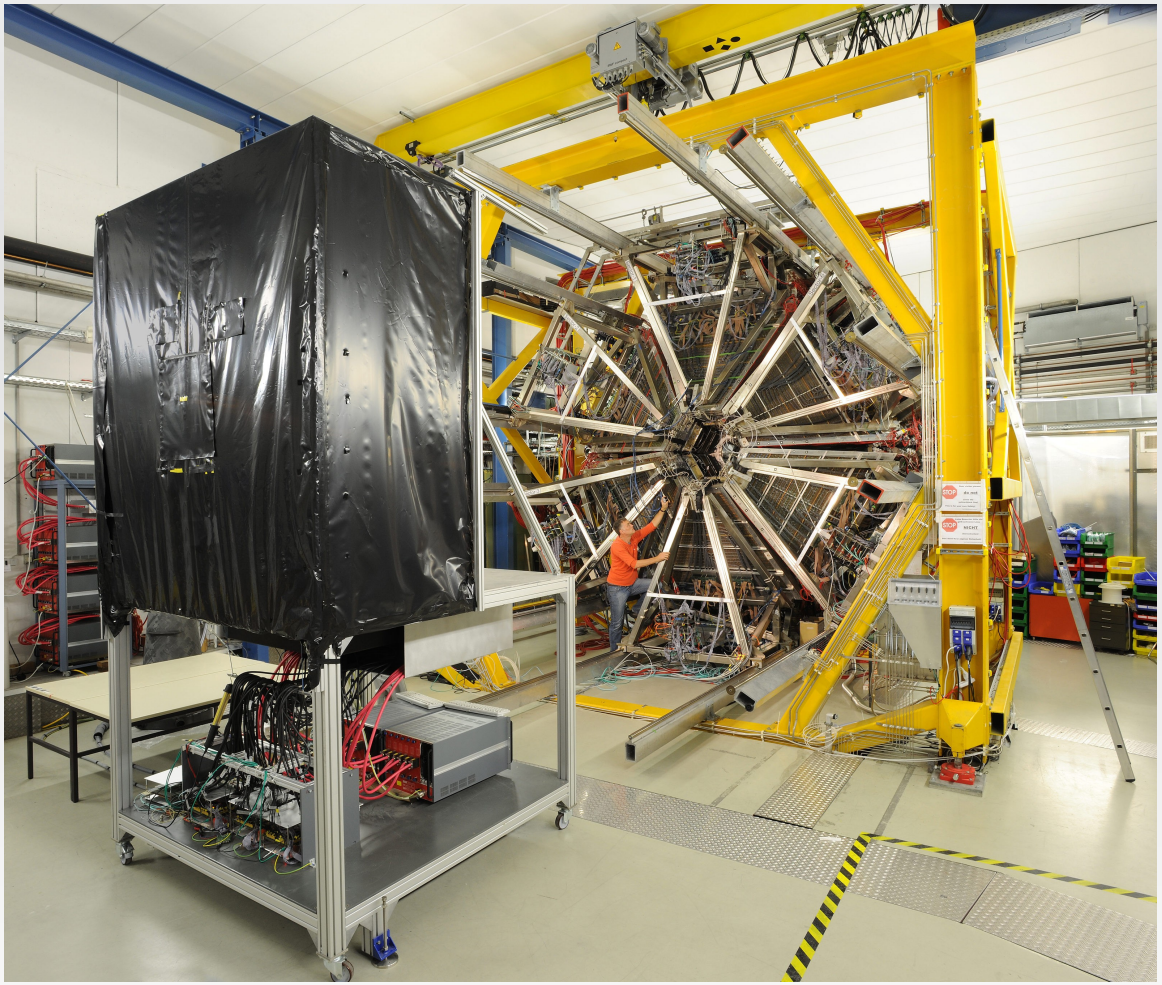

[1]

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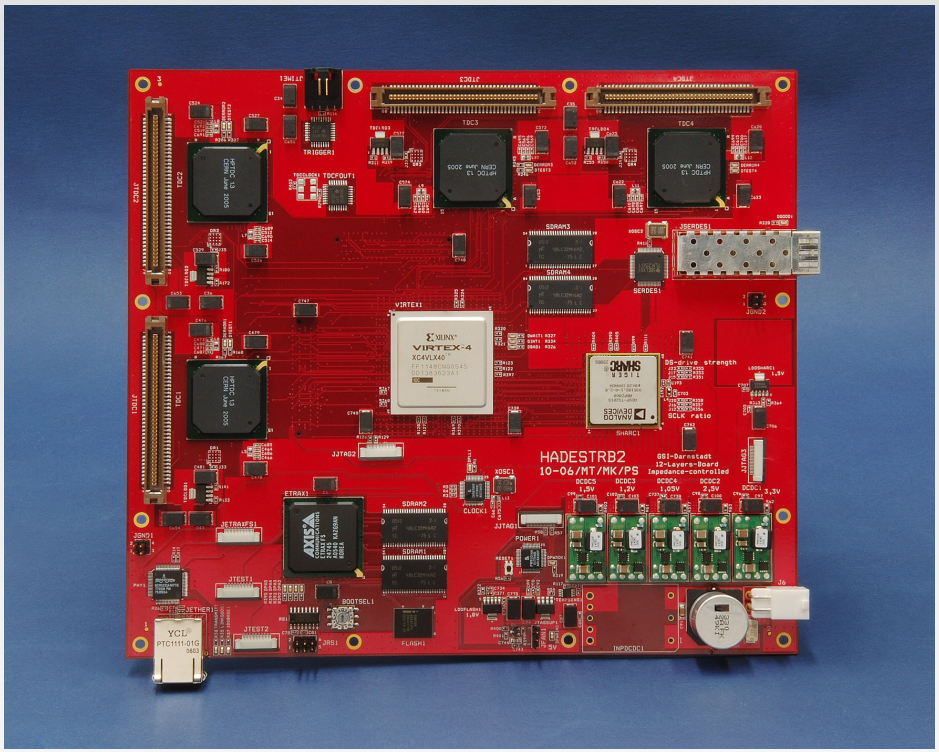

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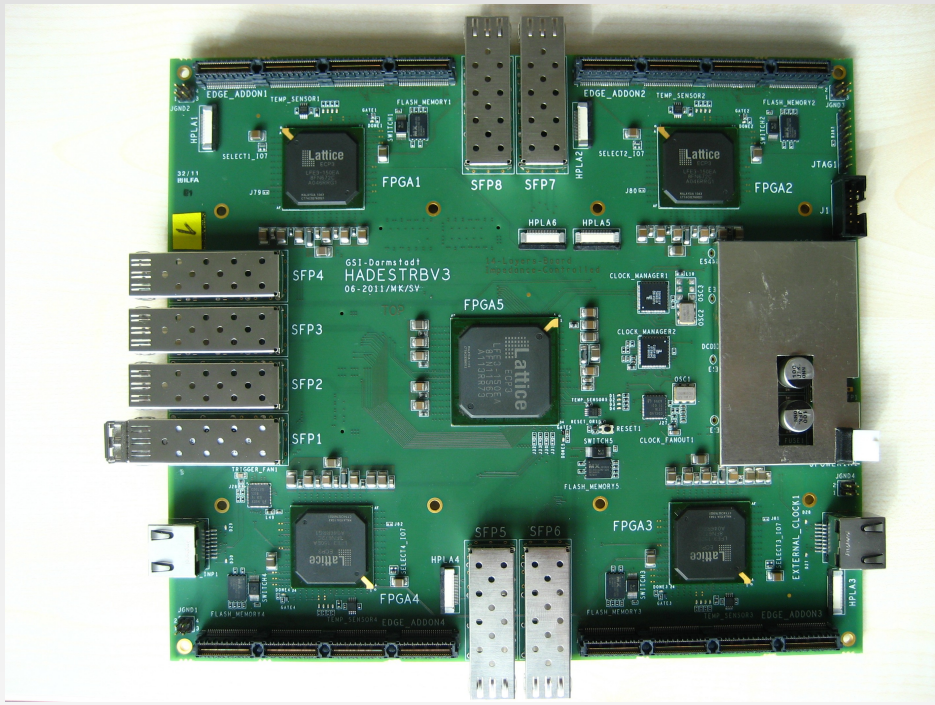

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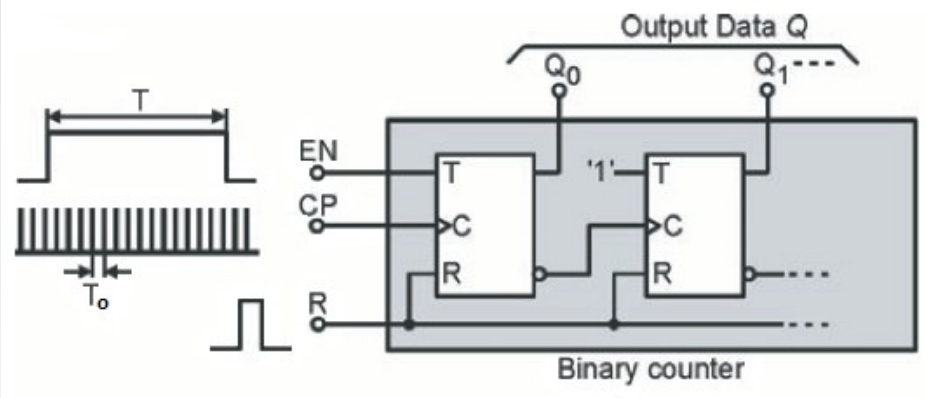
Architectural Methods

- Coarse measurement method
- Fine measurement methods
  - Time stretching
  - Double conversion
  - Vernier method
  - Tapped delay line method
- Interpolation methods



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Tapped Delay Line Method

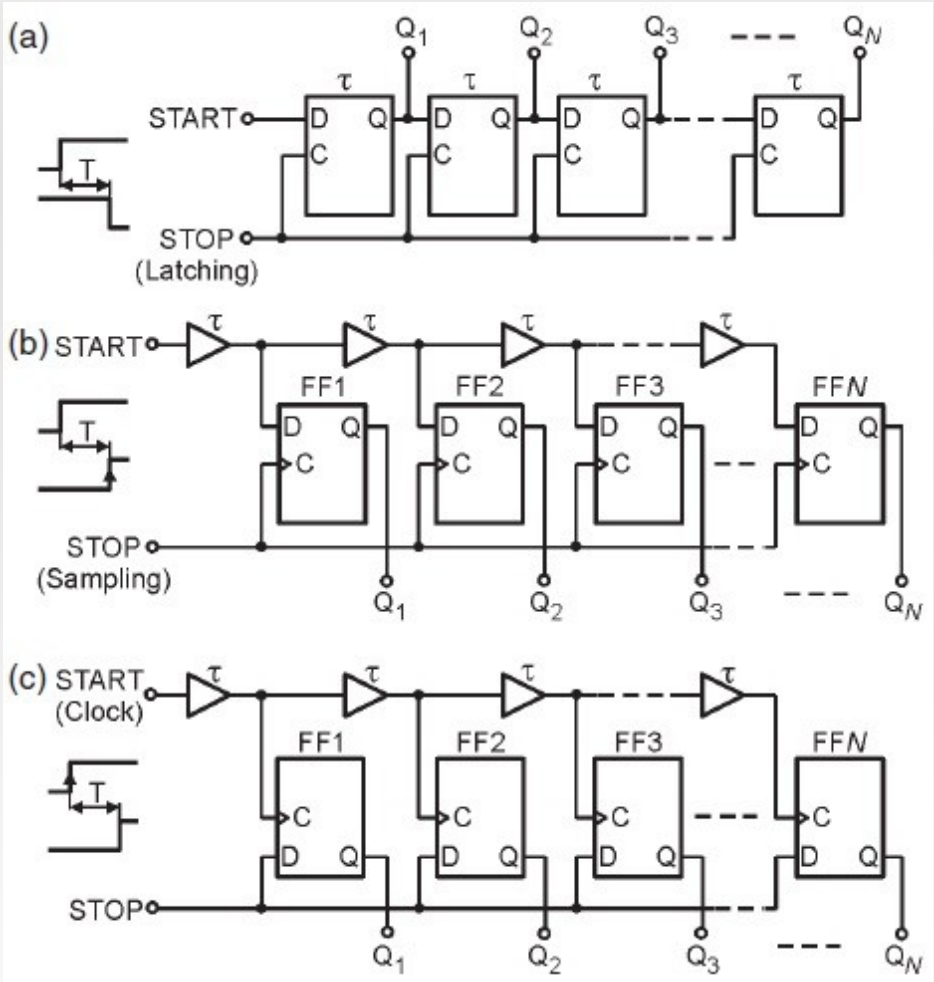
- Composed of a number of delay elements with propagation delay of τ
- Measurement result:

$$T = n.\tau$$

- Thermometer code to binary code converter is needed
- Fast conversion time
- Number of delay elements:

$$N = MR/\tau$$

MR: Measurement range



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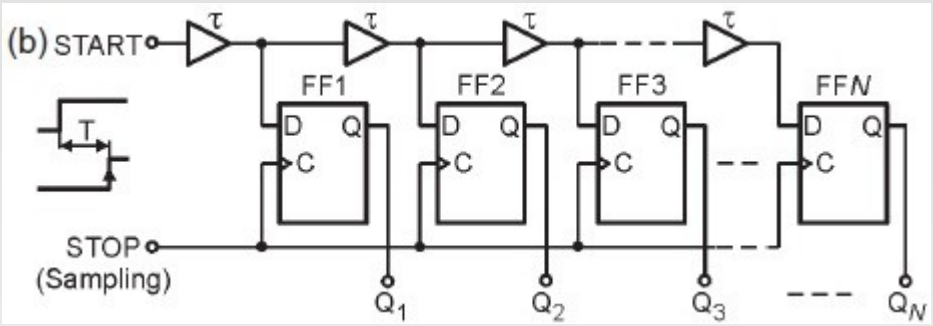
Architecture of Time-to-Digital Converter



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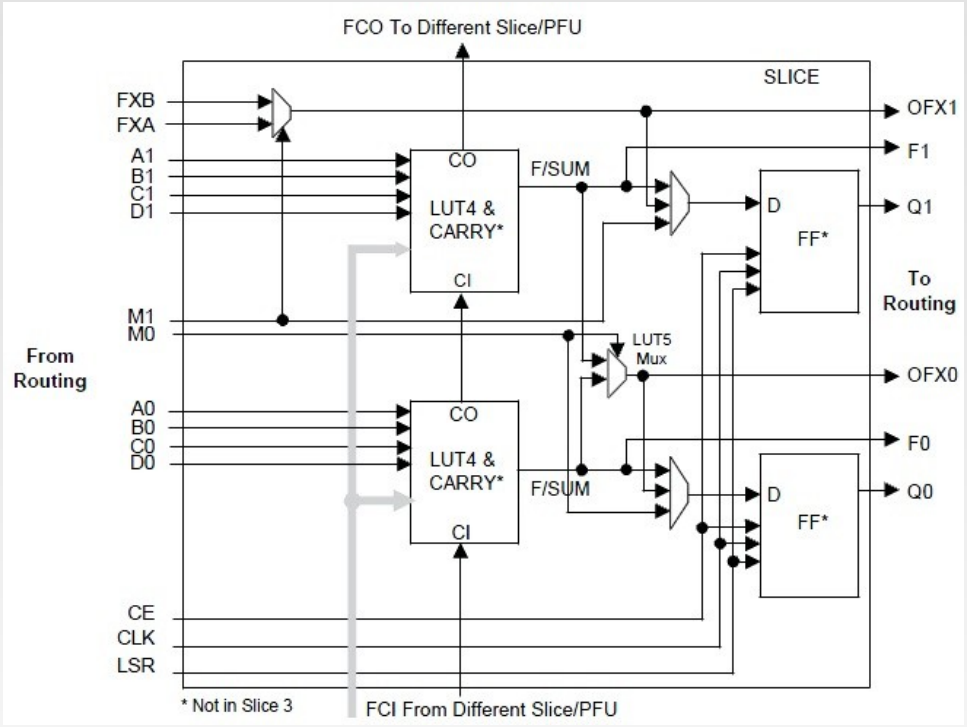
- LUTs used as delay elements
- Fast carry-chain structure
- Registers exist in the same slice



Lattice ECP2M FPGA Slice Diagram [4]

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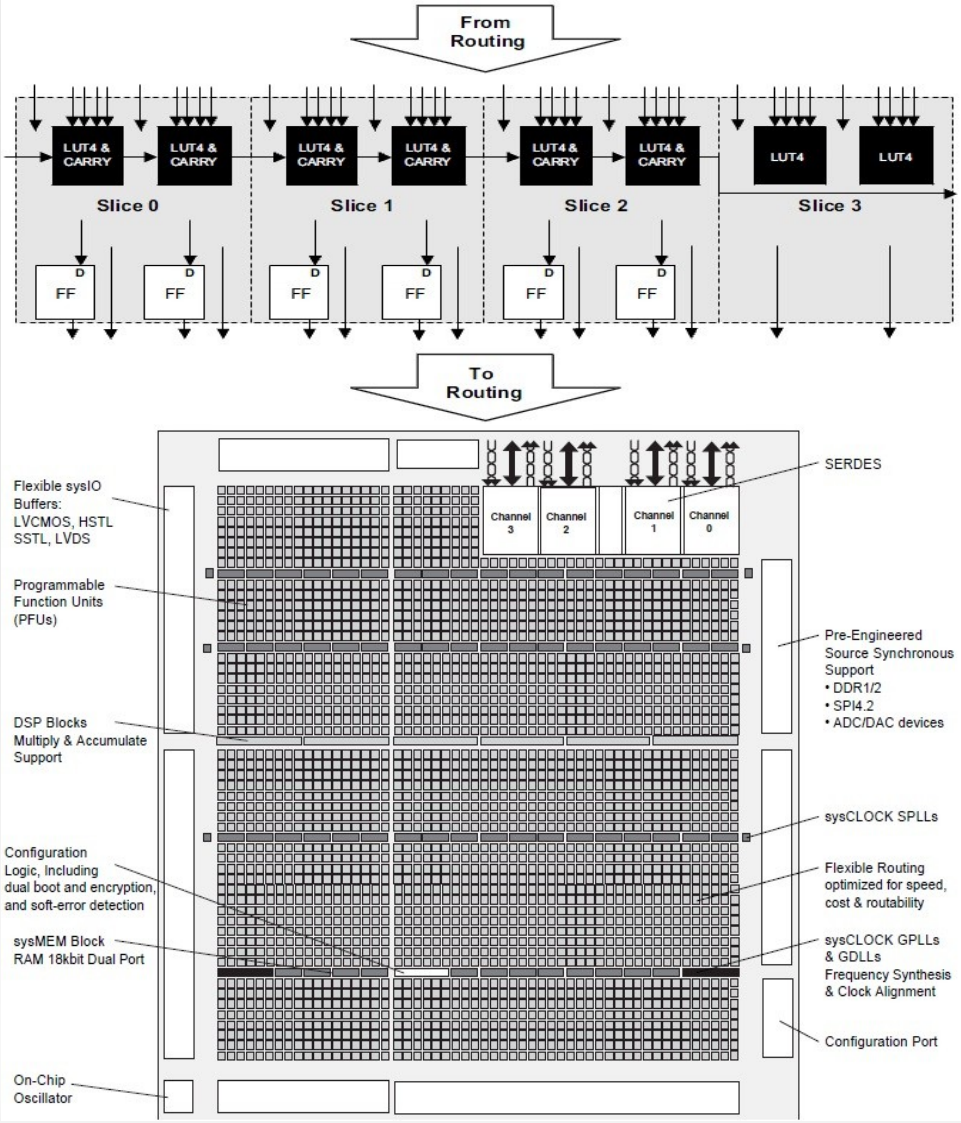
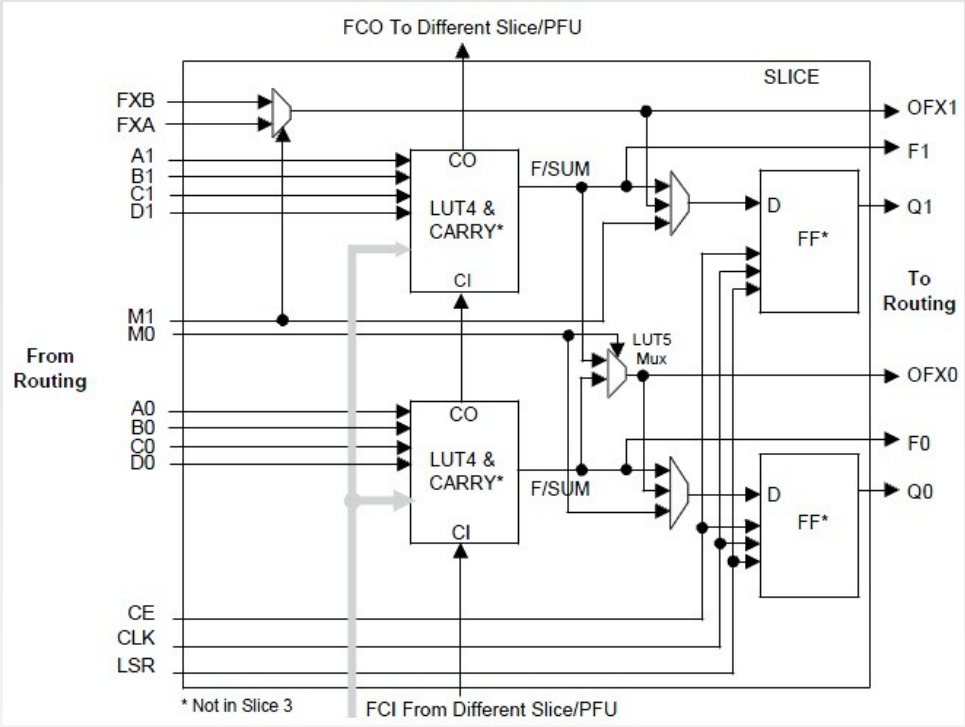
Architecture of Time-to-Digital Converter





Lattice ECP2M FPGA Slice Diagram, PFU Diagram and Floorplan [4]

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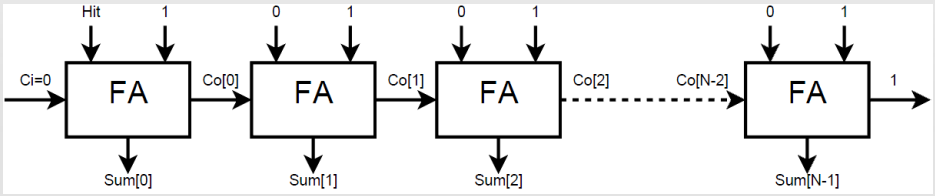
Architecture of Time-to-Digital Converter



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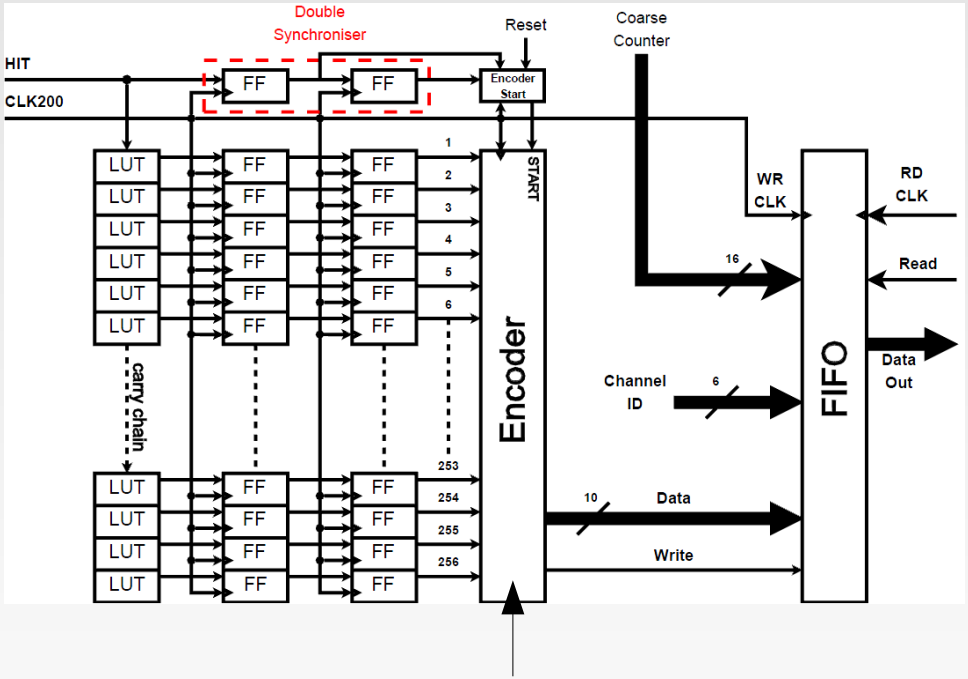
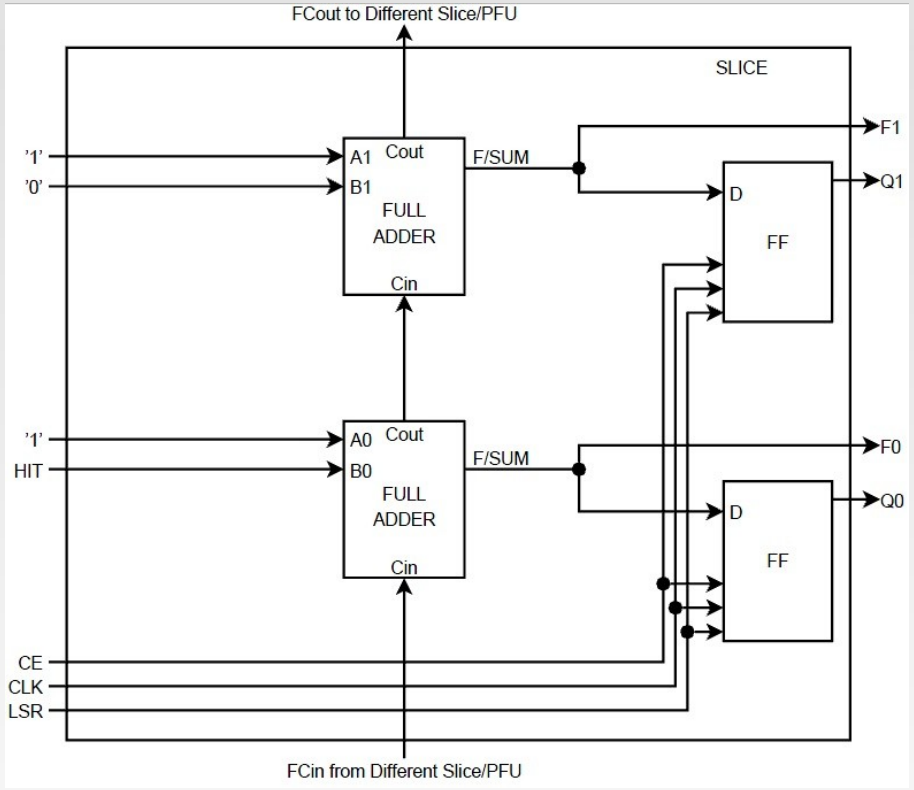
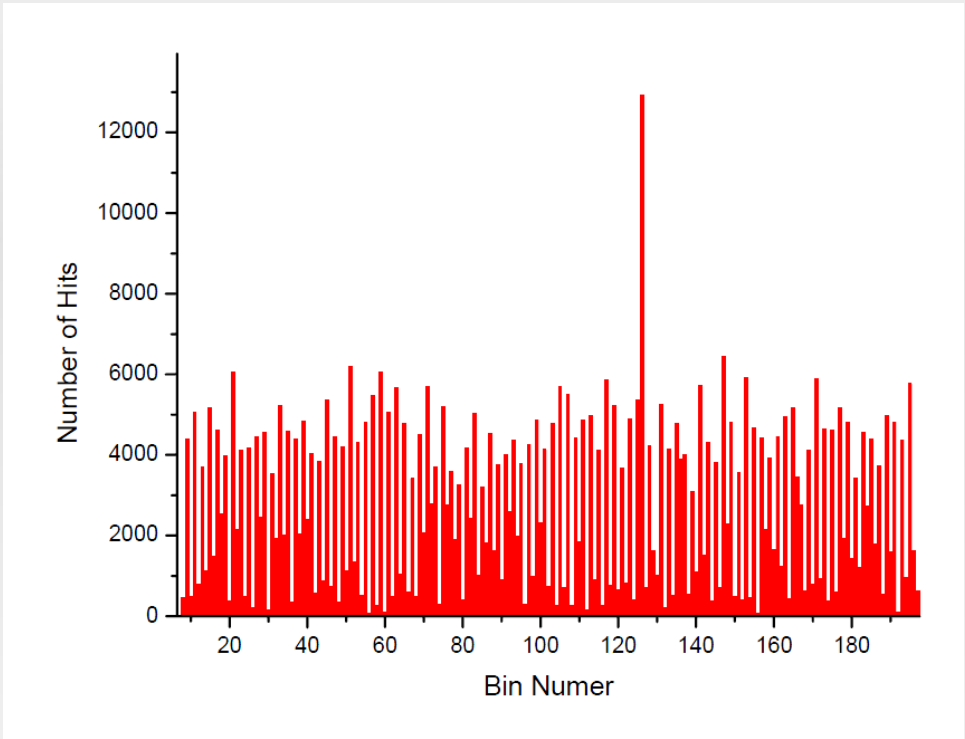


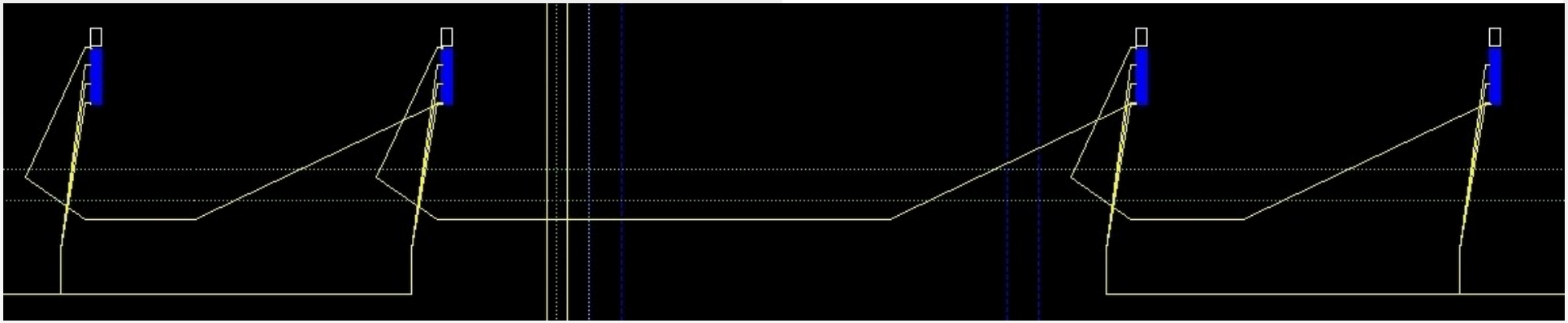


Bubble Error!!!

Architectural Effects of FPGA

- Effect of primary clock line in the FPGA
- Effect of longer inter-slice routings
- Effect of PFU architecture





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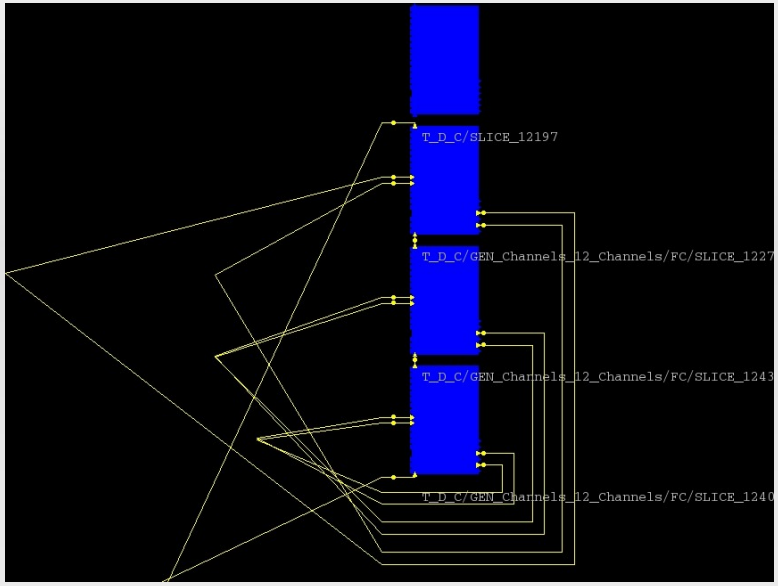

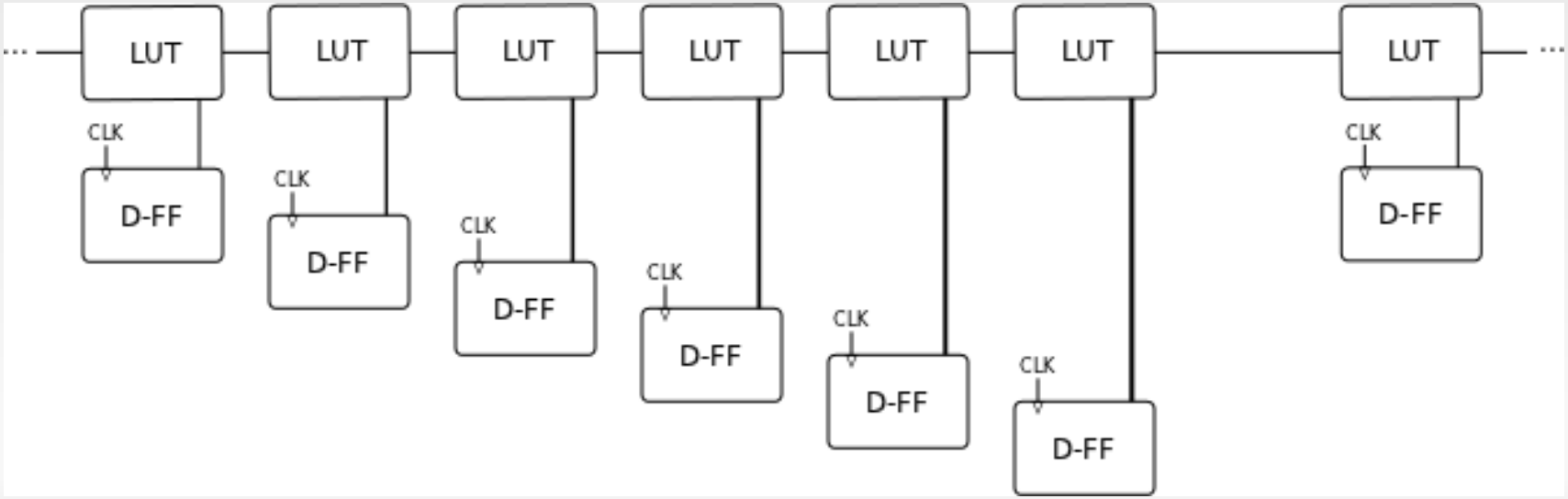

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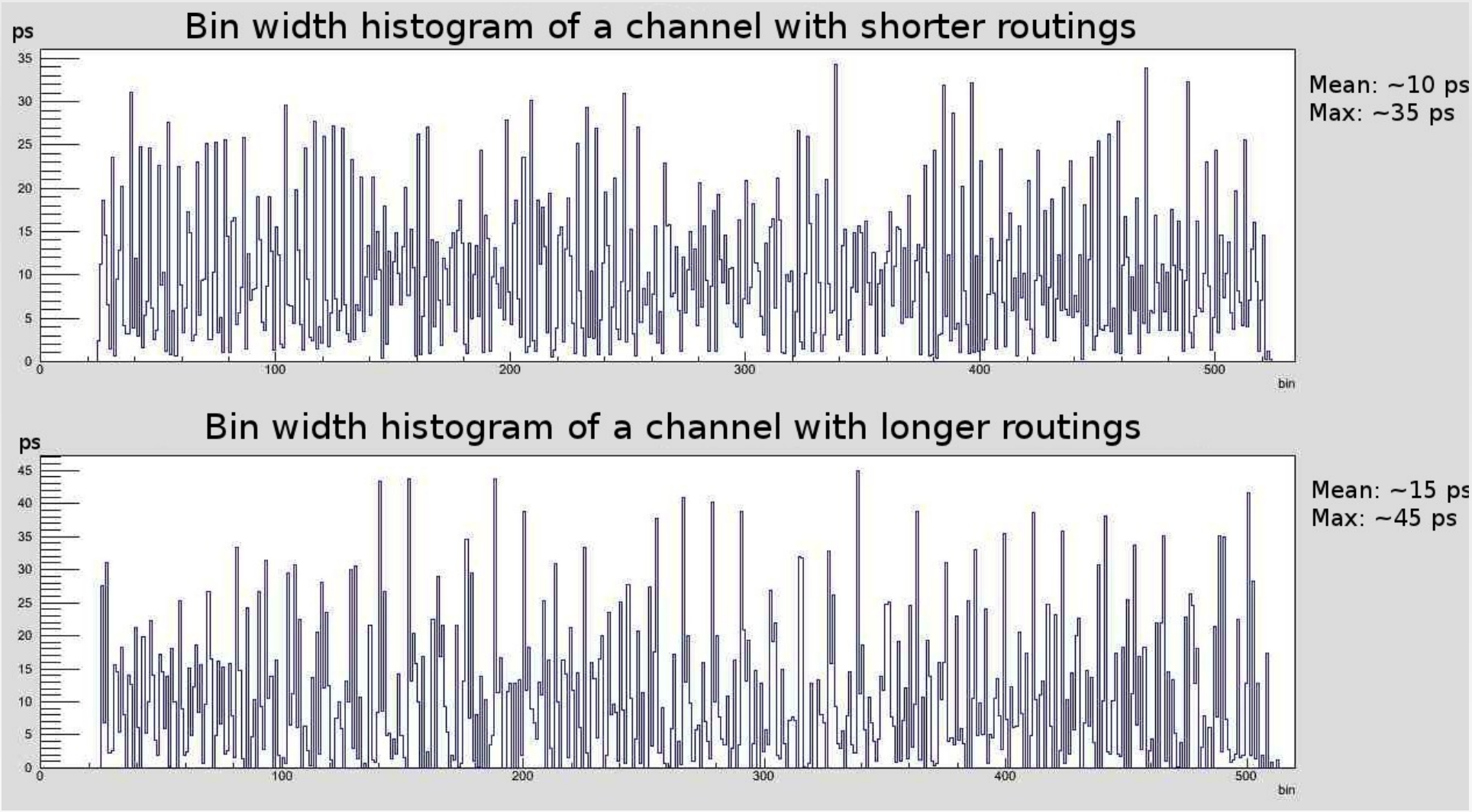

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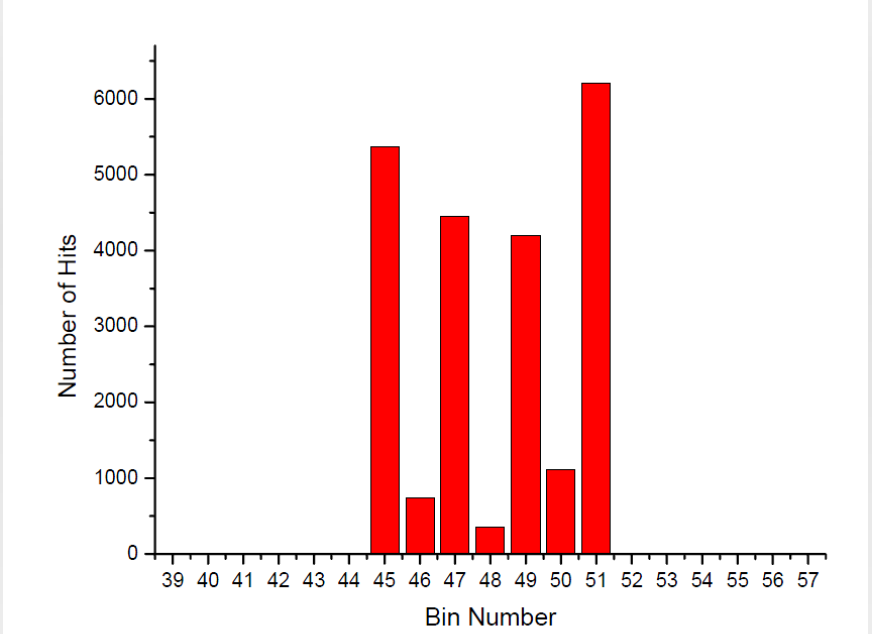

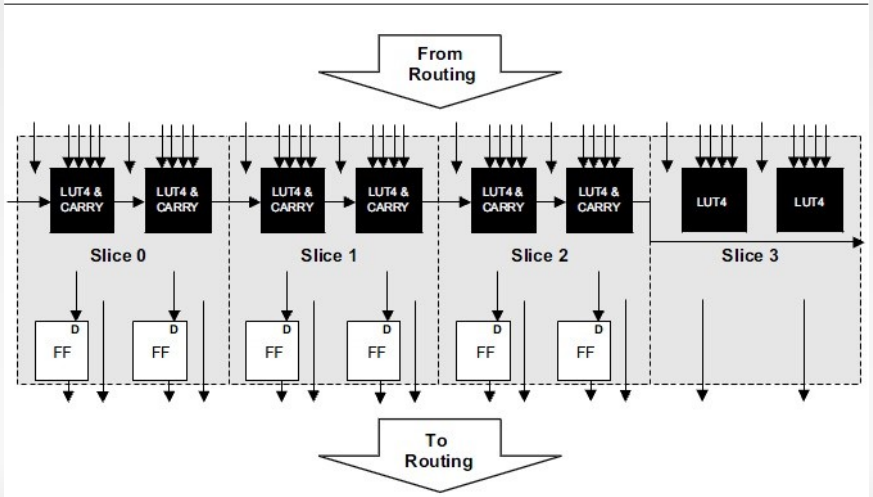

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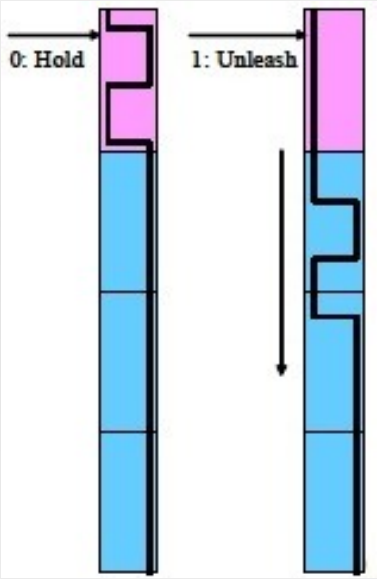
Wave Union Launcher

- More than one delay line is necessary in order to reduce the effect of wide bins
- Wave union launcher[8] is implemented
- Bin widths & non-linearities are reduced



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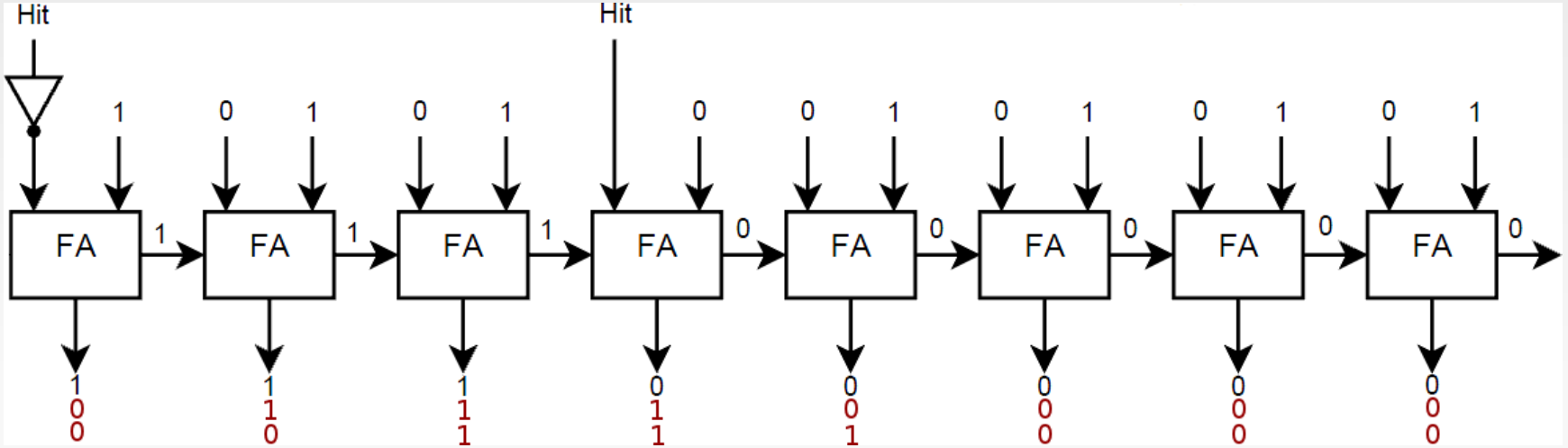

[7]

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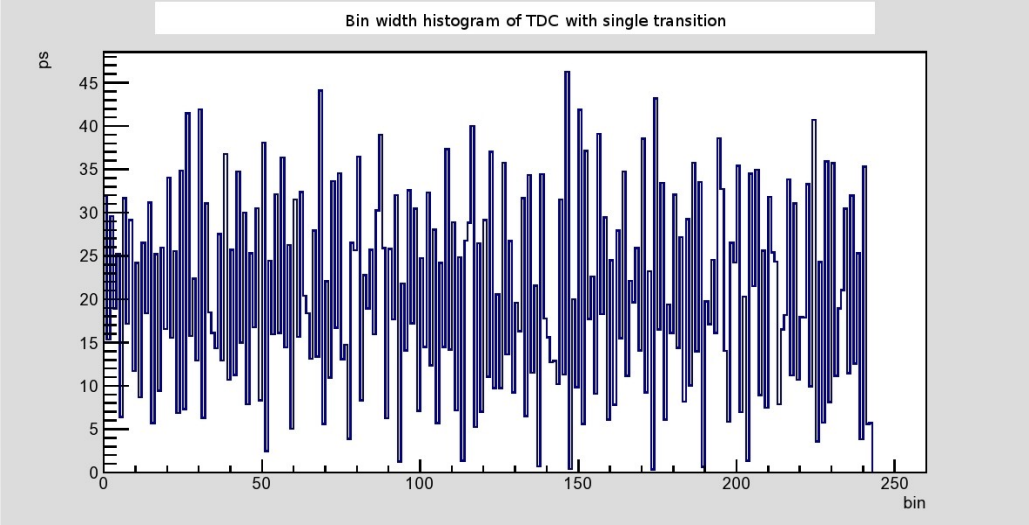
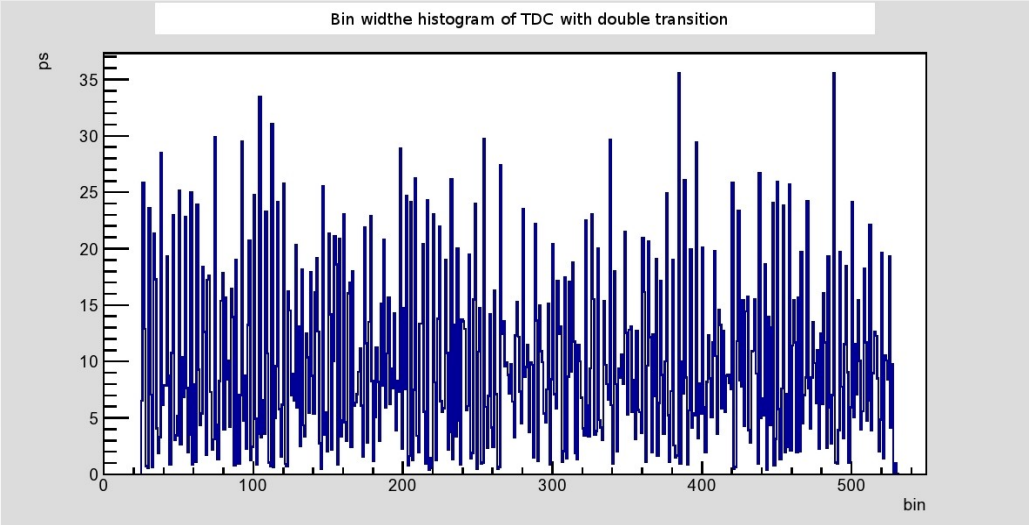
Wave Union Launcher

- More virtual bins
- Narrower bins
- Homogeneous bin distribution



Bins: ~240
Mean: ~20 ps
Max: ~45 ps



Bins: ~520
Mean: ~10 ps
Max: ~35 ps

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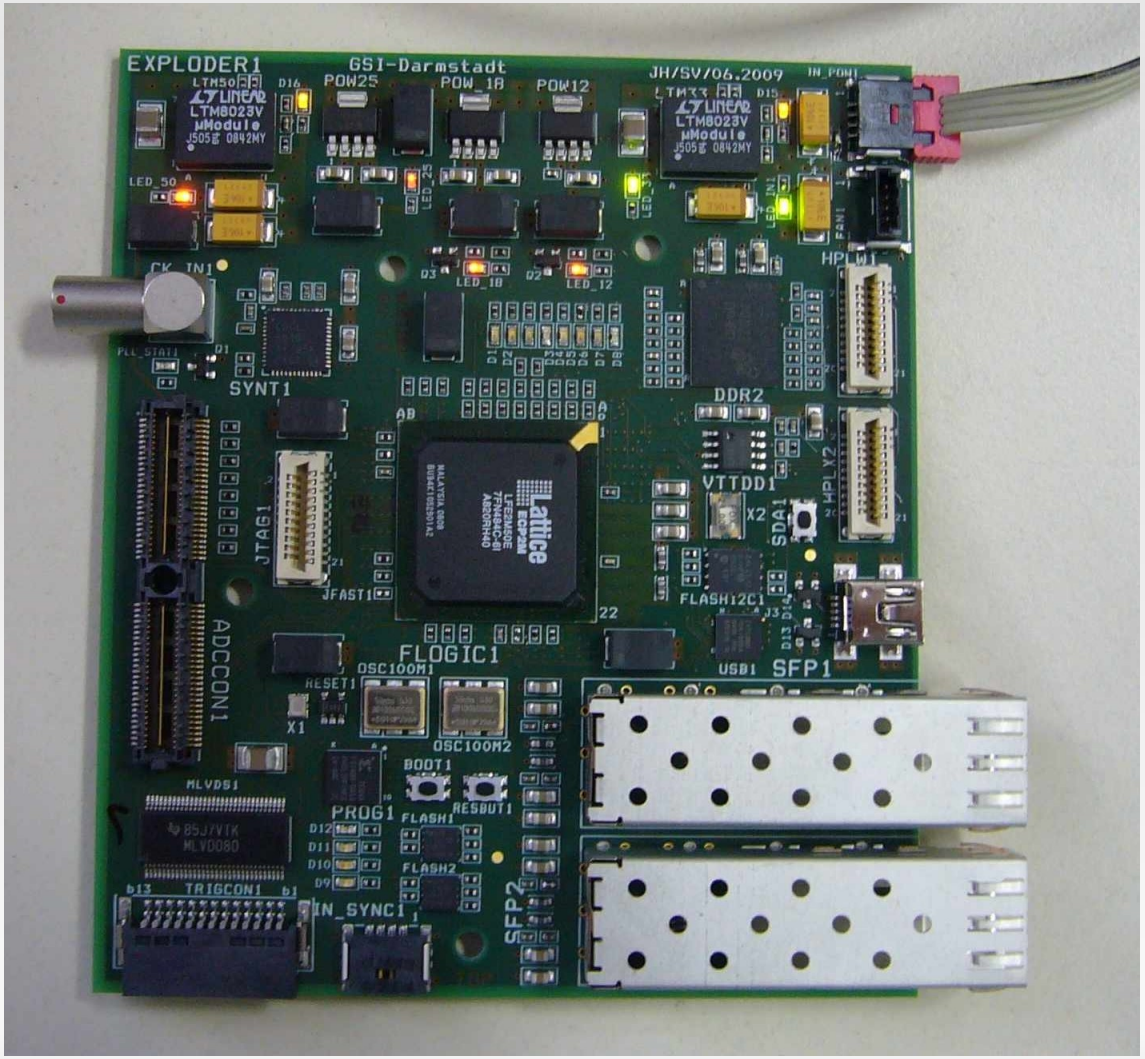
Measurement Setup

EXPLODERv1



[8]

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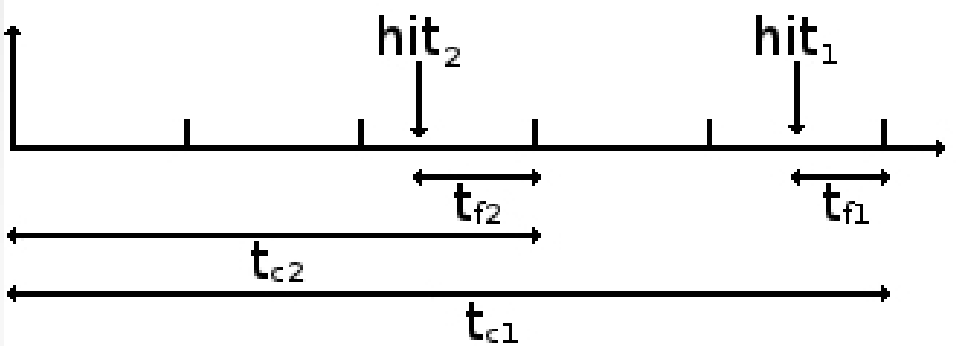
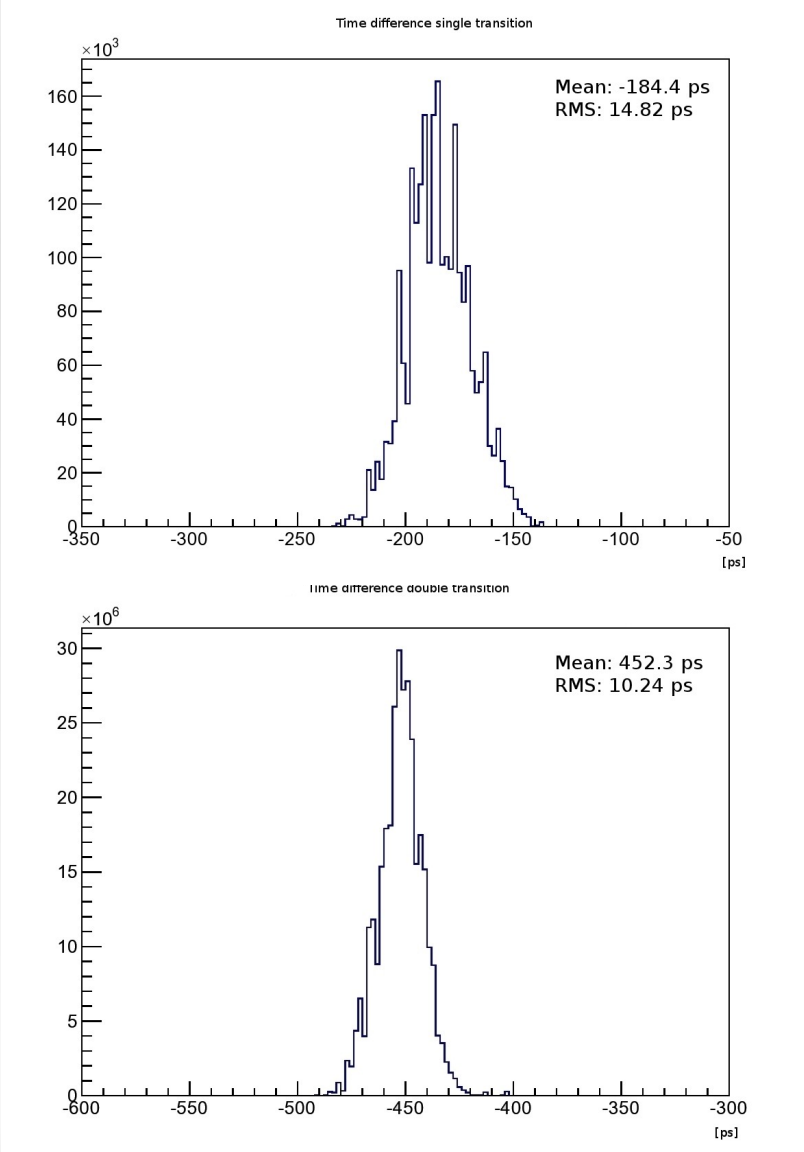
Statistical Error & Resolution

- Time difference measured between 2 channels
- $\Delta t = (t_{coarse1} - t_{coarse2}) - (t_{fine1} - t_{fine2})$
- RMS measured: 10.34 ps

  against same clock
- Resolution: 10.34 ps / √2 = 7.3 ps
- Effect of 2 transitions:

  14.82 ps / 10.34 ps = 1.43 factor





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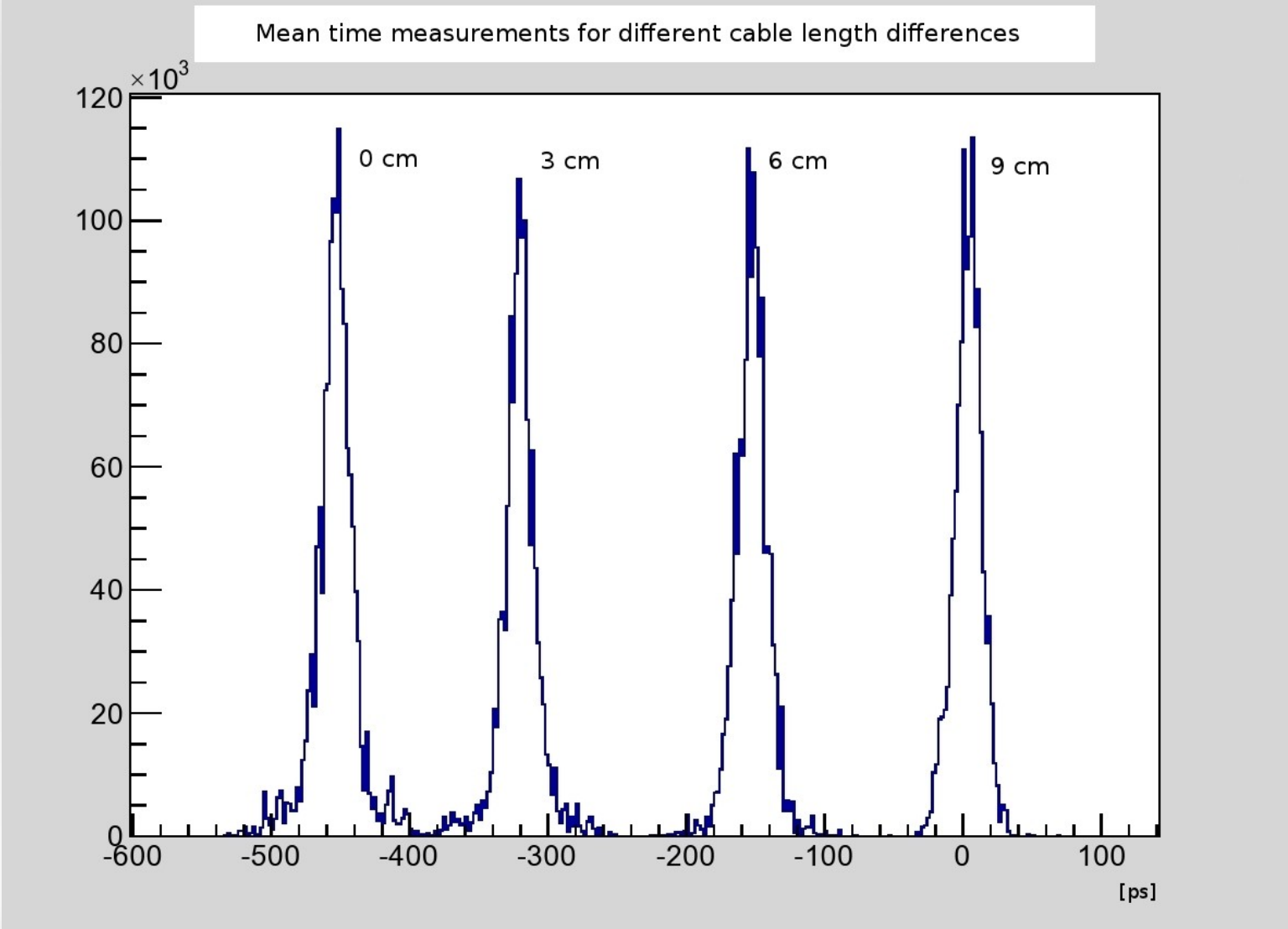
Mean Time Measurements



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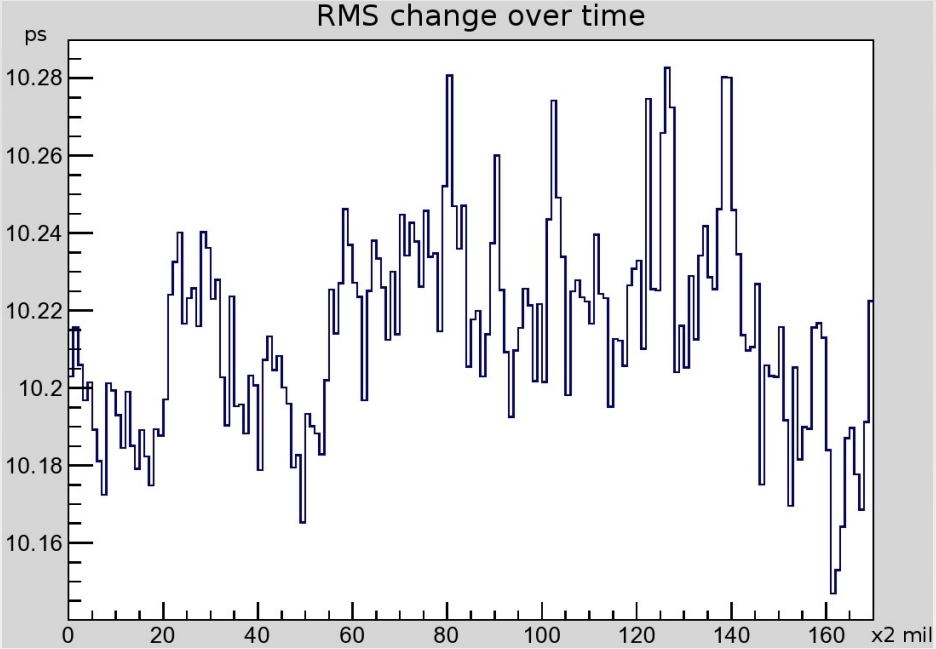
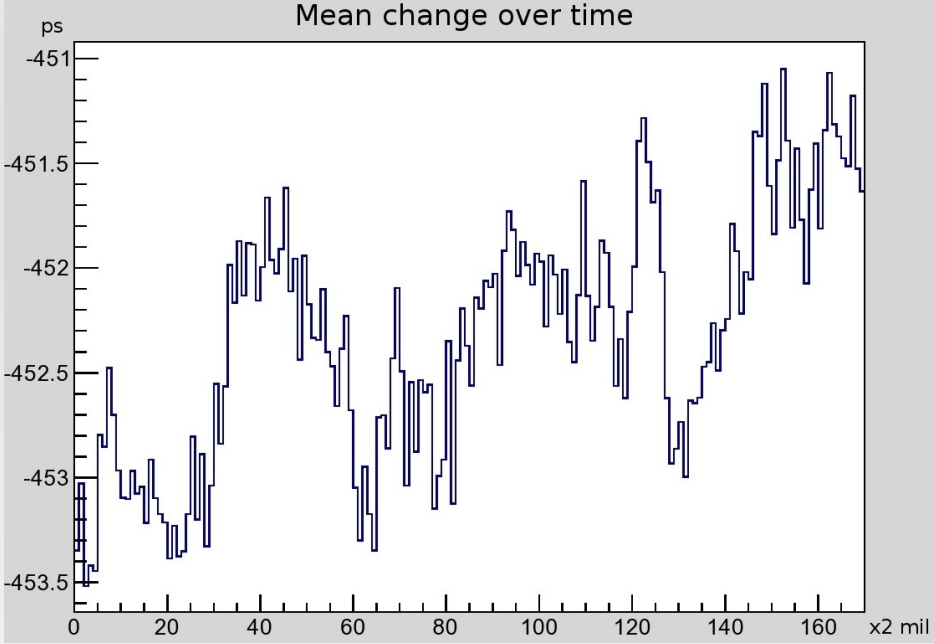
Stability





Max change 0.15 ps

Max change 2.5 ps

340.000.000 hits

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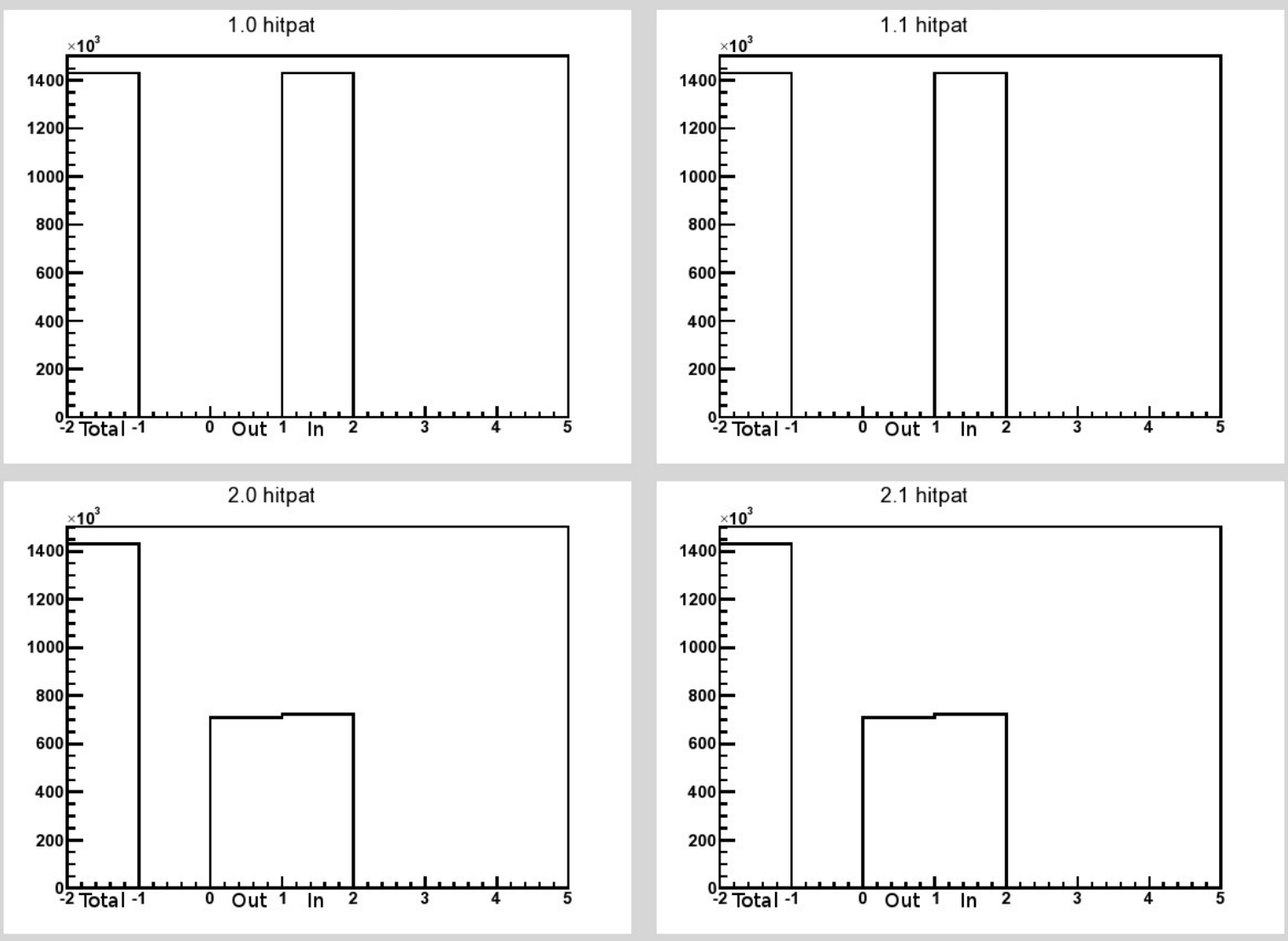
Extra Feature – Trigger Window

•Fiexed signal relative to the trigger.

• 1MHz Random signal
• 500 ns post-trigger window



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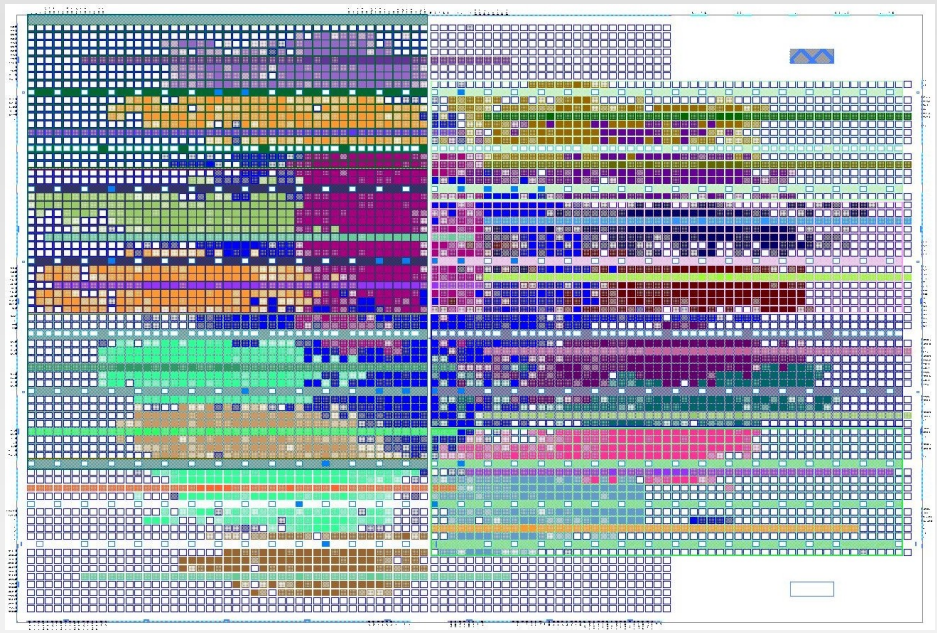
Resource Usage & Important Parameters

Resource (slice)	57% of ~24K slice
Resource (LUT)	40% of ~50K LUTs
# of channels	16
Max bin width	34 ps
Avg. bin width	~10 ps
RMS	10.3 – 12 ps
Max conversion time	45 ns
Dead time	30 ns
Carry chain length	320



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Conclusion

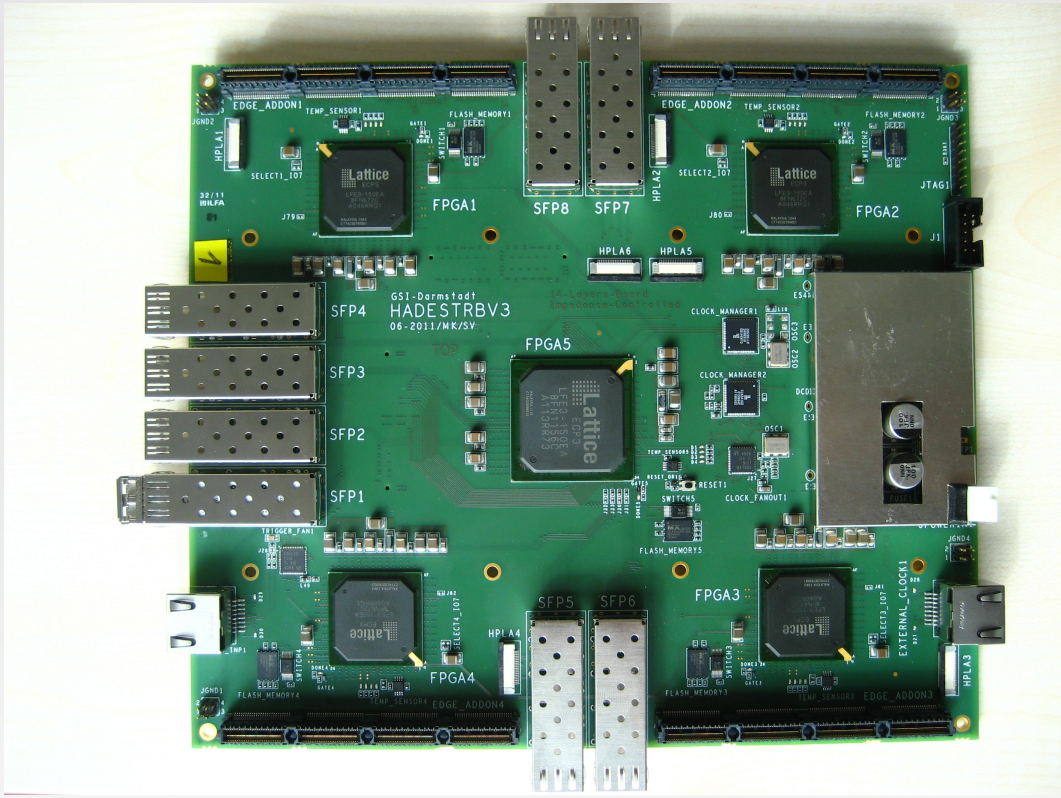
- 16 channels implemented in 50K LUT Lattice FPGA
- ~10 ps RMS is reached with 2 transitions
- Avg. bin width ~10 ps, yielding long delay line
- Very good results with one of the cheapest FPGA.

Outlook

- Higher system clock frequency, 400MHz
- Remove double synchroniser
- Reduce resource consumption
- Implement more channels, 64
- Reduce dead time

TRBv3

- 256 channel on board
- ~10 ps RMS
- FEE, Readout on-board
- Will be used for Hades, PANDA, CBM, etc.
- Per channel cost similar with ASIC-HPTDC from CERN, but 10 times higher resolution!!!



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References

- [1] G. Otto, Presse und Kommunikation, GSI Helmholtzzentrum für Schwerionenforschung GmbH, G.Otto@gsi.de
- [2] http://hades-wiki.gsi.de/pub/DaqSlowControl/TRBPublicationList/TRBv2_pic_22.12.06.jpg
- [3] J. Kalisz, “Review of methods for time interval measurements with picosecond resolution,” *Metrologia*, vol. 41, no. 1, pp. 17–32, 2004.
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- [5] J. Song, Q. An, and S. Liu, “A high-resolution time-to-digital converter implemented in field-programmable-gate-array,” *IEEE Transactions on Nuclear Science*, vol. 53, pp. 236–241, February 2006.
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