

Next Generation Data Acquisition Systems for FAIR based on TrbNet

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- The HADES Data Acquisition System
 - Set-up and Functionality
 - Succesful Au+Au run (Apr 12)
- Synergy Effects
 - TRB3 as wide-spread platform
 - Example: CBM-RICH test @ Cern, PANDA DISC-Dirc (Nov '12)
- DAQ for FAIR Experiments
 - Time distribution system for PANDA (SODA)
 - · CBM-MVD read-out



The HADES Detector @ GSI





Data Acquisition



HADES DAQ network

- located inside detector
 - space constraints, optical network
- 50 kHz event rate in trigger-busy-release architecture
 - low latency (5us) triggers, asynchronous read-out
- uniform network for all sub-systems
 - code reuse, identical tools, easy maintenance



DAQ Network





DAQ Network





The April 2012 Beamtime

- Au target, 15-fold segmented, 1% interaction
- Au beam, 1.23 AGeV, 2 million ions/second
- Typical rates 150 MByte/s, 10 kHz
 - · Limited by detectors
 - DAQ test: 500 MByte/s, 65 kHz
- 5 weeks
- Result: 140 TByte of data, 7.7 billion recorded events





Au + Au (1.23 AGeV) = ?





Status Visualization

- All Front-ends are individually adressable and contain a huge number of status and control registers
- Operators for 5-week beam-time are mainly non-experts
 - · Intuitive GUI
 - Prepared automatic procedures
 - needed to assure fast handling of all error conditions

0x00000004	0x00000000	0x00000000	0x00000c00
0x00000100	0x00000000	0x00140020	0x0010de0b
0x00000000	0x00000000	0x00000000	0x00000000
0x00000000	0x00000000	0x00000000	0x00000000
0x0005a860	0x00000000	0x00819518	0x000009a4
0x003bcdfc	0x00408356	0x00000000	0x00000000
0x00000000	0x004d7132	0x00000000	0x03479216
0x00000000	0x00000000	0x00000002	0x00000000
0x8b2bae66	0x0000198f	0x003f4304	0x07ce9695
0x0039b414	0x0000951a	0x00000000	0x00000000
0x00000000	0x00000000	0x00000000	0x00000000
0x00000000	0x00000000	0x00000000	0x00000000







Tactical Overview

02:4	02:44:42 Tactical Overview													
Main	Wall Clock 02:44:40	Current Rate 6946	Online QA											
DAQ	TrbNet OK	Timeouts on 0 boards	Busy 14.5%	Read-out										
Trig	Spill Sum 56k (13s)	Trigger Source M5/8C M20C	Accept. PT3 49% / 49%	PT3 / Start 11.5k/s / 0.62%	Start Count 1.9M / 16.0M									
Srv	Disk Level 94%	Max. CPU 27%	lcinga OK	TRB OK	Pwrsply OK									
8	#EB running act: 8/8 (be)	ΔRate EB-CTS 94 (1%)	Data Rate 132 MB - 19 kB	#Evt Discarded 0	#Evt w/ errors 0 (0.0%)									
MDC	MBO Reinit	MBO w/o data	Temperature 66/62/60/58	Link Errors	Voltages 25 warnings									
Endp	MDC system OK	RICH system OK	TOF system OK	RPC system OK	Sh/FW/S/V/CTS OK									
Fee	Rich APVs	TRB TDC	FEE Error	Trg. Inputs	Trigger									
Other	Magnet	Speech Output running	Shower OK	RICH HV 116 nA	MDC HV									

Trig-Start Count (02:44:41): OK Start counts per second 1.9M/s - Start counts per spill 16.0M

15	:44:51	Ta	ctical Overview		bigger	stop	close			
Main	Wall Clock 15:44:49	Current Rate 0	Online QA Not found							
Ø¥Ø	TrbNet OK	Timeouts on 15 boards								
Trig	Spill Sum No Spills	Trigger Source	Accept. PT3 0% / 0%	PT3 / Start 0/s / 0.00%		Start Co 0 / 0	unt			
ŝ	Disk Level 94%	Max. CPU 6%	lcinga Problem	TRB Problem		Pwrsp Proble	ly m			
8	#EB running act: 0/0 ()	∆Rate EB-CTS 0 (%)	Data Rate 0 MB - 0 kB	#Evt Discarde 0	ed #l	Evt w/ ei 0 (0.0%	rrors 6)			
MDC	MBO Reinit	MBO w/o data	Temperature 65/70/57/57	Link Errors	4	Voltage 5 warni	es ngs			
Endp	MDC system 27 missing	RICH system OK	TOF system OK	RPC system OK	n Sh	/FW/S/\ OK	//CTS			
Fee	Rich APVs	TRB TDC	FEE Error	Trg. Inputs		Trigge	r			
Other	magnet	Speech Output running	RICH HV 0 nA	MDC HV						
		Othor M								

No OEP is out-of-order and sending the invalid data flag due to low HV



Electronics built for HADES





New Versatile Platform: TRB3

- Multi-purpose FPGA platform
- Extension via AddOn-Boards
- 200 I/O per FPGA
- Full control via GbE
 - Stand-alone operation
 - Read-out & Slow-Control
 - Inter-FPGA communication via TrbNet
- Internal trigger system
 - many trigger options
 - connection to other DAQ systems
- Fully scalable to any number of boards

In use / planned to be used / evaluated by many groups: HADES (Start, Pion-Tracker) CBM (RICH, TOF, PSD, MVD) PANDA (Barrel/Disc-DIRC, STT) A2 (Crystal Ball/TAPS)



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CBM-RICH (Nov 12)



Amplifiers

FPGA with 65 TDC ch.

indiv. thresholds power supply optical 2 GBit/s link

- CBM-RICH prototype test @ CERN PS
- very short development time:
 6 months from schematics to beam-test
- 64 channel PMT read-out
 - 5x16 cm to be plugged on the back of an MCP-PMT

- optical link to TRB3
 - synchronization to DABC readout of CBM-TRD
 - send data via GbE

More about hardware: Next talk by Cahit Ugur



CBM-RICH Setup



DABC Read-out Framework



- Combined system to test different front-end hardware
- Full system run synchronized
- Data combined on-line
- TRBnet in quasi-free-running mode
 - triggered for coordinated read-out
 - recording data full time





Control System

- Control & Monitoring of the TRB3-integrated trigger system
- Full control via web interface

Central migger System	m	ste	Sy	gger	Tri	entral	Ce	
-----------------------	---	-----	----	------	-----	--------	----	--

- Status overview

Counter	Counts	Rate
Trigger asserted	1215509051 clks.	104.46 s ⁻¹
Trigger rising edges	7691389 edges	104.46 Hz
Trigger accepted	11432020 events	104.46 Hz
Last Idle Time	230120 ns	
Last Dead Time	1300 ns	769.23 KHz



- Trigger Channels

#	Ena	Assignment	Trigger Type	Current Rate	#	Ena Assignment	Trigge
0		Trigger Input 0	0x1_pysic 🔻	0.00 Hz	8	Periodical Pulser 0	0x1_p
1		Trigger Input 1	0x1_pysic 🗸	0.00 Hz	9	Periodical Pulser 1	0x1_p
2		Trigger Input 2	0x1_pysic 🔻	0.00 Hz	10	Periodical Pulser 2	0x1_p
3		Trigger Input 3	0x1_pysic 🔻	0.00 Hz	11	Periodical Pulser 3	0x1_p
4		Coincidence Module 0	0x1_pysic 🔻	0.00 Hz	12	👿 Random Pulser 0	0x1_p
5		Coincidence Module 1	0x1_pysic 🔻	0.00 Hz	13	unconnected	0x1_p
6		Coincidence Module 2	0x1_pysic 🕶	0.00 Hz	14	unconnected	0x1_p
7		Coincidence Module 3	0x1_pysic 🔻	0.00 Hz	15	unconnected	0x1_p

- Trigger Input Configuration and Coincidence Detectors

			Input Modu	les						Coincidence Detectors
#	Inp. Rate	Invert	Delay	Spike Re	ej.	Override	#	Window		Coin Mask (3:0)
0	0.00 Hz		0	ns C) ns	bypass 👻	0	150	ns	
1	0.00 Hz		0	ns () ns	bypass 👻	1	150	ns	
2	0.00 Hz		0	ns () ns	bypass 👻	2	150	ns	
3	0.00 Hz		0	ns C) ns	bypass 👻	3	150	ns	
Puls	ers									
										nI nI



PANDA Disc-DIRC





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Univ. Erlangen (Adrian Schmidt) test experiment @ Cosy November 2012

2600 TDC channels + beam hodoscope Fully stand-alone system





- Several detector groups of Panda already use TRB-based hardware
 in test setups running with TrbNet
- Can parts of the final DAQ be run with TrbNet?



Synchronous messages

- Reach all read-out controllers with small offset (ideal: < 10 ns)
- High timing accuracy (most systems: jitter < 100 ps)
- Synchronize to beam structure in storage ring (2us beam + 0.4us break)
 - Distribute common burst number
- Send control messages (start, stop, calibration...)

Slow-Control

- Debugging & status reporting
- Online configuration...





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 - Distribute common burst number
- Send control messages (start, stop, calibration...)

Slow-Control

- All boards accessible for debugging & status reporting
- On-line configuration of read-out, pre-processing modes...





Synchronous Networks



- Usual network (as in HADES)
 - · all components run independently
 - buffers within data stream
 - high-level features to "make life easier"
 - \rightarrow delays change over time
 - · precision ~ 100 ns
 - external signals for synchronization



- Deterministic network
 - run all boards with the same clock
 - remove all non-determinism
 - \rightarrow phase & latency between clocks unknown, but constant
 - can be corrected off-line
 - precision (jitter) < 100 ps



- Have a look on the implementation in CBMnet, because:
 - · Combination of TrbNet with CBM infrastructure neccessary, e.g. for CBM-MVD
 - It is available and thoroughly tested
- Insert a defined data word at any time into the data stream
 - · Special words can not appear anywhere else in the data
 - · "Deterministic Latency Message" (DLM)
 - · Restrict to 16 defined messages \rightarrow possibility to correct single bit errors





- Reuse existing definitions:
 - · development work only needed once
 - easier combination of mixed networks



- Define two types of messages, each with 32 Bit payload
 - "Start of burst" to mark the beginning of each super-burst (16 bursts)
 - number of super-burst used to idenfy data
 - sent in fixed intervals
 - · "Control" to select different operation modes, trigger calibration...
 - checksum to prove correctness of packet
 - can be sent at any time
- Link length measurement by returning messages
 - resolution: 4 ns (byte clock) is trivial, 400 ps (bit clock) should be possible
 - used for adjustment of delays in sending DLMs





SODAnet for PANDA





CBM-MVD



Cur. prototype control system

may be replaced with CBMnet + additional slow-control features



Timescales

Work based on existing systems gives fast results:

- CBM-RICH
 - First idea: January
 - Board fabrication: April
 - · Beamtest: November
- Panda SODA
 - January: DAQ workshop
 - Decision: Use TrbNet as basis for SODA
 - February:
 - Bi-directional communication in synchronous FPGA network
 - Validation of fixed-latency of messages
 - April (planned)
 - Finish first implementation of Soda message master & receiver
 - Test automatic link latency measurements
 - No full-time worker on this project!



The TRB3 "Collaboration"

- Hardware: Michael Traxler (GSI)
- TDC: Cahit Ugur (GSI)
- GbE: Grzegorz Korcyl (Krakow)
- CTS: Manuel Penschuck (Frankfurt)
- Data Network: Jan Michel (Frankfurt)
- Slow-Control Framework: Ludwig Maier (Munich)
- Data Unpacker: Matthias Hoek (Mainz)
- Event-Server: Jörn Adamczewski-Musch (GSI)
- DABC: Sergey Linev (GSI)
- and all the people...
 - ... who write there own additional code
 - ... who helped designing and implementing TrbNet
 - ... who were involved in the HADES DAQ upgrade
 - ... I forgot to mention



- The TRB3 platform is in use by many different groups and experiments
 - 70 TRB3 in operation up to now
- Trb3 and TrbNet are an easy-to-run solution to acquire data
 - · both for small test setups and huge detector setups
 - · compatible to other trigger systems
 - · almost plug'n'play few software parts to install, few cables to connect
- Rather small modifications are needed to adapt the HADES DAQ network to other FAIR experiments:
 - run as synchronous network
 - messages with deterministic latencies
 - free-running read-out
- The DAQ concepts for all FAIR experiments share many similar aspects
- Not everything needs to be as individual as it may seem



Next Generation Data Acquisition Systems for FAIR based on TrbNet

3rd Hic for FAIR Detector Systems Networking Workshop



Next Generation Data Acquisition Systems for FAIR based on TrbNet

3rd Hic for FAIR Detector Systems Networking Workshop

"Network networking makes your net work"







- Highly granular (500 FEE)
 - Placed directly on detector
 - · Strong space constraints for electronics and cables
- High trigger rate (50 kHz)
 - Compatible to trigger-busy-release architecture
 - With asynchronous data transfer
 - Low latency transport of trigger information (< 7 us Trigger System FEE)
- High Bandwidth (500 MByte/s)
- Simple Maintenance
 - High amount of reuseable code
 - · Common architecture of all sub-systems



- Conventional DAQ uses triggers
 - e.g. hand-shake between all sub-systems for each recorded event
 - · robust
 - easy to handle, discrete data
- Introduces time overhead for each event
- Not usable in high rate experiments (PANDA, CBM ...)
- "Free running" architecture
 - · all sub-systems continuously collect data
 - · data streams are sent to computing farm
- Need for time stamping



Triggerless System





- Task: Multiple front-ends need a precise time reference to combine measurements from different parts of a detector
- Classical approach:
 - Put a dedicated cable to each board
- In densely packed detectors, any additional cable should be avoided
 - An optical link for data transport is available



A high-speed serial link is not a cable



- Normal usage
 - data stream is recovered in each intermediate device
 - clock is extracted, data is parallelized
 - · buffers in receivers for data
 - high-level features to "make life easier"
 - → delays change over time precision \sim 200 ns



- Deterministic network
 - run all boards with the same clock
 - remove all non-determinism
 - \rightarrow phase & latency between clocks unknown, but constant
 - can be corrected off-line
 - precision (jitter) < 100 ps



Typical Set-up





- Typically, FPGAs serve as digital data processors only
- Analog signals are handled by dedicated chips
- Many customized chips (ASIC) needed for our applications
 - Very helpful for special applications (e.g. designed for radiation hardness, tailored to specific constraints...)
 - Common disadvantages:
 - Very long design and production phase
 - Expensive due to low quantities
 - No big vendors, i.e. no guaranteed lifetime
 - Difficult to handle because of nonstandard housings
 - If it's versatile, it doesn't fit perfectly





FPGA based signal processing



- 40x amplification
- adjustable thresholds
- digital signal shaping
- control via SPI:
 - temperature, input status, edge count, id, non-volatile memory, insystem programmable

- 16 channels
- component cost: 26 €
- power consumption: 1.2 W
- e.g. analog 500 uV, 6 ns signals \rightarrow LVDS, 20 ns $\rightarrow \Delta t \sim 200$ ps



- FPGA are well-suited for common DAQ systems
- The flexible architecture allows to adapt to any front-end electronics
- By using FPGA in non-standard ways, one can
 - measure time
 - discriminate signals
 - measure analog properties with ADC, QDC
- Very flexible designs, easy to adapt to other requirements



- How to upgrade firmware in ~400 FPGA distributed all over the detector?
 - Connect flash ROMs to logic in FPGA
 - One command in software framework
 - 30s to program + 60s to verify (full system, ~500 MByte)
- Failsafe?
 - Dual-boot with "golden image"



```
> trbflash program 0xfffd bit/mdcoep 20120307a.bit
Found 372 Endpoint(s) of group MDC OEP V3
NAME: mdcoep 20120307a.bit
DATE: Wed Mar 7 22:30:59 2012
Start programming ImageFile
'bit/mdcoep 20120307a.bit'
Programming Endpoint(s) @ Address 0xfffd
Symbols:
 E: Erasing
 P: Programming
 0: Success
  .: Skipped
Block: 0 1 2 3 4 5 6 7 8 9 A B C D E F
      00000000000...
0
1
       . . . . . . . . . . . . . . . . . . .
Success
Verifying Endpoint(s) @ Address 0xfffd
Block: 0 1 2 3 4 5 6 7 8 9 A B C D E F
\cap
       . . . . . . . . . . . . . . . . . . .
Success
```



Transmission Error Correction

Optical transceivers show BER > 10⁻



 Error topology was even used to track down HV problems
 PMTs





Monitoring for Disc-DIRC

Padiwa

			Configu	iration											
Boar	d		fe48												
Upda	te Inten	val (ms)	1000	0											
Optic	n		Tem	perature	• •										
Min/N	vlax		10		80										
					ок										
							_								
Board	0201	0203	0210	0211	0212	0213	0240	0241	0242	0243	0250	0251	0252	0253	026
0	37.4	34.1					40.4	45.3	41.4	44.6	37.4	36.0	35.1	35.4	
1	37.9	34.3					42.2	45.1	43.6	45.3	40.9	39.6	36.5	37.5	
2	37.8	32.4			32.3		42.5	42.7	41.9		42.9	41.7	37.9	39.9	
2	00.0						10.0	10.0	10.0		10.0	10.0	20.0	10.0	

Temperatures of few FEE

Individual thresholds for 2600 channels

Board 020	1 020	3 0210	0211	0212	0213	0240	0241	0242	0243	0250	0251	0252	0253	0260	0261	0262	0263	0270	0271	0272	0273	0280	0281	0282	0283	0290	0291	0292	0293	02a0	02aL	02a2	02a3
764	8 77	<u>د</u>				85f6	1010	8602	8654	8152	846c	87c1	87c1					816c	7eda	7df3	7d78	8564	843f	84fe	8693	767c	7560	7abe	7558	87c1	87c1		87c1
77a	a 77	· ···				864a		8570	8554	823a	8402	87c1	87c1					814a	7e10	7e47	7c9a	8699	8333	8464	8625	7650	7560	7afa	751e	87c1	87c1		87c1
775	0 77					8670	6f6d	8518	8550	8436	8410	87c1	87c1					8052	7648	7d97	7000	8514	8365	8542	84df	7620	7560	765a	7510	87c1	87c1		87c1
764	6 78					86+0	8448	85fa	8544	8546	847c	87c1	87c1					8128	7dd6	7dfd	7cf6	8518	8365	840c	8666	7bc0	7560	7650	74be	87c1	87c1		87c1
776	ic 77	2				86e0	8562	8566	8578	8436	8458	87c1	87c1					89e6	7e94	7f63	7e4e	85a0	8411	84ec	865d	7660	7560	7bd4	7568	87c1	87c1		87c1
776	4 78					8638	16.54	BSCE BSCE	8512	8498	8456	8/c1	8/c1					81/4	7TeS	2112	7690	8552	8396	8584	8633	7650	7560	78/8	74te	8761	8761		8/61
0 771	a 77					8644	1967	84bc	8410	83da	764+	87c1	87c1					7fd8	7578	7c91	7cd2	84.84	8403	83f0	852d	7628	7560	7ab0	7484	87c1	87c1		87c1
776	8 77	3				8672	5465	85ac	8548	82da	8334	87c1	87c1					7f88	7d38	7d8f	7c82	84fe	8355	84e6	85b7	7c28	7560	7a7c	7588	87c1	87c1		87c1
778	2 77		1090			8598	36d9	8580	8554	8674	835e	87c1	87c1					7cde	7594	7639	7872	8584	8305	84ea	8561	7ab4	7560	7bc2	7464	87c1	87c1		87c1
760	4 77		891			8634		8444	8404	8324	8526	87c1	87c1					805e	7468	7073	7680	855a	8317	84+2	851b	7656	7560	7406	7550	87c1	87c1		8761
760	2 78					8734	563	85d4	8496	82c6	8454	87c1	87c1					8178	7ea4	7e35	7dfc	85ba	81b3	8432	854b	7ba8	7560	760a	7420	87c1	87c1		87c1
761	e 78	2				86ea	ccde	85a8	84.26	8544	83d2	87c1	87c1					81fe	764a	7f8d	7+8+	863a	83f7	8554	8657	7ac4	7560	7ad0	736a	87c1	87c1		87c1
776	2 71	a				8690	8568	8626	8564	8516	8386	87c1	87c1					8356	802c	8141	7†2e	8655	8445	Bice	864d	7638	7560	7a16	73c6	87c1	87c1		87c1
768	18 764		8000		0	84/6	abec SCor	8510 pcfs	8364	8326	PShe	8/c1	8/c1					0	8140	80a2	7642	8525	8934	8649	8/9/	/aec	7904	7aec 7bbs	6e/a	87c1	8761	8/c1	8/c1
762	c 76		0			8566	8560	8500	8350	8540	8648	87c1	87c1						7fb0	7ed2	7c3a	854a	8868	BSfb	8829	7836	78f2	7cd0	7500	87c1	87c1	87c1	87c1
750	ic 77	4				8565	8Sec	8494	828a	84ae	86d6	87c1	87c1						80ea	808e	7e74	8582	88b2	85b7	86c9	7c26	7870	7540	5e54	87c1	87c1	87c1	87c1
774	2 77					851f	85a2	85ce	8384	8524	852c	87c1	87c1						811a	8000	7676	8598	8886	8613	8841	7c24	7964	7636	6eaa	87c1	87c1	87c1	87c1
756	2 77					8681	8662	8548	8358	8470	8508	87c1	87c1						8294	8288	7630	8550	8944	8741	8701	7668	7890	7afe	6dfa	87c1	87c1	87c1	8761
1 765	e 76:	i				8631	8559	8726	837a	8544	BEde	87c1	87c1						8340	83fe	7ffe	84ee	892a	871f	8783	7bec	7894	7656	6f80	87c1	87c1	87c1	87c1
764	8 77	4	0			8569	84e4	8460	8312	834c	86ba	87c1	87c1						7f70	8044	7c98	8466	8882	85c1	8696	7c0e	7820	76f2	6444	87c1	87c1	87c1	87c1
757	2 77		8090		8001	85a3	8512	8500	8390	8426	Biae	87c1	87c1						80e4	8054	7646	8448	8855	8585	87cd	7696	7946	7612	6e18	87c1	87c1	87c1	87c1
760	2 76					8653	ISTO	B4fe	8322	8514	852e	87c1	87c1						818e	80f8	7eb2	8594	8863	862f	8737	7af2	786a	7b16	6e22	87c1	87c1	87c1	87c1
763	16 773	4				86bf	8516	8612	8286	84f2	85a0	87c1	87c1						7c62	7f8a	7+20	8458	8828	85ef	85<5	7ade	792÷	7b3e	6dce	87c1	87c1	87c1	87c1
767	0 76					8577	862c	8648	846a	83d8	BEdc	87c1	87c1						82ae	820c	7676	84fc	8849	85e7	864f	7ba4	78f8	7bae	6e6e	87c1	87c1	87c1	87c1
769	8 76	2				8653	8629	8562	8420	83d4	8702	87c1	87c1						80ea	8380	7f6e	846a	8892	8665	8765	7670	7832	7ac8	6dBe	87c1	87c1	87c1	87c1
762	0 75		0		0	87f4	8698	8602		824+	8262	87c1	87c1					7edc	756a	7d84	6366	865e	8585	84ee		7a9e	7b7a	7ae6	792c	87c1	87c1	87c1	87c1
761	6 75	· ···	8090		0	87c8	859c	85fa		857c	84be	87c1	87c1					7ea0	7e92	7c12	6252	85:66	8635	84c8		7ace	7bf0	7294	78:00	87c1	87c1	87c1	87c1
7fa	8 75		0	4449		8770	8524	8634		863c	8462	87c1	87c1					7588	7c04	793e	6974	8564	864f	8542		7684	7c88	7aee	792c	87c1	87c1	87c1	87c1
700	c 75					8724	Bán	85b2		85ba	Báca	87c1	87c1					8004	0	7=10	5.98	8522	8694	8444		7638	7cle	79+0	792c	87c1	87c1	87c1	87c1
7e8	6 75	i	8090	000		8792	8384	8534		8572	8582	87c1	87c1					8964	7f2c	7faa	693c	8566	8533	8426		7664	7cf0	7abc	792c	87c1	87c1	87c1	87c1
7e9	8 75	• • • •				8878	8528	8522		8350	8612	87c1	87c1					8lec	802c	810e	687c	8572	85%	8462		7628	7c24	7826	78:00	87c1	87c1	87c1	87c1
2 761	0 75					8822	8524	8446		8422	8458	87c1	87c1					7+58	Zella	7554	5000	8413	8524	8470		7950	7c2a 7ha6	7918	7924	8701	87c1	8761	8761
760	a 75		8090			8775	834a	8638		8550	8425	87c1	87c1					7d18	7da6	7bec	5913	8538	85ad	8536		7254	7b9c	7948	7794	87c1	87c1	87c1	87c1
7fb	4 75	• •••	0	400		86c8	8410	8590		855e	84a6	87c1	87c1					7acc	7888	78ba	695 8	84:00	8679	8484		7bc0	7bbe	7833	799e	87c1	87c1	87c1	87c1
764	e 75					8754	834a	8630		8594	Stea	87c1	87c1					7116	7642	7dde 7e06	5245	8592	8669	8436		7636	76a2	7402	7953	87c1	87c1	87c1	87c1
769	6 75					8743	8459	8522		849a	8522	87c1	87c1					813e	8090	7ecc	57da	8566	BEFS	847a		764a	7b5e	7240	78:00	87c1	87c1	87c1	87c1
766	e 75	• • • •				86e4	8482	84ec		8358	84ce	87c1	87c1					8248	8066	80be	5874	8472	861f	84da		7886	7b62	796e	79±0	87c1	87c1	87c1	87c1
764	e 75	• •••				8740	8448	8716		841a	8308	87c1	87c1					8178	8144	8184	6958	856a	8735	85d8		7614	7694	7a72	2354	87c1	87c1	87c1	87c1
860			0			8523	8664	8880		8694	84Sc	87c1	87c1					8116	8016	807a	6498	8846	8562	85e8		79c8	799c	7c04		87c1	87c1	87c1	87c1
877						8658	85e8	8820		87c6	8892	87c1	87c1					7fac	7e68	7ee6	6860	8744	866c	8666		7966	739e	7c8a		87c1	87c1	87c1	87c1
863	ie					85c2	85e8	8750		875c	87ec	87c1	87c1					8134	7fee	8050	6da0	86f6	8656	8528		7a18	7ada	7814		87c1	87c1	87c1	87c1
860						85f8	8674	876		8828	882c	87c1	87c1					8098	815e	8080	6e34	8756	8748	85c8		7500	7afe	7cb2		87c1	87c1	87c1	87c1
855						8582	8510	873		8/64	8756	87c1	8701					8226	8140	8082	6048	8764	8583	8533		7914	7528	7880		8701	87c1	8761	8761
2 851						8632	Sec	87d4		8770	8712	87c1	87c1					81f2	8124	80f2	6Ce8	8740	8680	8500		79c8	7288	7a3c		87c1	87c1	87c1	87c1
852						8588	8588	87ec		8708	87ae	87c1	87c1					7f14	7fd0	7f08	Gefc	86c2	8586	8602		7a4c	7840	7976		87c1	87c1	87c1	87c1
854	· · ·					8658	8Sfe	87dd		87bc	850e	87c1	87c1					8968	8130	7ff4	6cd0	8782	8526	8548		7916	7a18	7660		87c1	87c1	87c1	87c1
840	2					85fa	84b2	8875		8788	8802	87c1	87c1					8840	Tee2	7f7e	5e12	8664	8524	8524		7950	7202	7bc0		87c1	87c1	87c1	87c1
846	ic					8588	85e8	8720		880.	86e6	87c1	87c1					821c	8054	8014	5+28	8782	86fa	85c0		7904	7846	7b1c		87c1	87c1	87c1	87c1
858	ic					85ec	85f2	8760		8690	87f8	87c1	87c1					81be	81d2	7602	6c7c	8756	8654	852a		7994	735e	7246		87c1	87c1	87c1	87c1
7cb						8616	8928	8802		5000	8744	8701	8701					B1eC	0105	0198	64530	8660	0500	6540		7982	Tade	7884		87c1	8761	8761	STC1



E.g. CBM-RICH

- CBM-RICH test-beam at CERN, Nov 12
- unfortunately only 84 ps time-resoultion due to some layout errors
- Combined with DABC based read-out for other components

7000

500

4000

3000

1000





Jan Michel - Goethe University Frankfurt



Triggerless?





- All network entities are encapsulated
- the "user" only has to deal with few signals
 - Trigger information & status feedback
 - · Data input
 - · Slow control bus
- All buffering, read-out control, error checking is internal





The Hmon Framework

- Standard Tools
 - · Perl Environment
 - · Apache Webserver
 - · Gnuplot
- Interface Libraries
 - · DAQ-Network (C-Library)
 - · Epics
 - · Icinga / Nagios
 - · All system tools
- GUI
 - · XHTML / JavaScript based
 - · Viewable from any device & anywhere
 - · Access to data plots from Root





Radiation?



- Theory
 - ~ 50 ions/cm²/s
 - 3 SEU/h (full system)
- Experiment
 - 2 FPGA/h failing for unknown reasons
 - Topology of errors hints at SEU



Radiation?



- FPGA are sensitive to ionizing radiation (as any electronics)
- Temporary damage by changing value of storage cells
 - · data corruption
 - change of configuration
- HADES: 3 SEU/h expected
- Triple redundancy
 - three instances of the same logic for cross-check of data
 - · lowers error rate up to 100x
- detection of configuration changes
 - reload correct configuration



Interface / GUI Selection

"commercial" Tools, e.g. EPICS

- Experts are quite rare
- Modern GUI requires lot of ressources
- Many interfaces / modules readily available
- Special software required for each client

Self-made code e.g. Perl & C-tools

- Very flexible
- Easy to extend by non-experts
- Needs some preparation time
- No I/O modules available
- Many tools ready from development phase



Eventbuilding

Detector Sub-systems



- 30x 1 GbE from detector
- 4 servers / 32 cores / 40 TB disk 2x 10 GbE
 - · Combine data to complete events
 - Temporary local storage
 - Transport to network file system (Lustre) and tape
 - Subset of data to Online Analysis



Eventbuilding

- UDP packets received from >30 sources
 - Stored in buffer memory
- Individual sub-events collected in one event
- Synchronization between 16 servers
 - Data automatically distributed by DAQ network
 - Inter-process communication with EPICS IOC
- Integration in DABC framework available





 \rightarrow J. Adamczewski-Musch



Online Analysis

- Idea: Use only basic Root classes, no external libraries
- Server
 - Reads & analyses HADES data files (hld)
 - Fills all defined histograms
 - Provides histograms over TCP
- Clients
 - Access histograms from server via TCP
 - Encapsulated in one executable
- Configuration
 - All configuration, histogram definitions defined in one XML file



(very small demonstration set-up)
Typical: 10 windows / 10 tabs /
6 histograms ~ 600 histograms



DAQ Monitoring

Monitoring Main Control Interface +		
HADES DA	AQ Monitoring	
Main Tactical Overview (the central screen) Logfile (most important messages) Chat Log		
Other Ressources QA Plots (updated every 5 minutes) Vertex Plots (updated after each file) Beamtime Logbook Icinga Server Monitoring Archive of Hmon Windows (updated every 10 minut	tes)	
DAQ Network Hub Monitor Busy times of subsystems Histogram of busy times Data amount on GbE Data rate histogram	Trigger Rates on CTS Trigger I/O Eventrate histogram (10s) Eventrate histogram (60s) Eventrate histogram (10m) Start counts per spill Ratio of accented PT3 per spill	
MDC MDC Overview MDC Busy Times MDC Data Rates MDC Missing Tokens	Recorded events per spill Start hit count histograms Veto hit count histograms CTS mux output histograms CTS mux output ratio histo.	

Eventbuilder

MDC Missing Tokens MDC Retransmission MDC Temperature

- Central Webpage gives access to all monitoring features
 - · Data QA Plots
 - · DAQ Network
 - · Operator Logbook
 - · Server Status





- The upgraded Hades DAQ System was succesfully used during the 5-week April 2012 beam-time
- The DAQ / Eventbuilder / Monitoring performance was more than sufficient
- All error conditions could be succesfully identified and resolved
 - Most common errors within < 30 seconds
 - · Very few calls to experts necessary
- The framework is flexible to be adapted to many other projects