The HADES DAQ System - Trigger and Readout Board Network (TrbNet)

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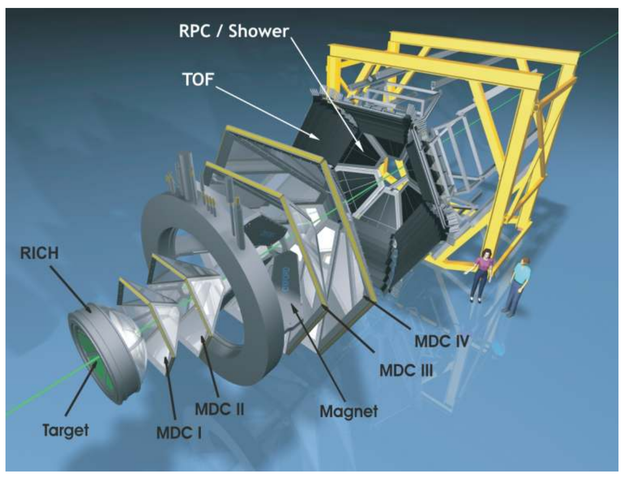
The HADES Spectrometer



The HADES spectrometer is a versatile di-electron and hadron spectrometer located at the GSI Facility for heavy ion research in Darmstadt, Germany, and operational since 2002. The setup includes:

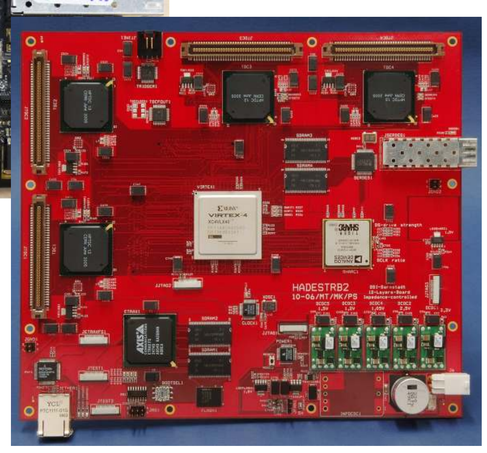
- Four layers of multi-wire drift chambers (MDC) providing particle tracking
- Ring Imaging CHerenkov detector (RICH)
- Pre-Shower detector for electron identification
- Time-of-flight detector (TOF / RPC) for hadron identification.

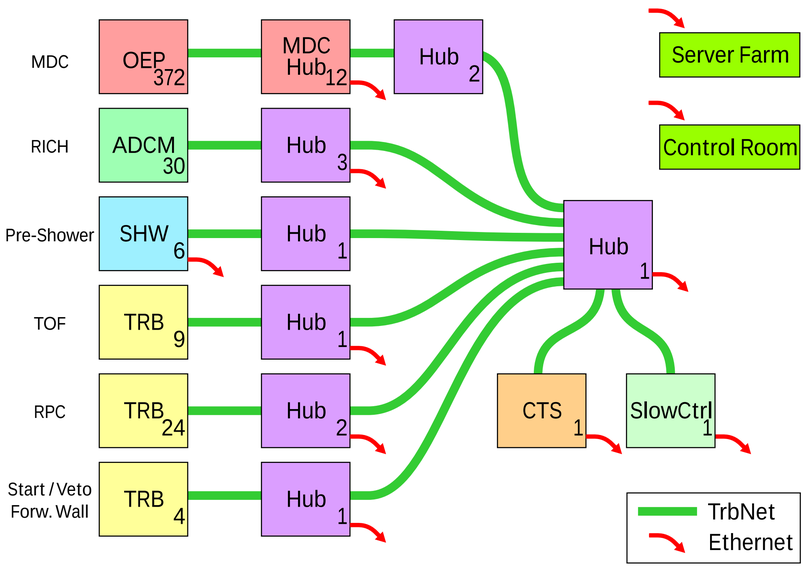
Overview / Key Features

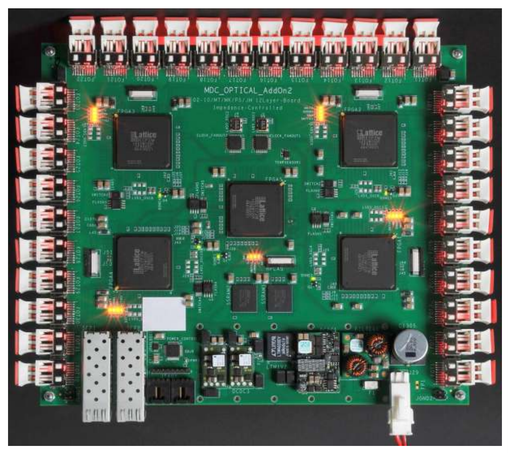
During the last 2 years the DAQ system of HADES has been completely rebuilt to gain higher data rates. The key features are:

- DAQ capability: up to 100 kHz event rate / up to 250 MByte/s
- Optical transmission - reduces induced noise in detectors
- One common protocol for all subsystems - simplifies development and operation
- No other data link than one pair of optical fibers to parts of the FEE (space constraints)
- LVL1 trigger, event data and slow control information combined
- Low-latency transfer of trigger information (< 3 µs broadcast to all systems)
- Combining data from front-ends into data blocks ("sub-events")
- Back-pressure - no data loss due to buffer overflow / discarded data
- Sending event data to server farm using Gigabit Ethernet
- Busy logic for LVL1 trigger - prevents sending new triggers while front-ends are busy

The Complete Network / Electronics







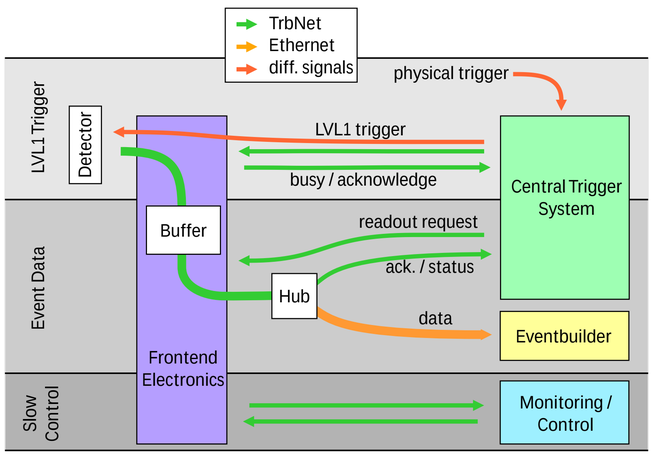
- ADCMv3: 16 channel, 40 MSPS, 12 bit ADC, Lattice FPGA, 2.5 GBit/s optical link, µC, power supply for front-ends, reads out 2048 channels of RICH detector
- TRBv2: Trigger and Readout Board. Virtex 4 FPGA, 2 GBit/s optical link, 128 TDC channels (30ps RMS), TigerSharc DSP, Etrax FS embedded Linux system, Ethernet. Reads out all timing relevant detectors.

- The full DAQ network contains 23 Hubs, 450 front-end boards.
- Hubs distribute trigger information and control commands and combine data from several front-ends
- Data is transported through 28 GbE-links to the event-builders (data servers)
- All boards are controlled from two central places: The central trigger system (CTS) and the slow control

The MDC read-out system:

- MDC-Hub: Data concentrator board, 5 Lattice FPGA, 32x 250 MBit/s optical transceivers (FOT / plastic optical fibers), 2x 2.5 GBit/s optical link, Gigabit Ethernet
- MDC OEP: MDC front-end read-out controller. Lattice ECP2M FPGA, 250 MBit/s optical transceiver, 5 voltage regulators, ADC, size: 4 x 5 cm

Network Features



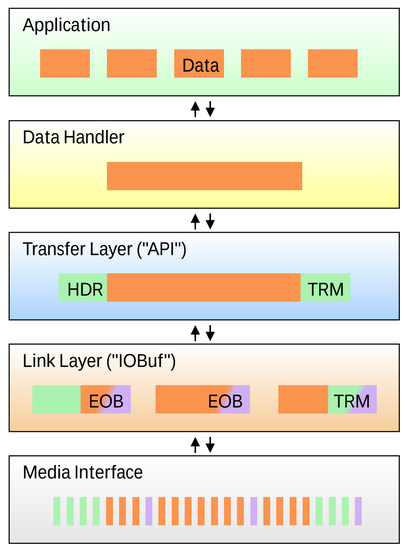
The network is divided into three virtual channels. Switching channels takes less than 100 ns.

All DAQ information is transported using one common optical network and one common protocol:

- LVL1 trigger information (e.g. trigger number and trigger type) and busy handling
- Event data is sent through TrbNet to network hubs and then converted to Ethernet and sent to our data servers
- Control- and monitoring data

All data transport is controlled by a central instance, the CTS. Monitoring uses a PCI-Express card equipped with optical transceivers.

Protocol Stack

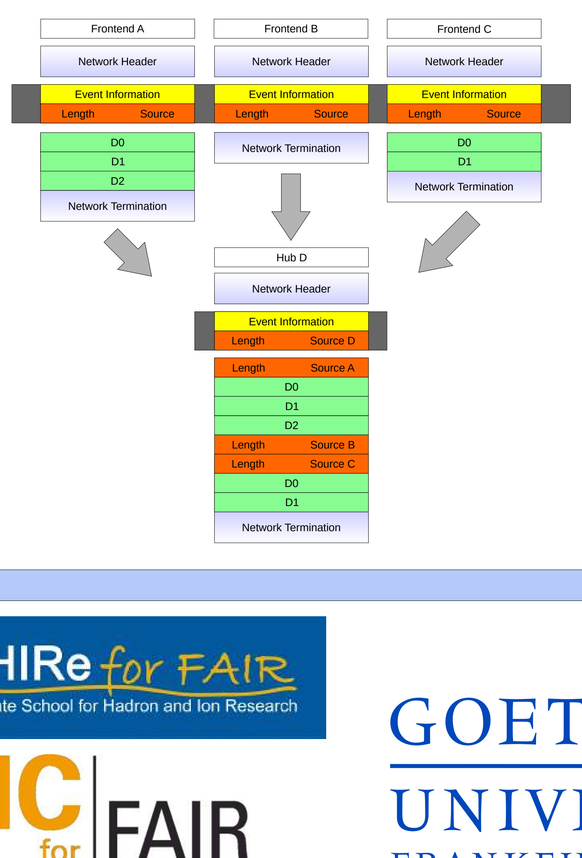


The network access is handled through 5 layers of control instances:

- The application provides data words
- The data handler packs data into TrbNet packets
- The transfer layer adds header and termination words, containing network addresses and channel information
- The link layer divides the transfer into blocks, adds checksums and handshakes with the receiver side
- The media interface provides the physical link, e.g. using an optical fiber

Data Transport & Combining

- Hubs are not only routing data through the network:
  - Collecting busy information of front-ends
  - Data from different front-ends is merged into one stream ("data concentrating")
  - Monitoring status of Frontends
- Data is organized in 32 bit words
- Each event data packet is preceded by a standard header containing all event information
- TrbNet produces about 30 of these data streams (SubEvents) which are combined to a full event in the server farm (Event-builders)



Slow Control / Monitoring

The slow control and monitoring system provides a variety of features:

- the whole network forms a global 32 bit address space with registers on each FPGA
  - each front-end can be monitored and configured individually
- the same network as for data transport has to be used due to space constraints, but:
  - slow control is independent from other channels, can not be blocked by mal-function
- every board is identifiable by on-board id-chip
- DHCP-like assignment of network addresses
  - every board can be addressed individually or in groups (broadcast)
- Further features:
  - allows to upgrade firmware stored in flash memories
  - standard registers provide global status information
- User Interface:
  - a software library provides an easy-to-use basis for any kind of monitoring software
  - User front-end gives access via command line tools and graphical interfaces (EPICS)

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